Paper No. 1 Filed: August 10, 2020

PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO. 7,149,867

Mail Stop **PATENT BOARD**Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450



TABLE OF CONTENTS

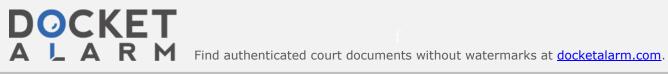
			Page
I.	IN	TRODUCTION	1
II.	MA	ANDATORY NOTICES UNDER 37 C.F.R. § 42.8	2
	A.	Real party-in-interest under 37 C.F.R. § 42.8(b)(1)	2
		Related matters under 37 C.F.R. § 42.8(b)(2)	
	C.	Lead and back-up counsel under 37 C.F.R. § 42.8(b)(3)	3
	D.	Service information under 37 C.F.R. § 42.8(b)(4)	3
III.	RE	QUIREMENTS FOR IPR	3
	A.	Payment under 37 C.F.R. § 42.103	4
	B.	Certification of standing under 37 C.F.R. § 42.104(a)	4
		Identification of challenge under 37 C.F.R. § 42.104(b)	
		1. Challenged claims and claim constructions	4
		2. Specific grounds, supporting evidence and claim-by-claim analysis, and exhibit number and relevance of supporting evidence	1
IV	DIS	SCRETIONARY FACTORS	
		Denial is not warranted under §314(a)	
		Denial is not warranted under §325(d)	
V.		CHNOLOGICAL BACKGROUND	
		Conventional computer architecture and data prefetch	
		FPGAs	
	C.	Scatter/Gather	12
VI.		IE '867 PATENT	
	A.	Summary of the patent	13
	В.		
	C.	Level of ordinary skill in the art	
		Claim construction	
		1. "reconfigurable processor" in all claims	14
		2. "data prefetch unit" in all claims	
		3. "data access unit" in claims 11-19	



	4.	"fu	ınctional unit"	15
	5.	"m	emory hierarchy"	15
	6.	"cc	omputational unit" in claims 11-19	15
VII.	SP	ECI	FIC GROUNDS	16
A.	Ov	ervi	iew of the cited prior art references	16
	1.	Zh	ang (EX1003)	17
	2.	Gu	pta (EX1004)	19
	3.	Ch	ien (EX1005)	21
В.	-		on of ordinary skill in the art would have been motivated bine the Zhang, Gupta and Chien references	22
C.			d 1: Claims 1-2, 4-8 and 13-19 are obvious over Zhang upta	28
	1.	Cla	aim 1:	28
		a.	Preamble: A reconfigurable processor that instantiates an algorithm as hardware comprising:	28
		b.	1(a): a first memory having a first characteristic memory bandwidth and/or memory utilization	30
		c.	1(b): a data prefetch unit coupled to the first memory	32
		d.	1(c): wherein the data prefetch unit retrieves only computational data required by the algorithm from a second memory of second characteristic memory bandwidth and/or memory utilization and places the retrieved computational data in the first memory	36
		e.	1(d): wherein the data prefetch unit operates independent of and in parallel with logic blocks using the computional [sic] data	41
		f.	1(e): wherein at least the first memory and data prefetch unit are configured to conform to needs of the algorithm	46
		g.	1(f): the data prefetch unit is configured to match format and location of data in the second memory	49
	2.	Cla	aim 2: The reconfigurable processor of claim 1, wherein:	53



	a.	2(a): the data prefetch unit is coupled to a memory controller that controls the transfer of data between the second memory and the data prefetch unit	53			
	b.	2(b): and [the memory controller] transmits only portions of data desired by the data prefetch unit and discards other portions of data prior to transmission of the data to the data prefetch unit				
3.	the	Claim 4: The reconfigurable processor of claim 1, wherein he data prefetch unit comprises at least one register from he reconfigurable processor				
4.	the	Claim 5: The reconfigurable processor of claim 1, wherein the data prefetch unit is disassembled when another program is executed on the reconfigurable processor				
5.	sai sai	Claim 6: The reconfigurable processor of claim 1 wherein said second memory comprises a processor memory and said data prefetch unit is operative to retrieve data from the processor memory				
6.		Claim 7: The reconfigurable processor of claim 6 wherein said processor memory is a microprocessor memory6				
7.	sai	Claim 8: The reconfigurable processor of claim 6 wherein aid processor memory is a reconfigurable processor nemory				
8.		aim 13: A method of transferring data comprising:				
	a.	13(a): transferring data between a memory and a data prefetch unit in a reconfigurable processor	63			
	b.	13(b): transferring the data between a computational unit and a data access unit	64			
	c.	13(c): wherein the computational unit and the data access unit, and the data prefetch unit are configured to conform to needs of an algorithm implemented on the computational unit and transfer only data necessary for computations by the computational unit	67			
	d.	13(d): wherein the prefetch unit operates independent of and in parallel with the computational unit	69			
Q	C1	aim 14	60			



	a.	14(a): The method of claim 13, wherein the data is written to the memory, said method comprising:	69
	b.	14(b): transferring the data from the computational unit to the data access unit	70
	c.	14(c): writing the data to the memory from the prefetch unit	71
10.	Cla	nim 15:	72
	a.	15(a): The method of claim 13, wherein the data is read from the memory, said method comprising:	72
	b.	15(b): transferring only the data desired by the data prefetch unit as required by the computational unit from the memory to the data prefetch unit	73
	c.	15(c): reading the data directly from the data prefetch unit to the computational unit through a data access unit	74
11.	traı	nim 16: The method of claim 15, wherein all the data insferred from the memory to the data prefetch unit is beessed by the computational unit	74
12.	sel	nim 17: The method of claim 15, wherein the data is ected by the data prefetch unit based on an explicit uest from the computational unit	75
13.	traı	nim 18: The method of claim 13, wherein the data insferred between the memory and the data prefetch unit not a complete cache line	75
14.	cor	nim 19: The method of claim 13, wherein a memory attroller coupled to the memory and the data prefetch unit, attrols the transfer of the data between the memory and the a prefetch unit	76
	Ground 2: Claims 3 and 9-12 are obvious over Zhang, Gupta and Chien		
1.	the pro	data prefetch unit receives processed data from on- bcessor memory and writes the processed data to an ernal off-processor memory	76
2		im 0.	70 23



D.

DOCKET

Explore Litigation Insights



Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time** alerts and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.

