

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53

Proceedings

**International Conference on
Computer Design
VLSI in Computers and Processors**

October 12-15, 1997
Austin, Texas

Sponsored by
IEEE Computer Society Technical Committee on Design Automation
IEEE Circuits and Systems Society



Los Alamitos, California

Washington • Brussels • Tokyo

1
2
3
4 Copyright © 1997 by The Institute of Electrical and Electronics Engineers, Inc.
5 All rights reserved
6
7

8
9
10 *Copyright and Reprint Permissions:* Abstracting is permitted with credit to the source. Libraries may
11 photocopy beyond the limits of US copyright law, for private use of patrons, those articles in this volume that
12 carry a code at the bottom of the first page, provided that the per-copy fee indicated in the code is paid
13 through the Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

14 Other copying, reprint, or republication requests should be addressed to: IEEE Copyrights Manager, IEEE
15 Service Center, 445 Hoes Lane, P.O. Box 133, Piscataway, NJ 08855-1331.

16 *The papers in this book comprise the proceedings of the meeting mentioned on the cover and title page. They*
17 *reflect the authors' opinions and, in the interests of timely dissemination, are published as presented and*
18 *without change. Their inclusion in this publication does not necessarily constitute endorsement by the*
19 *editors, the IEEE Computer Society, or the Institute of Electrical and Electronics Engineers, Inc.*

20
21 IEEE Computer Society Order Number PR08026
22 ISBN 0-8186-8026-X
23 ISBN 0-8186-8207-8 (case)
24 ISBN 0-8186-8208-6 (microfiche)
25 IEEE Order Plan Catalog Number 97CB36149
26 ISSN 1063-6404

27
28 *Additional copies may be ordered from:*

29
30 IEEE Computer Society
31 Customer Service Center
32 10662 Los Vaqueros Circle
33 P.O. Box 3014
34 Los Alamitos, CA 90720-1314
35 Tel: + 1-714-821-8380
36 Fax: + 1-714-821-4641
37 E-mail: cs.books@computer.org

38 IEEE Service Center
39 445 Hoes Lane
40 P.O. Box 1331
41 Piscataway, NJ 08855-1331
42 Tel: + 1-908-981-1393
43 Fax: + 1-908-981-9667
44 mis.custserv@computer.org

45 IEEE Computer Society
46 13, Avenue de l'Aquilon
47 B-1200 Brussels
48 BELGIUM
49 Tel: + 32-2-770-2198
50 Fax: + 32-2-770-8505
51 euro.ofc@computer.org

52 IEEE Computer Society
53 Ooshima Building
2-19-1 Minami-Aoyama
Minato-ku, Tokyo 107
JAPAN
Tel: + 81-3-3408-3118
Fax: + 81-3-3408-3553
tokyo.ofc@computer.org

54
55 Editorial production by Ian Torwick

56 Cover design by Joseph Daigle/Studio Productions

57 Printed in the United States of America by Technical Communication Services

58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
226
227
228
229
230
231
232
233
234
235
236
237
238
239
240
241
242
243
244
245
246
247
248
249
250
251
252
253
254
255
256
257
258
259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395
396
397
398
399
400
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451
452
453
454
455
456
457
458
459
460
461
462
463
464
465
466
467
468
469
470
471
472
473
474
475
476
477
478
479
480
481
482
483
484
485
486
487
488
489
490
491
492
493
494
495
496
497
498
499
500
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
529
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547
548
549
550
551
552
553
554
555
556
557
558
559
560
561
562
563
564
565
566
567
568
569
570
571
572
573
574
575
576
577
578
579
580
581
582
583
584
585
586
587
588
589
590
591
592
593
594
595
596
597
598
599
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646
647
648
649
650
651
652
653
654
655
656
657
658
659
660
661
662
663
664
665
666
667
668
669
670
671
672
673
674
675
676
677
678
679
680
681
682
683
684
685
686
687
688
689
690
691
692
693
694
695
696
697
698
699
700
701
702
703
704
705
706
707
708
709
710
711
712
713
714
715
716
717
718
719
720
721
722
723
724
725
726
727
728
729
730
731
732
733
734
735
736
737
738
739
740
741
742
743
744
745
746
747
748
749
750
751
752
753
754
755
756
757
758
759
760
761
762
763
764
765
766
767
768
769
770
771
772
773
774
775
776
777
778
779
780
781
782
783
784
785
786
787
788
789
790
791
792
793
794
795
796
797
798
799
800
801
802
803
804
805
806
807
808
809
810
811
812
813
814
815
816
817
818
819
820
821
822
823
824
825
826
827
828
829
830
831
832
833
834
835
836
837
838
839
840
841
842
843
844
845
846
847
848
849
850
851
852
853
854
855
856
857
858
859
860
861
862
863
864
865
866
867
868
869
870
871
872
873
874
875
876
877
878
879
880
881
882
883
884
885
886
887
888
889
890
891
892
893
894
895
896
897
898
899
900
901
902
903
904
905
906
907
908
909
910
911
912
913
914
915
916
917
918
919
920
921
922
923
924
925
926
927
928
929
930
931
932
933
934
935
936
937
938
939
940
941
942
943
944
945
946
947
948
949
950
951
952
953
954
955
956
957
958
959
960
961
962
963
964
965
966
967
968
969
970
971
972
973
974
975
976
977
978
979
980
981
982
983
984
985
986
987
988
989
990
991
992
993
994
995
996
997
998
999
1000



Table of Contents

ICCD '97 Conference Program

1997 Technical Program

Welcome to ICCD'97	xiv
Program Committee	xvi
Additional Referees	xix
 Session 1.1: Keynote Speech	
Intelligent RAM (IRAM): the Industrial Setting, Applications, and Architectures	2
<i>D. Patterson, K. Asanovic, A. Brown, R. Fromm, J. Golbus, B. Gribstad, K. Keeton, C. Kozyrakis, D. Martin, S. Perissakis, R. Thomas, N. Treuhft, and K Yelick, University of California at Berkeley, California</i>	
 Session 1.2: CAD Plenary	
<i>Chair: Andreas Kuehlmann, IBM T. J. Watson Research Center</i>	
A Brief History of the Future of Semiconductor Electronic Design Automation	10
<i>Ron Rohrer, TBD Consultants</i>	
 Concurrent Sessions 1.3	
 Session 1.3.1: Special Session: Industrial Applications of Formal Verification	
<i>Organizer and Chair: Andreas Kuehlmann, IBM T. J. Watson Research Center</i>	
Formal Implementation Verification of the Bus Interface Unit for the Alpha 21264 Microprocessor	16
<i>G.P. Bischoff, K.S. Brace, S. Jain, and R. Razdan</i>	
Intertwined Development and Formal Verification of a 60x bus Model	25
<i>M. Kaufmann and C. Pixley</i>	
Formally Specifying and Mechanically Verifying Programs for the Motorola Complex Arithmetic Processor DSP	31
<i>B.C. Brock and W.A. Hunt, Jr.</i>	
BIST-Based Fault Diagnosis in the Presence of Embedded Memories	37
<i>J. Savir</i>	
Built-in Self Test for Content Addressable Memories	48
<i>Y.-S. Kang, J.-C. Lee, and S. Kang</i>	
Pseudo-Random Pattern Testing of Bridging Faults	54
<i>N.A. Toubas and E.J. McCluskey</i>	
 Session 1.3.3: Simulation and Power Estimation	
<i>Chair: Teng-Sheng Moh, Silicon Valley Research, Inc.</i>	
Novel Simulation of Deep-Submicron MOSFET Circuits	62
<i>S. Bruma and R.H.J.M. Otten</i>	
Time-Stamped Transition Density for the Estimation of Delay Dependent Switching Activities	68
<i>H. Choi and S.H. Hwang</i>	

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53

Power Compiler: A Gate-Level Power Optimization and Synthesis System 74
B. Chen and I. Nedelchev

Session 1.3.4: Branch Prediction

Chair: Jim Bondi, Texas Instruments

Elastic History Buffer: A Low-Cost Method to Improve Branch
Prediction Accuracy 82

M.-D. Tarlescu, K.B. Theobald, and G.R. Gao

Design Optimization for High-Speed Per-address Two-level Branch Predictors 88

I.-C.K. Chen, C.-C. Lee, M.A. Postiff, and T.N. Mudge

PA-8000: A Case Study of Static and Dynamic Branch Prediction 97

C. Burch

Concurrent Sessions 1.4

Session 1.4.1: New Techniques for Gate-Sizing and Retiming

Chair: Derek Beatty, Motorola, Inc.

Discrete Drive Selection for Continuous Sizing 110

R. Haddad, L.P.P.P. van Ginneken, and N. Shenoy

Continuous Retiming: Algorithms and Applications 116

P. Pan

Optimal Clock Period Clustering for Sequential Circuits with Retiming 122

A.K. Karandikar, P. Pan, and C.L. Liu

Session 1.4.2: Circuit Modeling

Chair: Sandip Kundu, IBM Corp.

Comparison between nMOS Pass-Transistor logic style vs. CMOS
Complementary Cells 130

R. Mehrotra, M. Pedram, and X. Wu

Circuit-Based Description and Modeling of Electromagnetic Noise Effects
in Packaged Low-Power Electronics 136

A.C. Cangellaris, W. Pinello, and A. Ruehli

Transistor-Level Sizing and Timing Verification of Domino Circuits in the
Power PC Microprocessor 143

A. Dharchoudhury, D. Blaauw, J. Norton, S. Pullela, and J. Dunning

Session 1.4.3: Novel Architectures

Chair: Greg Fisher, Printronix Corporation

Architectural Adaptation for Application-Specific Locality Optimization 150

X. Zhang, A. Dasdan, M. Schulz, R.K. Gupta, and A.A. Chien

A New Processor Architecture for Digital Signal Transport Systems 157

M. Inamori, K. Ishii, A. Tsutsui, K. Shirakawa H. Nakada, and T. Miyazaki

Short Papers

PROPHID: A Heterogeneous Multi-Processor Architecture for Multimedia 164

J.A. Leijten, J.L. van Meerbergen, A.A. Timmer, and J.A.G. Jess

1		
2		
3		
4	Enhanced Compression Techniques to Simplify Program Decompression	
5	and Execution	170
6	<i>M. Breternitz, Jr. and R. Smith</i>	
7		
8	Session 1.4.4: Low Power Architectures	
9	Chair: Tim Brodnax, IBM	
10	A Low Power Approach to Floating Point Adder Design	178
11	<i>R.V.K. Pillai, D. Al-Khalili, and A.J. Al-Khalili</i>	
12	Design and Implementation of Low-Power Digit-Serial Multipliers	186
13	<i>Y.-N. Chang, J.H. Satyanarayana, and K.K. Parhi</i>	
14	On Complexity Reduction of FIR Digital Filters Using Constrained	
15	Least Squares Solution.....	196
16	<i>K. Muhammad and K. Roy</i>	
17		
18	Concurrent Session 1.5	
19		
20	Session 1.5.1: Timing Optimization for Deep Submicron Technology	
21	Chair: Masahiro Fujita, Fujitsu Laboratories of America	
22	An Integrated Placement and Synthesis Approach for Timing Closure of	
23	PowerPC™ Microprocessors	206
24	<i>S. Hojat and P. Villarrubia</i>	
25	Post-Layout Circuit Speed-up by Event Elimination.....	211
26	<i>H. Vaishnav, C.-K. Lee, and M. Pedram</i>	
27	Clustering and Load Balancing for Buffered Clock Tree Synthesis.....	217
28	<i>A.D. Mehta, Y.-P. Chen, N. Menezes, D.F. Wong, and L.T. Pileggi</i>	
29	CMOS Gate Delay Models for General RLC Loading	224
30	<i>R. Arunachalam, F. Dartu, and L.T. Pileggi</i>	
31		
32		
33	Session 1.5.2: Special Session: The G4 S/390 Microprocessor	
34	Organizer: Andreas Kuehlmann, IBM T. J. Watson Research Center	
35	Chair: Sumit Dasgupta, IBM	
36	Design Methodology for the High-Performance G4 S/390 Microprocessor	232
37	<i>K.L. Shepard, S. Carey, D.K. Beece, R. Hatch, and G. Northrop</i>	
38	A High-Frequency Custom CMOS S/390 Microprocessor	241
39	<i>C.F. Webb and J.S. Liptay</i>	
40	High Performance CMOS Circuit Techniques for the G-4 S/390 Microprocessor	247
41	<i>J. Warnock, L. Sigal, B. Curran, and Y. Chan</i>	
42	A 400 MHz, 144Kb CMOS ROM MACRO for an IBM S/390-Class Microprocessor.....	253
43	<i>A. Tuminaro</i>	
44		
45		
46	Session 1.5.3: Multiprocessor Communication	
47	Chair: Wai-Chi Fang, Jet Propulsion Laboratory	
48	A Comparative Evaluation of Hierarchical Network Architecture of the	
49	HP-Convex Exemplar	258
50	<i>R. Castaneda, X. Zhang, and J.M. Hoover, Jr.</i>	
51		
52		
53		

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.