UNITED STATES PATENT AND TRADEMA
BEFORE THE PATENT TRIAL AND APPE

INTEL CORPORATION and XILINX
Petitioners
v.
FG SRC LLC
Patent Owner

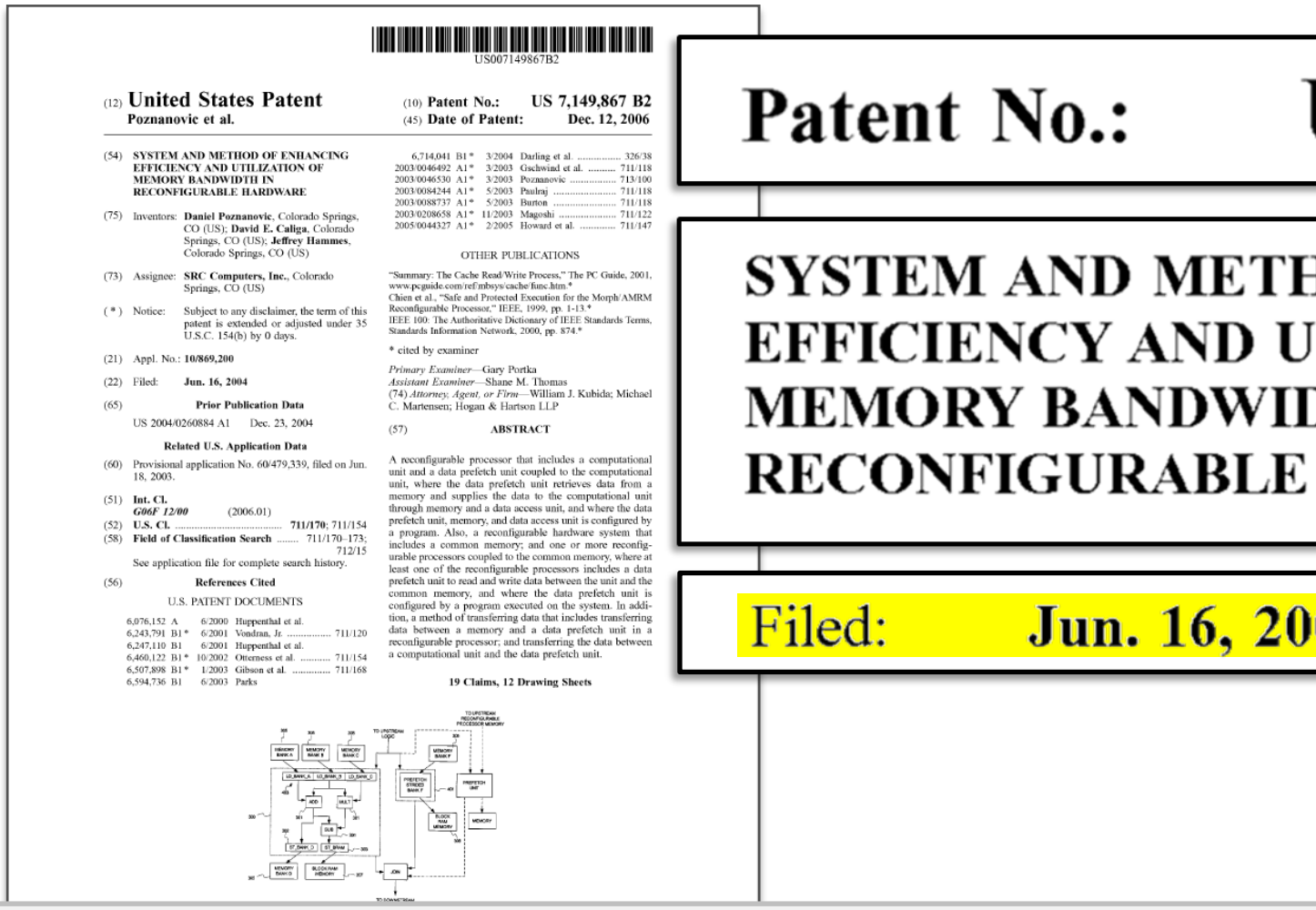
Case IPR2020-01449
U.S. Patent No. 7,149,867

PETITIONERS' DEMONSTRATIV

IPR2020-01449 – Pat. No. 7,149,86

- Overview of ’867 patent & asserted art
- Disputed issues
  - Zhang, Gupta, Chien are prior art
  - PO’s constructions for the “only” limitations
  - Instituted combination discloses each limitation
  - Secondary considerations
- PO’s Revised Motion to Amend

Overview: The ’867 Patent



US007149867B2

(12) **United States Patent**
Poznanovic et al.

(10) **Patent No.: US 7,149,867 B2**
(45) **Date of Patent: Dec. 12, 2006**

(54) **SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE**

(75) Inventors: **Daniel Poznanovic**, Colorado Springs, CO (US); **David E. Caliga**, Colorado Springs, CO (US); **Jeffrey Hammes**, Colorado Springs, CO (US)

(73) Assignee: **SRC Computers, Inc.**, Colorado Springs, CO (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/869,200**

(22) Filed: **Jun. 16, 2004**

(65) **Prior Publication Data**

US 2004/0260884 A1 Dec. 23, 2004

Related U.S. Application Data

(60) Provisional application No. 60/479,339, filed on Jun. 18, 2003.

(51) **Int. Cl.**
G06F 12/00 (2006.01)

(52) **U.S. Cl.** **711/170**; 711/154

(58) **Field of Classification Search** 711/170–173; 712/15

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,076,152 A 6/2000 Huppenthal et al.
6,243,791 B1 * 6/2001 Vondran, Jr. 711/120
6,247,110 B1 6/2001 Huppenthal et al.
6,460,122 B1 * 10/2002 Otterness et al. 711/154
6,507,898 B1 * 1/2003 Gibson et al. 711/168
6,594,736 B1 6/2003 Parks
6,714,041 B1 * 3/2004 Darling et al. 326/38
2003/0046492 A1 * 3/2003 Gschwind et al. 711/118
2003/0046530 A1 * 3/2003 Poznanovic 713/100
2003/0084244 A1 * 5/2003 Paulraj 711/118
2003/0088737 A1 * 5/2003 Burton 711/118
2003/0208658 A1 * 11/2003 Magoshi 711/122
2005/0044327 A1 * 2/2005 Howard et al. 711/147

OTHER PUBLICATIONS

"Summary: The Cache Read/Write Process," The PC Guide, 2001, www.pcguide.com/ref/mbsys/cache/func.htm.*
Chien et al., "Safe and Protected Execution for the Morph/AMRM Reconfigurable Processor," IEEE, 1999, pp. 1-13.*
IEEE 100: The Authoritative Dictionary of IEEE Standards Terms, Standards Information Network, 2000, pp. 874.*

* cited by examiner

Primary Examiner—Gary Portka
Assistant Examiner—Shane M. Thomas
(74) *Attorney, Agent, or Firm*—William J. Kubida; Michael C. Martensen; Hogan & Hartson LLP

(57) **ABSTRACT**

A reconfigurable processor that includes a computational unit and a data prefetch unit coupled to the computational unit, where the data prefetch unit retrieves data from a memory and supplies the data to the computational unit through memory and a data access unit, and where the data prefetch unit, memory, and data access unit is configured by a program. Also, a reconfigurable hardware system that includes a common memory; and one or more reconfigurable processors coupled to the common memory, where at least one of the reconfigurable processors includes a data prefetch unit to read and write data between the unit and the common memory, and where the data prefetch unit is configured by a program executed on the system. In addition, a method of transferring data that includes transferring data between a memory and a data prefetch unit in a reconfigurable processor; and transferring the data between a computational unit and the data prefetch unit.

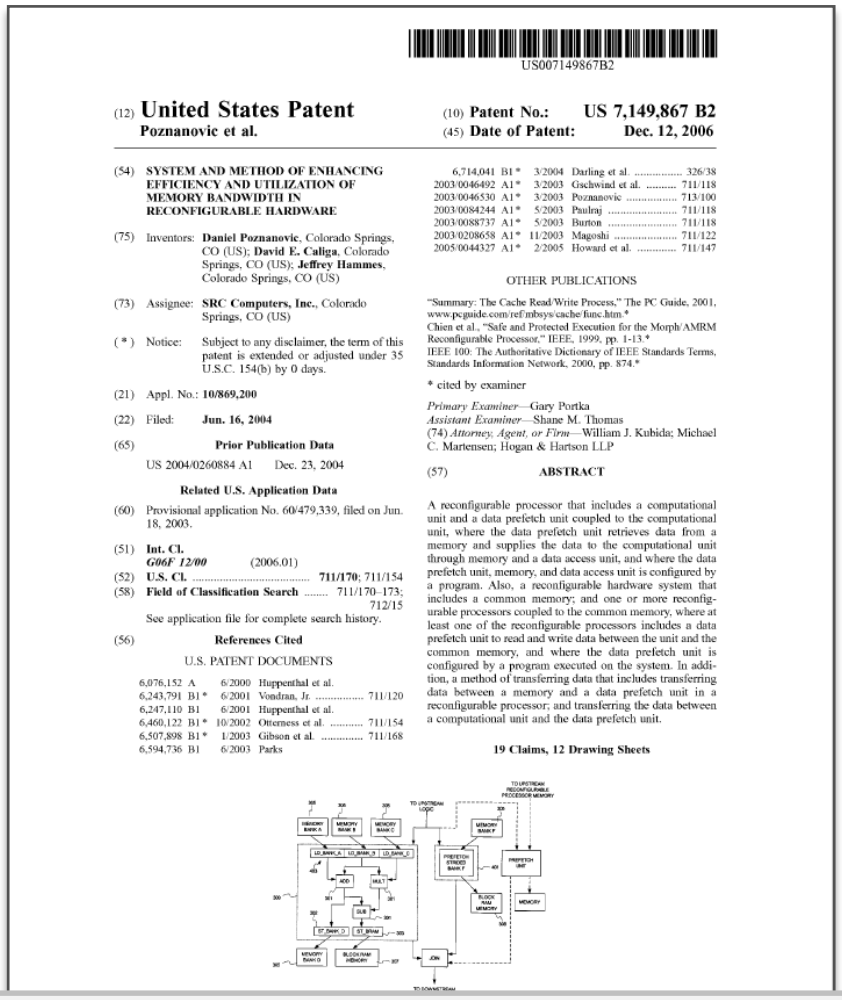
19 Claims, 12 Drawing Sheets

Patent No.:

SYSTEM AND METH
EFFICIENCY AND U
MEMORY BANDWII
RECONFIGURABLE

Filed: **Jun. 16, 20**

Overview: The ’867 Patent



US007149867B2

(12) **United States Patent**
Poznanovic et al.

(10) **Patent No.: US 7,149,867 B2**
(45) **Date of Patent: Dec. 12, 2006**

(54) **SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE**

(75) Inventors: **Daniel Poznanovic**, Colorado Springs, CO (US); **David E. Caliga**, Colorado Springs, CO (US); **Jeffrey Hammes**, Colorado Springs, CO (US)

(73) Assignee: **SRC Computers, Inc.**, Colorado Springs, CO (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/869,200**

(22) Filed: **Jun. 16, 2004**

(65) **Prior Publication Data**

US 2004/0260884 A1 Dec. 23, 2004

Related U.S. Application Data

(60) Provisional application No. 60/479,339, filed on Jun. 18, 2003.

(51) **Int. Cl.**
G06F 12/00 (2006.01)

(52) **U.S. Cl.** **711/170**; 711/154

(58) **Field of Classification Search** 711/170–173; 712/15

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,076,152 A 6/2000 Huppenthal et al.
6,243,791 B1 * 6/2001 Vondran, Jr. 711/120
6,247,110 B1 6/2001 Huppenthal et al.
6,460,122 B1 * 10/2002 Otterness et al. 711/154
6,507,898 B1 * 1/2003 Gibson et al. 711/168
6,594,736 B1 6/2003 Parks
6,714,041 B1 * 3/2004 Darling et al. 326/38
2003/0046492 A1 * 3/2003 Gschwind et al. 711/118
2003/0046530 A1 * 3/2003 Poznanovic 713/100
2003/0084244 A1 * 5/2003 Paulraj 711/118
2003/0088737 A1 * 5/2003 Burton 711/118
2003/0208658 A1 * 11/2003 Magoshi 711/122
2005/0044327 A1 * 2/2005 Howard et al. 711/147

OTHER PUBLICATIONS

"Summary: The Cache Read/Write Process," The PC Guide, 2001, www.pcguide.com/ref/mbsys/cache/func.htm.*
Chien et al., "Safe and Protected Execution for the Morph/AMRM Reconfigurable Processor," IEEE, 1999, pp. 1-13.*
IEEE 100: The Authoritative Dictionary of IEEE Standards Terms, Standards Information Network, 2000, pp. 874.*

* cited by examiner

Primary Examiner—Gary Portka
Assistant Examiner—Shane M. Thomas
(74) *Attorney, Agent, or Firm*—William J. Kubida; Michael C. Martensen; Hogan & Hartson LLP

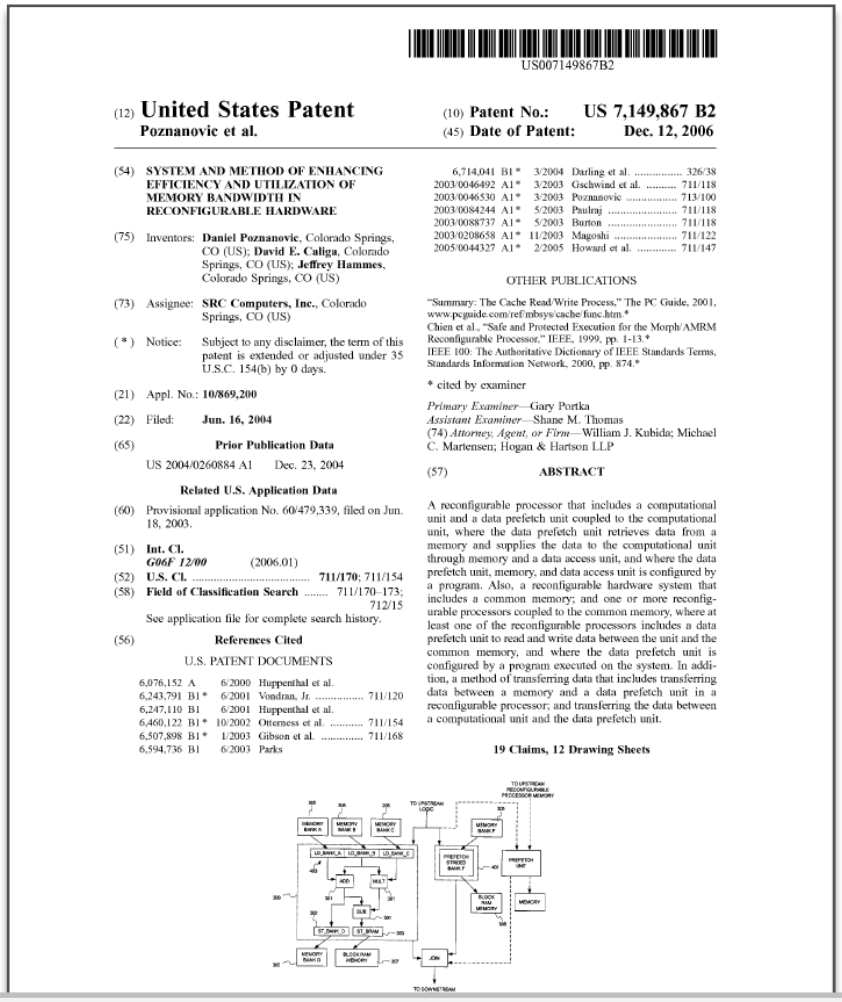
(57) **ABSTRACT**

A reconfigurable processor that includes a computational unit and a data prefetch unit coupled to the computational unit, where the data prefetch unit retrieves data from a memory and supplies the data to the computational unit through memory and a data access unit, and where the data prefetch unit, memory, and data access unit is configured by a program. Also, a reconfigurable hardware system that includes a common memory; and one or more reconfigurable processors coupled to the common memory, where at least one of the reconfigurable processors includes a data prefetch unit to read and write data between the unit and the common memory, and where the data prefetch unit is configured by a program executed on the system. In addition, a method of transferring data that includes transferring data between a memory and a data prefetch unit in a reconfigurable processor; and transferring the data between a computational unit and the data prefetch unit.

19 Claims, 12 Drawing Sheets

- Key element
  - Reconfigurab
    instantiates a
  - One or more
  - Data prefetcl
    - retrieves (re
      computatio
    - “configured
    - operates in
      with compu
      using compu

Overview: The ’867 Patent



US007149867B2

(12) **United States Patent**
Poznanovic et al.

(10) **Patent No.: US 7,149,867 B2**
(45) **Date of Patent: Dec. 12, 2006**

(54) **SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE**

(75) Inventors: **Daniel Poznanovic**, Colorado Springs, CO (US); **David E. Caliga**, Colorado Springs, CO (US); **Jeffrey Hammes**, Colorado Springs, CO (US)

(73) Assignee: **SRC Computers, Inc.**, Colorado Springs, CO (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/869,200**

(22) Filed: **Jun. 16, 2004**

(65) **Prior Publication Data**

US 2004/0260884 A1 Dec. 23, 2004

Related U.S. Application Data

(60) Provisional application No. 60/479,339, filed on Jun. 18, 2003.

(51) **Int. Cl.**
G06F 12/00 (2006.01)

(52) **U.S. Cl.** **711/170**; 711/154

(58) **Field of Classification Search** 711/170–173; 712/15

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,076,152 A 6/2000 Huppenthal et al.
6,243,791 B1 * 6/2001 Vondran, Jr. 711/120
6,247,110 B1 6/2001 Huppenthal et al.
6,460,122 B1 * 10/2002 Otterness et al. 711/154
6,507,898 B1 * 1/2003 Gibson et al. 711/168
6,594,736 B1 6/2003 Parks
6,714,041 B1 * 3/2004 Darling et al. 326/38
2003/0046492 A1 * 3/2003 Gschwind et al. 711/118
2003/0046530 A1 * 3/2003 Poznanovic 713/100
2003/0084244 A1 * 5/2003 Paulraj 711/118
2003/0088737 A1 * 5/2003 Burton 711/118
2003/0208658 A1 * 11/2003 Magoshi 711/122
2005/0044327 A1 * 2/2005 Howard et al. 711/147

OTHER PUBLICATIONS

"Summary: The Cache Read/Write Process," The PC Guide, 2001, www.pcguide.com/ref/mbsys/cache/func.htm.*
Chien et al., "Safe and Protected Execution for the Morph/AMRM Reconfigurable Processor," IEEE, 1999, pp. 1-13.*
IEEE 100: The Authoritative Dictionary of IEEE Standards Terms, Standards Information Network, 2000, pp. 874.*

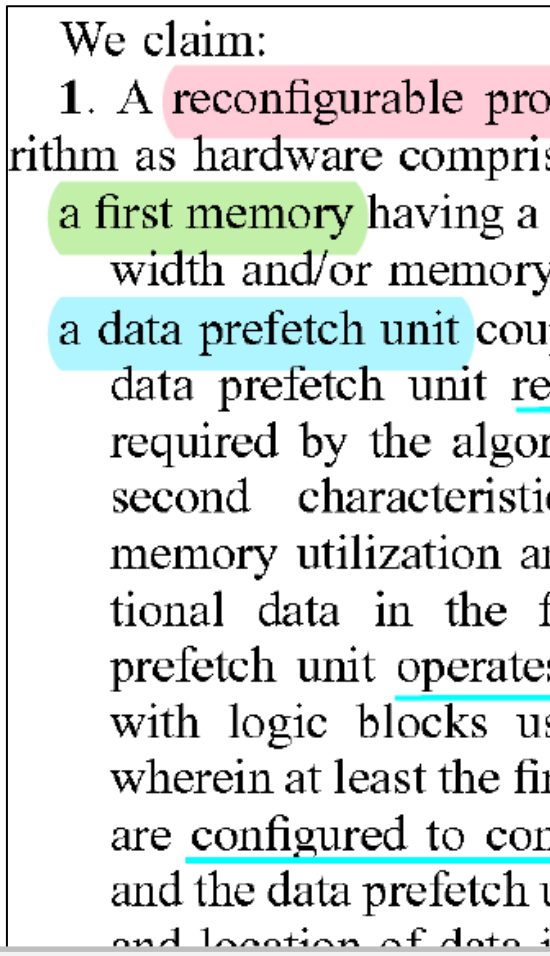
* cited by examiner

Primary Examiner—Gary Portka
Assistant Examiner—Shane M. Thomas
(74) *Attorney, Agent, or Firm*—William J. Kubida; Michael C. Martensen; Hogan & Hartson LLP

(57) **ABSTRACT**

A reconfigurable processor that includes a computational unit and a data prefetch unit coupled to the computational unit, where the data prefetch unit retrieves data from a memory and supplies the data to the computational unit through memory and a data access unit, and where the data prefetch unit, memory, and data access unit is configured by a program. Also, a reconfigurable hardware system that includes a common memory; and one or more reconfigurable processors coupled to the common memory, where at least one of the reconfigurable processors includes a data prefetch unit to read and write data between the unit and the common memory, and where the data prefetch unit is configured by a program executed on the system. In addition, a method of transferring data that includes transferring data between a memory and a data prefetch unit in a reconfigurable processor; and transferring the data between a computational unit and the data prefetch unit.

19 Claims, 12 Drawing Sheets



We claim:

1. A reconfigurable pro
rithm as hardware compris
a first memory having a
width and/or memory
a data prefetch unit cou
data prefetch unit re
required by the algor
second characteristi
memory utilization a
tional data in the f
prefetch unit operates
with logic blocks us
wherein at least the fi
are configured to con
and the data prefetch u
and location of data i

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.