

UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE PATENT TRIAL AND APPEALS BOARD

INTEL CORPORATION and XILINX  
Petitioners

v.

FG SRC LLC  
Patent Owner

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Case IPR2020-01449  
U.S. Patent No. 7,149,867

PETITIONERS' DEMONSTRATIVE

# IPR2020-01449 – Pat. No. 7,149,867

- Overview of '867 patent & asserted art
- Disputed issues
  - Zhang, Gupta, Chien are prior art
  - PO's constructions for the "only" limitations
  - Instituted combination discloses each limitation
  - Secondary considerations
- PO's Revised Motion to Amend

# Overview: The '867 Patent



US007149867B2

(12) **United States Patent**  
**Poznanovic et al.**

(10) **Patent No.:** US 7,149,867 B2  
 (45) **Date of Patent:** Dec. 12, 2006

(54) **SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE**

(75) **Inventors:** Daniel Poznanovic, Colorado Springs, CO (US); David E. Calliga, Colorado Springs, CO (US); Jeffrey Hammes, Colorado Springs, CO (US)

(73) **Assignee:** SRC Computers, Inc., Colorado Springs, CO (US)

(\* ) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) **Appl. No.:** 10/869,200  
 (22) **Filed:** Jun. 16, 2004

(65) **Prior Publication Data**  
 US 2004/0260884 A1 Dec. 23, 2004

**Related U.S. Application Data**

(60) **Provisional application No. 60/479,339, filed on Jun. 18, 2003.**

(51) **Int. Cl.**  
**G06F 12/00** (2006.01)

(52) **U.S. Cl.** 711/170; 711/154

(58) **Field of Classification Search** 711/170-173; 712/15

See application file for complete search history.

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"Summary: The Cache Read/Write Process," The PC Guide, 2001, www.pcguide.com/ref/mboys/cache/func.htm.\*  
 Chien et al., "Safe and Protected Execution for the Morph/AMRM Reconfigurable Processor," IEEE, 1999, pp. 1-13.\*  
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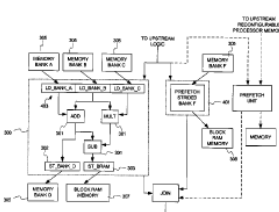
\* cited by examiner

**Primary Examiner**—Gary Portka  
**Assistant Examiner**—Shane M. Thomas  
 (74) **Attorney, Agent, or Firm**—William J. Kubida; Michael C. Martensen; Hogan & Hartson LLP

(57) **ABSTRACT**

A reconfigurable processor that includes a computational unit and a data prefetch unit coupled to the computational unit, where the data prefetch unit retrieves data from a memory and supplies the data to the computational unit through memory and a data access unit, and where the data prefetch unit, memory, and data access unit is configured by a program. Also, a reconfigurable hardware system that includes a common memory; and one or more reconfigurable processors coupled to the common memory, where at least one of the reconfigurable processors includes a data prefetch unit to read and write data between the unit and the common memory, and where the data prefetch unit is configured by a program executed on the system. In addition, a method of transferring data that includes transferring data between a memory and a data prefetch unit in a reconfigurable processor; and transferring the data between a computational unit and the data prefetch unit.

**19 Claims, 12 Drawing Sheets**




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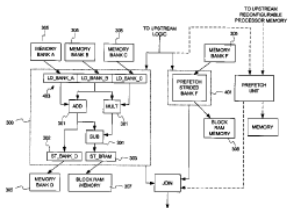
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(19) **Claims, 12 Drawing Sheets**


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A reconfigurable processor that includes a computational unit and a data prefetch unit coupled to the computational unit, where the data prefetch unit retrieves data from a memory and supplies the data to the computational unit through memory and a data access unit, and where the data prefetch unit, memory, and data access unit is configured by a program. Also, a reconfigurable hardware system that includes a common memory; and one or more reconfigurable processors coupled to the common memory, where at least one of the reconfigurable processors includes a data prefetch unit to read and write data between the unit and the common memory, and where the data prefetch unit is configured by a program executed on the system. In addition, a method of transferring data that includes transferring data between a memory and a data prefetch unit in a reconfigurable processor; and transferring the data between a computational unit and the data prefetch unit.



- Key elements
  - Reconfigurable hardware system instantiates a
  - One or more
  - Data prefetch
  - retrieves (re) data from computational
  - “configured”
  - operates in conjunction with computational unit using comp

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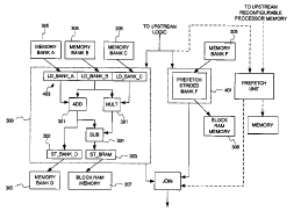
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19 Claims, 12 Drawing Sheets



We claim:

1. A reconfigurable processor comprising a first memory having a memory bandwidth and/or memory depth, a data prefetch unit coupled to the first memory, the data prefetch unit required by the algorithm, a second characteristic memory utilization and additional data in the first memory, the data prefetch unit operates with logic blocks used wherein at least the first memory are configured to control and the data prefetch unit and location of data is

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