

IPR2020-01449
U.S. Patent No. 7,149,867
Patent Owner, FG SRC LLC

Oral Argument Demonstrative

Patent Trial and Appeal Board
January 6, 2022

Demonstrative Exhibits – Not Evidence

The Revised Amended Claims

- Petitioner challenges ALL 19 claims
- PO offers 4 Revised Amended Claims
 - claims 20 and 21 replacing claim 1
 - claim 28 replacing claim 9
 - claim 32 replacing claim 13
- The remaining claims are amended virtue of depending from an amended

Demonstrative Exhibits – Not Evidence

THE REVISED AMENDED CLAIMS

Demonstrative Exhibits – Not Evidence

The Revised Amended Claims

- 20. A reconfigurable processor that instantiates an algorithm as h comprising:
- a first memory having a first characteristic memory bandwidth and utilization; and
- a data prefetch unit coupled to the memory, wherein the data pre retrieves only computational data required by the a second memory of second characteristic memory bandwidth and utilization and places the retrieved computational data in the first wherein the data prefetch unit operates independent of and in pa blocks using the computational data, and wherein at least the first data prefetch unit are configured to conform to needs of the algo data prefetch unit is configured to match format and location of d second memory,
- **wherein the reconfigurable processor is neither integrated w comprises a conventional microprocessor, and**
- **wherein the reconfigurable processor operates independent parallel with a conventional microprocessor.**

Demonstrative Exhibits – Not Evidence

The Revised Amended Claims

- 21. A reconfigurable processor that instantiates an algorithm as h comprising:
- a first memory having a first characteristic memory bandwidth and utilization; and
- a data prefetch unit coupled to the memory, wherein the data pre **configured to** retrieves only computational data required by the a second memory of second characteristic memory bandwidth and utilization and places the retrieved computational data in the first wherein the data prefetch unit operates independent of and in pa blocks using the computational data, and wherein at least the first data prefetch unit are configured to conform to needs of the algo data prefetch unit is configured to match format and location of d second memory,
- **wherein the reconfigurable processor is neither integrated w comprises a conventional microprocessor, and**
- **wherein the reconfigurable processor operates independent parallel with a conventional microprocessor.**

Demonstrative Exhibits – Not Evidence

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