UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

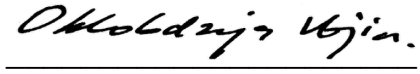
v.

FG SRC LLC,
Patent Owner.

IPR2020-01449
Patent No. 7,149,867

DECLARATION OF VOJIN G. OKLOBDZIJA, PH.D., IN SUPPORT OF FG SRC LLC'S PRELIMINARY RESPONSE

I, Dr. Vojin G. Oklobdzija, under the penalty of perjury under the laws of the United States, declare that the following is true and correct based on the best of my ability.

Date: 4 December 2020 Signed: 

VOJIN G. OKLOBDZIJA, PH.D.

1. I have been retained by DiMuro Ginsberg, P.C., as an independent technical expert in the Expert in the Inter Partes Review dispute between FG SRC, and Intel Corp, case, No. IPR2020-01449 which involves U.S. Patent No. 7,149,867 ("the '867 Patent").

2. I have been paid for my work as a technical expert at my rate of $500 per hour. My compensation does not in any way depend on the outcome of this review, and I have no personal interest in the outcome of this review.

I. Qualifications

3. I am an expert in the field of digital integrated circuit design. I have over 45 years of relevant design experience working in the field of electrical engineering: analog and digital design, processor and microprocessor design, testing, optimization and performance.

4. I hold a Master of Science (1978) and PhD (1982) in Computer Sciences with minor in Electronics, from UCLA, and a Dipl. Ing. (MSEE equivalent), in Electronics and Telecommunications, from the University of Belgrade, Yugoslavia (1971).

5. My career spans 4 years at Xerox Microelectronics, 9 years at IBM T. J. Watson Research Center, over 20 years in academia, and 28 years as a consultant. At IBM I have been involved in two parallel computer projects: GF-11, which was 560 processor parallel computer, which held a world record in 1989

of 11 Giga Flop peak performance, and TF-1, the first machine to achieve 1 Terra-Flop peak performance, containing 32,000 processors.

6. I have consulted extensively in the areas of microprocessor design and architecture for the Silicon Valley companies such as Sun Microsystems, Bell Laboratories, Texas Instruments, Hitachi, Fujitsu, Siemens, Sony, Intel, Samsung, and others that are listed in my CV.

7. I am currently a Professor Emeritus at the University of California, Davis, continuing my research activities, reviewing papers, and attending conferences and seminars. In academia I have taught courses in computer architecture, digital design, high-performance computer architecture and specialty courses in computer engineering at several prestigious universities world-wide (see my CV, Attachment A.).

8. I have been designing microprocessors for over 40 years. My current work involves design and optimization of processors used in machine learning. I have done extensive work on the CPU and memory architecture while working for Skyera Inc, a Silicon Valley startup company.

9. From 1991 to 2006, I was a tenured Full Professor at the University of California, Davis. While there, I established a Computer Engineering (CE) program in the Electrical Engineering Department, which later became the Electrical and Computer Engineering Department to reflect the addition of

Computer Engineering. I taught all the important courses in the CE curriculum, such as Digital Systems I and Digital Systems II, Computer Architecture, Assembly Language and Computer Organization, Digital Integrated Circuits, and graduate courses, such as Advanced Logic Design, Computer Architecture, High-Performance Computer Architecture and Computer Arithmetic. During my tenure at other universities, I also taught courses in Computer Architecture, VLSI Design, Low-Power VLSI Circuits Design, and Digital Logic Design.

10. I established digital design laboratory at U.C. Davis where FPGA chips were used to implement student design projects. I supervised and created laboratory exercises including use of FPGA. In 1995 I attended the first Workshop on FPGA held at Napa Valley and I wrote a funding proposal for a project in reconfigurable computing. I proposed reconfigurable computing elements which will adopt to the most optimal topology as the computation requirements change.

11. I started the Advanced Computer System Engineering Laboratory (ACSEL), at the University of California, Davis in 1992. ACSEL consisted of my graduate students, professors associated with the group, industrial researchers, and past doctoral students. ACSEL has been working on the problems associated with computer system design.

12. Since 1995, I have been a Fellow of IEEE (Institute of Electrical and Electronics Engineers), a professional organization with over 400,000 members in

more than 160 countries. IEEE states: "*IEEE Fellow is a distinction reserved for select IEEE members whose extraordinary accomplishments in any of the IEEE fields of interest are deemed fitting of this prestigious grade elevation.*" No more than 0.1% of the IEEE voting membership on record may be elevated to Fellow in a year. Since 2015, I have been a Life Fellow of IEEE.

13. From 2014 to 2016, I served as President of IEEE Circuits and Systems Society, one of the oldest IEEE Societies. I served for 8 years on the IEEE Technical Activities Board, as Vice President for Technical Activities, and Chair of Vision Committee of IEEE Circuits and Systems Society prior to 2014.

14. Upon my retirement as a university professor in 2012, I returned to work full-time in the industry. I joined Skyera Inc. (Skyera), a startup in San Jose, California, where I had the title of Senior Director, Processor Design. I managed a group of engineers involved in designing a proprietary processor for Skyera Inc. Skyera processor consisted of many CPUs on the chip and an efficient memory architecture was very important.

15. When Skyera was acquired in 2014 by Hitachi, I started working as a consultant for Wave Semi Inc., again on the multi CPU chip design. My work was on the CPU and arithmetic elements of the processor.

16. In December of 2015 I started working with Esperanto Technologies Inc. (Esperanto Tech.), a startup company working on a "machine-learning" chip

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