United States Patent [19]

Trimberger

[54] **REPROGRAMMABLE INSTRUCTION SET ACCELERATOR**

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[*] Notice: The term of this patent shall not extend beyond the expiration date of Pat. No. 5,737,631.

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[51] Int. Cl.^{6} **G06F 15/76**; G06F 9/30
[52] U.S. Cl. **395/800.37**; 395/376
[58] Field of Search 395/430, 384, 395/385, 386, 387, 388, 389, 800.37, 376; 326/39

[56] **References Cited**

U.S. PATENT DOCUMENTS

Re. 34,363	8/1993	Freeman	307/465
5,109,503	4/1992	Cruickshank et al.	395/500
5,301,344	4/1994	Kolchinsky	395/800
5,321,845	6/1994	Sawase et al.	395/800
5,336,950	8/1994	Popli et al.	307/465
5,361,373	11/1994	Gilson	395/800
5,386,518	1/1995	Reagle et al.	395/325
5,430,734	7/1995	Gilson	371/22.2
5,471,593	11/1995	Branigin	395/375
5,511,173	4/1996	Yamaura et al.	395/375
5,517,628	5/1996	Morrison et al.	395/375
5,535,406	7/1996	Kolchinsky	395/800
5,537,601	7/1996	Kimura et al.	395/800
5,574,930	11/1996	Halverson, Jr. et al.	395/800

OTHER PUBLICATIONS

DeHon, A. "DPGA–Coupled Microprocessors: Commodity ICs for the Early 21st Century", M.I.T. Transit Project, Transit Note #100, from internet site http://www.ai.mit.edu/projects/transit/tn100/tn100.html, Jan. 29, 1994.

French, P. et al. "A Self–Reconfiguring Processor", Proceedings from 1993 Workshop on FPGAs for Custom Computing Machines, IEEE, pp. 50–59, 1993.

(List continued on next page.)

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[57] **ABSTRACT**

A microprocessor comprises a defined execution unit coupled to internal buses of the processor for execution of a predefined set of instructions, combined with a programmable execution unit coupled to the internal buses for execution of a programmed instruction providing an on chip reprogrammable instruction set accelerator RISA. The programmable execution unit may be made using a field programmable gate array having a configuration store, and resources for accessing the configuration store to program the programmable execution unit. An instruction register is included in the data processor which holds a current instruction for execution, and is coupled to an instruction data path to supply the instruction to the defined instruction unit and to the programmable instruction unit in parallel, through appropriate decoding resources. A condition code register is coupled to instruction fetching resources, and connected to receive condition codes from both the defined execution unit and from the programmable execution unit. The programmable execution unit includes logic to signal the instruction fetching resources to provide a next instruction when execution of the programmed instruction is done. Resources for accessing the configuration store to program the programmable execution unit are provided, which can utilize the internal buses of the data processor or be completely independent of them.
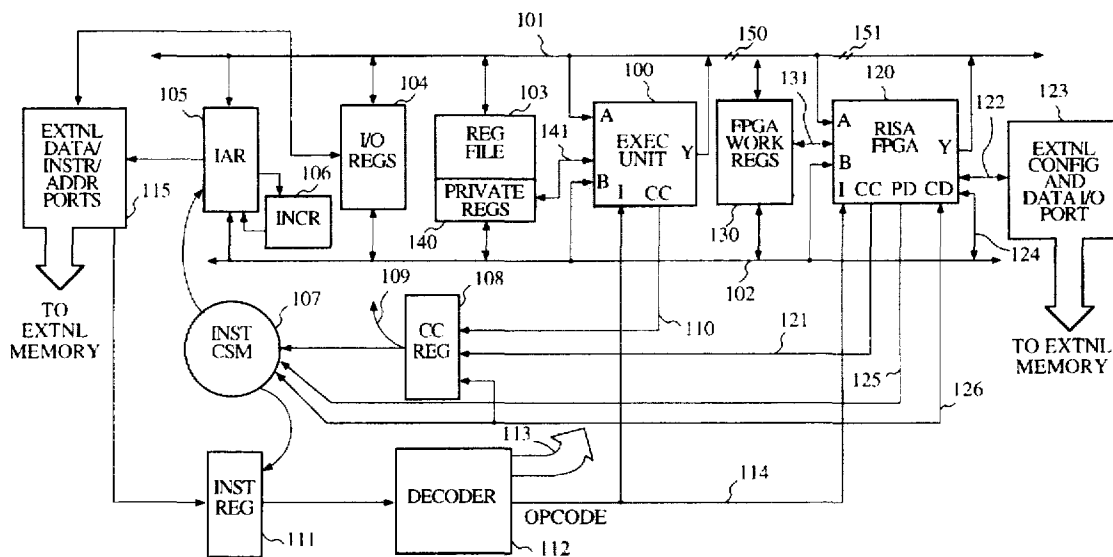
40 Claims, 3 Drawing Sheets

Iseli, C. et al. "Spyder: A Reconfigurable VLIW Processor using FPGAs", Proceedings from 1993 Workshop on FPGAs for Custom Computing Machines, IEEE, pp. 17–24, 1993.

Casselman, S. "Virtual Computing and The Virtual Computer", Proceedings from 1993 Workshop on FPGAsfro Custom Computing Machines, pp. 43–48, 1993.

Trimberger, S. "A Reprogrammable Gate Array and Applications", Proceedings of the IEEE, pp. 1030–1041, Jul. 1993.

Hennessy J. et al. Computer Architecture: A Quantitative Approach, Chapter 5, Appendix E, 1990.

Box, B., "Field Programmable Gate Array Based Reconfigurable Preprocessor", Apr. 10, 1994; IEEE, pp. 40–48.

DeHon, A., "DPGA–Coupled Microprocessors: Commodity ICs for the Early 21st Century", Apr. 10, 1994, IEEE, pp. 31–39.

Thorson, M., "General–Purpose Coprocessors", E–Mail Transcript, Jul. 3, 1992, 5 pages.

Razdan, R., "PRISC: Programmable Reduced Instruction Set Computers", Doctor of Philosophy Thesis, May 1994, 116 pages.

Razdan, R.; Brace, K; and Smith, M.; "PRISC Software Acceleration Techniques", IEEE, May 1994, pp. 145–149.

Trimberger, S., "Field–Programmable Gate Array Technology", Design Applications, Section 2.6, pp. 68–90, Copyright 1994.

Wirthlin, M., Hutchings, Brad, Gilson, K., "The Nano Processor: a Low Resource Reconfigurable Processor", Apr. 10, 1994, IEEE, pp. 23–30.
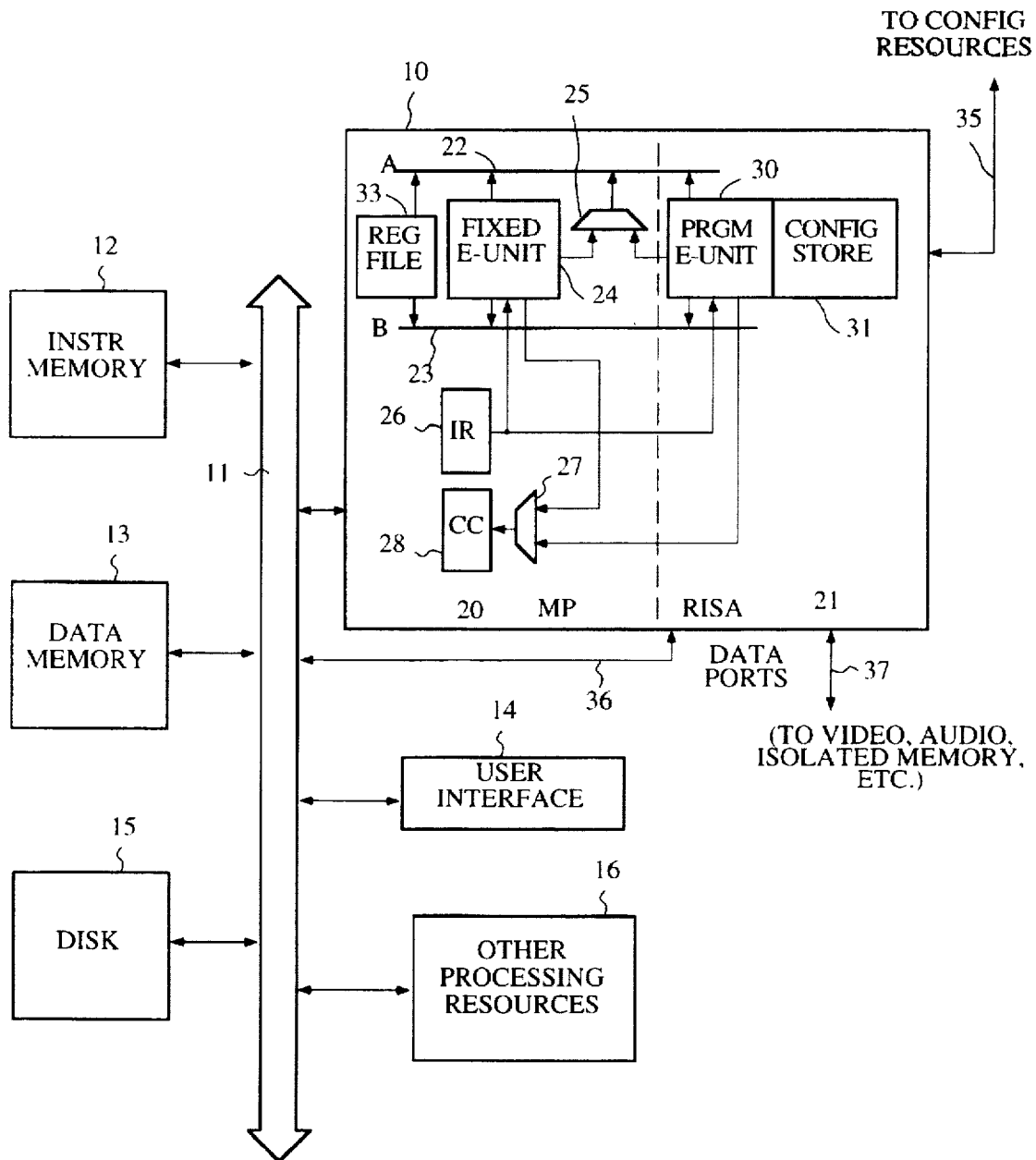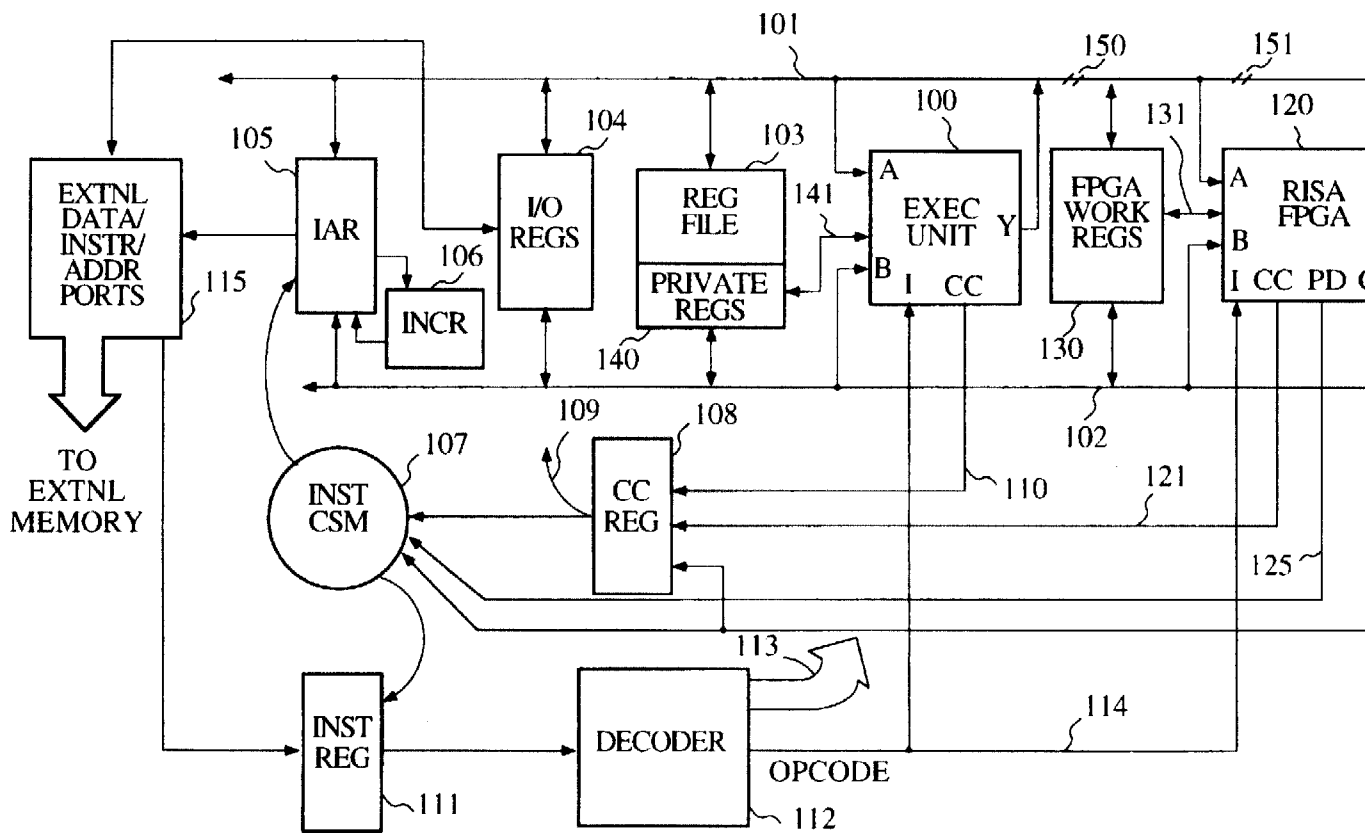
FIG. 1

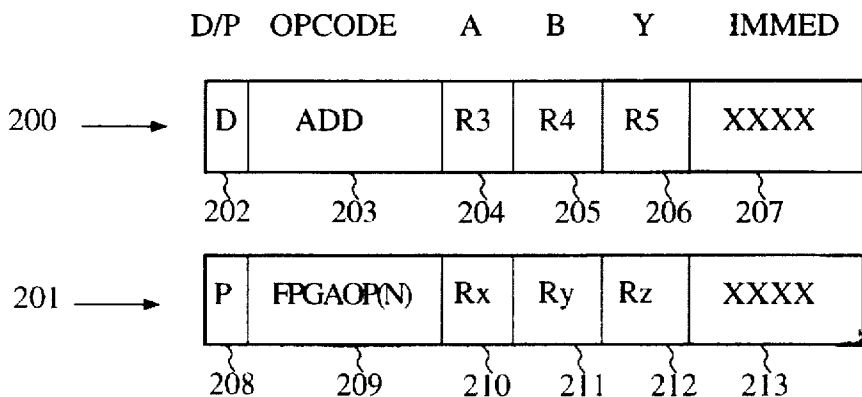**FIG. 2**

D/P	OPCODE	A	B	Y	IMMED
D	ADD	R3	R4	R5	XXXX

200 →

202   203   204   205   206   207

D/P	OPCODE	A	B	Y	IMMED
P	FPGAOP(N)	Rx	Ry	Rz	XXXX

201 →

208   209   210   211   212   213

FIG. 3

OPCODE	A	B	Y	IMMED
ADD	R3	R4	R5	XXXX

250 →

251   252   253   254   255

OPCODE	A	B	Y	IMMED
FPGAOP	Rx	Ry	Rz	PGMD OPCODE

256 →

257   258   259   260   261

FIG. 4

FIXED OPCODE	A	B	Y	PGM OPCODE	C	IMMED
AND	R3	R4	R5	FPGAOP(N)	R22	XXXX

270   271   272   273   274   275   276

FIG. 5

DOCKET ALARM
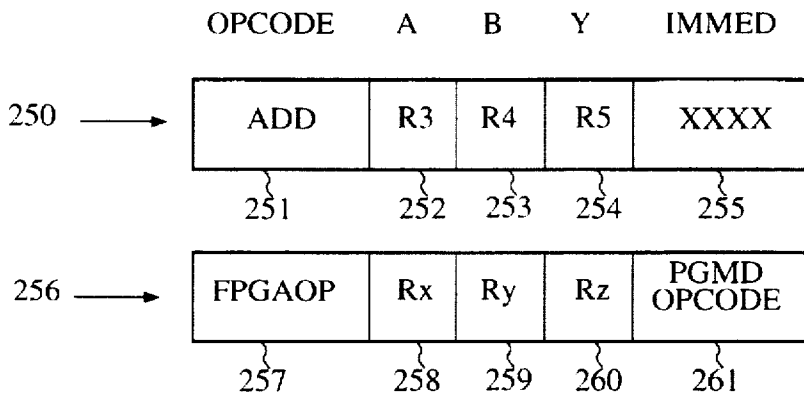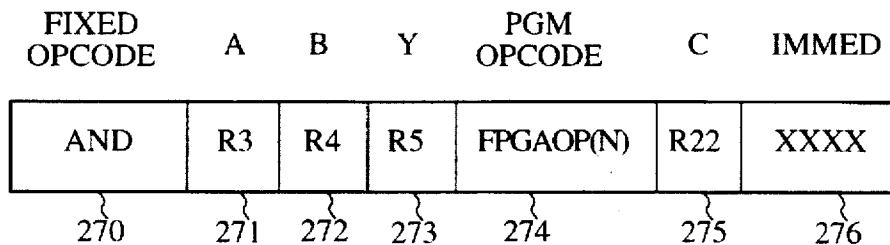
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