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United States Patent [19]

Trimberger

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[54] **REPROGRAMMABLE INSTRUCTION SET ACCELERATOR**

[76] Inventor: **Stephen M. Trimberger**, 1261 Chateau Dr., San Jose, Calif. 95120

[*] Notice: The term of this patent shall not extend beyond the expiration date of Pat. No. 5,737,631.

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[22] Filed: **Apr. 5, 1995**

[51] **Int. Cl.**[6] **G06F 15/76**; G06F 9/30

[52] **U.S. Cl.** **395/800.37**; 395/376

[58] **Field of Search** 395/430, 384, 395/385, 386, 387, 388, 389, 800.37, 376; 326/39

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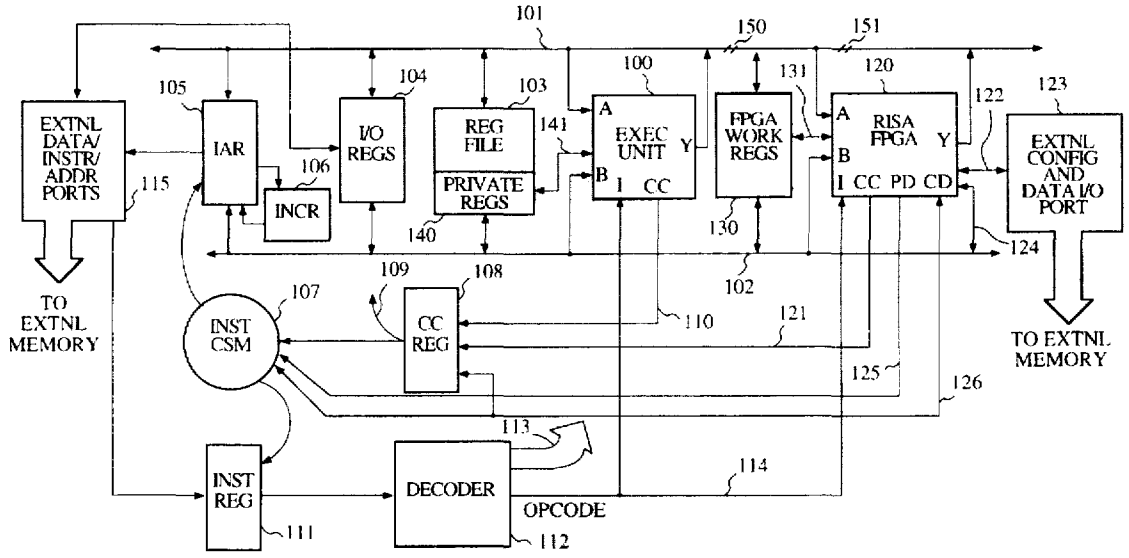
[57] **ABSTRACT**

A microprocessor comprises a defined execution unit coupled to internal buses of the processor for execution of a predefined set of instructions, combined with a programmable execution unit coupled to the internal buses for execution of a programmed instruction providing an on chip reprogrammable instruction set accelerator RISA. The programmable execution unit may be made using a field programmable gate array having a configuration store, and resources for accessing the configuration store to program the programmable execution unit. An instruction register is included in the data processor which holds a current instruction for execution, and is coupled to an instruction data path to supply the instruction to the defined instruction unit and to the programmable instruction unit in parallel, through appropriate decoding resources. A condition code register is coupled to instruction fetching resources, and connected to receive condition codes from both the defined execution unit and from the programmable execution unit. The programmable execution unit includes logic to signal the instruction fetching resources to provide a next instruction when execution of the programmed instruction is done. Resources for accessing the configuration store to program the programmable execution unit are provided, which can utilize the internal buses of the data processor or be completely independent of them.

40 Claims, 3 Drawing Sheets



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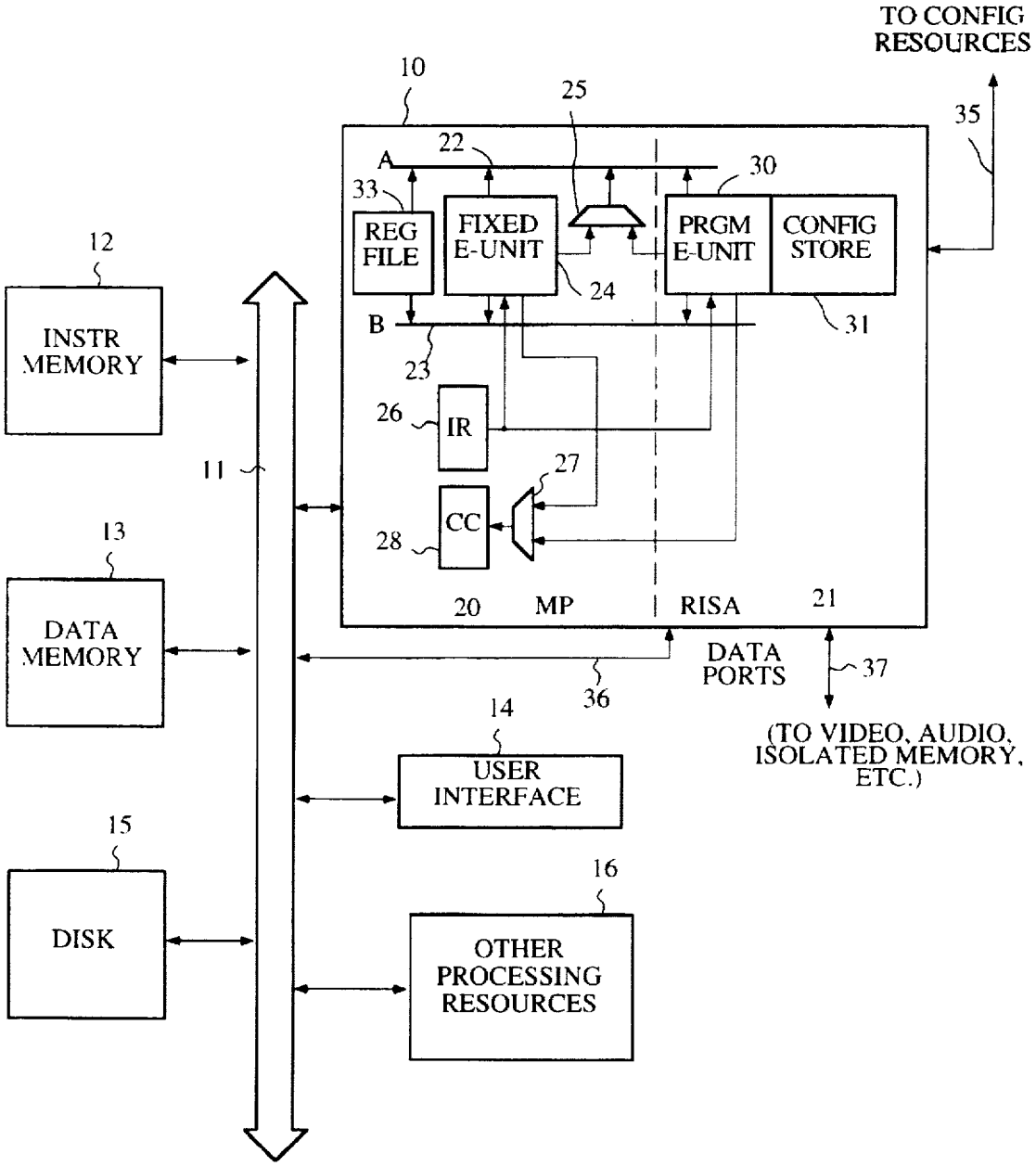

FIG. 1

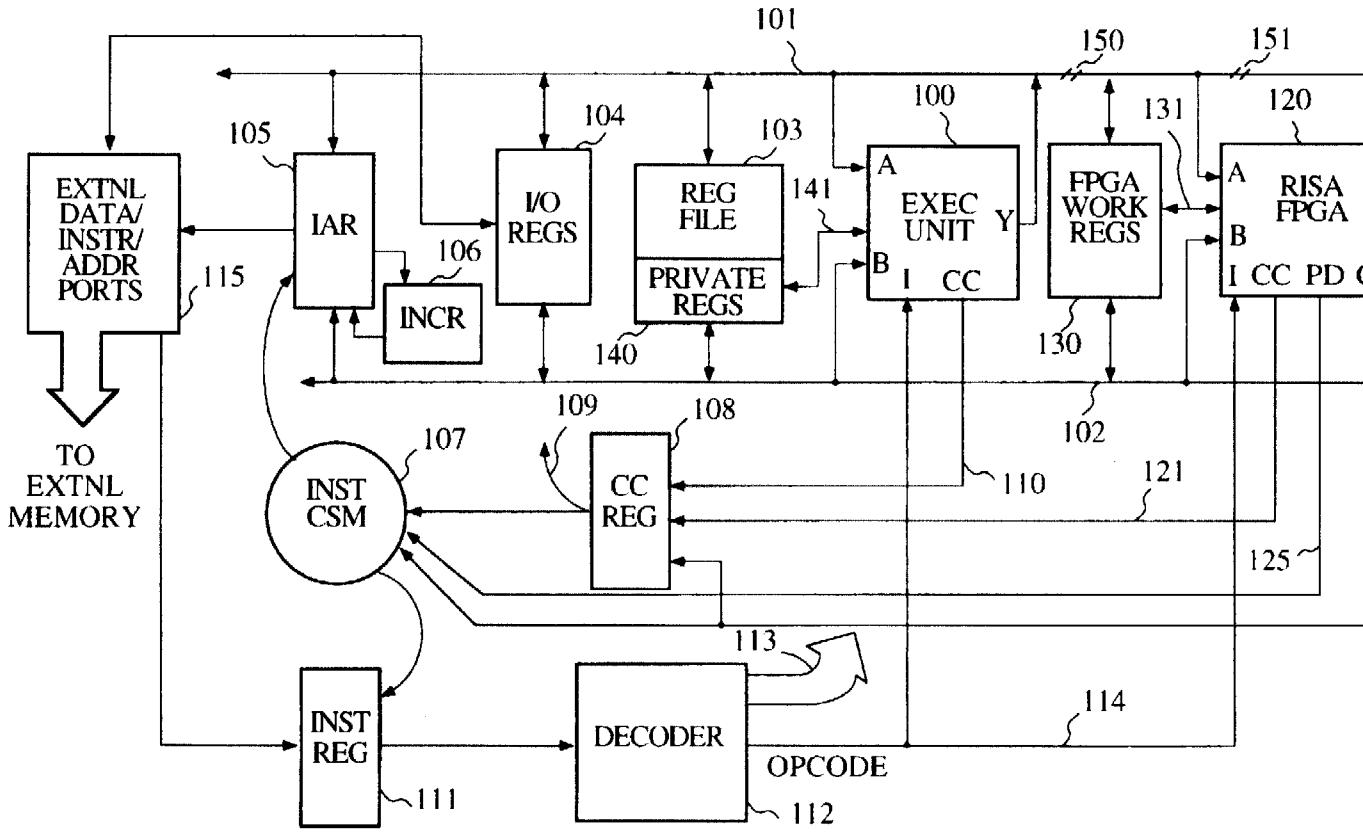

FIG. 2

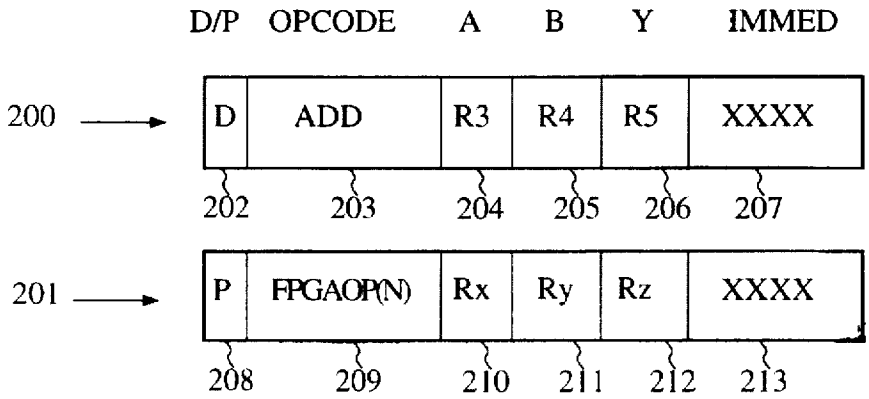

FIG. 3

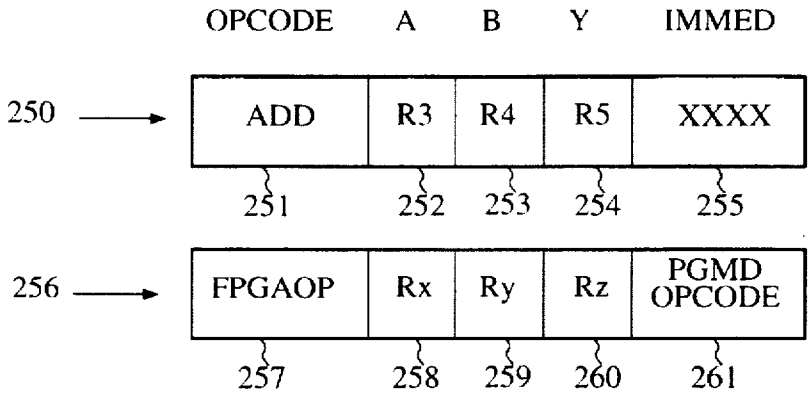

FIG. 4

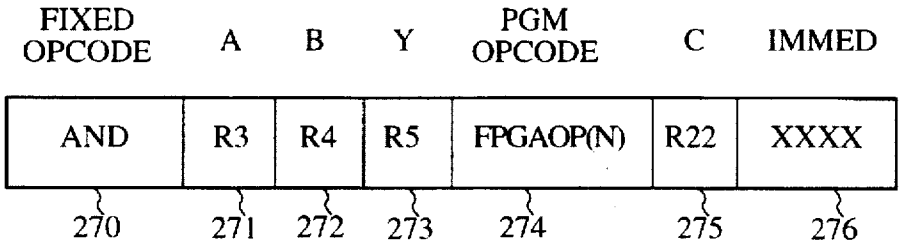

FIG. 5

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