UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

FG SRC LLC,
Patent Owner.

IPR2020-01449
Patent No. 7,149,867

PATENT OWNER FG SRC LLC'S RESPONSE TO PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO. 7,149,867

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2. "read and write only data required for computations by the algorithm between the data prefetch unit and the common memory" 33

IX. PETITIONER HAS FAILED TO DEMONSTRATE A REASONABLE LIKELIHOOD OF PREVAILING AS TO ANY CHALLENGED CLAIM. 33

A. Ground 1: Claims 1-2, 4-8 And 13-19 Are Not Obvious Over *Zhang* And *Gupta* 33

1. The combination does not render obvious a "reconfigurable processor that instantiates an algorithm as hardware." 33
2. The combination does not render obvious a "data prefetch unit." 38
3. The combination does not render obvious a data prefetch unit "wherein the data prefetch unit retrieves only computational data required by the algorithm." 40
4. The combination does not render obvious a first memory and a data prefetch unit "wherein at least the *first memory* and *data prefetch unit* are configured to conform to needs of the algorithm." 44
5. The combination does not render obvious a data prefetch unit "configured to match format and location of data in the second memory." 49
6. The combination does not render obvious a memory controller that "transmits only portions of data desired by the data prefetch unit and discards other portions of data prior to transmission of the data to the data prefetch unit." 50
7. The combination does not render obvious a "reconfigurable processor" as required by claim 13. 51
8. The combination does not render obvious a reconfigurable processor "wherein the computational unit

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and the data access unit, and the data prefetch unit are configured to conform to needs of an algorithm implemented on the computational unit and transfer only data necessary for computations by the computational unit" as required by claim 13 52

B. Ground 2: Claims 3 And 9-12 Are Not Obvious Over *Zhang*, *Gupta*, And *Chien*. 53

1. The combination does not render obvious a "reconfigurable processor[] that can instantiate an algorithm as hardware." 53
2. The combination does not render obvious a "data prefetch unit." 54
3. The combination does not render obvious "a data prefetch unit to read and write only data required for computations by the algorithm." 54
4. The combination does not render obvious a data prefetch unit configured to "match format and location of data in the common memory." 55
5. The combination does not render obvious a memory controller that "transmits to the prefetch unit only data desired by the data prefetch unit as required by the algorithm." 56
6. The combination does not render obvious a "reconfigurable processor [that] also includes a computational unit" as required by claim 11 57

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