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發明 新型 專利說明書

一、發明新型名稱	中文	光阻剝離組成物及剝離光阻之方法
	英文	RESIST STRIPPING GOMPOSITION AND PROCESS FOR STRIPPING RESIST
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四、中文發明摘要（發明之名稱：光阻剝離組成物及剝離光阻之方法）

一種水性剝離組成物含(a)氧化劑，(b)鉗合劑，(c)水溶性氟化合物，視情況地及(d)有機溶劑。亦提供爲一種利用此水性光阻剝離組成物剝離在蝕刻處理後殘留之光阻膜及光阻殘渣之方法。在此方法中，使半導體材料、電路形成材料、絕緣膜等之腐蝕最小，而且僅以水充份地清洗而無需如醇之有機溶劑。

英文發明摘要（發明之名稱：RESIST STRIPPING COMPOSITION AND PROCESS FOR STRIPPING RESIST）

An aqueous resist stripping composition contains (a) an oxidizing agent, (b) a chelating agent, (c) a water-soluble fluorine compound, and optionally (d) an organic solvent. Also provided is a process of stripping resist films and resist residues remaining after etching treatment utilizing the aqueous resist stripping composition. In the process, corrosion of semiconductor materials, circuit-forming materials, insulating films, etc. is minimized and the rinsing is sufficiently made with only water without needing organic solvent such as alcohol.

五、發明說明（ / ）

發明背景

本發明係關於一種光阻剝離組成物及一種使用此光阻剝離組成物剝離光阻之方法，更特別地，關於一種去除光阻膜用之剝離組成物及一種在半導體積體電路與液晶顯示器之製造中剝離光阻膜之方法。

微影術常用於如IC與LSI之半導體裝置之製造。藉微影術製造半導體裝置包括通常在如矽晶圓之基質上形成如矽氧化物膜之絕緣膜或如金屬膜之導電薄膜作爲電路電線；在膜上均勻地塗佈光阻組成物以形成感光層；藉由感光層對光之選擇性曝光及顯影形成所需之光阻圖案；使用光阻圖案作爲光罩而選擇性蝕刻底下之薄膜；然後完全地去除光阻圖案之循序步驟。

近來比從前更整合之半導體裝置之需求需要四分之一微米或更小級數之圖案。在此種製造尺寸之大幅降低，選擇性蝕刻主要藉乾蝕刻完成，而且圖案化光阻藉氧－電漿灰化去除。

然而，已知乾蝕刻法在圖案之週邊製造由乾蝕刻氣體、光阻及導電薄膜生成之殘渣。此殘渣在以下稱爲“光阻殘渣”。光阻殘渣造成如電阻增加及發生電短路之問題，特別是在通路孔內或附近。因此，去除光阻殘渣對於高品質半導體裝置之製造爲非常重要的。

日本專利申請案公開62-49355及64-42653教示藉有機胺剝離溶液去除光阻殘渣，其包括烷醇胺與有機溶劑之混

五、發明說明（2）

合物，然而，由於在相當高之溫度使用提議之剝離溶液，剝離溶液中之易燃有機化合物蒸發而易於造成忽然燃燒。在以有機胺剝離溶液清潔之基質以水清洗而不使用如醇之有機溶劑時，基質上之金屬膜被殘留有機胺之鹼本性腐蝕。因此，清洗需要使用如醇之有機溶劑。爲了解決此問題，日本專利申請案公開 7-201794 及 8-20205 揭示含氟化合物、有機溶劑及抗腐蝕劑之以氟爲主水溶液。其教示溶液具有比有機胺剝離溶液高之去除光阻殘渣之能力，而且可在低溫使用。

近來半導體裝置及液晶顯示面版用基質製造中嚴格之乾蝕刻及灰化之條件製造更複雜地修改之光阻殘渣，其無法藉以上之有機胺剝離溶液及以氟爲主水溶液完全去除。殘留未去除之光阻殘渣造成許多電問題，如電阻增加、導電線路不連續、電短路及不當組態之電路。因此，可完全去除此種光阻殘渣之清潔劑爲非常需要的。

因此，本發明之目的爲提供一種光阻剝離組成物，其在用於半導體積體電路或液晶顯示器之半導體裝置電路形成製程中，在短時間去除在乾蝕刻後殘留在無機基材上之圖案化光阻膜及光阻殘渣，而且其不造成對各種電路材料或絕緣材料之腐蝕。本發明之目的亦爲提供一種使用此光阻剝離組成物之光阻剝離方法。

發明概述

關於以上目的之廣泛研究之結果，發明人已發現包括（a）

五、發明說明（3）

氧化劑，(b)鉗合劑及(c)水溶性氟化合物之水性光阻剝離組成物易於在短時間去除在乾蝕刻後殘留在無機基質上之光阻殘渣及圖案化光阻膜，或在乾蝕刻後之灰化後殘留之光阻殘渣。更已發現此光阻剝離組成物造成特級電路處理而不腐蝕電路形成材料或絕緣膜，而且不需要如醇之有機溶劑作爲清洗溶液，即，可僅以水清洗半導體裝置，因而確定精確電路之製造。

因此，在本發明之一第一狀態中，提供一種包括(a)氧化劑，(b)鉗合劑及(c)水溶性氟化合物之水性光阻組成物。

在本發明之第二狀態中，提供一種包括(a)氧化劑，(b)鉗合劑，(c)水溶性氟化合物，及(d)有機溶劑之水性光阻組成物。

在本發明之第三狀態中，提供一種使用此剝離組成物剝離光阻之方法。

圖式簡單說明

第1圖爲使用圖案化光阻膜作爲光罩之乾蝕刻後之氧-電漿灰化後之電路裝置之示意剖視圖。

發明之詳細說明

用於本發明之氧化劑(a)可包括無機氧化物，如過氧化氫、臭氧、氫氯酸等，而且較佳爲過氧化氫。光阻剝離組成物中之氧化劑含量爲0.0001至60重量%，較佳爲0.0005至30重量%。

用於本發明之鉗合劑(b)可爲胺基聚羧酸及其鹽，如銨鹽

五、發明說明（4）

、金屬鹽與有機鹼鹽。胺基聚羧酸可包括伸乙二胺四乙酸(EDTA)、二羥基乙基伸乙二胺四乙酸(DHEDTA)、1,3-丙二胺四乙酸(1,3-PDTA)、二伸乙三胺五乙酸(DTPA)、三伸乙四胺六乙酸(TINA)、氮基三乙酸(NTA)及羥基乙基亞胺基二乙酸(HIMDA)。

另一種鉗合劑可爲在一個分子具有至少一個磷酸基之磷鉗合劑，其氧化衍生物及其鹽，如銨鹽、有機胺鹽與鹼金屬鹽。磷鉗合劑可包括甲基二磷酸、胺基參亞甲基磷酸、亞乙基二磷酸、1-羥基亞乙基-1,1-二磷酸、1-羥基亞內基-1,1-二磷酸、乙胺基貳亞甲基磷酸、十二胺基貳亞甲基磷酸、氮基參亞甲基磷酸、伸乙二胺貳亞甲基磷酸、伸乙二胺肆亞甲基磷酸、己烷二胺肆亞甲基磷酸、二伸乙三胺五亞甲基磷酸及1,2-丙烷二胺四亞甲基磷酸。磷鉗合劑分子中之氮原子可氧化形成N-氧化物衍生物。

仍可作爲鉗合劑爲縮合磷酸，如偏磷酸、四偏磷酸、六偏磷酸與三聚磷酸，及其鹽，如銨鹽、金屬鹽與有機胺鹽。

以上鉗合劑之中，在一個分子具有至少兩個磷酸基者較佳，而且具有2至6個磷酸基者更佳。特別地，1,2-丙烷二胺四亞甲基磷酸、二伸乙三胺五亞甲基磷酸與伸乙二胺肆亞甲基磷酸較佳，而且特佳爲1,2-丙烷二胺四亞甲基磷酸。

以上之鉗合劑可單獨或以二或更多之組合使用。

五、發明說明（5）

鉗合劑之濃度基於剝離組成物之總重量較佳爲0.01至5重量%，更佳爲0.05至3重量%。

用於本發明之水溶性氟化合物(c)可包括有機胺氟鹽，如氟化銨、酸銨氟鹽與單乙醇胺氟鹽、及四甲基銨氟鹽。水溶性氟化合物之濃度基於剝離組成物之總重量較佳爲0.001至10重量%，更佳爲0.005至5重量%。

用於本發明之有機溶劑(d)可包括醚溶劑，如乙二醇單乙醚、乙二醇單丁醚、二乙二醇單甲醚、二乙二醇單乙醚、二乙二醇單丁醚、丙二醇單甲醚、丙二醇單乙醚、丙二醇單丁醚、二丙二醇單甲醚、二丙二醇單乙醚、二丙二醇單丁醚、二乙二醇二甲醚與二丙二醇二甲醚；醯胺溶劑，如甲醯胺、單甲基甲醯胺、二甲基甲醯胺、單乙基甲醯胺、二乙基甲醯胺、單乙基乙醯胺、二甲基之醯胺、單乙基乙醯胺、二乙基乙醯胺、N-甲基吡咯啶酮與N-乙基吡咯啶酮；及硫化合物溶劑，如二甲基亞碸、二甲碸、二乙碸、貳(2-羥基)碸與四亞甲碸。較佳爲二甲基亞碸、N,N-二甲基甲醯胺、N,N-二甲基乙醯胺、N-甲基吡咯啶酮、二乙二醇單甲醚、二乙二醇單丁醚、二丙二醇單甲醚與二丙二醇單丁醚。

有機溶劑可單獨或以二或更多之組合使用。有機溶劑之濃度基於剝離組成物之總重量選自1至7重量%。不論是否使用有機溶劑，其濃度易視乾蝕刻及／或灰化條件及熟悉此技藝者熟知之其他因素決定。

五、發明說明（6）

依照本發明之剝離組成物爲含成份(a)至(c)、選用成份(d)、及其餘爲水之水性組成物。此剝離組成物可爲分散液或懸浮液，而且通常爲水溶液。此光阻剝離溶液可含用於習知光阻剝離溶液之添加物，除非其添加負面地影響本發明之目的。

剝離組成物之pH並未特別地限制，而且一般選自pH3至pH12之範圍，視蝕刻條件、無機基質用之材料等而定。在意圖爲鹼性剝離組成物時，可加入氨、胺或如四甲銨氫氧化物之第四銨氫氧化物，而且在意圖爲酸性剝離組成物時，可加入有機酸或無機酸。

爲了改良剝離組成物之濕潤力，可使用任何陽離子性、非離子性及陰離子性界面活性劑。

本發明之光阻剝離組成物可藉任何此技藝已知方法製造。例如，在攪拌下將成份(a)至(c)及選用成份(d)加入水中直到混合物達成均勻狀態。加入成份之次序並不重要。

依照本發明之剝離方法通常在一般溫度至80℃之溫度進行，而且可視蝕刻條件及使用之無機基質用之材料而適當地選擇特定剝離溫度。

無機基質用之材料可爲半導體電路形成材料，如矽、非晶矽、聚矽、矽氧化物膜、矽氮化物膜、鋁、鋁合金、銅、銅合金、鈦、鈦-鎢、鈦氮化物、鎢、鉭、鉭化合物、鉭合金、鉻、鉻氧化物、鉻合金與ITO(銦-錫氧化物)；複合半導體，如鎵-砷、鎵-磷與銦-磷；及LCD用之玻璃

五、發明說明（7）

基質。

本發明之剝離方法用以去除塗覆在無機基質上之光阻膜、在蝕刻後殘留之圖案化光阻膜、或在蝕刻後之灰化後殘留之光阻殘渣。在剝離方法中，光阻膜及／或光阻殘渣藉浸泡、浸漬等接觸光阻剝離組成物。如果需要，可適當地組合使用加熱、超音波暴露等。

"灰化"在此指一種光阻去除方法，例如，其中有機聚合物製成之光阻藉由在氧電漿中燃燒而蒸發成CO與CO_2。特別地，將被處理之灰化基質及灰化氣體密封在置於一對電極之間之槽中。在對電極施加高頻電壓時，在槽中產生灰化氣體之電漿。藉由電漿中活化離子及基質表面上物質之間之反應，光阻蒸發。

本發明光阻剝離組成物之處理後之清洗可僅使用水完成，而無需如醇之有機溶劑。

本發明藉實例及比較例而更詳細地敘述。然而，應注意，以下之實例爲描述性且不意圖限制本發明。

實例1至10及比較例1至8

第1圖爲接受形成Al合金(Al-Cu)電路圖案5之乾蝕刻繼而氧電漿灰化後之Al合金電路裝置之剖視圖。在第1圖中，氧化物膜2在矽基質1上形成，而且Al合金電路圖案5在其上經作爲障壁金屬膜之鈦膜3及鈦氮化物膜4而形成。在Al合金電路圖案5上，配置另一層鈦氮化物膜4'。光阻殘渣6殘留在堆疊膜之側壁上。

五、發明說明（8）

更特別地，第1圖爲氧電漿灰化後之Al合金電路裝置之剖視圖。其藉由將電路圖案用之Al合金(Al-Cu)膜配置於矽基質上而得。在Al合金膜上，塗覆光阻組成物以形成光阻膜，其然後藉微影術圖案化。然後使用圖案化光阻膜作爲光罩進行以氟爲主氣體之乾蝕刻，以將Al合金膜製成電路圖案，繼而爲氧電漿灰化。在第1圖中，光阻殘渣殘留在Al合金電路圖案之側壁上。

Al合金電路裝置在各條件下浸於具有如表1所示之化學組成物之光阻剝離組成物中，以超純水清洗然後乾燥。然後，在掃描電子顯微鏡(SEM)下觀察電路裝置之表面，以依照以下之評分評估光阻殘渣之去除及Al合金之腐蝕。結果示於表1。

SEM觀察之評分：

去除

++：完全去除

+ ：幾乎完全去除

- ：部份殘留

--：大部份殘留

腐蝕：

++：無腐蝕

+ ：幾乎無腐蝕

- ：腐蝕之坑洞或凹痕

--：粗糙全表面及Al合金膜損失

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五、發明說明（9）

表 1

光阻剝離組成物

實例	氧化劑(wt.%)	鉗合劑(wt.%)	氟化合物(wt.%)	有機溶劑(wt.%)	水
1	HP(5)	C1(0.2)	AF(0.05)	-	其餘
2	HP(2)	C1(0.5)	AF(0.1)	-	其餘
3	HP(1)	C1(0.1)	AF(0.5)	-	其餘
4	HP(5)	C2(0.2)	AF(0.1)	-	其餘
5	HP(5)	C3(0.2)	AF(0.1)	-	其餘
6	HP(5)	C4(0.2)	AF(0.1)	-	其餘
7	HP(0.5)	C1(0.2)	AF(0.01)	-	其餘
8	HP(7)	C1(0.2)	AF(0.8)	S1(45)	其餘
9	HP(8)	C5(0.3)	AF(0.8)	S2(45)	其餘
10	HP(9)	C6(0.3)	AF(0.8)	S2(50)	其餘
比較例					
1	HP(5)	-	-	-	其餘
2	-	C1(0.5)	-	-	其餘
3	-	-	AF(0.5)	-	其餘
4	-	-	-	S1(40)	其餘
5	HP(5)	C1(0.2)	-	-	其餘
6	HP(5)	-	AF(0.1)	-	其餘
7	-	-	AF(0.5)	S1(45)	其餘
8	-	C1(0.2)	AF(0.5)	S1(45)	其餘

HP：過氧化氫

C1：1,2-丙二胺四亞甲基磷酸

C2：二伸乙三胺五亞甲基磷酸

C3：伸乙二胺肆亞甲基磷酸

C4：伸乙二胺四乙酸

五、發明說明（10）

C5：1-羥基亞乙基-1,1-二磷酸

C6：磷酸

AF：氟化銨

S1：二甲基乙醯胺

S2：二甲基甲醯胺

表 1（續）

實例	溫度(℃)	剝離條件 時間(min)	光阻殘渣之去除	Al 合金之腐蝕
1	23	5	++	++
2	23	5	++	++
3	23	5	++	++
4	23	5	++	++
5	23	5	++	++
6	23	5	++	++
7	40	5	++	++
8	23	3	++	++
9	23	3	++	++
10	23	5	++	++
比較例				
1	23	5	--	++
2	23	5	--	++
3	23	5	-	+
4	23	5	--	++
5	23	5	-	++
6	23	5	+	-
7	23	5	-	+
8	23	5	+	+

五、發明說明（11）

實例 11

以如實例 1 之相同方法，Al 合金(Al-Cu)膜在矽基質上形成且塗覆光阻膜，其接受微影術以形成圖案化光阻膜。然後合金膜使用圖案化光阻膜作爲光罩而以以氯爲主氣體乾蝕刻。如此得到之電路裝置在 50℃ 浸於實例 1 使用之相同光阻剝離組成物中 5 分鐘，以去除作爲光罩之圖案化光阻膜及在乾蝕刻時產生之光阻殘渣，以超純水清洗然後乾燥。然後，在掃描電子顯微鏡(SEM)下觀察電路裝置之表面，以依照以上提及之評分評估圖案化光阻膜與光阻殘渣之去除及 Al 合金之腐蝕。結果，證實完全地去除圖案化光阻膜與光阻殘渣而未腐蝕 Al 合金電路圖案。

藉由使用依照本發明之光阻剝離組成物，易於在低溫短時間去除塗覆於無機基質上之光阻膜、蝕刻後殘留之圖案化光阻膜、或在蝕刻後之灰化後殘留之光阻殘渣。由於底下之電路形成材料未腐蝕，以此剝離處理得到精細處理之電路圖案。此外，在剝離處理後電路裝置之清洗僅以水充份地完成，而不需使用如醇之有機溶劑，生成高正確性及高品質之電路圖案製造。

主要元件符號對照表

1　矽基質

2　氧化物膜

3　鈦膜

4　鈦氮化物膜

A7
B7

五、發明說明（12）

4' 鈦氮化物膜

5 Al合金電路圖案

6 光阻殘渣

91年9月13日修正/更正/補充

六、申請專利範圍

第 89103662 號「光阻剝離組成物及剝離光阻之方法」專利案

(91 年 9 月 13 日修正)

六申請專利範圍：

1.一種水性光阻剝離組成物，包含(a)0.0001 至 60 重量%之氧化劑，(b)0.01 至 5 重量%之鉗合劑，(c)0.001 至 10 重量%之水溶性氟化合物，及其餘爲水。

2.一種水性光阻剝離組成物，包含(a)0.0001 至 60 重量%之氧化劑，(b)0.01 至 5 重量%之鉗合劑，(c)0.001 至 10 重量%之水溶性氟化合物，(d)1 至 70 重量%之有機溶劑，及其餘爲水。

3.如申請專利範圍第 1 或 2 項之水性光阻剝離組成物，其中該氧化劑爲至少一種選自於過氧化氫、臭氧及氫氨酸之氧化物。

4.如申請專利範圍第 1 或 2 項之水性光阻剝離組成物，其中該氧化劑爲過氧化氫。

5.如申請專利範圍第 1 或 2 項之水性光阻剝離組成物，其中該鉗合劑爲至少一種選自於胺基聚羧酸、胺基聚羧酸之銨鹽、胺基聚羧酸之金屬鹽、胺基聚羧酸之有機鹼鹽、磷鉗合劑、磷鉗合劑之銨鹽、磷鉗合劑之有機胺鹽、磷鉗合劑之鹼金屬鹽、磷鉗合劑之 N-氧化物、縮合磷酸、縮合磷酸之銨鹽、縮合磷酸之金屬鹽

六、申請專利範圍

、及縮合磷酸之有機胺鹽之化合物。

6.如申請專利範圍第 5 項之水性光阻剝離組成物，其中該胺基聚羧酸爲至少一種選自於伸乙二胺四乙酸、二羥基乙基伸乙二胺四乙酸、1,3-丙二胺四乙酸、二伸乙三胺五乙酸、三伸乙四胺六乙酸、氮基三乙酸及羥基乙基亞胺基二乙酸之化合物。

7.如申請專利範圍第 5 項之水性光阻剝離組成物，其中該磷鉗合劑爲至少一種選自於甲基二磷酸、胺基參亞甲基磷酸、亞乙基二磷酸、1-羥基亞乙基-1,1-二磷酸、1-羥基亞丙基-1,1-二磷酸、乙胺基貳亞甲基磷酸、十二胺基貳亞甲基磷酸、氮基參亞甲基磷酸、伸乙二胺貳亞甲基磷酸、伸乙二胺肆亞甲基磷酸、己烷二胺肆亞甲基磷酸、二伸乙三胺五亞甲基磷酸及1,2-丙烷二胺四亞甲基磷酸之化合物。

8.如申請專利範圍第 5 項之水性光阻剝離組成物，其中該縮合磷酸爲至少一種選自於偏磷酸、四偏磷酸、六偏磷酸及三聚磷酸之化合物。

9.如申請專利範圍第 1 或 2 項之水性光阻剝離組成物，其中該鉗合劑爲磷鉗合劑。

10.如申請專利範圍第 9 項之水性光阻剝離組成物，其中該磷鉗合劑具有 2 至 6 個磷酸基。

11.如申請專利範圍第 9 項之水性光阻剝離組成物，其中該磷鉗合劑爲至少一種選自於 1,2-丙烷二胺四亞

六、申請專利範圍

甲基磷酸、二伸乙三胺五亞甲基磷酸及伸乙二胺肆亞甲基磷酸之化合物。

12.如申請專利範圍第 1 或 2 項之水性光阻剝離組成物，其中該水溶性氟化合物爲至少一種選自於氟化銨、酸銨氟鹽、單乙醇胺氟鹽及四甲基銨氟鹽之化合物。

13.如申請專利範圍第 1 或 2 項之水性光阻剝離組成物，其中該水溶性氟化合物爲氟化銨。

14.如申請專利範圍第 2 項之水性光阻剝離組成物，其中該有機溶劑爲至少一種選自於乙二醇單乙醚、乙二醇單丁醚、二乙二醇單甲醚、二乙二醇單乙醚、二乙二醇單丁醚、丙二醇單甲醚、丙二醇單乙醚、丙二醇單丁醚、二丙二醇單甲醚、二丙二醇單乙醚、二丙二醇單丁醚、二乙二醇二甲醚、二丙二醇二甲醚、甲醯胺、單甲基甲醯胺、二甲基甲醯胺、單乙基甲醯胺、二乙基甲醯胺、單乙基乙醯胺、二甲基乙醯胺、單乙基乙醯胺、二乙基乙醯胺、N-甲基吡咯啶酮、N-乙基吡咯啶酮、二甲基亞碸、二甲碸、二乙碸、貳(2-羥基)碸與四亞甲碸之溶劑。

15.如申請專利範圍第 2 項之水性光阻剝離組成物，其中該有機溶劑爲至少一種選自於二甲基亞碸、N,N-二甲基甲醯胺、N,N-二甲基乙醯胺、N-甲基吡咯啶酮、二乙二醇單甲醚、二乙二醇單乙醚、二丙二醇單甲醚與二丙二醇單丁醚之溶劑。

六、申請專利範圍

16.一種剝離光阻膜及光阻殘渣之方法，其包括步驟：

在無機基質上形成光阻膜；

將光阻膜圖案化以形成圖案化光阻膜；

乾蝕刻圖案化光阻膜底下之膜，同時使用圖案化光阻膜作爲光罩以去除底下膜之非遮蔽區域；及

藉由使如申請專利範圍第 1 至 15 項中任一項之水性光阻剝離組成物接觸光阻殘渣及／或圖案化光阻膜，去除在乾蝕刻時形成之光阻殘渣及／或在乾蝕刻後殘留之圖案化光阻膜。

17.一種剝離光阻膜及光阻殘渣之方法，其包括步驟：

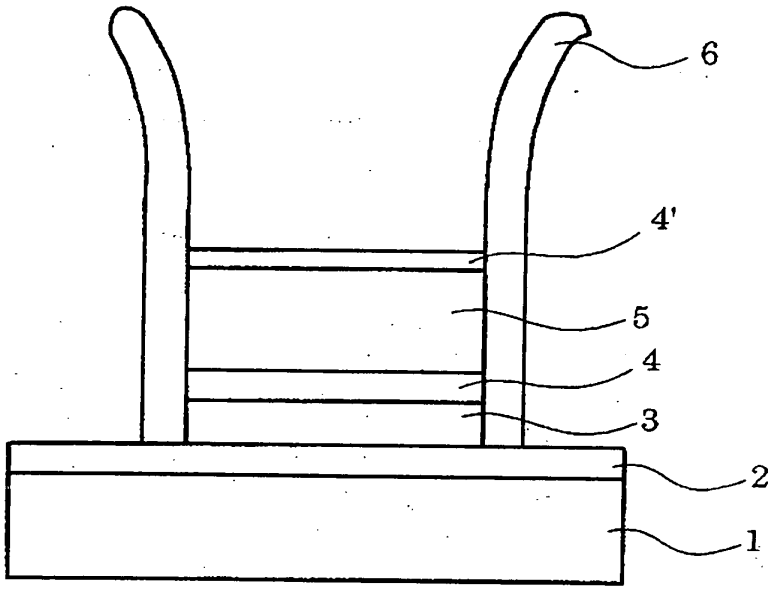
在無機基質上形成光阻膜；

將光阻膜圖案化以形成圖案化光阻膜；

乾蝕刻圖案化光阻膜底下之膜，同時使用圖案化光阻膜作爲光罩以去除底下膜之非遮蔽區域；

將圖案化光阻膜灰化；及

藉由使如申請專利範圍第 1 至 15 項中任一項之水性光阻剝離組成物接觸光阻殘渣，去除在乾蝕刻時形成之光阻殘渣。



第 1 圖

公告本

FREE

584824

發明專利說明書

（填寫本書件時請先行詳閱申請書後之申請須知，作※記號部分請勿填寫）

※ 申請案號：P21067841　※IPC分類：G09F9/30
G09G3/30

※ 申請日期：92.3.26

壹、發明名稱

（中文）顯示器裝置、有機發光二極體面板、用於薄膜電晶體之控制裝置、控制薄膜電晶體之方法及控制有機發光二極體顯示器之方法

（英文）DISPLAY DEVICE, ORGANIC LIGHT-EMITTING DIODE PANEL, CONTROL DEVICE FOR THIN-FILM TRANSISTOR, METHOD OF CONTROLLING THIN-FILM TRANSISTOR AND METHOD OF CONTROLLING ORGANIC LIGHT-EMITTING DIODE DISPLAY

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肆、中文發明摘要

藉由間歇地和同步地升高閘極電壓和汲極電壓(drain voltage)來去除一非晶矽薄膜電晶體(amorphous silicon TFT)中之一臨限電壓(threshold voltage, Vth)的增加分量，該電晶體係用以驅動一有機發光二極體(OLED)。明確地說，一種OLED顯示器包括：一驅動電路，其藉由非晶矽TFT來驅動OLED；以及一電源線驅動器(supply-line driver)，當間歇地升高施加到非晶矽TFT之閘極電極的閘極電壓時，其用來升高供應到非晶矽TFT之汲極電極的電壓。

伍、英文發明摘要

An increased component of a threshold voltage (Vth) in an amorphous silicon TFT which is a transistor for driving an OLED is removed by rising a gate electrode and a drain electrode intermittently and simultaneously. Specifically, an OLED display includes a drive circuit for driving an OLED by an amorphous silicon TFT, and a supply-line driver for dropping a voltage supplied to a drain electrode of the amorphous silicon TFT, when a gate voltage to a gate electrode of the amorphous silicon TFT is intermittently risen.

陸、(一)、本案指定代表圖為：第 1 圖

(二)、本代表圖之元件代表符號簡單說明：

10 有機發光二極體(OLED)顯示器

11 控制單元

12 掃描線驅動器

13 資料線驅動器

14 電源線驅動器

15 公用線驅動器

20 驅動電路

柒、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

捌、聲明事項

☐ 本案係符合專利法第二十條第一項☐第一款但書或☐第二款但書規定之期間，其日期為：＿＿＿＿＿＿＿＿＿＿

☑ 本案已向下列國家（地區）申請專利，申請日期及案號資料如下：

【格式請依：申請國家（地區）；申請日期；申請案號　順序註記】

1.日本　2002 年 03 月 29 日　特願 2002-097545

2.＿＿＿＿＿＿＿＿＿＿

3.＿＿＿＿＿＿＿＿＿＿

☑ 主張專利法第二十四條第一項優先權：

【格式請依：受理國家（地區）；日期；案號　順序註記】

1.日本　2002 年 03 月 29 日　特願 2002-097545

2.＿＿＿＿＿＿＿＿＿＿

3.＿＿＿＿＿＿＿＿＿＿

4.＿＿＿＿＿＿＿＿＿＿

5.＿＿＿＿＿＿＿＿＿＿

6.＿＿＿＿＿＿＿＿＿＿

7.＿＿＿＿＿＿＿＿＿＿

8.＿＿＿＿＿＿＿＿＿＿

9.＿＿＿＿＿＿＿＿＿＿

10.＿＿＿＿＿＿＿＿＿＿

☐ 主張專利法第二十五條之一第一項優先權：

【格式請依：申請日；申請案號　順序註記】

1.＿＿＿＿＿＿＿＿＿＿

2.＿＿＿＿＿＿＿＿＿＿

3.＿＿＿＿＿＿＿＿＿＿

☐ 主張專利法第二十六條微生物：

☐國內微生物　【格式請依：寄存機構；日期；號碼　順序註記】

1.＿＿＿＿＿＿＿＿＿＿

2.＿＿＿＿＿＿＿＿＿＿

3.＿＿＿＿＿＿＿＿＿＿

☐國外微生物　【格式請依：寄存國名；機構；日期；號碼　順序註記】

1.＿＿＿＿＿＿＿＿＿＿

2.＿＿＿＿＿＿＿＿＿＿

3.＿＿＿＿＿＿＿＿＿＿

☐熟習該項技術者易於獲得，不須寄存。

(1)

玖、發明說明

(發明說明應敘明：發明所屬之技術領域、先前技術、內容、實施方式及圖式簡單說明)

發明背景

本發明與採用有機發光二極體(organic light-emitting diode，簡稱OLED)的顯示裝置及其同類者有機。說得更明確些，本發明與使用薄膜電晶體作為驅動OLED之電晶體的顯示裝置及同類者(以下稱之為OLED顯示器)有關。

OLED(也將它稱為有機電致發光(organic EL))是一種科技，它藉由將直流電流流動於一種由施加電場所激勵之具有螢光(fluorescence)的有機化合物上來產生光發射(light emission)。從低外形(low profile)，寬視角(view angle)，寬色域(wide gamut)等等的角度看來，OLED作為下一代顯示裝置已經引起注意。適於OLED的驅動模式有兩種類型，即：無源型(passive type)和有源型(active type)。然而，從材料，耐用期(life duration)，串擾(cross talks)等等的角度看來，對於獲得一種寬螢幕和高解析度顯示器而言，有源型比較適合。在這種有源型中，需要薄膜電晶體(以下稱之為TFT)驅動操作。這樣一種TFT科技會使用兩種類型的材料，它們是：低溫多晶矽(poly silicon)和非晶矽(amorphous silicon，簡稱a-Si)。

應用低溫多晶矽的多晶矽TFT之所以被廣泛地使用，是因為它具有：導因於大遷移率(mobility)而流出大電流之能力，以及增加螢幕亮度之能力。然而，一種用來產生多晶矽TFT的方法就需要譬如說是9個利用目前科技的光刻製程(photoengraving processes，簡稱PEP)。因此，多晶矽TFT涉

及成本增加複雜製程數目的增加。而且，藉由使用多晶矽TFT來獲得大螢幕是挺困難的；因此，這時候其最大尺寸會被限制在大約15吋。正好相反，藉由較少製程就能夠形成非晶矽(a-Si)TFT；因此，從控制成本(curbing cost)的角度看來是挺有利的。而且，能夠將非晶矽TFT形成為大螢幕；並且從諸如發光均勻性(luminance uniformity)之影像品質的觀點，它會運用諸多有利結果。於是，針對非晶矽TFT的研究和針對多晶矽TFT的研究現在都正在進行中。

此處，OLED是一種由電流驅動的元件(current-driven element)。於是，在諸多驅動電晶體之中的不均勻性(unevenness)或者是由於隨時間變質(deterioration with time)所產生的電流不均勻性會直接導致影像品質降低。從TFT之臨限電壓(Vth)的角度看來，在使用多晶矽TFT的驅動電晶體中，臨限電壓(Vth)的變化有限。正好相反，在非晶矽TFT中，Vth實質上會隨著隨時間變質而偏移。

針對臨限電壓(Vth)之偏移的第一個理由是：當電子流動於TFT之通道上時，電子就會投入(jump into)閘極絕緣膜中。而且，第二個理由是：因為電子會切斷矽鍵合(Si bonding)，所以當電子流動於TFT之通道上時，就會藉由電子來充電矽。

圖6是一種曲線圖，它顯示：當使用非晶矽TFT時，隨著時間流逝之臨限電壓(Vth)的偏移量(shift amount)。橫軸指示時間，而縱軸則指示Vth的偏移量。如圖6中所顯示，當藉由使用非晶矽TFT來驅動OLED時，Vth實質上會隨著

合。在下文中，這種敘述句是可以等效地應用。

而且，在應用本發月的顯示裝置中，當藉由驅動電晶體來驅動OLED時，在間歇地升高供應電壓的時候，電源線驅動器會供應電壓到驅動電晶體之源極電極和汲極電極其中任何一個電極。此處，電源線驅動器會依照與間歇地升高驅動電晶體之閘極電壓類似的時序，加以間歇地升高施加到源極電極和汲極電極其中任何一個電極的電源線電壓。

於其時，應用本發明的顯示裝置包括：驅動裝置(driving means)，它藉由使用TFT來驅動OLED；閘極電壓供應裝置，它用來間歇地升高施加到驅動裝置中的TFT之閘極電極的閘極電壓；以及控制裝置，它會執行控制，使得：當藉由閘極電壓供應裝置來降低施加到閘極電極的閘極電壓時，將TFT的汲極電極與源極電極之間的電位差加以消除。此處，閘極電壓供應裝置會基於從掃描線驅動器供應之掃描線訊號(scan-line signal)和從資料線驅動器供應之資料線訊號(data-line signal)而間歇地升高閘極電壓，以及控制裝置會隨著藉由閘極電壓供應裝置來降低閘極電壓而同步地降低施加到TFT的電源線電壓。

而且，應用本發明的OLED面板包括：一自發光(self-luminous) OLED，將它配備在每個像素(pixel)上；以及一非晶矽TFT，它用來驅動OLED。此處，以下列方式來控制非晶矽TFT。明確地說，當降低施加到閘極電極的電壓時，會使跨接於汲極和源極的電壓等於0伏；並且當降低施加

到閘極電極的電壓時，會造成將正電洞(positive holes)捕獲於非晶矽中；於是，降低了臨限電壓(Vth)的偏移量。

再者，在應用本發明的一種適於TFT之控制裝置中，閘極電壓供應裝置會供應閘極電壓到驅動OLED之TFT的閘極電極。而且，電壓供應裝置會供應電壓到TFT之源極電極和汲極電極其中任何一個電極；並且當藉由閘極電壓供應裝置來降低閘極電壓時，它會降低施加到源極電極和汲極電極其中任何一個電極的電壓。能夠構成電壓供應裝置，使得：當藉由閘極電壓供應裝置來供應閘極電壓時，將供應到源極電極和汲極電極其中任何一個電極的電壓保持(retained)上升。

從其它的觀點，應用本發明的一種控制TFT之方法包括下列步驟：控制施加到TFT之源極電極和汲極電極其中任何一個電極的電壓，使得：當升高供應到TFT之閘極電極的閘極電壓時，將該電壓保持上升；以及控制施加到源極電極和汲極電極其中任何一個電極的電壓，使得：當降低閘極電壓時，將該電壓降低。此處，有可能容許供應到源極電極和汲極電極其中任何一個電極的電壓隨著閘極電壓的升高而同步地升高。

再者，本發明提供一種控制OLED顯示器的方法，它包括下列步驟：將一種基於資料訊號的電壓供應到驅動OLED之TFT；以及根據預定工作比(duty ratio)，在間歇地升高電源線電壓的時候，將電源線電壓供應到TFT。而且，在供應電源線電壓的步驟中，基於打算供應到TFT的整體電荷

量而確定電源線電壓之數值。

附圖概述

為了更加徹底瞭解本發明及其中的諸多優點，現在參考連同諸多附圖所採取的下列描述。

圖1是：用來顯示一種採用本發明之一實施例的有源矩陣型(active-matrix)OLED顯示器之示意圖。

圖2是：用來顯示使用在OLED顯示器中之驅動電路的構造之示意圖。

圖3A和3B都是：用來顯示藉由本實施例之一控制單元來控制的驅動電路之時序圖的示意圖。

圖4是：用來說明在50[攝氏度]時之被驅動的驅動TFT的Vth之偏移量的示意圖。

圖5是：用來顯示在35[攝氏度]時驅動著驅動TFT的時候加以去除可歸因於一種具有大活化能(activation energy)的電流之變質分量(正偏移)的結果之示意圖。

圖6是：用來顯示當使用非晶矽TFT時之隨著時間的臨限電壓(Vth)之偏移量的示意圖。

較佳實施例之詳細描述

現在，參考諸多附圖，基於一實施例，將要詳細地描述本發明。

圖1是：用來顯示一種採用本發明之一實施例的有源矩陣型OLED顯示器10之示意圖。本實施例是以使用非晶矽(a-Si)TFT的有源矩陣型OLED顯示器10為目標。為了要驅動一種具有m[乘以]n佈置的點矩陣(dot-matrix)顯示器，這

種OLED顯示器10包括：一控制單元11，它會依照由處理已供應視頻訊號(video signal)所要求的時序，加以輸出打算供應到每個驅動電路的控制訊號；一掃描線驅動器12，它基於來自控制單元11的控制訊號而供應選擇訊號(位址訊號(address signal))到諸多掃描線Y1到Yn；一資料線驅動器13，它基於來自控制單元11的控制訊號而供應資料訊號到諸多資料線X1到Xm；一電源線驅動器14，它是一種電源，用來將電流流動於OLED中；一公用線驅動器(common-line driver)15，它用來將供應到OLED的電流接地；以及諸多驅動電路20，將它們個別地配備在m[乘以]n個像素上；該公用線驅動器15是藉由：來自掃描線驅動器12的選擇訊號和來自資料線驅動器13的資料訊號加以控制的。此處，前述的構造可能進一步包括用來產生打算供應到控制單元11之視頻訊號的電路結構，因而可能被集體視為一種顯示裝置。於其時，前述的構造可能不包括控制單元11及其同類者，因而可能被流傳(circulated)為一種OLED面板。再者，也有可能構成OLED顯示器而沒有配備公用線驅動器15，使得：只是將供應到OLED的電流接地。

圖2是：用來顯示使用在OLED顯示器10中之驅動電路20的構造之示意圖。顯示於圖2的驅動電路20包括：一OLED 21，它應用適於發光層(light-emitting layer)之有機化合物；一驅動TFT 22，它是由一種用來驅動OLED 21的非晶矽TFT所製成；一切換TFT 23，它基於：經由掃描線而從掃描線驅動器12獲得的掃描訊號以及經由資料線而從資料線驅動

器13獲得的資料訊號而執行切換操作(switching operations)；以及一電容器24，將它連接到來自電源線驅動器14之一電流供應線，該電容器24會儲存電荷以保持閘極電位。在本實施例中，控制單元11會控制電源線驅動器14，以便間歇地和幾乎同時地升高：打算供應到驅動TFT 22的閘極電壓，以及經由電流供應線所獲得的電源線電壓(在本實施例中，將它指稱為汲極電壓)。注意：依照不同命名順序，也可能將電源線電壓指稱為源極電壓。

在常態下，不會間歇地升高：譬如說，在15伏時之打算從電源線驅動器14供應到驅動TFT 22的電源線電壓。於是，通常會保持供應一種恒定電流(constant current)。然而，在本實施例中，電源線電壓(汲極電壓)會隨著閘極電壓而間歇地升高；藉此，減少了在驅動TFT 22中之臨限電壓(Vth)的偏移量。注意：詞句"停止電壓"不一定意謂著將電壓設定成0伏。這樣一種觀點指出傳導電子幾乎從驅動TFT 22之通道中消失的狀態。換言之，該觀點也可能被指稱為閘極電壓跌落低於一臨限值(threshold)的狀態。

在容許譬如說是1[微安培]的電流流經驅動TFT 22的情形下，有容許1[微安培]的電流流經該處的各種方法。譬如說，有容許以直流電流之形式呈現的1[微安培]電流流經該處之一方法，根據50%之工作比而容許2[微安培]電流流經該處之一方法，以及其它方法。而且，也可以想像得到的是：閘極電壓和汲極電壓被視為一組；並且當間歇地升高閘極電壓時，用來降低汲極電壓的方法也會變化多端。

結果是，統合(coordinate)總電荷量是必要的。本發明之發明者已經擴展關於如何容許電流之方法的研究；並且已經發現：藉由間歇地和幾乎同時地升高閘極電壓和汲極電壓，就能夠減少臨限電壓(Vth)的正偏移變質。

圖3A和3B都是：用來顯示藉由本實施例之控制單元11來控制的驅動電路20之時序圖的示意圖。圖3A和3B顯示兩個實例。此處，每個示意圖都會顯示：從公用線驅動器15得到的公用線訊號，從電源線驅動器14得到的電源線訊號，從掃描線驅動器12得到的掃描線訊號，從資料線驅動器13得到的資料線訊號，以及出現在驅動電路20之驅動TFT 22之閘極電極處的閘極電位(gate potential)。電源線訊號是依照譬如說是50%之工作比而運作的。電源線訊號會在掃描線訊號的兩個脈波之間通斷切換著(在圖3A的情形下)，或者是根據掃描線訊號的各個脈波而循序地通斷切換著(在圖3B的情形下)。閘極電位會隨著電源線訊號的降低而降低。明確地說，藉由降低來自電源線驅動器14的電源線訊號，就能夠執行降低如以上提及的閘極電位和汲極電位。

在圖3A和3B中，會有間歇地和同時地升高驅動TFT 22之閘極電位和電源線訊號的時序。此時序可歸因於下列事實：將來自電源驅動器14的電流供應線連接到驅動TFT 22之閘極電極。在本實施例中，將電容器24插入驅動TFT 22的汲極電極與閘極電極之間，以便藉由使用電容器24來間歇地和同時地升高閘極電位和電源線訊號。將用來間歇地

和同時地升高閘極電位和電源線訊號的電源線驅動器14配備在針對驅動TFT 22之汲極電極和閘極電極的電流供應線與電源之間。注意：術語"同時地"(simultaneously)不只是意謂著時間完全符合之狀態。為了得到本實施例之優點，藉由"幾乎同時地"(almost simultaneously)設定時序(它包括其間有一既定時間間隔)，就能夠獲得類似效果。這樣一種觀點可以等效地應用在指出該術語的其它場合中。

圖4是：用來說明在50[攝氏度]時之被驅動的驅動TFT 22的Vth之偏移量的示意圖。在圖4中，縱軸指示臨限電壓(Vth)的偏移量(伏)，而橫軸則指示時間(小時)。圖4顯示：藉由依照50%之工作比而循序地改變閘極電壓和汲極/源極電壓來驅動的狀態。由圖4中的諸多三角形標記所指示之一曲線(plot)顯示基於傳統模式之Vth的偏移量，其中：將汲極電壓Vd保持上升(在10伏處)而與閘極電壓Vg的間歇性升高無關。於其時，由圖4中的諸多正方形標記所指示之一曲線顯示：當汲極電壓Vd隨著閘極電壓Vg的間歇性升高而一起間歇地升高(10伏和0伏)時之Vth的偏移量。如圖4中所顯示，會瞭解到：當間歇地和同時地升高閘極電壓Vg和汲極電壓Vd時，就會減少Vth的偏移量。結果是，有可能將驅動TFT 22的耐用期延長二倍或更長。

圖5是：用來顯示在35[攝氏度]時驅動著驅動TFT 22的時候加以去除導因於一種具有大活化能的電流之變質分量(正偏移)的結果之示意圖。縱軸指示臨限電壓(Vth)的偏移量(伏)，而橫軸則指示時間(小時)。由圖中的諸多三角形

除汲極與源極之間的電位差。由於電子都未受激勵，故而可以想像得到的是：將正電洞捕獲於非晶矽中，因而造成臨限電壓(Vth)的負偏移。雖然在一初始狀態中會將正電洞(正電荷)捕獲於非晶矽TFT中，但是藉由上述的機制卻會隨著時間流逝而將正電洞逐漸地捕獲於其中。這樣一種負偏移效果會抵消部份的正偏移。最後，能夠減少臨限電壓(Vth)之偏移。

因此，為了要以負偏移效果來抵消部份的正偏移進而藉以減少臨限電壓(Vth)之偏移，其方法是不會受限於間歇地和幾乎同時地升高電壓的情形。換成是，當將閘極電壓供應到閘極電極時，若將電壓供應到源極電極或汲極電極，則其效果是令人滿意的。為了消除當降低閘極電壓時的汲極與源極之間的電位差，最好是：當降低閘極電壓時，停止供應電壓到源極電極或汲極電極。而且，將針對間歇地升高打算供應到源極電極或汲極電極的電壓之電流值和工作比加以確定，使得總電荷量符合作為結果。

如以上描述的，在本實施例中，構成當作驅動OLED之驅動TFT來使用的非晶矽TFT，以便間歇地和幾乎同時地升高閘極電壓和汲極電壓(電源線電壓)。以此方式，藉由間歇地升高來自電源線驅動器14之電源線訊號，就能夠利用導因於閘極電壓和汲極電壓(電源線電壓)之間歇性和同時地升高的Vth之負偏移分量來抵消：在非晶矽TFT中之臨限電壓(Vth)的正偏移變質。結果是，有可能減少臨限電壓(Vth)之偏移。藉由減少臨限電壓(Vth)之偏移，就有可能延長非晶矽TFT的耐用期，因而藉以延長使用非晶矽TFT之OLED顯示器的耐用

期。雖然針對非晶矽TFT作為實例而已經描述本實施例，但是關於通常具有挺小臨限電壓(Vth)偏移的多晶矽TFT方面，類似的控制是切實可行的。然而，毋庸贅言的是：關於臨限電壓(Vth)之偏移問題，本發明針對非晶矽TFT會更有效地執行功能。

如以上描述的，根據本發明，假若以TFT來驅動OLED，則有可能減少在TFT中所產生的臨限電壓(Vth)之正偏移，進而達成延長這樣一種由TFT驅動的OLED顯示器之耐用期。

雖然已經詳細地描述本發明的較佳實施例，但是應該瞭解的是：在沒有背離像由所附申請專利範圍所界定那樣的本發明之精神和範圍的前提下，其中能夠做出各種改變、替換以及交替。

圖式代表符號說明

10 有機發光二極體(OLED)顯示器

11 控制單元

12 掃描線驅動器

13 資料線驅動器

14 電源線驅動器

15 公用線驅動器

20 驅動電路

21 有機發光二極體(OLED)

22 驅動薄膜電晶體(TFT)

23 切換薄膜電晶體(TFT)

24 電容器

拾、申請專利範圍

1. 一種顯示裝置，包括：

一有機發光二極體；

一非晶矽薄膜電晶體，其用來驅動有機發光二極體；以及

一電源線驅動器，當降低施加到非晶矽薄膜電晶體之閘極電極的閘極電壓時，其用來降低施加到源極電極和汲極電極其中之一電極的電源線電壓。

2. 根據申請專利範圍第1項之顯示裝置，其中當升高閘極電壓時，電源線驅動器會將電源線電壓保持上升。

3. 一種顯示裝置，包括：

一有機發光二極體；

一驅動電晶體，其用來驅動有機發光二極體；以及

一電源線驅動器，當間歇地升高電壓時，其用來供應電壓到驅動電晶體之源極電極和汲極電極其中任何一個電極。

4. 根據申請專利範圍第3項之顯示裝置，其中電源線驅動器會依照與間歇地升高驅動電晶體之閘極電極相同的時序加以間歇地升高施加到源極電極和汲極電極其中任何一個電極的電源線電壓。

5. 一種顯示裝置，包括：

驅動裝置，其藉由使用薄膜電晶體來驅動有機發光二極體；

閘極電壓供應裝置，其用來間歇地升高施加到驅動裝

置中的薄膜電晶體之閘極電極的閘極電壓；以及

控制裝置，其執行控制，使得當藉由閘極電壓供應裝置來降低施加到閘極電極的閘極電壓時，將跨接於薄膜電晶體之汲極電極和源極電極的電位差加以消除。

6. 根據申請專利範圍第5項之顯示裝置，其中

閘極電壓供應裝置會基於從掃描線驅動器供應之掃描線訊號和從資料線驅動器供應之資料線訊號而間歇地升高閘極電壓，以及

控制裝置會隨著藉由閘極電壓供應裝置來降低閘極電壓而同步地降低施加到薄膜電晶體的電源線電壓。

7. 一種有機發光二極體面板，包括：

一自發光有機發光二極體，將其配備在每個像素上；以及

一非晶矽薄膜電晶體，其用來驅動有機發光二極體；

其中將非晶矽薄膜電晶體加以控制，使得當停止供應電壓到閘極電極時，藉由造成將正電洞捕獲於非晶矽中來減少臨限電壓(Vth)的偏移量。

8. 根據申請專利範圍第7項之有機發光二極體面板，其中當停止供應電壓到閘極電極時，跨接於非晶矽薄膜電晶體之汲極和源極的電壓變成等於0伏。

9. 一種用於薄膜電晶體的控制裝置，包括：

閘極電壓供應裝置，其會供應閘極電壓到驅動有機發光二極體之薄膜電晶體的閘極電極；以及

電壓供應裝置，其會供應電壓到薄膜電晶體之源極電

極和汲極電極其中任何一個電極，並且當藉由閘極電壓供應裝置來降低閘極電壓時，其會降低施加到源極電極和汲極電極其中任何一個電極的電壓。

10. 根據申請專利範圍第9項之用於薄膜電晶體的控制裝置，其中當藉由閘極電壓供應裝置來供應閘極電壓到薄膜電晶體的閘極電極時，電壓供應裝置會將供應到源極電極和汲極電極其中任何一個電極的電壓保持上升。

11. 一種用來控制會驅動有機發光二極體之薄膜電晶體的方法，包括下列步驟：

控制施加到薄膜電晶體之源極電極和汲極電極其中任何一個電極的電壓，使得當升高供應到薄膜電晶體之閘極電極的閘極電壓時，將該電壓保持上升；以及

控制施加到源極電極和汲極電極其中任何一個電極的電壓，使得當降低閘極電壓時，將該電壓降低。

12. 根據申請專利範圍第11項之用來控制薄膜電晶體的方法，其中供應到源極電極和汲極電極其中任何一個電極的電壓隨著閘極電壓的升高而同步地升高。

13. 一種用來控制有機發光二極體顯示器的方法，包括下列步驟：

將一種基於資料訊號的電壓供應到驅動有機發光二極體之薄膜電晶體；以及

根據預定工作比，在間歇地升高電源線電壓的時候，將電源線電壓供應到薄膜電晶體。

14. 根據申請專利範圍第13項之用來控制有機發光二極體顯

示器的方法，其中在供應電源線電壓的步驟中，藉由打算供應到薄膜電晶體的整體電荷量來確定電源線電壓之電壓值。

拾壹、圖式

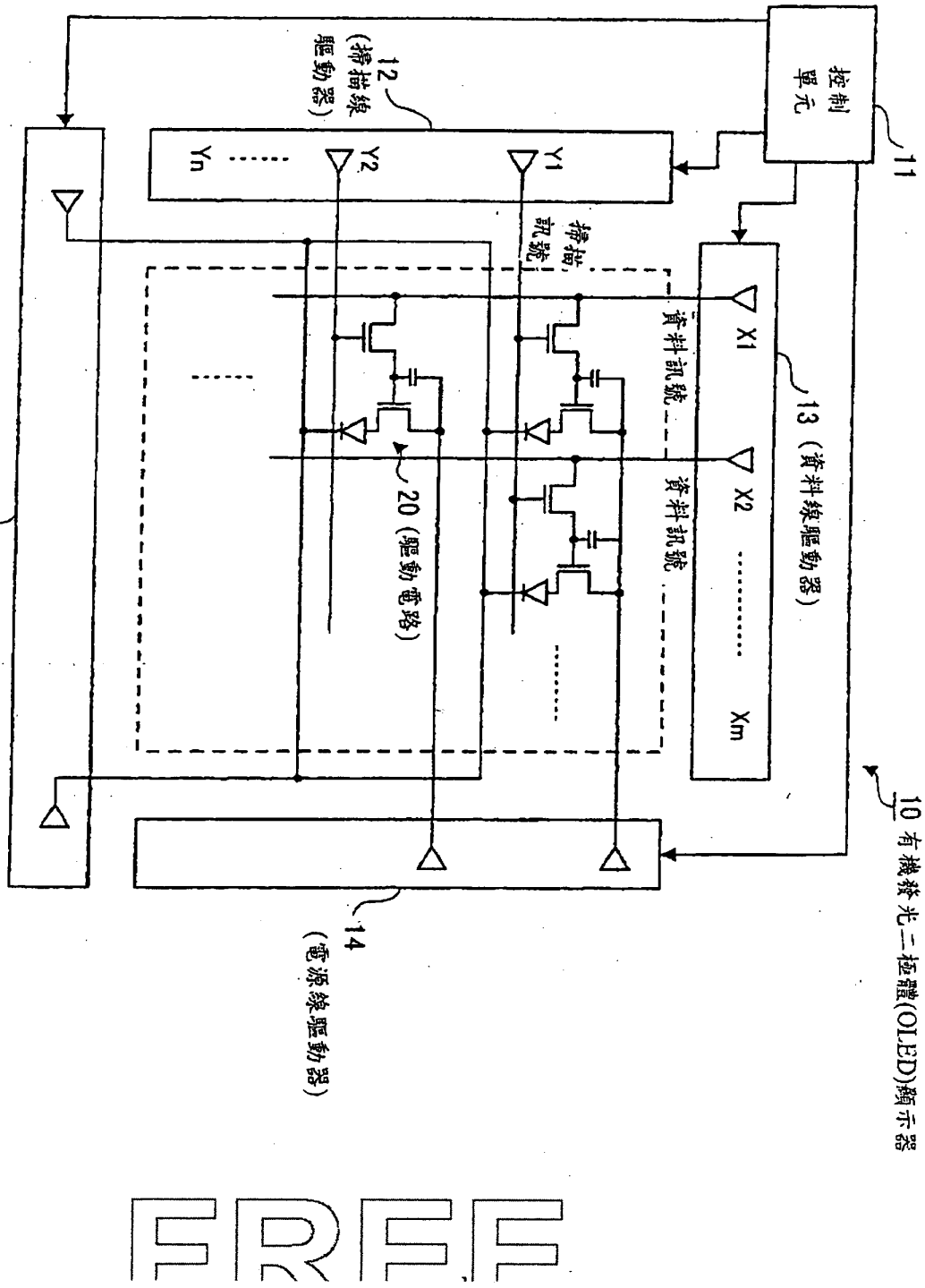

圖 1

來自資料線驅動器13
資料訊號
來自掃描線驅動器12
掃描訊號
23
(切換薄膜電晶體(TFT)
24
(電容器)
20 (驅動電路)
電流供應線
來自電源線驅動器14
22 (驅動薄膜電晶體(TFT)
21 有機發光二極體(OLED)
陰極
到公用線驅動器15

圖 2

圖式頁

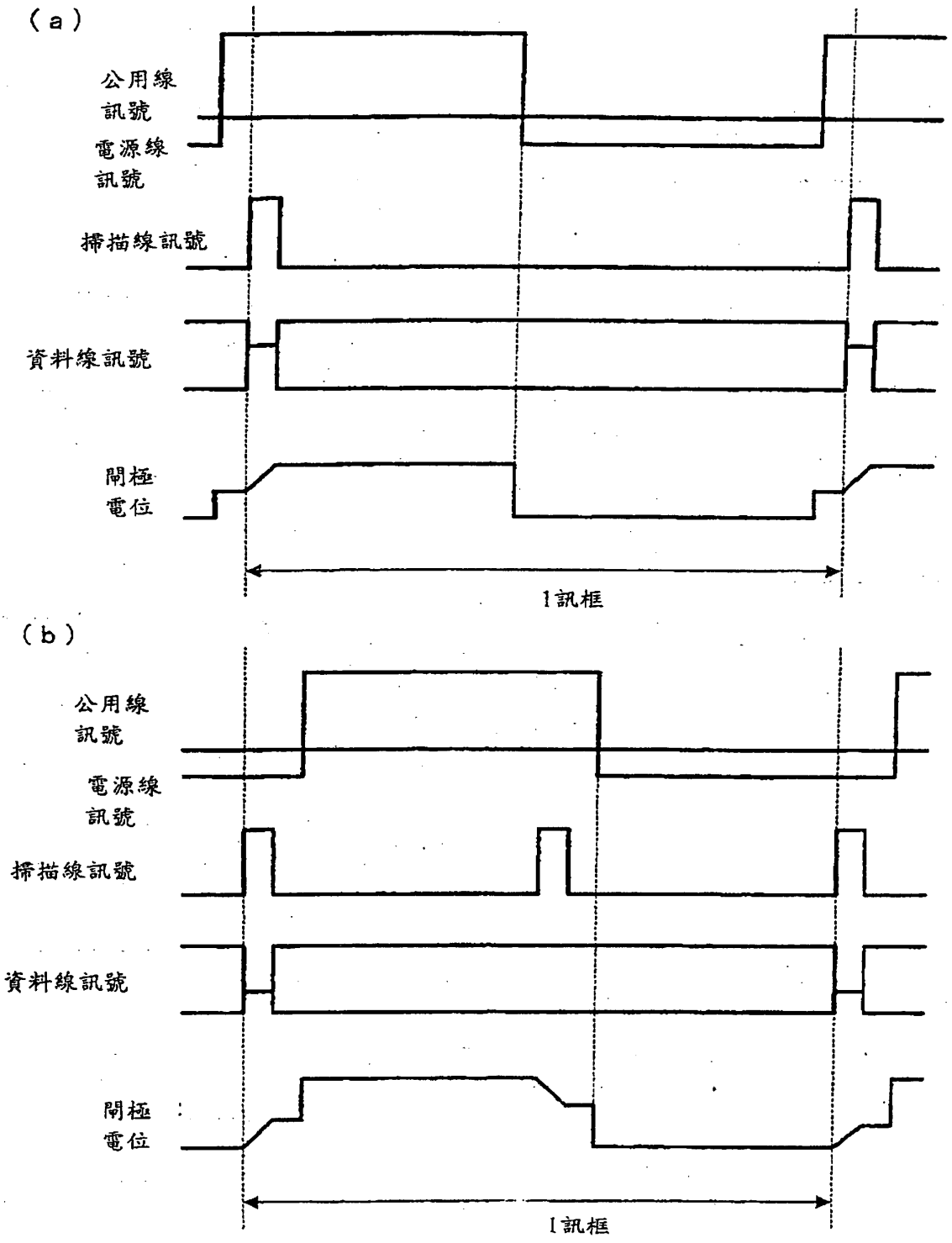

圖 3

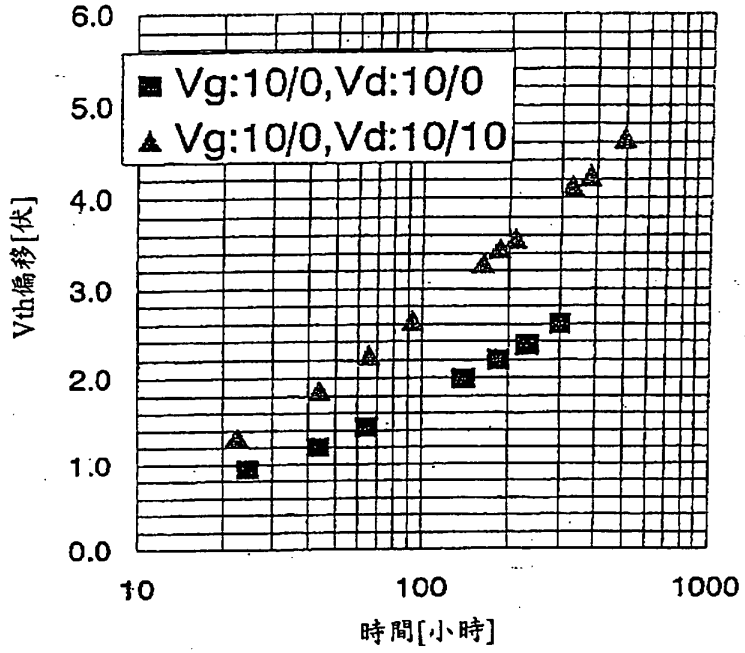

圖 4

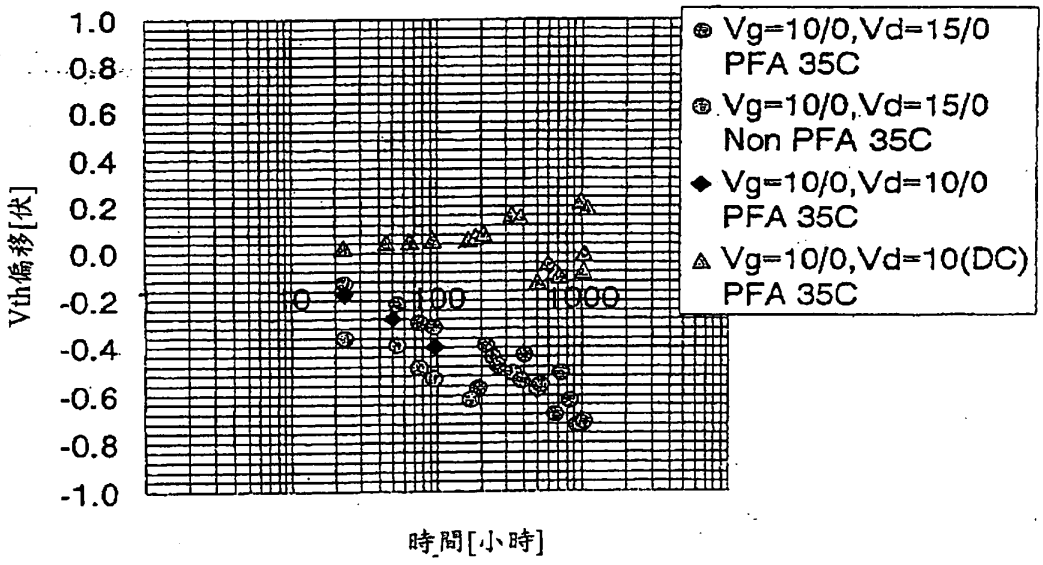

圖 5

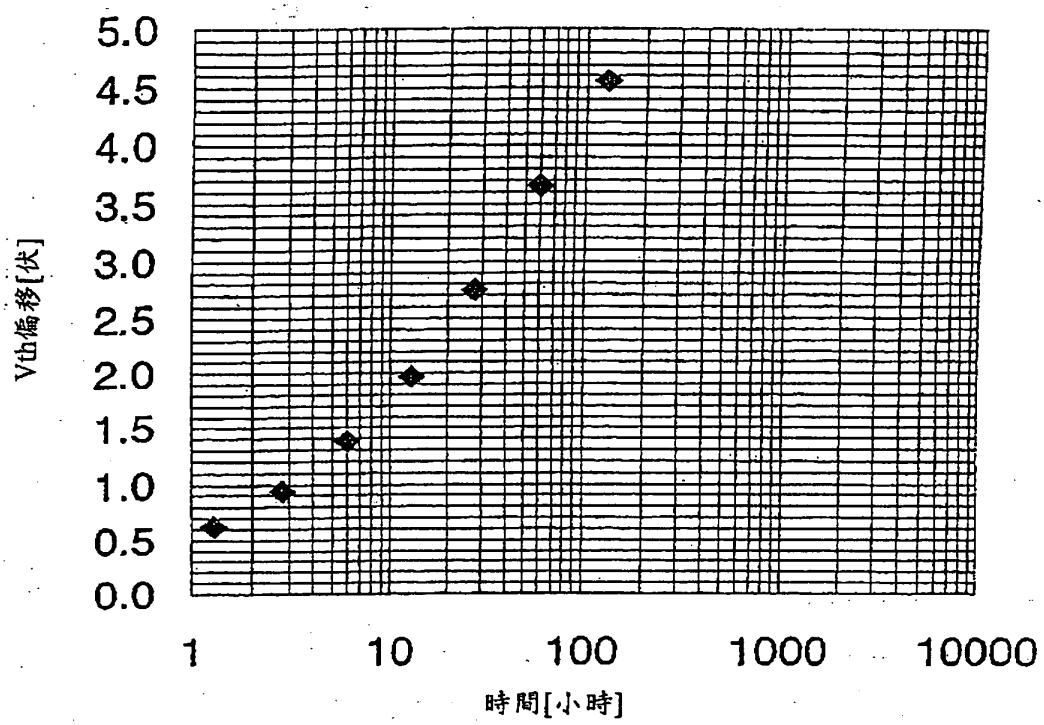

圖 6

公告本

申請日期：	91.10.12 案號： 91117606
類別：	G09G 3/00

（以上各欄由本局填註）

發明專利說明書 594628

一、發明名稱	中文	有機電激發光顯示器之單位像素驅動電路
	英文	
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	代表人姓名（中文）	1. 李焜耀
	代表人姓名（英文）	1.

本案已向

國(地區)申請專利	申請日期	案號	主張優先權
無			

有關微生物已寄存於

寄存日期	寄存號碼
無	

五、發明說明 (1)

發明領域：

本發明與一種有機發光元件之驅動電路有關，特別是關於一種應用於有機發光二極體元件(Organic Light Emitting Diode; OLED)與非晶矽薄膜電晶體(a-Si TFT)之單位像素驅動電路，以便有效的延長有機電激發光顯示器的壽命。

發明背景：

隨著積體電路製作技術突飛猛進的腳步，電子科技持續的發展與進步，促使各式各樣的電子產品皆朝著「數位化」發展。並且，為了符合輕便性與實用性之考量，在電子產品在設計上，都趨向以輕薄短小、功能多、處理速度快來作為設計規格，以便製作的產品能更容易攜帶，且更符合現代的生活需求。特別是在多媒體電子產品大行其道後，夾著其強大的運算能力，可輕易的處理各種音效、影像、圖樣等數位化資料，連帶的使影像播放設備受到廣泛的發展與運用。不論是個人數位處理器、筆記型電腦、隨身聽、數位相機、或行動電話等等，皆會裝設顯示螢幕以方便消費者瀏覽資訊或影像。

在傳統的顯示器製作中，由於薄膜電晶體技術的成熟，使得具備了輕薄、省電、無幅射線等優點的液晶顯示

五、發明說明 (2)

器，廣受消費者的喜愛與使用。然而，隨著有機發光二極體技術的研究與開發，新式的有機電激發光顯示器由於具備了高發光效率、高應答速度、省電、無視角限制、重量輕、厚度薄、高亮度以及可全彩化等優點，而可促使各種可攜性電子產品，在設計上更為輕薄短小，且具有更加精緻的影像顯示效果。

請參照第一圖，此圖顯示了有機電激發光顯示器中單位像素之電路結構10。此電路結構10係製作於非晶矽底材上，其元件包括了兩個薄膜電晶體12與14、以及一個儲存電容16，用以電壓驅動有機發光二極體元件18。其中，電晶體12主要作為一開關使用，其汲極端係連接至資料線，而其閘極端則連接於掃描線，至於其源極端則同時連接於儲存電容16之一端、以及電晶體14之閘極。另一方面，電晶體14的汲極端，係連接於操作電壓源(V_{dd})，並且其源極、以及儲存電容16的另一端皆連接於有機發光二極體元件18的正極，至於有機發光二極體元件18的負極則會連接至電壓源(V_{ss})。

如此，在進行操作程序時，可藉著由掃描線輸入之訊號，導通電晶體12，而使資料線上的影像資料得以傳送至此單元像素中。其中，當電晶體12導通時，位於資料線上的電壓訊號可施加於電晶體14的閘極，且儲存於電容16中。此電壓訊號並會導通電晶體14，使電壓源V_{dd}上的電壓

五、發明說明（3）

施加於有機發光二極體元件18的正極，並使元件18產生發光效果。其中，藉著使用電容16來儲存資料電壓，可以在掃描線上的訊號關閉電晶體12時，繼續維持電晶體14的開啟，以便在資料供給的空檔中，仍可讓有機發光二極體元件18維持在一定的電流位準。

然而，值得注意的是，以上述的電路設計而言，由於有機發光二極體元件18係直接連接於電晶體14的源極端，是以其跨壓（V_{OLED}）會直接影響到電晶體14的閘-源極電壓（V_{gs}），進而影響電晶體14的汲極電流（I_d）。其電流公式如下所示：

$$I_d = 1/2 * K(V_{gs} - V_{th})^2$$
$$= 1/2 * K[V_{data} - (V_{OLED} - V_{ss}) - V_{th}]^2$$

其中，K為常數，V_{data}為資料線上的電壓訊號，至於V_{th}則為電晶體14的啟始電壓。由於有機發光二極體元件18在長時間的操作後，其跨壓（V_{OLED}）會逐漸增加，而造成汲極電流I_d變小。如此一來，會導致有機發光二極體元件18的亮度變小，並導致顯示器的壽命縮短。

發明目的及概述：

本發明之目的在提供一種應用於有機電激發光顯示器之單位像素電路設計，以防止有機發光二極體元件的跨壓改變，而降低了驅動電晶體的操作電流。

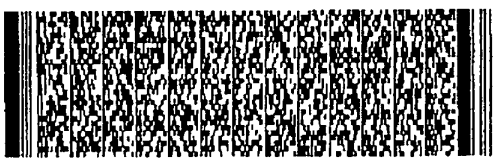
五、發明說明（4）

本發明之另一目的在提供一種防止有機電激發光顯示器亮度下降之電路設計，以延長顯示器的使用壽命。

本發明揭露了一種有機發光二極體元件之電壓驅動電路。此電壓驅動電路至少包括下列元件。一驅動電晶體，具有閘極、源極與汲極，其中汲極係連接於電源線，源極則連接於有機發光二極體元件。第一開關電晶體，具有第一閘極、第一汲極與第一源極，其中第一閘極係連接於一掃描線，第一源極係連接於電源端，而第一汲極則連接於驅動電晶體之閘極，當第一開關電晶體回應於掃描線上之掃描訊號而導通時，可讓電源端之電壓訊號施加於驅動電晶體並將其導通。第二開關電晶體，具有第二閘極、第二汲極與第二源極，其中第二閘極係連接於掃描線，第二汲極係連接於一資料線，而第二源極則連接於驅動電晶體之源極，當第二開關電晶體回應於掃描線上之掃描訊號而導通時，可讓資料線上之資料訊號施加於驅動電晶體之源極。

發明詳細說明：

本發明提供了一種單元像素電路結構之設計，可應用於結合了非晶矽薄膜電晶體(a-Si TFT)與有機發光二極體元件(OLED)之主動驅動有機電激發光顯示器(AMOLED)。藉



著使用兩個開關電晶體，來控制驅動電晶體的開關、以及維持其閘極-源極電壓位準，可防止有機發光二極體元件的跨壓(V_{OLED})，影響驅動電晶體的操作電流。如此，即使在長時間的操作下，上述跨壓(V_{OLED})增加，也不會影響到驅動電晶體的操作電流。由此，有機發光二極體元件的亮度就不會減少，且能有效的增加顯示器的使用壽命。

請參照第二圖，此圖顯示了本發明所提供應用於有機電激發光顯示器之單位像素電路結構30。如同熟知技術一般，在顯示器的相關製程中，會在一玻璃基板上依序定義薄膜電晶體圖案與各式的連線圖案。其中，這些連線圖案包括了滿佈於面板上交錯縱橫的掃描線與資料線，以便連接至每一個單位像素，而傳送相關的掃描訊號與資料訊號。至於在每一個單位像素結構30中，則包括了一有機發光二極體32、一驅動電晶體34、以及兩個開關電晶體36與38。

所述有機發光二極體元件32具有正極與負極，其負極係連接於接地端V_{ss}，至於其正極則會經由驅動電晶體34，而連接至電源端V_{dd}。至於驅動電晶體34，則具有作為控制端使用之閘極、汲極與源極等三個接腳。其中，驅動電晶體34的閘極連接於掃描線，以便根據掃描訊號控制此電晶體導通。至於其汲極與源極，則分別連接於上述電源端V_{dd}與有機發光二極體32之正極端，而可在導通時將電源端V_{dd}

的電壓訊號施加於有機發光二極體元件32，以使其產生發光效果。

為了有效防止驅動電晶體34的汲極電流受到有機發光二極體元件32其跨壓的影響，本發明中利用了兩個電晶體來控制驅動電晶體34開關、以及維持其閘極-源極的電壓位準。其中，開關電晶體36之閘極係連接於所述掃描線，其源極係連接於電源端V_{dd}，而汲極則連接於驅動電晶體34之閘極。當此開關電晶體36回應於掃描線上的掃描訊號而導通時，可使電源端V_{dd}的電壓訊號施加於驅動電晶體34的閘極並將其導通。此時，驅動電晶體34的閘極端，可維持於所述掃描訊號的位準。

至於，另一個開關電晶體38，其閘極係連接於上述掃描線，其汲極則係連接於上述資料線，至於其源極則連接於驅動電晶體34之源極。當此開關電晶體38回應於掃描訊號而導通時，可讓資料線上的資料訊號，直接施加於驅動電晶體34的源極，而使其維持於資料訊號的電壓位準。

要特別說明的，在本發明所提供的單位像素電路結構中，並具有一儲存電容40。此儲存電容40之一端，分別連接於驅動電晶體34的閘極、以及開關電晶體36的源極。至於儲存電容40的另一端，則分別連接於驅動電晶體34的源極、以及開關電晶體38的源極。如此一來，當開關電晶體

持續作用後，驅動電晶體的操作電流，亦不會因有機發光二極體元件壓降的變化而下降。

（2）由於驅動電晶體的操作電流可維持不變，是以有機發光二極體元件的發光亮度也不會減少，而可使顯示器的影像品質獲得提昇，並有效的延長顯示器的壽命。

本發明雖以較佳實例闡明如上，然其並非用以限定本發明精神與發明實體，僅止於上述實施例爾。例如，在上述的實施例中，雖然是以NMOS來做為開關元件說明。其中，利用了第一開關元件來控制驅動電晶體開關、且維持其閘極的電壓位準，並且利用了第二開關元件，來控制驅動電晶體的源極電壓位準。對熟悉此項技術者，當可輕易了解並利用其它元件，來產生相同的開關功能。是以，在不脫離本發明之精神與範圍內所作之修改，均應包含在下述之申請專利範圍內。

圖式簡單說明

藉由以下詳細之描述結合所附圖示，將可輕易的了解上述內容及此項發明之諸多優點，其中：

第一圖顯示傳統技術中有機電激發光顯示器之單元像素電路結構；以及

第二圖顯示本發明所提供有機發光二極體元件之單元像素電路結構。

圖號對照表：

單位像素電路結構 10	薄膜電晶體 12、14
儲存電容 16	有機發光二極體元件 18
單位像素電路結構 30	有機發光二極體 32
驅動電晶體 34	開關電晶體 36、38
接地端 V_{ss}	電源端 V_{dd}
儲存電容 40	

六、申請專利範圍

1. 一種有機發光二極體元件之驅動電路，該驅動電路至少包括：

一驅動電晶體，具有一控制端、一第一電極與一第二電極，其中該第一電極與該第二電極分別連接於一電源端與一有機發光二極體；

一第一開關元件，回應於一掃描訊號而開啟，以導通該電源端與該驅動電晶體之該控制端，以便該控制端維持於該電源端之位準；及

一第二開關元件，回應於該掃描訊號而開啟，以導通一資料線與該驅動電晶體之該第二電極，並將該資料線上之資料訊號施加於該第二電極，以便該第二電極維持於該資料訊號之位準；

其中，藉著維持該驅動電晶體之該控制端以及該第二電極的電壓位準，可防止該驅動電晶體之操作電流，受到該有機發光二極體元件其跨壓變化的影響。

2. 如申請專利範圍第1項之驅動電路，其中該第一開關元件是由一電晶體所構成，其閘極係連接於一掃描線，其源極與汲極則分別連接於該電源端與該驅動電晶體之該控制端。

3. 如申請專利範圍第1項之驅動電路，其中該第二開關元件是由一電晶體所構成，其閘極係連接於該掃描線，其汲極與源極則分別連接於該資料線與該驅動電晶體之該

六、申請專利範圍

第二電極。

4. 如申請專利範圍第1項之驅動電路，其中該驅動電晶體之該控制端為閘極，而該第一電極為汲極，該第二電極則為源極。

5. 如申請專利範圍第1項之驅動電路，其中更包括一儲存電容，該儲存電容之兩端，分別連接於該驅動電晶體之該閘極與該源極。

6. 一種有機發光二極體元件之驅動電路，該驅動電路至少包括：

一驅動電晶體，具有一閘極、一源極與一汲極，其中該汲極係連接於一電源端，該源極則連接於該有機發光二極體元件；

一第一開關電晶體，具有一第一閘極、一第一汲極與一第一源極，其中該第一閘極係連接於一掃描線，該第一源極係連接於該電源端，而該第一汲極則連接於該驅動電晶體之該閘極，當該第一開關電晶體回應於該掃描線上之掃描訊號而導通時，可讓該電源端之電壓訊號施加於該驅動電晶體並將其導通；

一第二開關電晶體，具有一第二閘極、一第二汲極與一第二源極，其中該第二閘極係連接於該掃描線，該第二汲極係連接於一資料線，而該第二源極則連接於該驅動電

六、申請專利範圍

晶體之該源極，當該第二開關電晶體回應於該掃描線上之該掃描訊號而導通時，可讓該資料線上之資料訊號施加於該驅動電晶體之該源極。

7. 如申請專利範圍第6項之驅動電路，其中更包括一儲存電容，該儲存電容之兩端，分別連接於該第一開關電晶體之該第一汲極、以及該第二開關電晶體之該第二源極。

8. 一種應用於有機電激發光顯示器之單位像素電路，至少包括：

一掃描線，用以傳送該單位像素之掃描訊號；

一資料線，用以傳送該單位像素之資料訊號；

一有機發光二極體，具有一正極與一負極，且該負極係連接於一接地端；

一驅動電晶體，具有一控制端、一第一電極與一第二電極，該第一電極與該第二電極分別連接於一電源端與該有機發光二極體之該正極；

一第一開關電晶體，回應於該掃描線上之該掃描訊號，而導通該電源端與該驅動電晶體之該控制端，以便該控制端可維持於該掃描訊號之位準；

一第二開關電晶體，回應於該掃描線上之該掃描訊號，而導通該資料線與該驅動電晶體之該第二電極，以便該第二電極可維持於該資料訊號之位準；

六、申請專利範圍

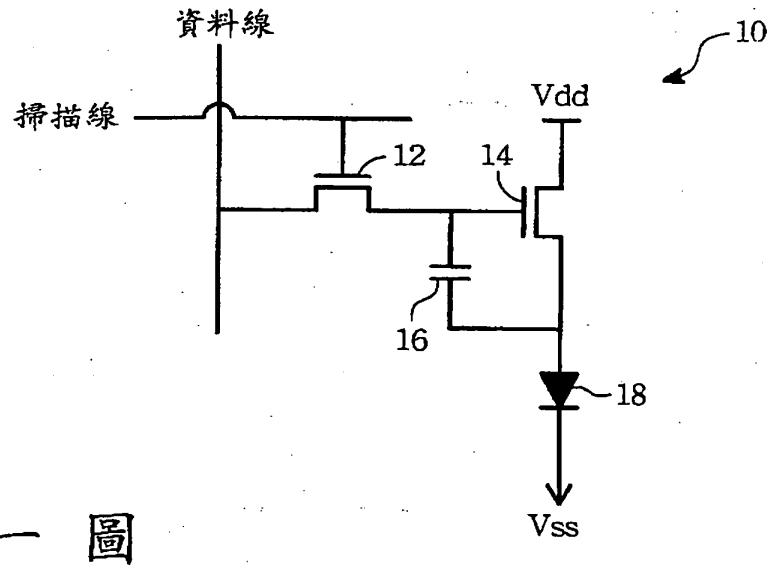
如此，當該掃描訊號同時導通該第一開關電晶體與該第二開關電晶體時，可導通該驅動電晶體之該第一電極與該第二電極，而使該有機發光二極體元件產生發光效果。

9. 如申請專利範圍第8項之單位像素電路，其中該第一開關電晶體之閘極係連接於該掃描線，其源極與汲極則分別連接於該電源端與該驅動電晶體之該控制端。

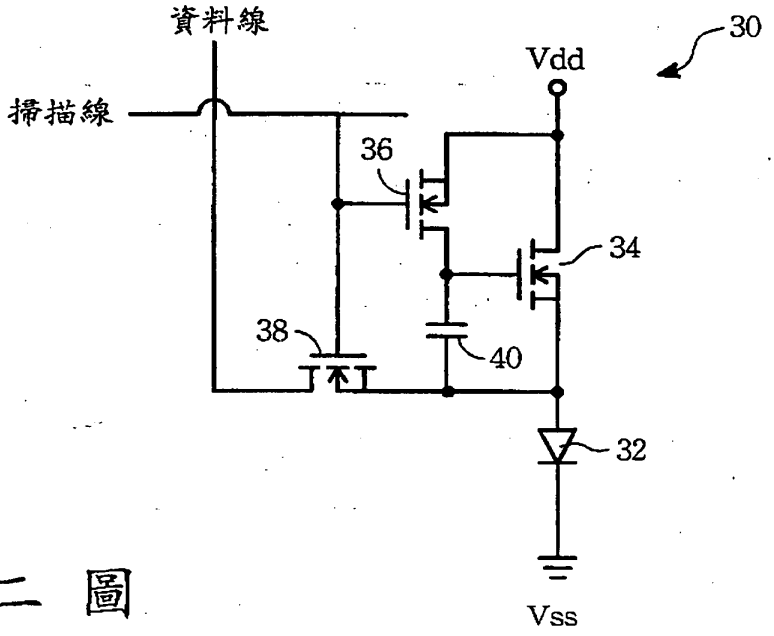
10. 如申請專利範圍第8項之單位像素電路，其中該第二開關電晶體之閘極係連接於該掃描線，其汲極與源極則分別連接於該資料線與該驅動電晶體之該第二電極。

11. 如申請專利範圍第8項之單位像素電路，其中該驅動電晶體之該控制端為閘極，而該第一電極為汲極，該第二電極則為源極。

12. 如申請專利範圍第8項之單位像素電路，其中更包括一儲存電容，該儲存電容之兩端，分別連接於該驅動電晶體之該閘極與該源極。



第 一 圖



第 二 圖

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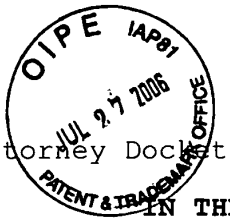

Attorney Docket No. 05644/LH

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Tomoyuki SHIRASAKI et al

Serial No. : 11/235,579

Filed : September 26, 2005

For : DISPLAY PANEL

Art Unit : 2673

Examiner :

Customer No.: 01933

Express Mail Mailing Label No.: EV 919 339 798 US
Date of Deposit: July 27, 2006
I hereby certify that this paper is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service with sufficient postage under 37 CFR 1.10 on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

S. Dianne Franklin

In the event that this Paper is late filed, and the necessary petition for extension of time is not filed concurrently herewith, please consider this as a Petition for the requisite extension of time, and to the extent not tendered by credit card (Form PTO-2038 attached hereto), authorization to charge the extension fee, or any other fee required in connection with this Paper to Account No. 06-1378.

INFORMATION DISCLOSURE STATEMENT WITH STATEMENTS UNDER 37 CFR 1.97)(e) AND 37 CFR 1.704(d)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

S I R :

Submitted herewith are the following:

(1) Copy of an International Search Report and Written Opinion dated June 30, 2006 issued in a counterpart International application;

(2) Copies of cited publications (except U.S. patents and publications); and

(3) Forms PTO/SB/08A and PTO/SB/08B.

The International Search report is in English, thereby satisfying the requirements for a concise explanation of relevance for any non-English language publications cited therein (MPEP 609 III A(3)).

Said communication is in English, thereby satisfying the requirements for a concise explanation of relevance for any non-English language publications cited therein (MPEP 609 III A(3)).

As seen from the listing of family members, US 2003/137325 is a U.S. counterpart of EP 1,331,666, US 2003/193056 is a U.S. counterpart of EP 1,349,208, and US 2004/256617 is a U.S. counterpart of WO 2004/019314.

RELATED APPLICATION

The following application is related to the above-identified present application:

Serial No. 11/235,605, filed September 26, 2005.

Attached is a Form PTO/SB/08B listing the particulars of the related application. Said pending U.S. related application is stored in the USPTO's Image File Wrapper system.

References cited in said related application, and which have not yet been cited herein, are now cited.

STATEMENT UNDER 37 CFR 1.97(e)(1)

Each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the present Information Disclosure Statement. Said Communication bears a mailing date of June 30, 2006. Therefore, the filing of this Information Disclosure Statement is timely under the provisions of 37 CFR 1.97(e) and does not require a fee.

STATEMENT UNDER 37 CFR 1.704(d)

Each item of information contained in this Information Disclosure Statement was cited in said communication from a foreign patent office in a counterpart application, and this communication was not received by any individual designated in §1.56(c) more than thirty days prior to the filing of the present Information Disclosure Statement.

It is respectfully requested that the Examiner return initialed copies of the attached Forms PTO/SB/08A and PTO/SB/08B to confirm that the documents listed therein have all been considered and made of record.

Respectfully submitted,

Leonard Holtz, Esq.
Reg. No. 22,974

Encs.

Dated: July 27, 2006

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PTO/SB/08A (08-00)

U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Substitute for Form 1449A/PTO	Application Number	11/235,579
	Filing Date	September 26, 2005
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	First Named Inventor	Tomoyuki SHIRASAKI et al
	Group Art Unit	2673
	Examiner Name	
Sheet 1 of 2	Attorney Docket Number	05644/LH

U.S. PATENT DOCUMENTS

Exam. Inits*	Cite No[1]	Document Number	Kind Code[2]	Name of Patentee or Applicant	Publication Date MM-DD-YYYY	Relevant Portion
		2003/0047730	A1	KONUMA	03-13-2003	
		2003/0146693	A1	ISHIHARA et al	08-07-2003	
		2003/0151355	A1	HOSOKAWA	08-14-2003	
		2004/0160170	A1	SATO et al	08-19-2004	
		2003/137325	A1	YAMAZAKI et al	07-24-2003	
		2004/256617	A1	YAMADA et al	12-23-2004	
		2003/0168992	A1	NOGUCHI et al	09-11-2003	
		2003/193056	A1	TAKAYAMA et al	10-16-2003	

FOREIGN PATENT DOCUMENTS

Exam Inits*	Cite No[1]	Offc[3]	Document Number[4]	Kind Code[5]	Name of Patentee or Applicant	Publication Date MM-DD-YYYY	Relevant Portion	T[6]
		EP	1 331 666	A2	SEMICONDUCTOR ENERGY LABORATORY CO.,LTD.	07-30-2003		
		WO	2004/019314	A1	CASIO COMPUTER CO., LTD.	03-04-2004		
		EP	1 349 208	A1	SEMICONDUCTOR ENERGY LABORATORY CO., LTD.	10-01-2003		

Examiner Signature		Date Considered	

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Unique citation designation number. [2] See kinds of U.S. Patent Documents. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Place a check here if English translation is attached.

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PTO/SB/08B (08-00)

U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Substitute for Form 1449A/PTO				Application Number	11/235,579
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date	September 26, 2005
				First Named Inventor	Tomoyuki SHIRASAKI et al
				Group Art Unit	2673
				Examiner Name	
Sheet	2	of	2	Attorney Docket Number	05645/LH

OTHER DOCUMENTS - NON-PATENT LITERATURE DOCUMENTS

Examiner Initials[1]	Cite No.[1]	Include name of author (in CAPITAL LETTERS), title of article, title of item, date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
		Related U.S. Patent Application Serial No. 11/235,605, filed: September 26, 2005; Inventors: Satoru SHIMODA et al; Title: DISPLAY PANEL.	

Examiner Signature		Date Considered	

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[1] Unique citation designation number. [2] Place a check here if English translation is attached.

DATE MAILED: July 27, 2006

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(11) EP 1 331 666 A2

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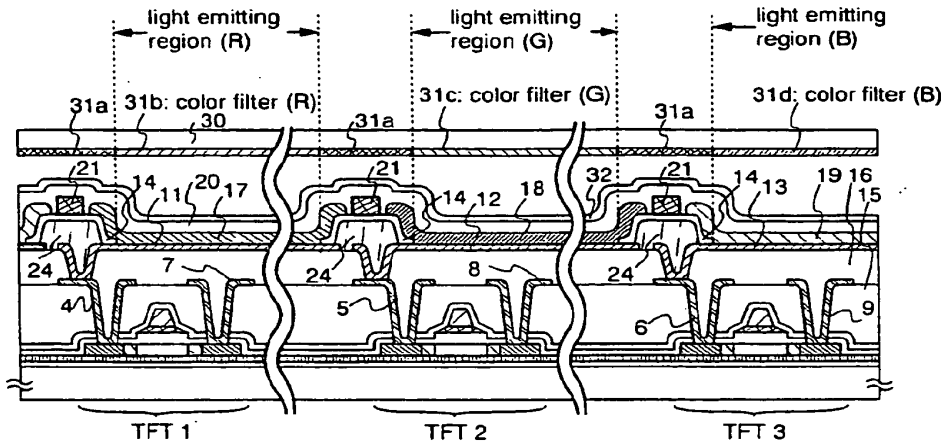
(54) Light emitting device and method of manufacturing the same

(57) To provide a light emitting device high in reliability with a pixel portion having high definition with a large screen. According to a light emitting device of the present invention, on an insulator (24) provided between pixel electrodes, an auxiliary electrode (21) made of a metal film is formed, whereby a conductive layer (20) made of a transparent conductive film in contact with the auxiliary electrode can be made low in resistance and thin. Also, the auxiliary electrode (21) is used to achieve connection with an electrode on a lower layer, whereby the electrode can be led out with the transparent conductive film formed on an EL layer. Further, a protective film (32) made of a film containing hydrogen and a silicon nitride film which are laminated is formed, whereby high reliability can be achieved.

FIG. 1A sectional view of A-A'



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EP 1 331 666 A2

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a semiconductor device and, particularly, to a light emitting device having an organic light emitting element formed over a substrate having an insulating surface and a manufacturing method therefor. The present invention also relates to a module in which an IC etc. including a controller is mounted on a panel having the organic light emitting element. Note that, in this specification, the panel and the module which have the organic light emitting element are collectively referred to as a light emitting device. Further, the present invention relates to an apparatus for manufacturing the light emitting device.

[0002] Note that, in this specification, the term semiconductor device refers to the devices in general which can function by utilizing semiconductor characteristics. The light emitting device, an electro-optic device, a semiconductor circuit, and an electronic device are all included in the category of the semiconductor device.

2. Description of the Related Art

[0003] Techniques of forming TFTs (thin film transistors) on substrates have been progressing greatly in recent years, and developments in their application to active matrix display devices is advancing. In particular, TFTs that use polysilicon films have a higher electric field effect mobility (also referred to as mobility) than TFTs that use conventional amorphous silicon films, and therefore high speed operation is possible. Developments in performing control of pixels by forming driver circuits made from TFTs that use polysilicon films over a substrate on which the pixels are formed have therefore been flourishing. It has been expected that various advantages can be obtained by using active matrix display devices in which pixels and driver circuits are mounted on the same substrate, such as reductions in manufacturing cost, miniaturization of the display device, increases in yield, and increases in throughput.

[0004] Furthermore, research on active matrix light emitting devices using organic light emitting elements as self light emitting elements (hereinafter referred to simply as light emitting devices) has become more active. The light emitting devices are also referred to as organic EL displays (OELDs) and organic light emitting diodes (OLEDs).

[0005] TFT switching elements (hereinafter referred to as switching elements) are formed for each pixel in active matrix light emitting devices, and driver elements for performing electric current control using the switching TFTs (hereinafter referred to as electric current control TFTs) are operated, thus making EL layers (strictly speaking, light emitting layers) emit light. For example, a light emitting device disclosed in JP 10-189252 is known.

[0006] Organic light emitting elements are self light emitting, and therefore have high visibility. Backlights, necessary for liquid crystal display devices (LCDs), are not required for organic light emitting elements, which are optimal for making display devices thinner and have no limitations in viewing angle. Light emitting devices using organic light emitting elements are consequently being focused upon as substitutes for CRTs and LCDs.

[0007] Note that EL elements have a layer containing an organic compound in which luminescence develops by the addition of an electric field (Electro Luminescence) (hereinafter referred to as EL layer), an anode, and a cathode. There is light emission when returning to a base state from a singlet excitation state (fluorescence), and light emission when returning to a base state from a triplet excitation state (phosphorescence) in the organic compound layer, and it is possible to apply both types of light emission to light emitting devices manufactured by the manufacturing apparatus and film formation method of the present invention.

[0008] EL elements have a structure in which an EL layer is sandwiched between a pair of electrodes, and the EL layer normally has a laminate structure. A "hole transporting layer / light emitting layer / electron transporting layer" laminate structure can be given as a typical example. This structure has extremely high light emitting efficiency, and at present almost all light emitting devices undergoing research and development employ this structure.

[0009] Further, a structure in which: a hole injecting layer, a hole transporting layer, a light emitting layer, and an electron transporting layer are laminated in order on an anode; or a hole injecting layer, a hole transporting layer, a light emitting layer, an electron transporting layer, and an electron injecting layer are laminated in order on an anode may also be used. Fluorescent pigments and the like may also be doped into the light emitting layers. Further, all of the layers may be formed by using low molecular weight materials, and all of the layers may be formed by using high molecular weight materials.

[0010] The conventional active matrix type light emitting device is composed of a light emitting element in which an electrode electrically connected with TFT on the substrate is formed as an anode, then the organic compound layer was formed on the anode. Light generated at the organic compound layer is radiated from the anode that is a transparent electrode to TFT.

[0011] However, in this structure, the problem has arisen when the resolution is intended to be risen that an aperture ratio is limited due to an arrangement of TFT and wirings in the pixel unit.

SUMMARY OF THE INVENTION

[0012] According to the present invention, manufactured is an active matrix light emitting device having the

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light emitting element with a structure in which an electrode on the TFT side electrically connected to the TFT on the substrate is formed as a cathode, on which an organic compound layer and an anode as a transparent electrode are formed in the stated order (hereinafter, referred to as upper surface emission structure). Alternatively, manufactured is an active matrix light emitting device having the light emitting element with a structure in which an electrode on the TFT side electrically connected to the TFT on the substrate is formed as an anode, on which an organic compound layer and a cathode as a transparent electrode are formed in the stated order (hereinafter, also referred to as upper surface emission structure).

[0013] In the above-mentioned respective structures, there arises a problem concerning a higher film resistance of a transparent electrode. In particular, when a film thickness of the transparent electrode is reduced, the film resistance further increases. If the film resistance of the transparent electrode serving as an anode or a cathode is increased, there arises a problem in that a potential distribution in the surface becomes nonuniform due to voltage drop, which involves variations in luminance of the light emitting element. Accordingly, an object of the present invention is to provide a light emitting device having a structure useful in decreasing the film resistance of the transparent electrode of the light emitting element and a manufacturing method therefor and further to provide an electronic device using the above light emitting device as a display portion.

[0014] In addition, another object of the present invention is to increase reliability in the light emitting element and the light emitting device.

[0015] According to the present invention, in manufacturing the light emitting element formed over the substrate, a conductive film is formed on an insulator arranged between pixel electrodes prior to formation of an organic compound layer for the purpose of suppressing the film resistance of the transparent electrode.

[0016] Further, the present invention is characterized in that a lead wiring is formed using the above conductive film to achieve connection with other wirings on a lower layer as well.

[0017] According to a structure of the invention disclosed in this specification, there is provided a light emitting device, including:

a pixel portion having a plurality of light emitting elements each including: a first electrode; an organic compound layer formed on the first electrode in contact therewith; and a second electrode formed on the organic compound layer in contact therewith;
a driver circuit; and
a terminal portion,

the device being characterized in that:

in the pixel portion, end portions of the first electrode connected to a thin film transistor are covered with an insulator, a third electrode made of a conductive material is formed on the insulator, the organic compound layer is formed on the insulator and the first electrode, and the second electrode is formed on the organic compound layer and the third electrode in contact therewith; and
a portion where a wiring made of a material identical to that of the third electrode or that of the second electrode is connected with a wiring extended from a terminal is formed between the terminal portion and the pixel portion.

[0018] In the above-mentioned structure, the third electrode may have a pattern shape identical to that of the insulator. In this case, it is formed using a mask identical to that of the insulator.

[0019] Alternatively, in the above-mentioned structure, the third electrode may have a pattern shape different from that of the insulator. In this case, after patterning the insulator, a film made of a conductive material is formed to form the third electrode using a mask different from that used for patterning the insulator.

[0020] Also, according to another structure of the present invention, in manufacturing a light emitting element formed over a substrate, a conductive film is formed on an insulator arranged between pixel electrodes prior to formation of the organic compound layer, and after the organic compound layer and a transparent electrode are formed, an electrode made of a material high in conductivity is formed on the transparent electrode to realize low film resistance of the transparent electrode. Note that, the electrode formed on the transparent electrode is not formed in a portion serving as a light emitting region. Further, the present invention is also characterized in that a lead wiring is formed using the conductive film to achieve connection with other wirings formed on a lower layer.

[0021] According to another structure of the invention disclosed in this specification, there is provided the light emitting device, including:

a pixel portion having a plurality of light emitting elements each including: a first electrode; an organic compound layer formed on the first electrode in contact therewith; and a second electrode formed on the organic compound layer in contact therewith;
a driver circuit; and
a terminal portion,

the device being characterized in that:

in the pixel portion, end portions of the first electrode connected to a thin film transistor are covered with an insulator, the organic compound layer is formed on a part of the insulator and the first electrode, the second electrode is formed on the organic compound layer in contact therewith, and a third elec-

trode made of a conductive material is formed on a region of the second electrode which is not overlapped with the first electrode in contact therewith; and

a portion where a wiring made of a material identical to that of the third electrode or that of the second electrode is connected with a wiring extended from a terminal is formed between the terminal portion and the pixel portion.

[0022] Also, in the above-mentioned structures, the light emitting device is characterized in that the second electrode is a cathode or an anode of the light emitting element.

[0023] Also, in the above-mentioned structures, the light emitting device is characterized in that the third electrode is made of a material having electric resistance lower than that constituting the second electrode and is made of poly-Si doped with an impurity element imparting a conductivity type, an element selected from the group consisting of W, WSi_x, Al, Ti, Mo, Cu, Ta, Cr, and Mo, a film mainly containing an alloy material or a compound material mainly containing the element, or a laminate film thereof. For example, it is preferable that the third electrode is an electrode made of a laminate having a nitride layer or a fluoride layer as an uppermost layer.

[0024] Also, in the above-mentioned structures, the light emitting device is characterized in that the first electrode is a cathode or an anode of the light emitting element. For example, when the second electrode is a cathode, the first electrode serves as an anode, whereas when the second electrode is an anode, the first electrode serves as a cathode.

[0025] Also, in the above-mentioned structures, the light emitting device is characterized in that the insulator is a barrier (also referred to as bank) made of organic resin covered with an inorganic insulating film or is an inorganic insulating film. Note that, the light emitting device is characterized in that the inorganic insulating film is an insulating film mainly containing silicon nitride with a film thickness of 10 to 100 nm.

[0026] Also in the light emitting device, there is a problem in that in a pixel emitting no light, an incident outside light (light outside the light emitting device) is reflected by the rear surface of the cathode (surface brought into contact with an light emitting layer) which acts as mirror and outside scenes are reflected in an observation surface (surface facing an observer side). In order to avoid the problem, the following is devised such that a circular polarization film is attached to the observation surface of the light emitting device to prevent the observation surface from reflecting the outside scenes. However, there arises a problem in that the circular polarization film is extremely expensive, which involves an increase in manufacturing cost.

[0027] Another object of the present invention is to prevent the light emitting device from acting as mirror without using the circular polarization film to accordingly provide an inexpensive light emitting device which attains low manufacturing cost thereof. Accordingly, the present invention is characterized by using an inexpensive color filter instead of using the circular polarization film. In the above-mentioned structure, it is preferable to provide a color filter corresponding to each pixel in the light emitting device in order to increase color purity. Also, a black portion (black organic resin) of the color filter may be arranged so as to overlap each portion between light emitting regions. Further, the black portion (black colored layer) of the color filter may be also arranged so as to overlap a portion where different organic compound layers are partially overlapped with each other.

[0028] Note that, the color filter is provided in an emission direction of an emitted light, i.e., provided between the light emitting element and the observer. For example, when the light is not allowed to pass through the substrate having formed the light emitting element thereon, the color filter may be attached to the sealing substrate. Alternatively, when the light is allowed to pass through the substrate having formed the light emitting element thereon, the color filter may be attached thereto. Thus, it is possible to dispense with the circular polarization film.

[0029] In addition, it is extremely effective that as an anode on a layer containing an organic compound, a transparent conductive film (typically, ITO or ZnO) is used, on which a protective film made of an inorganic insulating film is formed. The following is also effective: as a cathode containing an organic compound, a metal thin film (with a film thickness allowing a light to pass the film) made of Al, Ag, and Mg, or an alloy thereof (typically, AlLi) is used, on which the protective film made of the inorganic insulating film is formed.

[0030] Also, before the protective film made of the inorganic insulating film is formed, it is preferable that a film containing hydrogen, typically a thin film mainly containing carbon, or a silicon nitride film is formed by a plasma CVD method or a sputtering method. Also, the film containing hydrogen may be a laminate film consisting of the thin film mainly containing carbon and the silicon nitride film.

[0031] Further, according to another structure of the present invention, there is provided the light emitting device including a light emitting element over a substrate having an insulating surface, the light emitting element including an anode, a cathode, and an organic compound layer interposed between the anode and the cathode, characterized in that the light emitting element is covered with a film containing hydrogen.

[0032] If heat treatment is performed within a range of temperature to which the organic compound layer can be resistant and heat generated when the light emitting element emits the light is utilized, hydrogen can be diffused from the film containing hydrogen to terminate defects in the organic compound layer with hydrogen (ter-

mination). By terminating the defects in the organic compound layer with hydrogen, the light emitting device can be increased in its reliability. Also, when the film containing hydrogen is formed, hydrogen turned into a plasma can be used to terminate defects in the organic compound layer with hydrogen. The protective film formed so as to cover the film containing hydrogen also functions to block hydrogen diffused toward the protective film side and to efficiently diffuse hydrogen into the organic compound layer to terminate defects in the organic compound layer with hydrogen. Further, the film containing hydrogen can serve as the protective film for the light emitting element.

[0033] Further, the film containing hydrogen can serve as a buffer layer. When the silicon nitride film is formed in contact with the transparent conductive film by a sputtering method, there is a possibility that impurities (In, Sn, Zn, etc.) contained in the transparent conductive film are mixed into the silicon nitride film. However, by forming the film containing hydrogen as a buffer layer therebetween, it is also possible to prevent mixture of the impurities into the silicon nitride film. According to the above structure, the buffer layer is formed, so that the impurities (In, Sn, etc.) can be prevented from mixing therein from the transparent conductive film and a superior protective film having no impurities can be formed.

[0034] According to another structure of the present invention, there is provided the light emitting device including a light emitting element over a substrate having an insulating surface, the light emitting element including an anode, a cathode, and an organic compound layer interposed between the anode and the cathode, characterized in that the light emitting element is covered with a film containing hydrogen which is covered with a protective film made of an inorganic insulating film.

[0035] Also, a manufacturing method capable of realizing the above-mentioned structure is included in the present invention. According to a structure relating to a manufacturing method of the present invention, there is provided a manufacturing method for a light emitting device, characterized by including:

forming a TFT on an insulating surface;
forming a cathode electrically connected to the TFT;
forming an organic compound layer on the cathode; and
forming an anode on the organic compound layer and then forming a film containing hydrogen on the anode.

[0036] Also, according to another structure relating to the manufacturing method of the present invention, there is provided the manufacturing method for a light emitting device, characterized by including:

forming a TFT on an insulating surface;
forming an anode electrically connected to the TFT;
forming an organic compound layer on the anode; and
forming a cathode on the organic compound layer and then forming a film containing hydrogen on the cathode.

[0037] In the above-mentioned structures relating to the manufacturing method of the present invention, the method is characterized in that the film containing hydrogen is formed by a plasma CVD method or a sputtering method within a range of temperature to which the organic compound layer can be resistant, for example, a range from room temperature to 100°C or less and that the film containing hydrogen is a thin film mainly containing carbon or a silicon nitride film.

[0038] In the above-mentioned structures relating to the manufacturing method of the present invention, the method is characterized in that a step of forming the organic compound layer is performed by an evaporation method, a coating method, an ion plating method, or an ink jet method.

[0039] In the above-mentioned structures relating to the manufacturing method of the present invention, the method is characterized in that a protective film made of an inorganic insulating film is formed on the film containing hydrogen.

[0040] In the above-mentioned structures relating to the manufacturing method of the present invention, the method is characterized in that when the film containing hydrogen is formed, a defect in the organic compound layer is terminated with hydrogen.

[0041] Also, in order to prevent deterioration due to moisture or oxygen, when the light emitting element is sealed with a sealing can or a sealing substrate, a space to be sealed may be filled with a hydrogen gas or with hydrogen and inert gas (rare gas or nitrogen).

[0042] According to another structure of the present invention, there is provided the light emitting device including a light emitting element over a substrate having an insulating surface, the light emitting element including an anode, a cathode, and an organic compound layer interposed between the anode and the cathode, characterized in that the light emitting element is sealed with a substrate having a light-transmissive property and a sealing member, and a sealed space contains hydrogen.

[0043] In the above-mentioned structure, the light emitting device is characterized in that the light emitting element is covered with the film containing hydrogen (thin film mainly containing carbon or silicon nitride film).

[0044] Also, with the above-mentioned structure, heat treatment is performed within a range of temperature to which the organic compound layer can be resistant and heat generated when the light emitting element emits the light is utilized, so that hydrogen can be diffused from the space containing hydrogen to terminate defects in the organic compound layer with hydrogen. By terminating defects in the organic compound layer with hydro-

gen, the light emitting device can be increased in its reliability.

[0045] Note that, in this specification, all the layers provided between the cathode and the anode are collectively referred to as an EL layer. Thus, the above-mentioned hole injection layer, hole transportation layer, light emitting layer, electron transportation layer, and electron injection layer are all included in the EL layer.

[0046] The present invention is characterized in that the thin film mainly containing carbon is a DLC (diamond like carbon) film having a thickness of 3 to 50 nm. The DLC film has an SP^3 bond as a bond between carbons in terms of short range order but has an amorphous structure in a macro level. The composition of the DLC film is carbon and hydrogen with the contents of 70 to 95 atoms% and 5 to 30 atoms%, respectively. Thus, the film is extremely hard and superior in an insulating property. Such a DLC film is characterized in that gas permeability with respect to moisture, oxygen, etc. is low. Also, it is known that the film has hardness of 15 to 25 GPa as a result of measurement by a microhardness meter.

[0047] The DLC film can be formed by a plasma CVD method (typically, RF plasma CVD method, microwave CVD method, electron cyclotron resonance (ECR) CVD method, or the like), a sputtering method, or the like. Any film formation method can be adopted to form the DLC film with good adhesiveness. The DLC film is formed with the substrate placed on the cathode. Also, when a negative bias is applied thereto and ion impact is utilized to some degree, a minute and hard film can be formed.

[0048] As a reaction gas used for film formation, a hydrogen gas and a hydrocarbon-based gas (e.g., CH_4, C_2H_2, C_6H_6, or the like) are used, which are ionized due to glow discharge, and ions are accelerated and abutted against a cathode to which a negative self-bias is applied to thereby form the film. Thus, a minute and smooth DLC film can be obtained.

[0049] Also, the DLC film is characterized by including a transparent or semi-transparent insulating film with respect to a visible light.

[0050] Further, in this specification, the term transparent with respect to the visible light means a state in which transmittance of the visible light is 80 to 100% and the term semi-transparent with respect to the visible light means a state in which transmittance of the visible light is 50 to 80%.

BRIEF DESCRIPTION OF THE DRAWINGS

[0051] In the accompanying drawings:

FIGs. 1A to 1C are sectional views in accordance with Embodiment Mode 1 of the present invention;
FIG. 2 is a top view in accordance with Embodiment Mode 1 of the present invention;
FIGs. 3A to 3D each show a terminal portion in accordance with Embodiment Mode 1 of the present invention;
FIGs. 4A and 4B each show a laminate structure in accordance with Embodiment Mode 2 of the present invention;
FIGs. 5A and 5B are top views in accordance with Embodiment Mode 3 of the present invention;
FIGs. 6A to 6C are sectional views in accordance with Embodiment Mode 3 of the present invention;
FIGs. 7A to 7C are top views in accordance with Embodiment Mode 3 of the present invention;
FIGs. 8A to 8C each show a mask in accordance with Embodiment Mode 3 of the present invention;
FIGs. 9A to 9C are sectional views in accordance with Embodiment Mode 4 of the present invention;
FIGs. 10A to 10C are sectional views in accordance with Embodiment Mode 5 of the present invention;
FIG. 11 shows an example of a manufacturing apparatus in accordance with Embodiment 2 of the present invention;
FIG. 12 shows an example of a manufacturing apparatus in accordance with Embodiment 2 of the present invention;
FIGs. 13A to 13F each show an example of an electronic device; and
FIGs. 14A to 14C each show an example of an electronic device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0052] Embodiment modes of the present invention will be described below.

[Embodiment Mode 1]

[0053] FIG. 2 is a top view of an EL module. In the figure, over a substrate (also referred to as TFT substrate) where a number of TFTs are provided, there are formed a pixel portion 40 used for display, driver circuits 41a and 41b for driving pixels of the pixel portion, a connecting portion for connecting an electrode formed on an EL layer and a lead wiring, and a terminal portion 42 to which an FPC is attached for connecting an external circuit therewith. Also, a substrate for sealing an EL element and a sealing member 33 are used to attain a sealed state. FIG. 1A is a sectional view taken along the dashed line A-A' of FIG. 2.

[0054] The pixels are arranged regularly in the direction of the dashed line A-A'. Here, an example of the pixels arranged in the order of R, G, and B in an X direction will be shown.

[0055] In FIG. 1A, a light emitting region (R) indicates a region for emitting a red light; a light emitting region (G), a region for emitting a green light; and a light emitting region (B), a region for emitting a blue light. These light emitting regions of three colors realize a light emitting display device capable of full color display.

[0056] Also, in FIG. 1A, a TFT 1 is an element for con-

trolling a current flowing in an EL layer 17 emitting a red light and reference numerals 4 and 7 denote source or drain electrodes. Further, a TFT 2 is an element for controlling a current flowing in an EL layer 18 emitting a green light and reference numerals 5 and 8 denote source or drain electrodes. A TFT 3 is an element for controlling a current flowing in an EL layer 19 emitting a blue light and reference numerals 6 and 9 denote source or drain electrodes. Reference numerals 15 and 16 denote interlayer insulating films formed of an organic insulating material or an inorganic insulating film material.

[0057] Reference numerals 11 to 13 each denote an anode (or a cathode) of the organic light emitting element and 20 denotes a cathode (or an anode) of the organic light emitting element. In this example, the cathode 20 is made of a laminate film consisting of a thin metal layer (typically, an alloy of MgAg, MgIn, AlLi, or the like) and a transparent conductive film (an alloy of an indium oxide and a tin oxide (ITO), an alloy of an indium oxide and a zinc oxide (In_2O_3-ZnO), a zinc oxide (ZnO), and the like), through which light from the respective light emitting elements passes. Note that, the transparent conductive film is provided not to function as a cathode but to decrease the electric resistance. As an anode, the following may be used: a material having a high work function, specifically, platinum (Pt), chromium (Cr), tungsten (W), or a nickel (Ni); a transparent conductive film (ITO, ZnO, or the like); and a laminate thereof.

[0058] Also, organic insulators 24 (also referred to as barrier or bank) cover both ends of the anodes (or cathodes) 11 to 13 and portions therebetween. Further, the organic insulators 24 are covered with inorganic insulating films 14. An organic compound layer is partially formed on each organic insulator 24.

[0059] On the organic insulators 24 (also referred to as barrier or bank) covered with the inorganic insulating films 14, auxiliary electrodes 21 are formed. The auxiliary electrodes 21 function to decrease an electric resistance value of the cathode (or the anode). The above-mentioned transparent conductive film has a relatively high resistance value, so that it is difficult to achieve a large screen. However, by providing the auxiliary electrodes 21, the electrodes serving as a cathode (or an anode) can be reduced in resistance as a whole. In addition, the thickness of the transparent conductive film can be reduced.

[0060] Further, connection with the wiring or the electrode on the lower layer is achieved using the auxiliary electrodes 21. The auxiliary electrodes 21 may be subjected to film formation or patterning before the EL layer is formed. Through a sputtering method, an evaporation method, or the like, the auxiliary electrodes 21 may be formed of poly-Si doped with an impurity element imparting a conductivity type, an element selected from the group consisting of W, WSi_x, Al, Ti, Mo, Cu, Ta, Cr, and Mo, a film mainly containing an alloy material or a compound material mainly containing the element, or a laminate film thereof. Thus, if the transparent conductive film is formed on the auxiliary electrodes 21 in contact therewith which are brought into contact with the electrode on the lower layer, the cathode can be led out. Note that, FIG. 1C is a sectional view taken along the dashed line C-C' of FIG. 2. In FIG. 1C, electrodes connected by the dotted line are electrically connected to each other. Also, in the terminal portion, an electrode of the terminal is formed of the same material as a cathode 10.

[0061] Also, a sealing substrate 30 is bonded thereto using the sealing member 33 so as to maintain an interval of about 10 μm, so that all the light emitting elements are sealed. Here, it is desirable to turn the sealing member 33 into a shape like a frame with a small width so as to partially overlap the driver circuit. Annealing is preferably performed in the vacuum for degassing immediately before the sealing substrate 30 is bonded thereto using the sealing member 33. Also, it is preferable to bond the sealing substrate 30 thereto in an atmosphere containing hydrogen and an inert gas (rare gas or nitrogen) and to allow the space sealed by a protective film 32, the sealing member 33, and the sealing substrate 30 to contain hydrogen. Heat generated when the light emitting element emits a light is utilized, which makes it possible to diffuse hydrogen from the space containing it to thereby terminate defects in the organic compound layer with hydrogen. By terminating the defects in the organic compound layer with hydrogen; the light emitting device can be increased in its reliability.

[0062] Further, in order to increase color purity, color filters corresponding to the respective pixels are provided on the sealing substrate 30. Among the color filters, a red colored layer 31b is provided opposite to the red light emitting region (R), a green colored layer 31c is provided opposite to the green light emitting region (G), and a blue colored layer 31d is provided opposite to the blue light emitting region (B). Further, regions other than the light emitting regions are light-shielded with black portions of the color filters, i.e., light-shielding portions 31a. Here, the light-shielding portions 31a are formed of a metal film (containing chromium etc.) or an organic film containing a black pigment.

[0063] In the present invention, provision of the color filters makes a circular polarization plate unnecessary.

[0064] Also, FIG. 1B is a sectional view taken along the dashed line B-B' of FIG. 2. Also in FIG. 1B, the inorganic insulating films 14 cover both ends of portions denoted by 11a to 11c and regions therebetween. In this case, although an example in which an EL layer 17 emitting a red light is used in common is shown, the present invention is not particularly limited to the above. It may be also possible to form the EL layer for each pixel emitting the same color.

[0065] Also, in FIGs. 1A to 1C, the protective film 32 is formed so as to increase reliability of the light emitting device, which is an insulating film mainly containing sil-

icon nitride or silicon oxynitride and formed by the sputtering method. Also, in FIGs. 1A to 1C, the protective film is preferably made as thin as possible such that an emitted light passes therethrough.

[0066] Further, the protective film 32 is formed after a film containing hydrogen is formed in order to increase reliability of the light emitting device. By forming the film containing hydrogen prior to the formation of the protective film 32, the defects in the organic compound layers 17 to 19 are terminated. The film containing hydrogen may be a thin film mainly containing carbon or a silicon nitride film. As for a method of forming the film containing hydrogen, the film is formed by a plasma CVD method or a sputtering method within a range of temperature to which the organic compound layer can be resistant, for example, a range from room temperature to 100°C or less. Note that, in FIGs. 1A to 1C, the film containing hydrogen is assumed to partially constitute the protective film and thus is omitted in the figure. Also, the film containing hydrogen may be used as a buffer layer for relaxing a film stress of the protective film 32.

[0067] Needless to say, the present invention is not limited to the structure of FIG. 1C. An example of a structure partially different from the one of FIG. 1C is shown in FIGs. 3A to 3D. Here, in FIGs. 3A to 3D, components identical to those of FIGs. 1A to 1C are denoted by identical symbols for simplicity.

[0068] FIG. 1C shows an example in which the electrode formed of the same material as the cathode (transparent electrode) is provided in the terminal portion. However, FIG. 3A shows an example in which an electrode formed of the same material as a gate electrode of the TFT (a W film as an upper layer and a TaN film as a lower layer) is used to achieve connection with an FPC.

[0069] Also, FIG. 3B shows an example in which an electrode 10 made of the same material as a pixel electrode (anode) is used to achieve connection with the FPC. In this example, the electrode 10 is formed on the electrode made of the same material as the gate electrode of the TFT (a W film as an upper layer and a TaN film as a lower layer) in contact therewith.

[0070] FIG. 3C shows an example in which an electrode for achieving connection with the FPC is an electrode formed of the same material as the cathode 20 (transparent electrode) formed on the electrode 10 made of the same material as the pixel electrode (anode) formed on the lead wiring (wiring in which a TiN film, an Al film, and a TiN film are laminated in the stated order) of the TFT.

[0071] FIG. 3D shows an example in which an electrode for achieving connection with the FPC is an electrode made of the same material as the cathode 20 (transparent electrode) formed on the lead wiring (wiring in which a TiN film, an Al film, and a TiN film are laminated in the stated order) of the TFT.

[Embodiment Mode 2]

[0072] Here, the film containing hydrogen and the protective film will be described with reference to FIGs. 4A and 4B.

[0073] FIG. 4A is a schematic diagram showing an example of a laminate structure of the EL element. In FIG. 4A, reference numeral 200 denotes a cathode (or an anode); 201, an EL layer; 202, an anode (or a cathode); 203, a DLC film containing hydrogen; and 204, a protective film. When the emitted light is caused to pass through the anode 202, a conductive film having a light-transmissive property (ITO, ZnO, etc.) is preferably used as the anode 202. Also, as the cathode 200, a metal film (an alloy film of MgAg, MgIn, AlLi, etc. or a film formed by coevaporation of aluminum and an element belonging to Group 1 or 2 in the periodic table) or a laminate thereof is preferably used.

[0074] The protective film 204 may be made of an insulating film mainly containing silicon nitride or silicon oxynitride which is obtained by a sputtering method (DC system or RF system). The silicon nitride film may be obtained by using a silicon target through the formation in an atmosphere containing nitrogen and argon. Also, a silicon nitride target can be used. The protective film 204 may be also formed by a film formation apparatus using a remote plasma. Further, when the emitted light is caused to pass through the protective film, it is preferable that the protective film is made as thin as possible.

[0075] The DLC film 203 containing hydrogen contains carbon and hydrogen with the contents of 70 to 95 atoms% and 5 to 30 atoms%, respectively and thus is extremely hard and superior in an insulating property. The DLC film containing hydrogen may be formed by a plasma CVD method (typically, RF plasma CVD method, microwave CVD method, electron cyclotron resonance (ECR) CVD method, or the like), a sputtering method, or the like.

[0076] As a method of forming the DLC film 203 containing hydrogen, the film is formed within a range of temperature to which the organic compound layer can be resistant, for example, a range from room temperature to 100°C or less.

[0077] As a reaction gas used for the film formation when the plasma is generated, a hydrogen gas and a hydrocarbon-based gas (e.g., CH_4, C_2H_2, C6H6, or the like) may be used.

[0078] Heat treatment is performed within a range of temperature to which the organic compound layer can be resistant and heat generated when the light emitting element emits the light is utilized, so that hydrogen can be diffused from the DLC film containing hydrogen to terminate defects in the organic compound layer with hydrogen (termination). By terminating the defects in the organic compound layer with hydrogen, the light emitting device can be increased in its reliability. Also, when the DLC film containing hydrogen is formed, hydrogen

turned into a plasma can be used to terminate defects in the organic compound layer with hydrogen. In addition, the protective film formed so as to cover the DLC film containing hydrogen functions to block hydrogen diffused toward the protective film side and to efficiently diffuse hydrogen into the organic compound layer to thereby terminate defects in the organic compound layer with hydrogen as well. Note that, the DLC film containing hydrogen can serve as the protective film for the light emitting element.

[0079] Further, the DLC film containing hydrogen can also serve as a buffer layer. When the silicon nitride film is formed in contact with the film made of the transparent conductive film by a sputtering method, there is a possibility that impurities (In, Sn, Zn, etc.) contained in the transparent conductive film are mixed into the silicon nitride film. However, by forming the DLC film containing hydrogen as a buffer layer therebetween, it is also possible to prevent mixture of the impurities into the silicon nitride film. According to the above structure, the buffer layer is formed, so that the impurities (In, Sn, etc.) can be prevented from mixing therein from the transparent conductive film and a superior protective film having no impurities can be formed.

[0080] With such a structure, it is possible to improve reliability as well as to protect the light emitting element.

[0081] Also, FIG. 4B is a schematic diagram showing another example of the laminate structure of the EL element. In FIG. 4B, reference numeral 300 denotes a cathode (or an anode); 301, an EL layer; 302, an anode (or a cathode); 303, a silicon nitride film containing hydrogen; and 304, a protective film. When the emitted light is caused to pass through the anode 302, it is preferable to form the anode 302 using a conductive material having a light-transmissive property, an extremely thin metal film (MgAg), or a laminate thereof.

[0082] Also, when the emitted light is caused to pass through the anode 302, as the anode 302, a conductive film (ITO, ZnO, etc.) having a light-transmissive property is preferably used. Further, as the cathode 300, a metal film (an alloy film of MgAg, MgIn, AlLi, etc. or a film formed by coevaporation of aluminum and an element belonging to Group 1 or 2 in the periodic table) or a laminate thereof is preferably used.

[0083] The protective film 304 may be made of an insulating film mainly containing silicon nitride or silicon oxynitride which is obtained by a sputtering method (DC system or RF system). The silicon nitride film may be obtained by using a silicon target through the formation in an atmosphere containing nitrogen and argon. Also, a silicon nitride target can be used. The protective film 304 may be also formed by a film formation apparatus using a remote plasma. Further, when the emitted light is caused to pass through the protective film, it is preferable that the protective film is made as thin as possible.

[0084] The silicon nitride film 303 containing hydrogen may be formed by a plasma CVD method (typically, RF plasma CVD method, microwave CVD method, electron cyclotron resonance (ECR) CVD method, or the like), an RF sputtering method, a DC sputtering method, or the like.

[0085] As a method of forming the silicon nitride film 303 containing hydrogen, the film is formed within a range of temperature to which the organic compound layer can be resistant, for example, a range from room temperature to 100°C or less.

[0086] When the plasma CVD method is used as the forming method for the silicon nitride film 303 containing hydrogen, as a reaction gas, a gas containing nitrogen (nitrogen oxide-based gas represented by N_2 and NH_3NO_x or the like) and a hydrogen silicide-based gas (e.g., silane (SiH_4), disilane, trisilane, etc.) may be used.

[0087] When the sputtering method is used as the forming method for the silicon nitride film 303 containing hydrogen, a silicon nitride film containing hydrogen may be obtained by using a silicon target through the formation in an atmosphere containing hydrogen, nitrogen, and argon. Also, a silicon nitride target may be used.

[0088] Heat treatment is performed within a range of temperature to which the organic compound layer can be resistant and heat generated when the light emitting element emits the light is utilized, so that hydrogen can be diffused from the silicon nitride film containing hydrogen to terminate defects in the organic compound layer with hydrogen (termination). By terminating the defects in the organic compound layer with hydrogen, the light emitting device is increased in its reliability. Also, when the silicon nitride film containing hydrogen is formed, hydrogen turned into a plasma can be used to terminate the defects in the organic compound layer with hydrogen. In addition, the protective film formed so as to cover the silicon nitride film containing hydrogen functions to block hydrogen diffused toward the protective film side and to efficiently diffuse hydrogen into the organic compound layer to thereby terminate defects in the organic compound layer with hydrogen as well. Note that, the silicon nitride film containing hydrogen can also serve as the protective film for the light emitting element.

[0089] Further, the silicon nitride film containing hydrogen can serve as a buffer layer as well. When the silicon nitride film is formed in contact with the film made of the transparent conductive film by a sputtering method, there is a possibility that impurities (In, Sn, Zn, etc.) contained in the transparent conductive film are mixed into the silicon nitride film. However, by forming the silicon nitride film containing hydrogen as a buffer layer therebetween, it is also possible to prevent mixture of the impurities into the silicon nitride film. According to the above structure, the buffer layer is formed, so that the impurities (In, Sn, etc.) can be prevented from mixing therein from the transparent conductive film and a superior protective film having no impurities can be formed.

[0090] With such a structure, it is possible to improve reliability as well as to protect the light emitting element.

[0091] Also, FIGs. 4A and 4B show an example in which the film containing hydrogen is provided as a single layer, but the film may be a laminate consisting of the silicon nitride film containing hydrogen and the DLC film containing hydrogen or a laminate thereof having three or more layers.

[0092] Further, this embodiment mode can be applied not only to an active matrix display device but also to a passive display device.

[0093] Also, this embodiment mode can be freely combined with Embodiment Mode 1.

[Embodiment Mode 3]

[0094] Here, FIGs. 6A to 6C show an example of a structure partially different from FIGs. 1A to 1C. In this example, among a number of pixels arranged regularly in the pixel portion, pixels in a 3 x 3 matrix are used by way of example and the present invention will be described below. Note that, in a sectional structure, TFTs of FIGs. 6A to 6C are substantially the same as those of FIGs. 1A to 1C and thus components identical to those of FIGs. 1A to 1C are denoted by identical reference numerals for simplicity.

[0095] FIG. 6A is a sectional view taken along the alternate long and short dash line A-A' of FIG. 5A. A light emitting region 50R indicates a red light emitting region; a light emitting region 50G, a green light emitting region; and a light emitting region 50B, a blue light emitting region. These light emitting regions of three colors realize a light emitting display device capable of full color display.

[0096] As shown in FIG. 6A, this embodiment mode employs an example in which patterning is performed using the same mask. Thus, an auxiliary electrode 621 and an organic insulator 624 have substantially the same shape as viewed from the above. In this case, as shown in FIG. 6C, the auxiliary electrode 621 is electrically connected to the wiring made of the same material as a source wiring through the cathode 20.

[0097] Also, the pixel electrode 612 (612a to 612c) is formed on the interlayer insulating film 15 and contact holes of the TFTs are formed after the pixel electrode 612 is formed, through which electrodes 607 and 608 subsequently formed electrically connect the pixel electrode 612 and the TFTs. The inorganic insulating films 14 cover both ends of the pixel electrodes and portions therebetween. Also, similarly to FIGs. 1A to 1C, the organic compound layer is formed so as to partially cover the organic insulator 624.

[0098] FIG. 5B is a top view showing a pixel electrode immediately after its formation, which corresponds to FIG. 5A. In FIGs. 5A and 5B, the organic compound layer is provided for each pixel column (Y direction). The organic insulator 624 in a strip shape is provided between the organic compound layers differing from each other in color of the emitted light in a strip shape. Also, in FIG. 5A, the organic insulator 624 and the auxiliary electrode 621 are provided for each pixel column (Y direction).

[0099] FIG. 7A is a top view corresponding to FIGs. 5A to 6C. In FIG. 7A, the connection portion in the left-hand portion is partially shown in the right-hand portion in section, which corresponds to the portion shown in FIG. 6C. Further, when the auxiliary electrode 621 and the organic insulator of FIG. 7A are subjected to patterning, a metal mask shown in FIG. 8A as an example is used therefor.

[0100] Also, when the film thickness in total of the organic insulator and the auxiliary electrode is relatively large, steps are increased, so that there is a possibility that the transparent conductive film is difficult to use for electrical connection. In particular, in the case where the transparent conductive film is made thin, a line defect may occur due to a poor coverage. Therefore, in order to further ensure connection between the auxiliary electrode 621 and the electrode on the lower layer, as shown in FIG. 7B, the number of masks may be increased to form electrodes denoted by 622. Also, the metal mask may be used to form the electrodes 622 by an evaporation method.

[0101] In addition, as shown in FIG. 7C, a wiring 623 made of the same material as the source wiring is formed in advance so as to surround the pixel portion. Following this, second auxiliary electrodes 624 may be formed so as to intersect the auxiliary electrodes 621 at right angles. With this arrangement, each second auxiliary wiring 624 can be provided so as to directly contact the wiring 623 as well as the auxiliary electrode 621. Here, the auxiliary electrode 621 and the second auxiliary electrode 624 are designed such that a portion therebetween serves as the light emitting region as appropriate. Also, when the second auxiliary electrode 624 of FIG. 7A is subjected to patterning, a metal mask shown in FIG. 8B as an example is used therefor.

[0102] Further, FIG. 7C shows an example in which patterning is performed twice to form the first auxiliary electrode 621 and the second auxiliary electrode 624. However, the auxiliary electrodes may be formed in a lattice shape using the metal mask shown in FIG. 8C. As shown in a right-hand portion of FIG. 8C, openings are divided along the thin line. At the time of evaporation, there is a wrap-around portion, which partially makes a film thin, but the auxiliary electrodes can be formed in a lattice shape.

[0103] Also, this embodiment mode can be freely combined with Embodiment Mode 1 or 2.

[Embodiment Mode 4]

[0104] Here, an example of a structure partially different from FIGs. 1A to 1C is shown in FIGs. 9A to 9C. In this example, among a number of pixels arranged regularly in the pixel portion, pixels in a 3 x 3 matrix are used by way of example and the present invention will be described below. Note that, in a sectional structure,

the structure is substantially the same as those of FIGs. 1A to 1C except that the organic insulator 24 is not provided and an organic compound layer 60 made of a polymer is provided on the entire surface. Thus, in FIGs. 9A to 9C, components identical to those of FIGs. 1A to 1C are denoted by identical reference numerals for simplicity. Also, FIG. 9A is a sectional view taken along the dashed line A-A' of FIG. 2.

[0105] Instead of providing in the structure of FIGs. 9A to 9C the organic insulator 24 shown in FIGs. 1A to 1C, the inorganic insulating films 14 and auxiliary electrodes 721 serve to maintain the intervals among the organic compounds 17, 18, and 19.

[0106] Also, the organic compound layer 60 made of a polymer (typically, poly(ethylene dioxythiophene)/poly (styrene sulfonate) aqueous solution (hereinafter, referred to as "PEDOT/PSS") which serves as a hole injection layer for reference's sake) is formed by a coating method such as a spin coating method or a spray method and thus is formed on the entire surface. Also, the organic compound layer 60 made of a polymer has conductivity, through which electrical connection between the cathode 20 and the auxiliary electrode 721 is achieved. By providing the auxiliary electrode 721, the cathode (or the anode) can be decreased in resistance in its entirety. In addition, the transparent conductive film can be made thin. Further, the auxiliary electrode 721 is used to achieve connection with the wiring or electrode in the lower layer. The auxiliary electrode 721 may be subjected to film formation or patterning before the EL layer is formed. If the transparent conductive film is formed on the auxiliary electrode 721 brought into contact with the electrode in the lower layer, the cathode can be led out. Note that, FIG. 9C is a sectional view taken along the dashed line C-C' of FIG. 2. Further, in FIG. 9C, electrodes connected by the dotted line are electrically connected to each other. In the terminal portion, the electrode of the terminal is formed of the same material as the cathode 20.

[0107] Further, FIG. 9B is a sectional view taken along the dashed line B-B' of FIG. 2. Also in FIG. 9B, the inorganic insulating films 14 cover both ends of portions denoted by 11a to 11c and regions therebetween. In this case, although an example in which an EL layer 17 emitting a red light is used in common is shown, the present invention is not particularly limited to the above. It may be also possible to form the EL layer for each pixel emitting the same color.

[0108] Further, this embodiment mode can be freely combined with one of Embodiment Mode 1 to Embodiment Mode 3.

[Embodiment Mode 5]

[0109] Here, an example of a structure partially different from FIGs. 1A to 1C is shown in FIGs. 10A to 10C. In this example, among a number of pixels arranged regularly in the pixel portion, pixels in a 3 x 3 matrix are used by way of example and the present invention will be described below. Note that, in a sectional structure, the structure is substantially the same as those of FIGs. 1A to 1C except that auxiliary wirings 821 are provided on the cathode 20. Thus, in FIGs. 10A to 10C, components identical to those of FIGs. 1A to 1C are denoted by identical reference numerals for simplicity. Also, FIG. 10A is a sectional view taken along the dashed line A-A' of FIG. 2.

[0110] Also, the auxiliary electrodes 821 are formed on the cathode and thus is formed by an evaporation method using the metal mask. In this case, an example in which the auxiliary electrode 821 is formed in a lattice shape. By providing the auxiliary electrode 821, the cathode (or the anode) can be decreased in resistance in its entirety. In addition, the transparent conductive film can be made thin. Further, the auxiliary electrode 821 is used to achieve connection with the wiring or electrode in the lower layer. If the transparent conductive film is formed on the auxiliary electrode 821 brought into contact with the electrode in the lower layer, the cathode can be led out. Note that, FIG. 10C is a sectional view taken along the dashed line C-C' of FIG. 2. Further, in FIG. 10C, electrodes connected by the dotted line are electrically connected to each other. In the terminal portion, the electrode of the terminal is formed of the same material as the cathode 20.

[0111] Further, this embodiment mode can be freely combined with one of Embodiment Mode 1 to Embodiment Mode 4.

[0112] The present invention thus structured will be further described using the following embodiments in detail.

[Embodiment 1]

[0113] In this embodiment, the active matrix type light emitting device formed on the insulating surface is described. As an active element, a thin film transistor is used (hereinafter referred to as TFT) here, a MOS transistor may also be used.

[0114] A top gate TFT (specifically a planar TFT) is shown as an example, a bottom gate TFT (typically inverse staggered TFT) may also be used.

[0115] In this embodiment, a glass substrate is used, which is made of barium borosilicate glass or aluminoborosilicate glass, a quartz substrate, a silicon substrate, a metal substrate, or stainless substrate forming an insulating film on the surface may be used as a substrate. A plastic substrate having heat resistance enduring a treatment temperature of this embodiment also may be used, and further a flexible substrate may be used.

[0116] Next, a silicon oxynitride film is formed as a lower layer of a base insulating film on a heat-resistant glass substrate with a thickness of 0.7 mm by plasma CVD at a temperature of 400°C using SiH_4, NH_3, and N_2O as material gas (the composition ratio: Si = 32%,

O = 27%, N = 24%, H = 17%). The silicon oxynitride film has a thickness of 50 nm (preferably 10 to 200 nm). The surface of the film is washed with ozone water and then an oxide film on the surface is removed by diluted fluoric acid (diluted down to 1/100). Next, a silicon oxynitride film is formed as an upper layer of the base insulating film by plasma CVD at a temperature of 400°C using SiH_4 and N_2O as material gas (the composition ratio: Si = 32%, O = 59%, N = 7%, H = 2%). The silicon oxynitride film has a thickness of 100 nm (preferably 50 to 200 nm) and is laid on the lower layer to form a laminate. Without exposing the laminate to the air, a semiconductor film having an amorphous structure (here, an amorphous silicon film) is formed on the laminate by plasma CVD at a temperature of 300°C using SiH_4 as material gas. The semiconductor film (an amorphous silicon film is used here) is 54 nm (preferably 25 to 200 nm) in thickness.

[0117] A base insulating film in this embodiment has a two-layer structure. However, the base insulating film may be a single layer or more than two layers of insulating films mainly containing silicon. The material of the semiconductor film is not limited but it is preferable to form the semiconductor film from silicon or a silicon germanium alloy (Si_XGe_{1-X} (X = 0.0001 to 0.02)) by a known method (sputtering, LPCVD, plasma CVD, or the like). Plasma CVD apparatus used may be one that processes wafer by wafer or one that processes in batch. The base insulating film and the semiconductor film may be formed in succession in the same chamber to avoid contact with the air.

[0118] The surface of the semiconductor film having an amorphous structure is washed and then a very thin oxide film, about 2 nm in thickness, is formed on the surface using ozone water. Next, the semiconductor film is doped with a minute amount of impurity element (boron or phosphorus) in order to control the threshold of the TFTs. Here, the amorphous silicon film is doped with boron by ion doping in which diborane (B_2H_6) is excited by plasma without mass separation. The doping conditions include setting the acceleration voltage to 15 kV, the flow rate of gas obtained by diluting diborane to 1% with hydrogen to 30 sccm, and the dose to 2×10^{12} atoms/cm^2.

[0119] Next, a nickel acetate solution containing 10 ppm of nickel by weight is applied by a spinner. Instead of application, nickel may be sprayed onto the entire surface by sputtering.

[0120] The semiconductor film is subjected to heat treatment to crystallize it and obtain a semiconductor film having a crystal structure. The heat treatment is achieved in an electric furnace or by irradiation of intense light. When heat treatment in an electric furnace is employed, the temperature is set to 500 to 650°C and the treatment lasts for 4 to 24 hours. Here, a silicon film having a crystal structure is obtained by heat treatment for crystallization (at 550°C for 4 hours) after heat treatment for dehydrogenation (at 500°C for an hour). Although the semiconductor film is crystallized here by heat treatment using an electric furnace, it may be crystallized by a lamp annealing apparatus capable of achieving crystallization in a short time.

[0121] After an oxide film on the surface of the silicon film having a crystal structure is removed by diluted fluoric acid or the like, a continuous wave solid-state laser and the second to fourth harmonic of the fundamental wave are employed in order to obtain crystals of large grain size when crystallizing an amorphous semiconductor film. Since the laser light irradiation is conducted in the air or in an oxygen atmosphere; an oxide film is formed on the surface as a result. Typically, the second harmonic (532 nm) or third harmonic (355 nm) of a Nd: YVO_4 laser (fundamental wave: 1064 nm) is employed. When using a continuous wave laser, laser light emitted from a 10 W power continuous wave YVO_4 laser is converted into harmonic by a non-linear optical element. Alternatively, the harmonic is obtained by putting a YVO_4 crystal and a non-linear optical element in a resonator. The harmonic is preferably shaped into oblong or elliptical laser light on an irradiation surface by an optical system and then irradiates an irradiation object. The energy density required at this point is about 0.01 to 100 MW /cm^2 (preferably 0.1 to 10 MW /cm^2). During the irradiation, the semiconductor film is moved relative to the laser light at a rate of 10 to 2000 cm/s.

[0122] Of course, although a TFT can be formed by using the silicon film having a crystallizing structure before the second harmonics of the continuous wave YVO_4 laser is irradiated thereon, it is preferable that the silicon film having a crystalline structure after the laser light is irradiated thereon is used to form the TFT since the silicon film irradiated the laser light thereon has an improved crystallinity and electric characteristics of TFT are improved. For instance, although, when TFT is formed by using the silicon film having a crystalline structure before the laser light is irradiated thereon, a mobility is almost 300 cm^2/Vs, when TFT is formed by using the silicon film having a crystalline structure after the laser light is irradiated thereon, the mobility is extremely improved with about 500 to 600 cm^2/Vs.

[0123] After the crystallization is conducted using nickel as a metal element that promotes crystallization of silicon, the second harmonic of the continuous wave YVO_4 laser is irradiated thereon though, not limited thereof, after the silicon film is formed having an amorphous structure and the heat treatment is performed for dehydrogenation, and the silicon film having a crystalline structure may be obtained by the second harmonics of the continuous wave YVO_4 laser may be irradiated.

[0124] The pulse wave laser may be used for as a substitute of the continuous wave laser. In the case that the excimer laser of the pulse wave is used, it is preferable that the frequency is set to 300 Hz, and the laser density is set from 100 to 1000 mJ/cm^2 (typically 200 to 800 mJ/cm^2). Here, the laser light may be overlapped 50 to 98 %.

[0125] In addition to the oxide film formed by laser light irradiation, the surface is treated with ozone water

for 120 seconds to form as a barrier layer an oxide film having a thickness of 1 to 5 nm in total. The barrier layer here is formed using ozone water but it may be formed by oxidizing the surface of the semiconductor film having a crystal structure through ultraviolet irradiation in an oxygen atmosphere, or formed by oxidizing the surface of the semiconductor film having a crystal structure through oxygen plasma treatment, or by using plasma CVD, sputtering or evaporation to form an about 1 to 10 nm thick oxide film. The oxide film formed by the laser light irradiation may be removed before the barrier layer is formed.

[0126] Next, an amorphous silicon film containing argon is formed on the barrier layer by plasma CVD or sputtering to serve as a gettering site. The thickness of the amorphous silicon film is 50 to 400 nm, here 150 nm. The amorphous silicon film is formed in an argon atmosphere with the film formation pressure to 0.3 Pa by sputtering using the silicon target.

[0127] Thereafter, heat treatment is conducted in an electric furnace at 650°C for 3 minutes for gettering to reduce the nickel concentration in the semiconductor film having a crystal structure. Lamp annealing apparatus may be used instead of an electric furnace.

[0128] Using the barrier layer as an etching stopper, the gettering site, namely, the amorphous silicon film containing argon, is selectively removed. Then, the barrier layer is selectively removed by diluted fluoric acid. Nickel tends to move toward a region having high oxygen concentration during gettering, and therefore it is desirable to remove the barrier layer that is an oxide film after gettering.

[0129] Next, a thin oxide film is formed on the surface of the obtained silicon film containing a crystal structure (also referred to as a polysilicon film) using ozone water. A resist mask is then formed and the silicon film is etched to form island-like semiconductor layers separated from one another and having desired shapes. After the semiconductor layers are formed, the resist mask is removed.

[0130] The oxide film is removed by an etchant containing fluoric acid, and at the same time, the surface of the silicon film is washed. Then, an insulating film mainly containing silicon is formed to serve as a gate insulating film. The gate insulating film here is a silicon oxynitride film (composition ratio: Si = 32%, O = 59%, N = 7%, H = 2%) formed by plasma CVD to have a thickness of 115 nm.

[0131] Next, a laminate of a first conductive film with a thickness of 20 to 100 nm and a second conductive film with a thickness of 100 to 400 nm is formed on the gate insulating film. In this embodiment, a tantalum nitride film with a thickness of 50 nm is formed on the gate insulating film and then a tungsten film with a thickness of 370 nm is laid thereon. The conductive films are patterned by the procedure shown below to form gate electrodes and wirings.

[0132] The conductive materials of the first conductive film and second conductive film are elements selected from the group consisting of Ta, W, Ti, Mo, Al, and Cu, or alloys or compounds mainly containing the above elements. The first conductive film and the second conductive film may be semiconductor films, typically polycrystalline silicon films, doped with phosphorus or other impurity elements or may be Ag-Pd-Cu alloy films. The present invention is not limited to a two-layer structure conductive film. For example, a three-layer structure consisting of a 50 nm thick tungsten film, 500 nm thick aluminum-silicon alloy (Al-Si) film, and 30 nm thick titanium nitride film layered in this order may be employed. When the three-layer structure is employed, tungsten of the first conductive film may be replaced by tungsten nitride, the aluminum-silicon alloy (Al-Si) film of the second conductive film may be replaced by ah aluminum-titanium alloy (Al-Ti) film, and the titanium nitride film of the third conductive film may be replaced by a titanium film. Alternatively, a single-layer conductive film may be used.

[0133] ICP (Inductively Coupled Plasma) etching is preferred for etching of the first conductive film and second conductive film (first etching treatment and second etching treatment). By using ICP etching and adjusting etching conditions (the amount of electric power applied to a coiled electrode, the amount of electric power applied to a substrate side electrode, the temperature of the substrate side electrode, and the like), the films can be etched and tapered as desired. The first etching treatment is conducted after a resist mask is formed. The first etching conditions include applying an RF (13.56 MHz) power of 700 W to a coiled electrode at a pressure of 1 Pa, employing CF_4, Cl_2, and O_2 as etching gas, and setting the gas flow rate ratio thereof to 25/ 25/ 10 (sccm). The substrate side (sample stage) also receives an RF power of 150 W (13.56 MHz) to apply a substantially negative self-bias voltage. The area (size) of the substrate side electrode is 12.5 cm x 12.5 cm and the coiled electrode is a disc 25 cm in diameter (here, a quartz disc on which the coil is provided). The W film is etched under these first etching conditions to taper it around the edges. Thereafter, the first etching conditions are switched to the second etching conditions without removing the resist mask. The second etching conditions include using CF_4 and Cl_2 as etching gas, setting the gas flow rate ratio thereof to 30 / 30 (sccm), and giving an RF (13.56 MHz) power of 500 W to a coiled electrode at a pressure of 1 Pa to generate plasma for etching for about 30 seconds. The substrate side (sample stage) also receives an RF power of 20 W (13.56 MHz) to apply a substantially negative self-bias voltage. Under the second etching conditions where a mixture of CF_4 and Cl_2 is used, the W film and the TaN film are etched to almost the same degree. The first etching conditions and the second etching conditions constitute the first etching treatment.

[0134] Next follows the second etching treatment with the resist mask kept in place. The third etching condi-

tions include using CF_4 and Cl_2 as etching gas, setting the gas flow rate ratio thereof to 30/30 (sccm), and giving an RF (13.56 MHz) power of 500 W to a coiled electrode at a pressure of 1 Pa to generate plasma for etching for 60 seconds. The substrate side (sample stage) also receives an RF power of 20 W (13.56 MHz) to apply a substantially negative self-bias voltage. Then, the third etching conditions are switched to the fourth etching conditions without removing the resist mask. The fourth etching conditions include using CF_4, Cl_2, and O_2 as etching gas, setting the gas flow rate ratio thereof to 20 / 20 / 20 (sccm), and giving an RF (13.56 MHz) power of 500 W to a coiled electrode at a pressure of 1 Pa to generate plasma for etching for about 20 seconds. The substrate side (sample stage) also receives an RF power of 20 W (13.56 MHz) to apply a substantially negative self-bias voltage. The third etching conditions and the fourth etching conditions constitute the second etching treatment. At this stage, gate electrode and wirings having the first conductive layer as the lower layer and the second conductive layer as the upper layer are formed.

[0135] Next, the resist mask is removed for the first doping treatment to dope with the entire surface using the gate electrodes as masks. The first doping treatment employs ion doping or ion implantation. Here, ion doping conditions are that the dose is set to 1.5×10^{14} atoms/cm^2, and the acceleration voltage is set from 60 to 100 keV. As an impurity elements that imparts the n-type conductivity, phosphorus (P) or arsenic (As) is typically used. The first impurity regions (n^{--} region) are formed in a self-aligning manner.

[0136] Masks formed from resist are newly formed. At this moment, since the off current value of the switching TFT is lowered, the masks are formed to overlap the channel formation region of a semiconductor layer forming the switching TFT of the pixel portion, and a portion thereof. The masks are formed to protect the channel formation region of the semiconductor layer forming the p-channel TFT of the driver circuit and the periphery thereof. In addition, the masks are formed to overlap the channel formation region of the semiconductor layer forming the current control TFT of the pixel portion and the periphery thereof.

[0137] An impurity region (n^- region) that overlaps with a portion of the gate electrode is formed by conducting selectively the second doping treatment using the masks from the resist. The second doping treatment is employs ion doping or ion implantation. Here, ion doping is used, the flow rate of gas obtained by diluting phosphine (PH_3) with hydrogen to 5 % is set to 30 sccm, the dose is set to 1.5×10^{14} atoms/cm^2, and the acceleration voltage is set to 90 keV. In this case the masks made from resist and the second conductive layer serve as masks against the impurity element that imparts the n-type conductivity and second impurity regions are formed. The second impurity regions are doped with the impurity element that imparts the n-type conductivity in a concentration range of 1×10^{16} to 1×10^{17} atoms/cm^3. Here, the same concentration range as the second impurity region is referred to as a n^- region.

[0138] Third doping treatment is conducted without removing the resist masks. The third doping treatment employs ion doping or ion implantation. As impurity elements imparts n-type conductivity, phosphorus (P) or arsenic (As) are used typically. Here, ion doping is used, the flow rate of gas obtained by diluting phosphine (PH_3) with hydrogen to 5 % is set to 40 sccm, the dose is set to 2×10^{15} atoms/cm^2, and the acceleration voltage is set to 80 keV. In this case the masks made from resist and the second conductive layer serve as masks against the impurity element that imparts the n-type conductivity and third impurity regions are formed. The third impurity regions are doped with the impurity element that imparts the n-type conductivity in a concentration range of 1×10^{20} to 1×10^{21} atoms/cm^3. Here, the same concentration range as the third impurity region is referred to as a n^+ region.

[0139] After removing the resist mask and the new resist mask is formed, the fourth doping treatment is conducted. The fourth impurity regions and the fifth impurity regions are formed in which impurity elements imparts p-type conductivity are added to the semiconductor layer forming the p-channel TFT by the fourth doping treatment.

[0140] The concentration of the impurity element that imparts the p-type conductivity is set from 1×10^{20} to 1×10^{21} atoms/cm^3 to add to the fourth impurity regions. The fourth impurity regions being region (n^{--} region) are already doped with phosphorus (P) in the previous step but are doped with the impurity element that imparts the p-type conductivity in a concentration 1.5 to 3 times the phosphorus concentration to obtain the p-type conductivity. Here, a region having the same concentration range as the fourth impurity regions is also called a p^+ region.

[0141] The fifth impurity regions are formed in the region overlaps with the taper portion of the second conductive layer. The impurity elements imparts p-type conductivity is added thereto at the concentration range from 1×10^{18} to 1×10^{20} atoms/cm^3. Here, the region having the same concentration range as the fifth impurity regions is also referred to as p^- region.

[0142] Through the above steps, an impurity region having the n-type or p-type conductivity is formed in each semiconductor layer. The conductive layers become the gate electrode of TFT.

[0143] An insulating film is formed to cover almost the entire surface (not shown). In this embodiment, the silicon oxide film having 50 nm in thickness is formed by plasma CVD method. Of course, the insulating film is not limited to a silicon oxide film and a single layer or laminate of other insulating films containing silicon may be used.

[0144] The next step is activation treatment of the impurity elements used to dope the semiconductor layers. The activation step employs rapid thermal annealing

(RTA) using a lamp light source, irradiation of a laser, heat treatment using a furnace, or a combination of these methods.

[0145] In the example shown in this embodiment, the interlayer insulating film is formed after the above-described activation. However, the insulating film may be formed before the activation.

[0146] The first interlayer insulating film made from a silicon nitride film is formed. Then, the semiconductor layers are subjected to heat treatment (at 300 to 550°C for 1 to 12 hours) to hydrogenate the semiconductor layers. This step is for terminating dangling bonds in the semiconductor layers using hydrogen contained in the first interlayer insulating film. The semiconductor layers are hydrogenated irrespective of the presence of the interlayer insulating film that is a silicon oxide film. Other hydrogenation methods employable include plasma hydrogenation (using hydrogen excited by plasma).

[0147] Next, a second interlayer insulating film is formed on the first interlayer insulating film from an organic insulating material. In this embodiment, an acrylic resin film is formed to have a thickness of 1.6 μm by application method.

[0148] Formed next are contact holes reaching the conductive layers that serve as the gate electrodes or gate wirings and contact holes reaching the impurity regions. In this embodiment, etching treatment is conducted several times in succession. Also, in this embodiment, the first interlayer insulating film is used as an etching stopper to etch the second interlayer insulating film, and then the first interlayer insulating film is etched.

[0149] Thereafter, electrodes, specifically, a source wiring, a power supply line, a lead-out electrode, a connection electrode, etc. are formed from Al, Ti, Mo, or W. Here, the electrodes and wirings are obtained by patterning a laminate of a Ti film (100 nm in thickness), an Al film containing silicon (350 nm in thickness), and another Ti film (50 nm in thickness). The source electrode, source wiring, connection electrode, lead-out electrode, power supply line, and the like are thus formed as needed. A lead-out electrode for the contact with a gate wiring covered with an interlayer insulating film is provided at an end of the gate wiring, and other wirings also have at their ends input/output terminal portions having a plurality of electrodes for connecting to external circuits and external power supplies. A driving circuit having a CMOS circuit in which an n-channel TFT and a p-channel TFT are combined complementarily and a pixel portion with a plurality of pixels each having an n-channel TFT or a p-channel TFT are formed in the manner described above.

[0150] Next, the third interlayer insulating film made of inorganic insulating material is formed on the second interlayer insulating film. In this embodiment, the silicon nitride film with a thickness of 200 nm is formed by sputtering.

[0151] Next, a contact hole that reaches the connection electrode that contacts with the drain region of the current control TFT by p-channel type TFT is formed. Next, the pixel electrode is formed with connecting and overlapping the TFT connection electrode. In this embodiment, the materials with a large work function, concretely platinum (Pt), chrome (Cr), tungsten (W), nickel (Ni), because the pixel electrode is made to function as an anode of an organic light emitting element.

[0152] Next, inorganic insulators are formed at both ends to cover the edge of the pixel electrode. Inorganic insulators with covering the edge of pixel electrode are made with the insulating film containing silicon by sputtering and then performed patterning. Instead of insulators, a bank composed of organic materials may be formed.

[0153] Next, a supporting electrode is formed on the inorganic insulators as shown in Embodiment Mode 1.

[0154] Next, EL layer and a cathode of an organic light emitting element are formed on the pixel electrode of which both edges are covered by inorganic insulators. Inc jet method, evaporation method, spin coating method and the like may be used for forming the EL layer.

[0155] An EL layer (a layer for light emission and for moving of carriers to cause light emission) has a light emitting layer and a free combination of electric charge transporting layers and electric charge injection layers. For example, a low molecular weight organic EL material or a high molecular weight organic EL material is used to form an EL layer. An EL layer may be a thin film formed of a light emitting material that emits light by singlet excitation (fluorescence) (a singlet compound) or a thin film formed of a light emitting material that emits light by triplet excitation (phosphorescence) (a triplet compound). Inorganic materials such as silicon carbide may be used for the electric charge transporting layers and electric charge injection layers. Known organic EL materials and inorganic materials can be employed.

[0156] Also, it is assumed as being preferable that as a material for the cathode, metals having a low work function (typically, metal elements belonging to Group 1 or Group 2 in the periodic table) or alloys containing these are used. As the work function becomes lower, the light emission efficiency becomes higher. Thus, in particular, it is desirable that a material with a laminate structure is used as the material for the cathode, which is obtained by depositing an alloy of MgAg, MgIn, AlLi, etc. into a thin film or forming a thin film through coevaporation of aluminum and an element belonging to Group 1 or 2 in the periodic table, and subsequently forming a transparent conductive film (an alloy of an indium oxide and a tin oxide (ITO), an alloy of an indium oxide and a zinc oxide (In_2O_3-ZnO), an zinc oxide (ZnO), and the like).

[0157] Next, the protective film covering the cathode is formed. The protective film may be formed of an insulating film mainly containing silicon nitride or silicon oxynitride by a sputtering method. As shown in Embodiment Mode 2, the defects in the EL layer are terminated with hydrogen (termination) and thus, it is preferable to

form the film containing hydrogen on the cathode.

[0158] The film containing hydrogen may be formed of an insulating film mainly containing carbon or silicon nitride by a PCVD method. At the time of film formation, it is also possible to terminate the defects in the organic compound layer with hydrogen turned into a plasma. Heat treatment is performed within a range of temperature to which the organic compound layer can be resistant and heat generated when the light emitting element emits light is utilized, so that hydrogen can be diffused from the film containing hydrogen to terminate defects in the organic compound layer with hydrogen (termination).

[0159] Also, the film containing hydrogen and the protective film are used to prevent from entering from the outside the substance such as moisture or oxygen which causes deterioration of the EL layer due to oxidation. Note that, in an input/output terminal portion to be connected with the FPC later, there is not required to provide the protective film, the film containing hydrogen, and the like.

[0160] Also, various circuits composed of a plurality of TFTs etc. may be provided to lead to the gate electrode of the TFT arranged in the pixel portion. Needless to say, there is not imposed a particular limitation thereon.

[0161] Next, the organic light emitting element including at least the cathode, the organic compound layer, and the anode is enclosed by the sealing substrate or a sealing can. Thus, the organic light emitting element is preferably blocked from the outside completely to prevent from entering from the outside the substance such as moisture or oxygen which causes deterioration of the EL layer due to oxidation. It is preferable that degassing is performed by annealing in the vacuum immediately before enclosure with the sealing substrate or the sealing can. Also, when the sealing substrate is bonded to the substrate, it is preferable that the procedure is performed in an atmosphere containing hydrogen and inert gas (rare gas or nitrogen) and a space sealed by sealing contains hydrogen. Heat generated when the light emitting element emits a light is utilized, which makes it possible to diffuse hydrogen from the space containing hydrogen to thereby terminate defects in the organic compound layer with hydrogen. By terminating the defects in the organic compound layer with hydrogen, the light emitting device can be increased in its reliability.

[0162] Subsequently, an FPC (flexible printed circuit) is bonded to each electrode in the input/output terminal portion by using an anisotropic conductive member. The anisotropic conductive member consists of resin and conductive particles having a particle size of several tens to several hundreds of μm with its surface plated with Au or the like. The conductive particles serve to electrically connect each electrode of the input/output terminal portion and the wiring formed on the FPC.

[0163] Also, the substrate is provided with the color filters corresponding to the respective pixels and then, provision of the color filters makes a circular polarization plate unnecessary. Further, another optical film may be provided if necessary and an IC chip etc. may be mounted thereon.

[0164] Through the above steps, the modularized light emitting device connected with the FPC is completed.

[0165] Further, this embodiment can be freely combined with one of Embodiment Mode 1 to Embodiment Mode 5.

[Embodiment 2]

[0166] In this embodiment, a manufacturing apparatus will be shown with reference to FIG. 11.

[0167] In FIG. 11, reference symbols 100a to 100k, and 100m to 100v each denote a gate; 101 and 109, a delivery chamber; 102, 104a, 107, 108, 111, and 114, a transportation chamber; 105, 106R, 106B, 106G, 106H, 109, 110, 112, and 113, a film formation chamber; 103, a pretreatment chamber; 117a and 117b, a sealing substrate loading chamber; 115, a dispenser chamber; 116, a sealing chamber; 118a, a ultraviolet irradiating chamber; and 120, a substrate inverting chamber.

[0168] Hereinafter, the substrate previously having formed the TFT thereon is carried in the manufacturing apparatus shown in FIG. 11. Here, a procedure for forming a laminate structure shown in FIG. 4A is explained.

[0169] First, the substrate is set in the delivery chamber 101, on which the TFT and the cathode (or the anode) 200 are formed, and is then transported to the transportation chamber 102 connected to the delivery chamber 101. It is preferable that vacuum-exhausting is conducted on the transportation chamber to attain an atmospheric pressure by introducing the inert gas in advance such that the moisture or oxygen in the transportation chamber is suppressed to as low level as possible.

[0170] Also, the transportation chamber 102 is connected to a vacuum exhausting processing chamber for making the inside of the transportation chamber vacuum. The vacuum exhausting processing chamber is equipped with a magnetic levitation type turbo molecular pump, a cryopump, or a dry pump. With this structure, it is possible that the ultimate vacuum of the transportation chamber is set to 10^{-5} to 10^{-6} Pa and the impurity is controlled so as not to diffuse backward from the pump side or exhausting system. In order to prevent the introduction of the impurity into the inside of the apparatus, as a gas to be introduced, an inert gas such as nitrogen or a rare gas is used. These gases introduced to the inside of the apparatus are required to be highly purified by a gas purifier prior to the introduction into the apparatus when they are used. Accordingly, it is necessary to provide the gas purifier in order to introduce into the film formation apparatus the gas after being highly purified. Thus, the oxygen or moisture contained in the gas and other impurities can be eliminated in advance,

so that it is possible to prevent such impurities from being introduced to the inside of the apparatus.

[0171] Also, in order to eliminate the moisture or other gases contained in the substrate, it is preferable to perform annealing for degassing in the vacuum. Therefore, the substrate is transported to the pretreatment chamber 103 connected to the transportation chamber 102 and annealing may be performed there. Further, when the surface of the cathode is required to be cleaned, the substrate is transported to the pretreatment chamber 103 connected to the transportation chamber 102 and cleaning may be performed there.

[0172] It is also possible to form the poly(ethylene dioxythiophene)/poly(styrene sulfonate) aqueous solution (PEDOT/PSS) serving as a hole injection layer on the entire surface of the anode as needed. In the manufacturing apparatus of FIG. 11, the film formation chamber 105 for forming the organic compound layer made of a polymer is provided. When a spin coating method, an ink jet method, or a spray method is used for the formation thereof, the substrate is set under the atmospheric pressure such that a surface subjected to film formation is faced upward. The substrate is inverted as appropriate in the substrate inverting chamber 120 provided between the film formation chamber 105 and the transportation chamber 102. Also, after the film formation is performed using the aqueous solution, it is preferable to transport the substrate to the pretreatment chamber 103 where moisture is vaporized by performing heat treatment in the vacuum.

[0173] Next, a substrate 104c is transported to the transportation chamber 104 from the transportation chamber 102 without being exposed to the atmosphere and then, transported to the film formation chamber 106R by a transportation mechanism 104b to form on the cathode 200 the EL layer for emitting a red light as appropriate. Here, an example in which it is formed by evaporation is shown. The substrate is set in the film formation chamber 106R after being inverted in the substrate inverting chamber 120 such that the surface subjected to film formation is faced downward. Note that, it is preferable to perform vacuum exhausting on the film formation chamber before the substrate is carried therein.

[0174] For example, in the film formation chamber 106R subjected to vacuum exhausting to 5 x 10^{-3} Torr (0.665 Pa) or less, preferably 10^{-4} to 10^{-6} Pa in degree of vacuum, evaporation is conducted. At the time of evaporation, the organic compounds are vaporized in advance by resistance heating and are scattered toward the substrate when a shutter (not shown) is opened at this time. The vaporized organic compounds are scattered upward and evaporated onto the substrate through the opening (not shown) provided on the metal mask (not shown). Note that, upon the evaporation, a substrate temperature (T_1) is set to 50 to 200°C, preferably 65 to 150°C, using a means for heating the substrate.

[0175] When the three types of EL layers are formed in order to attain a full color display, after being formed in the film formation chamber 106R, they may be formed through film formation in the film formation chambers 106G and 106B in order.

[0176] After the desired EL layer 201 is formed on the cathode (or the anode) 200, the substrate is transported to the transportation chamber 107 from the transportation chamber 104 without being exposed to the air and is subsequently transported to the transportation chamber 108 from the transportation chamber 107 also without being exposed to the air.

[0177] Next, the substrate is transported to the film formation chamber 109 using a transportation mechanism placed in the transportation chamber 108. The anode 202 made of a transparent conductive film (ITO etc.) is formed on the EL layer 201 as appropriate. In the case where the cathode is formed, a thin metal layer serving as a cathode is formed in the film formation chamber 110, the substrate is then transported to the film formation chamber 109 to form a transparent conductive film, and a laminate consisting of the thin metal layer (cathode) and the transparent conductive film is appropriately formed. In this case, the film formation chamber 110 corresponds to an evaporation apparatus including Mg, Ag, or Al used as the cathode as an evaporation source and the film formation chamber 109 corresponds to a sputtering apparatus including at least a target made of a transparent conductive material used as the anode.

[0178] Next, the substrate is transported to the film formation chamber 112 using a transportation mechanism placed in the transportation chamber 108, in which the film 203 containing hydrogen is formed within a range of temperature to which the organic compound layer can be resistant. In this case, the film formation chamber 112 is provided with a plasma CVD apparatus and as a reaction gas used for the film formation, a hydrogen gas and a hydrocarbon-based gas (e.g., CH_4, C_2H_2, C_6H_6, or the like) are used to thereby form the DLC film containing hydrogen. Note that, there is not imposed a particular limitation thereon as long as a means for generating a hydrogen radical is provided therefor. At the time of the film formation of the DLC film containing hydrogen, the defects in the organic compound layer is terminated with hydrogen turned into a plasma.

[0179] Subsequently, the substrate is transported to the film formation chamber 113 from the transportation chamber 108 without being exposed to the air to form the protective film 204 on the film 203 containing hydrogen. Here, the sputtering apparatus is employed in which the target of silicon or silicon nitride is included in the film formation chamber 113. An atmosphere of the film formation chamber is set to a nitrogen atmosphere or an atmosphere containing nitrogen and argon, so that the silicon nitride film can be formed.

[0180] Through the above steps, the laminate structure shown in FIG. 4A, i.e., the light emitting element covered with the protective film and the film containing

hydrogen is formed on the substrate.

[0181] Next, the substrate having formed the light emitting element thereon is transported to the transportation chamber 111 from the transportation chamber 108 without being exposed to the air and further, is transported to the transportation chamber 114 from the transportation chamber 111.

[0182] Following this, the substrate having formed the light emitting element thereon is transported to the sealing chamber 116 from the transportation chamber 114. Here, it is preferable to prepare a sealing substrate provided with a sealing member in the sealing chamber 116.

[0183] The sealing substrate is set in the sealing substrate loading chambers 117a and 117b from the outside. Here, in order to eliminate the impurity such as moisture, it is preferable to perform annealing in advance in the vacuum, for example, in the sealing substrate loading chambers 117a and 117b. When the sealing member is formed on the sealing substrate, after the transportation chamber 108 is set to an atmospheric pressure, the sealing substrate is transported to the dispenser chamber 115 from the sealing substrate loading chamber, the sealing member is formed for bonding it to the substrate on which the light emitting element is formed, and the sealing substrate having formed the sealing member thereon is transported to the sealing chamber 116.

[0184] Next, for degassing the substrate on which the light emitting element is formed, annealing is performed in the vacuum or in the inert gas atmosphere. Then, the sealing substrate having formed the sealing member thereon and the substrate having formed the light emitting element thereon are bonded to each other. Also, a sealed space is filled with hydrogen or inert gas. Note that, in this case, an example is shown in which the sealing member is formed on the sealing substrate, but the present invention is not particularly limited to this and the sealing member may be formed on the substrate having formed the light emitting element thereon.

[0185] Next, a pair of substrates bonded to each other are transported from the transportation chamber 114 to the ultraviolet irradiating chamber 118, where the substrates are irradiated with a ultraviolet light to cure the sealing member. Note that, in this example, ultraviolet curable resin is used for the sealing member, but any sealing member can be used with no particular limitation as long as it is an adhesive.

[0186] Subsequently, the substrates are transported from the transportation chamber 114 to the delivery chamber 119 and are taken out.

[0187] As described above, the manufacturing apparatus shown in FIG. 11 is used, which makes it possible to prevent the light emitting element from being exposed to the outside air until it is completely enclosed in the sealed space. Thus, the light emitting device high in reliability can be manufactured. Note that, the transportation chambers 102 and 114 take repeatedly a vacuum state and a state at atmospheric pressure, whereas the transportation chambers 104a and 108 are always kept vacuum.

[0188] Note that, a film formation apparatus of an in-line system can be employed.

[0189] Further, FIG. 12 shows a manufacturing apparatus partially different from that of FIG. 11.

[0190] FIG. 11 shows an example in which the film formation chamber for forming the film using the spin coating method, ink jet method, or spray method is singly formed, whereas in an example of the manufacturing apparatus of FIG. 12, three film formation chambers for forming the film using the spin coating method, ink jet method, or spray method are formed. For example, when three types of EL layers are formed for achieving a full color display by the spin coating method, ink jet method, or spray method, after the film formation in the film formation chamber 121a, they may be formed sequentially in the respective film formation chambers 121b and 121c.

[0191] Note that, this embodiment can be freely with one of Embodiment Mode 1 to Embodiment Mode 5 and Embodiment 1.

[Embodiment 3]

[0192] The EL modules (active matrix EL module, passive EL module) can be completed by implementing the present invention. Namely, all of the electronic equipments are completed by implementing the present invention.

[0193] Following can be given as such electronic equipments: video cameras; digital cameras; head mounted displays (goggle type displays); car navigation systems; car stereos; personal computers; portable information terminals (mobile computers, cell phones or electronic books etc.) etc. Examples of these are shown in FIG. 13 and FIG. 14.

[0194] FIG. 13A is a personal computer which comprises: a main body 2001; an image input section 2002; a display section 2003; and a keyboard 2004 etc.

[0195] FIG. 13B is a video camera which comprises: a main body 2101; a display section 2102; a voice input section 2103; operation switches 2104; a battery 2105 and an image receiving section 2106 etc.

[0196] FIG. 13C is a mobile computer which comprises: a main body 2201; a camera section 2202; an image receiving section 2203; operation switches 2204 and a display section 2205 etc.

[0197] FIG. 13D is a goggle type display which comprises: a main body 2301; a display section 2302; and an arm section 2303 etc.

[0198] FIG. 13E is a player using a recording medium in which a program is recorded (hereinafter referred to as a recording medium) which comprises: a main body 2401; a display section 2402; a speaker section 2403; a recording medium 2404; and operation switches 2405 etc. This apparatus uses DVD (Digital Versatile Disc),

CD, etc. for the recording medium, and can perform music appreciation, film appreciation, games and use for Internet.

[0199] FIG. 13F is a digital camera which comprises: a main body 2501; a display section 2502; a view finder 2503; operation switches 2504; and an image receiving section (not shown in the figure) etc.

[0200] FIG. 14A is a portable telephone which comprises: a main body 2901; a voice output section 2902; a voice input section 2903; a display section 2904; operation switches 2905; an antenna 2906; and an image input section (CCD, image sensor, etc.) 2907 etc.

[0201] FIG. 14B is a portable book (electronic book) which comprises: a main body 3001; display sections 3002 and 3003; a recording medium 3004; operation switches 3005 and an antenna 3006 etc.

[0202] FIG. 14C is a display which comprises: a main body 3101; a supporting section 3102; and a display section 3103 etc.

[0203] In addition, the display shown in FIG. 14C has small and medium-sized or large-sized screen, for example a size of 5 to 20 inches. Further, to manufacture the display part with such sizes, it is preferable to mass-produce by gang printing by using a substrate with one meter on a side.

[0204] As described above, the applicable range of the present invention is extremely large, and the invention can be applied to electronic equipments of various areas. Note that the electronic devices of this embodiment can be achieved by utilizing any combination of constitutions in Embodiment Modes 1 to 5, Embodiment 1or 2.

[0205] According to the present invention, the defect in the organic compound layer can be terminated with hydrogen, whereby the light emitting device can be increased in its reliability.

[0206] Also, according to the present invention, it is possible to dispense with the circular polarization film extremely expensive, whereby the manufacturing cost can be reduced.

[0207] Also, according to the present invention, it is possible to realize high definition, high opening ratio, and high reliability in the flat panel display capable of full color display using light emission colors of red, green, and blue.

Claims

1. A light emitting device comprising:

   a pixel portion having a plurality of light emitting elements, each including a first electrode electrically connected to a thin film transistor, an organic compound layer formed on the first electrode, and a second electrode formed on the organic compound layer;
   a driver circuit; and
   a terminal portion,

   wherein an end portion of the first electrode is covered with an insulator, a third electrode comprising a conductive material is formed on the insulator, the organic compound layer is formed on the insulator and the first electrode, and the second electrode is formed on the organic compound layer and in contact with the third electrode, and

   wherein a portion where a wiring comprising a same material as the third electrode or the second electrode is connected with a wiring extended from a terminal is formed between the terminal portion and the pixel portion.

2. A light emitting device according to claim 1, wherein the third electrode has a pattern shape identical to that of the insulator.

3. A light emitting device according to claim 1, wherein the third electrode has a pattern shape different from that of the insulator.

4. A light emitting device comprising:

   a pixel portion having a plurality of light emitting elements, each including a first electrode electrically connected to a thin film transistor, an organic compound layer formed on the first electrode, and a second electrode formed on the organic compound layer;
   a driver circuit; and
   a terminal portion,

   wherein an end portion of the first electrode is covered with an insulator, the organic compound layer is formed on the first electrode and a part of the insulator, the second electrode is formed on the organic compound layer, and a third electrode is formed on a region of the second electrode which is not overlapped with the first electrode, and

   wherein a portion where a wiring comprising a same material as the third electrode or the second electrode is connected with a wiring extended from a terminal is formed between the terminal portion and the pixel portion.

5. A light emitting device according to any one of claims 1 and 4, wherein the second electrode is a cathode or an anode of the light emitting element.

6. A light emitting device according to any one of claims 1 and 4, wherein the third electrode comprises at least one selected from the group consisting of poly-Si doped with an impurity element imparting a conductivity type, W, WSi_x, Al, Ti, Mo, Cu, Ta, Cr, and Mo, a film mainly containing an alloy material or a compound material mainly containing thereof,

or a laminate film thereof.

7. A light emitting device according to any one of claims 1 and 4, wherein the first electrode is a cathode or an anode of the light emitting element.

8. A light emitting device according to any one of claims 1 and 4, wherein the insulator is a barrier comprising an organic resin covered with an inorganic insulating film.

9. A light emitting device according to any one of claims 1 and 4, wherein the insulator is an inorganic insulating film.

10. A light emitting device according to any one of claims 1 and 4, wherein the third electrode comprises a laminate having a nitride layer or a fluoride layer as an uppermost layer.

11. A light emitting device according to any one of claims 1 and 4, wherein the inorganic insulating film comprises silicon nitride.

12. A light emitting device according to any one of claims 1 and 4, wherein the light emitting device has a color filter corresponding to each of pixels composed of the light emitting element.

13. A light emitting device comprising:

a light emitting element over a substrate having an insulating surface, the light emitting element including an anode, a cathode, and an organic compound layer interposed between the anode and the cathode,

wherein the light emitting element is covered with a film containing hydrogen.

14. A light emitting device comprising:

a light emitting element over a substrate having an insulating surface, the light emitting element including an anode, a cathode, and an organic compound layer interposed between the anode and the cathode,

wherein the light emitting element is covered with a film containing hydrogen, and

wherein the film containing hydrogen is covered with a protective film comprising an inorganic insulating film.

15. A light emitting device comprising:

a light emitting element over a substrate having an insulating surface, the light emitting element including an anode, a cathode, and an organic compound layer interposed between the anode and the cathode,

wherein the light emitting element is sealed with a substrate having a light-transmissive property and a sealing member, and

wherein a sealed space contains hydrogen.

16. A light emitting device according to claim 15, wherein the light emitting element is covered with the film containing hydrogen.

17. A light emitting device according to any one of claims 13 to 15,

wherein the film containing hydrogen comprises carbon or a silicon nitride film.

18. A light emitting device according to any one of claims 1, 4, and 13 to 15, wherein the light emitting device is incorporated in at least one selected from the group consisting of a personal computer, a video camera, a mobile computer, a goggle type display, a player using a recording medium, a digital camera, a portable telephone, an electronic book, and a car navigation system.

19. A method of manufacturing a light emitting device comprising:

forming a thin film transistor on an insulating surface;
forming a cathode electrically connected to the thin film transistor;
forming an organic compound layer on the cathode;
forming an anode on the organic compound layer; and
forming a film containing hydrogen on the anode.

20. A method of manufacturing a light emitting device comprising:

forming a thin film transistor on an insulating surface;
forming an anode electrically connected to the thin film transistor;
forming an organic compound layer on the anode;
forming a cathode on the organic compound layer; and
forming a film containing hydrogen on the cathode.

21. A method of manufacturing a light emitting device according to any one of claims 19 and 20, wherein the film containing hydrogen is formed by a plasma

CVD method or a sputtering method.

22. A method of manufacturing a light emitting device according to any one of claims 19 and 20, wherein the film containing hydrogen comprises carbon or a silicon nitride film.

23. A method of manufacturing a light emitting device according to any one of claims 19 and 20, wherein a step of forming the organic compound layer is performed by an evaporation method, a coating method, an ion plating method, or an ink jet method.

24. A method of manufacturing a light emitting device according to any one of claims 19 and 20, wherein a protective film comprising an inorganic insulating film is formed on the film containing hydrogen.

25. A method of manufacturing a light emitting device according to any one of claims 19 and 20, wherein a defect in the organic compound layer is terminated with hydrogen when the film containing hydrogen is formed.

26. A method of manufacturing a light emitting device according to any one of claims 19 and 20, wherein the light emitting device is incorporated in at least one selected from the group consisting of a personal computer, a video camera, a mobile computer, a goggle type display, a player using a recording medium, a digital camera, a portable telephone, an electronic book, and a car navigation system.

FIG. 1A sectional view of A-A'

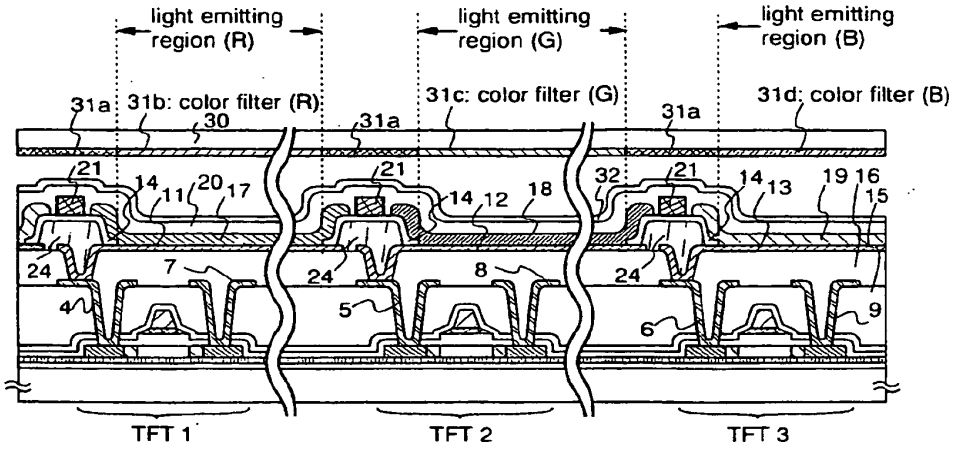


FIG. 1B sectional view of B-B'

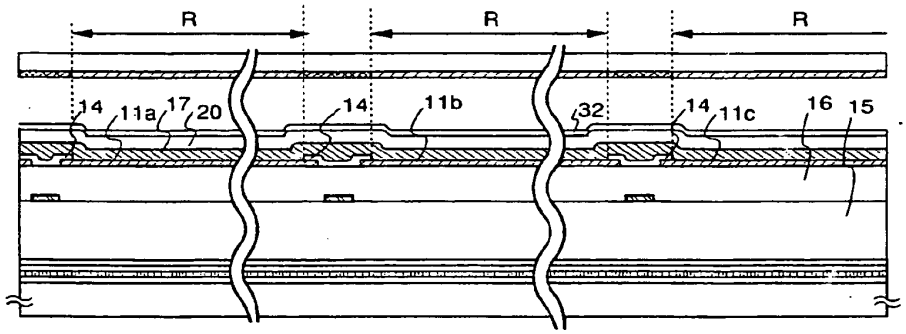


FIG. 1C sectional view of C-C'

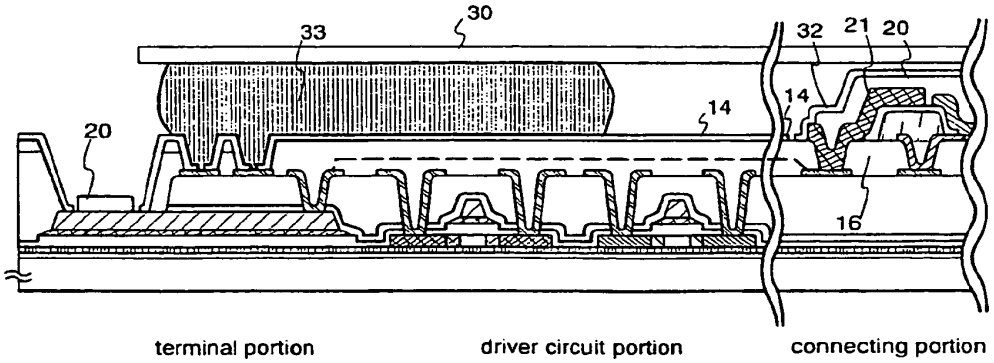


FIG. 2

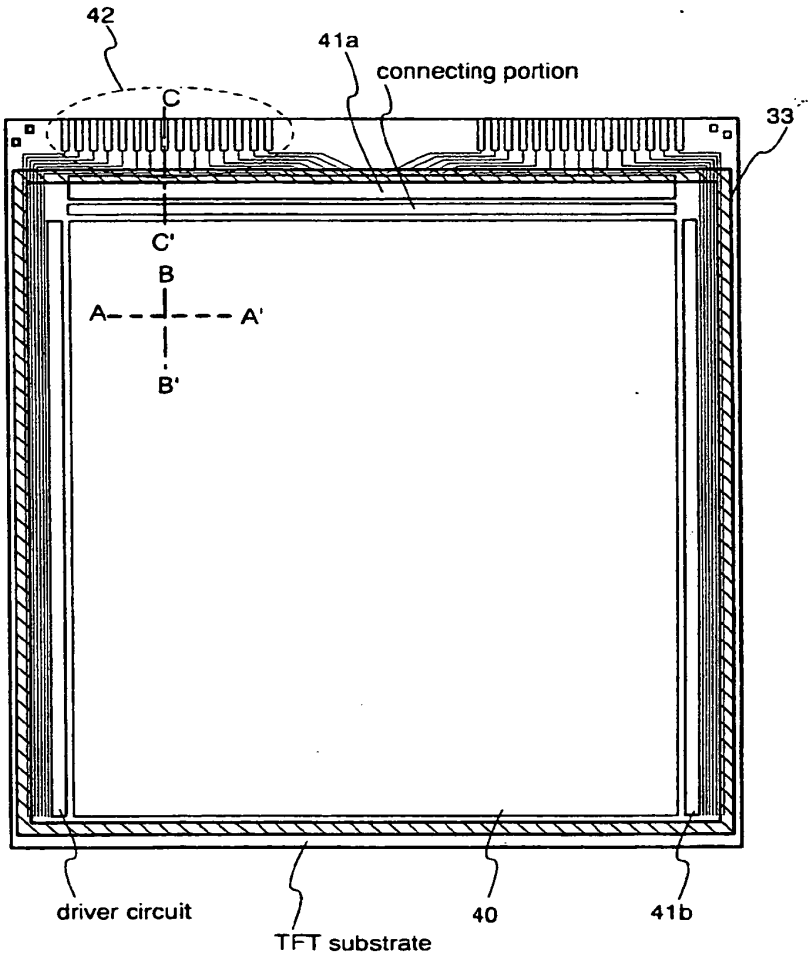


FIG. 3A

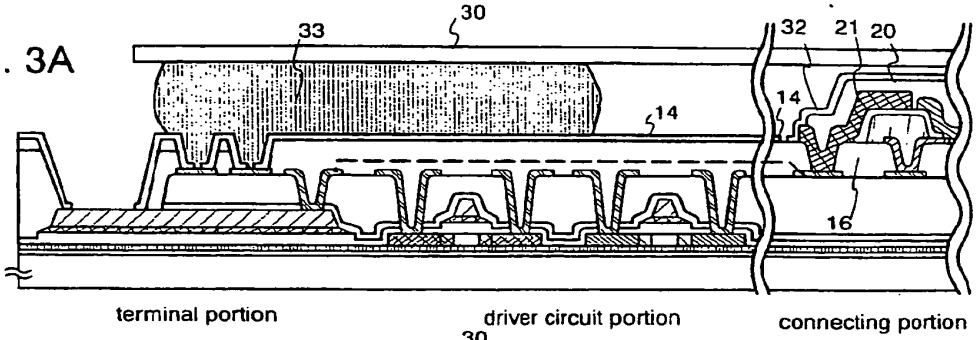


FIG. 3B

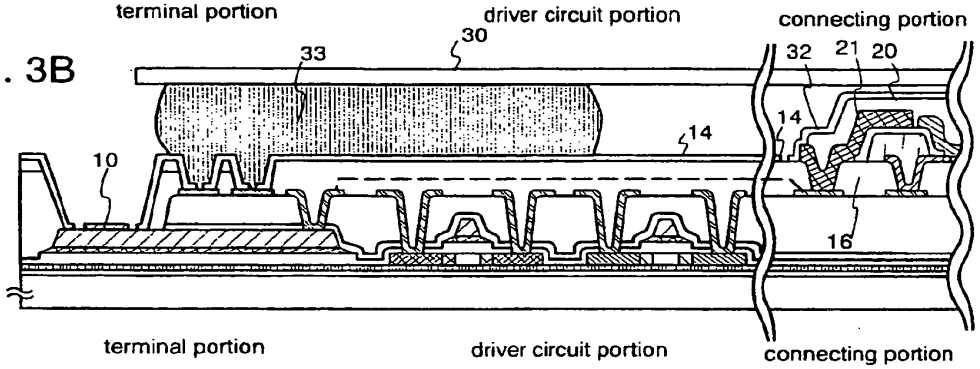


FIG. 3C

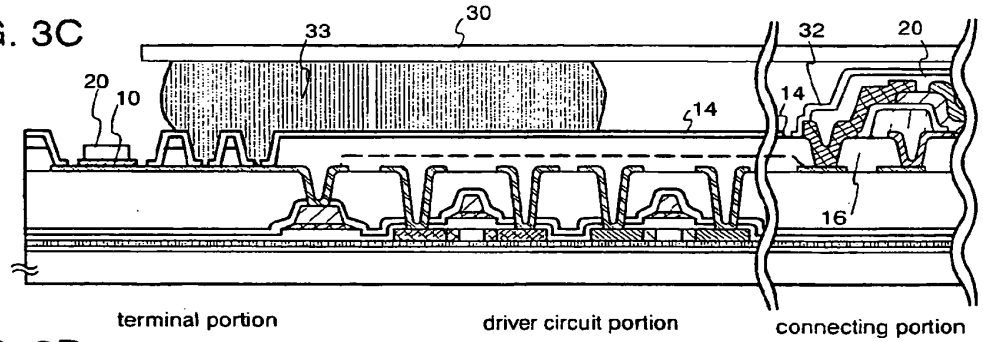


FIG. 3D

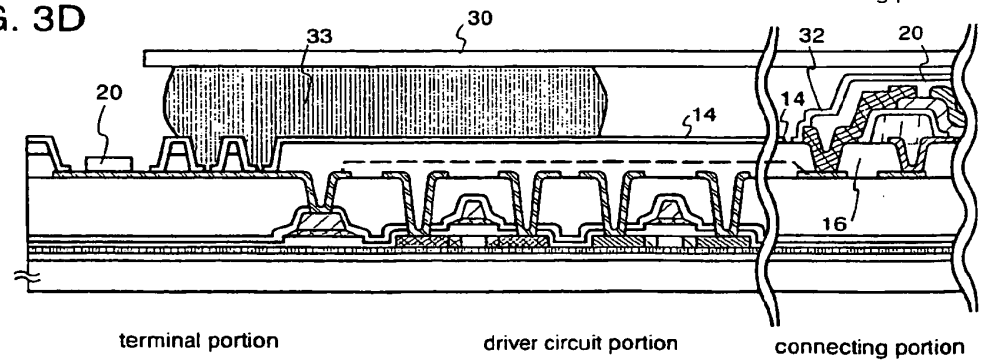


FIG. 4A

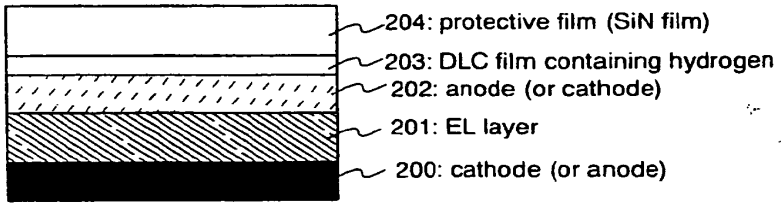


FIG. 4B

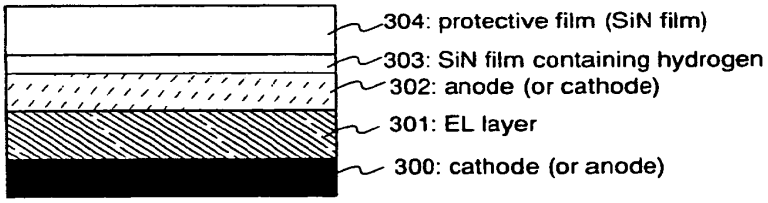


FIG. 5A

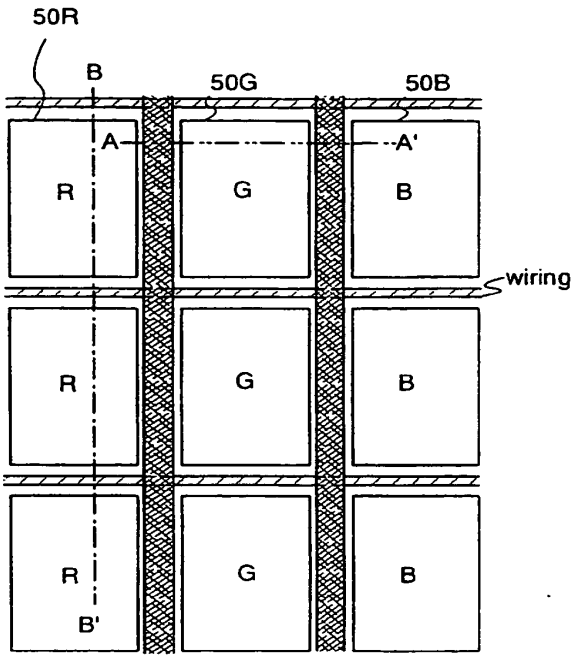


FIG. 5B

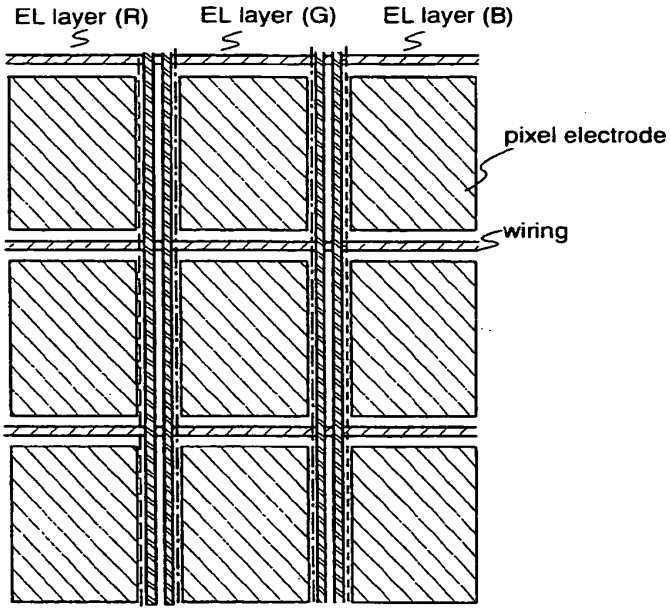


FIG. 6A sectional view of A-A'

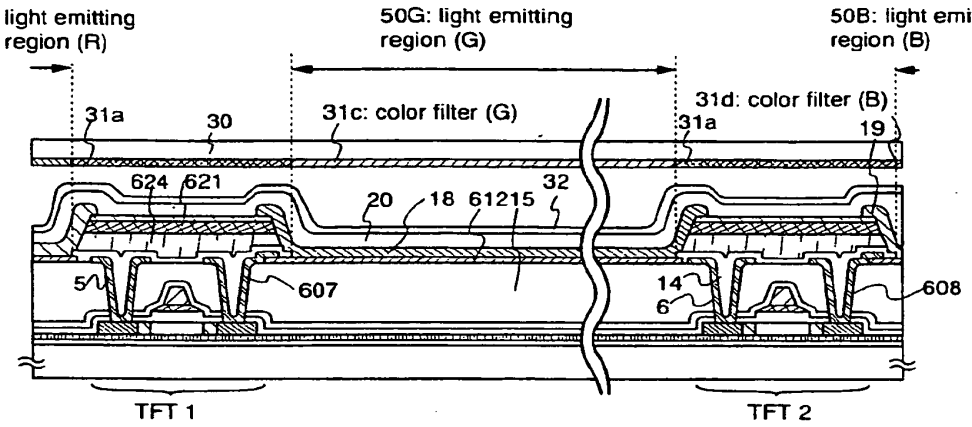


FIG. 6B sectional view of B-B'

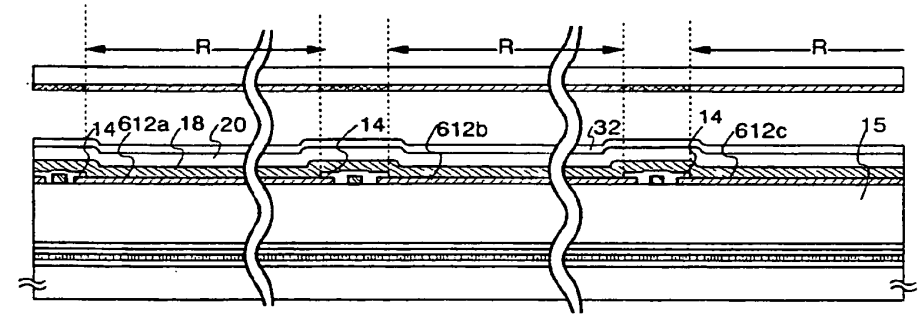


FIG. 6C sectional view of C-C'

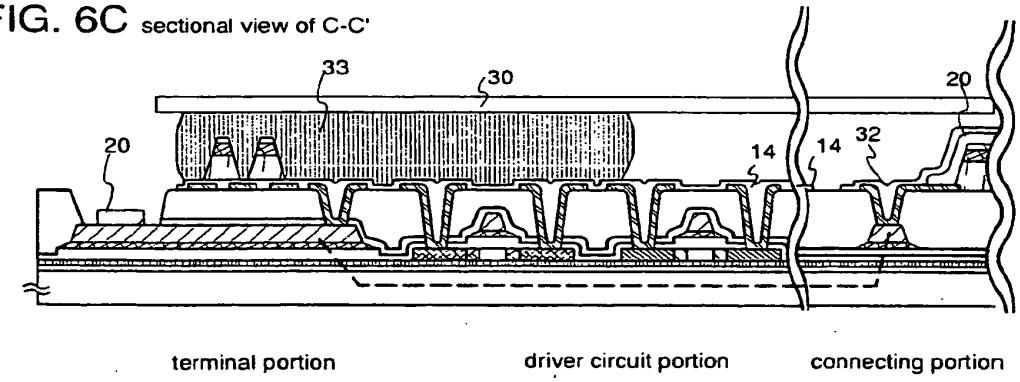
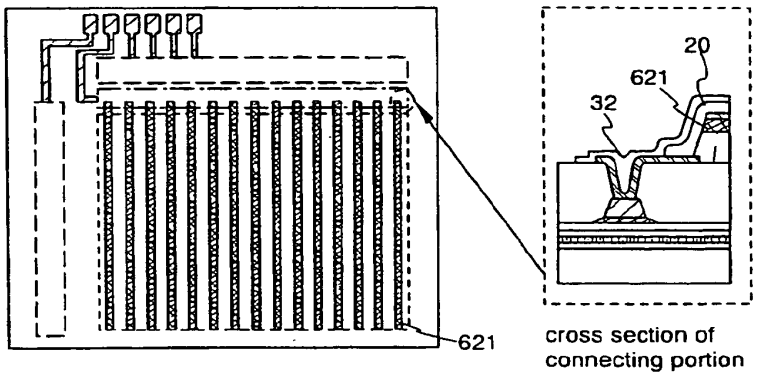
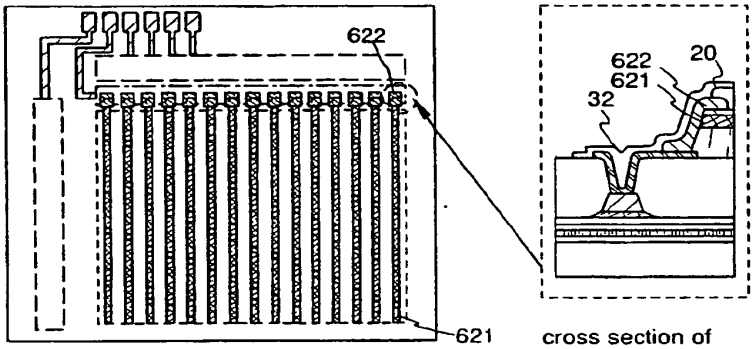


FIG. 7A



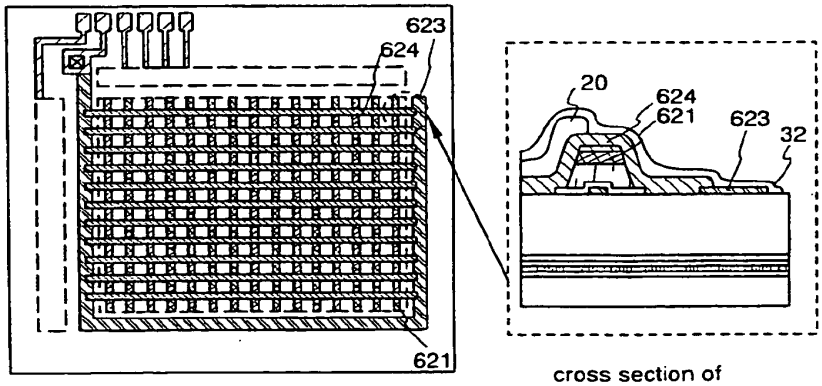
cross section of
connecting portion
(cut along Y direction)

FIG. 7B



cross section of
connecting portion
(cut along Y direction)

FIG. 7C



cross section of
connecting portion
(cut along X direction)

FIG. 8A

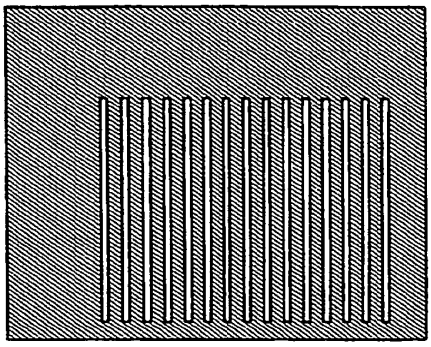


FIG. 8B

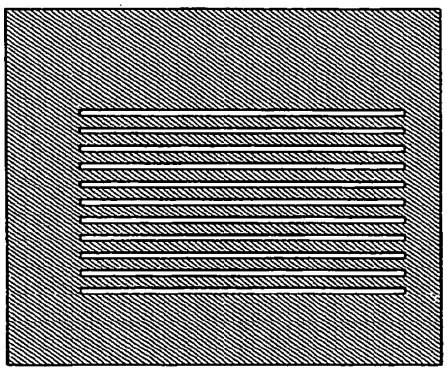


FIG. 8C

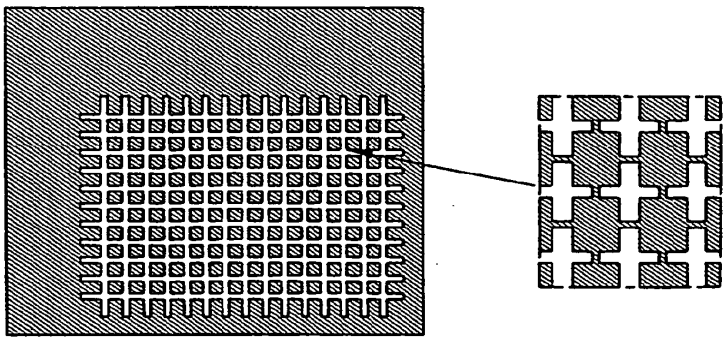


FIG. 9A sectional view of A-A'

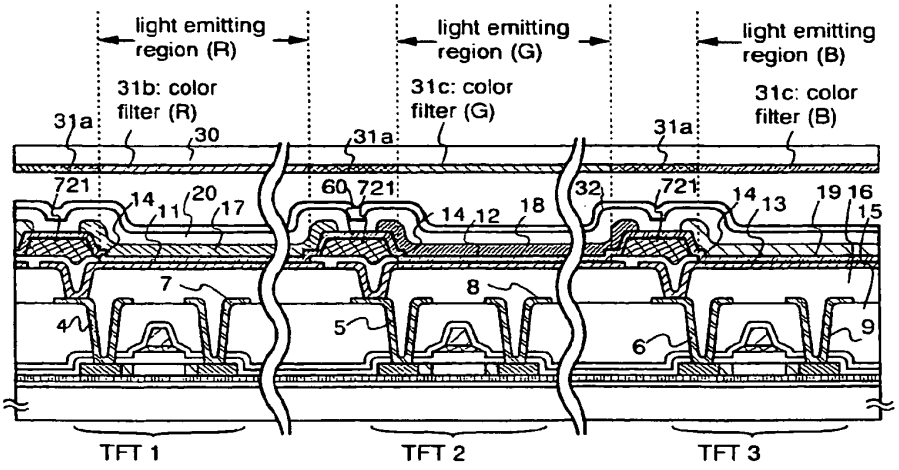


FIG. 9B sectional view of B-B'

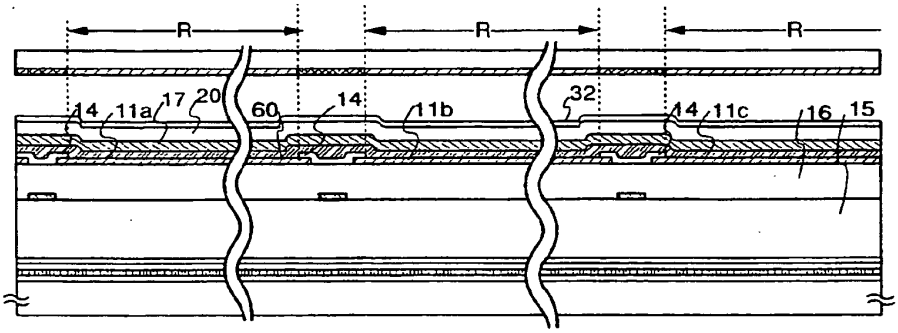


FIG. 9C sectional view of C-C'

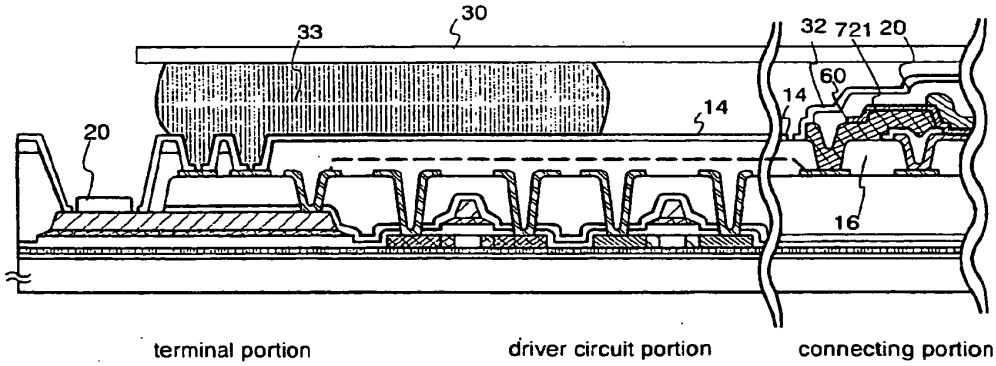


FIG. 10A sectional view of A-A'

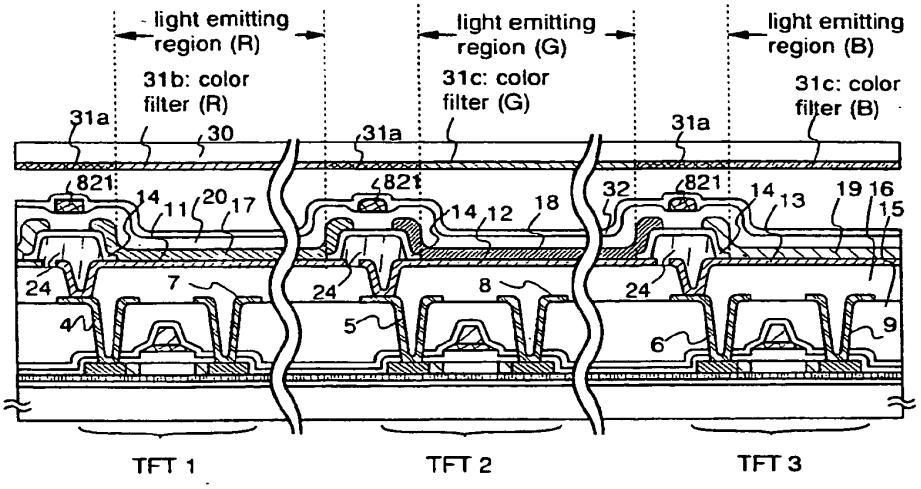


FIG. 10B sectional view of B-B'

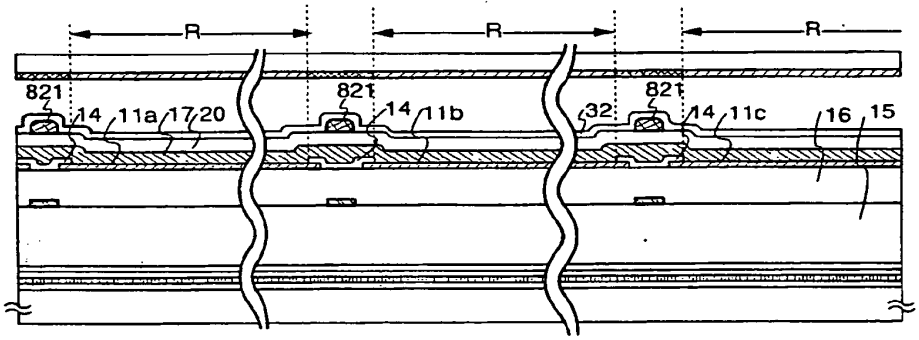


FIG. 10C sectional view of C-C'

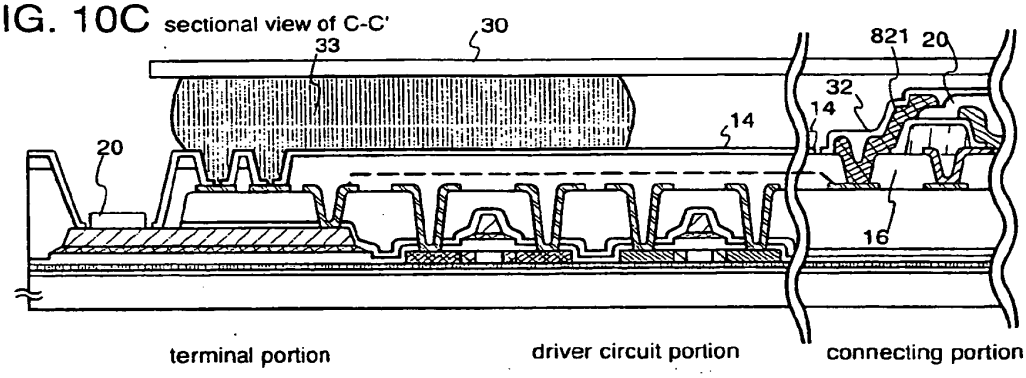


FIG. 11

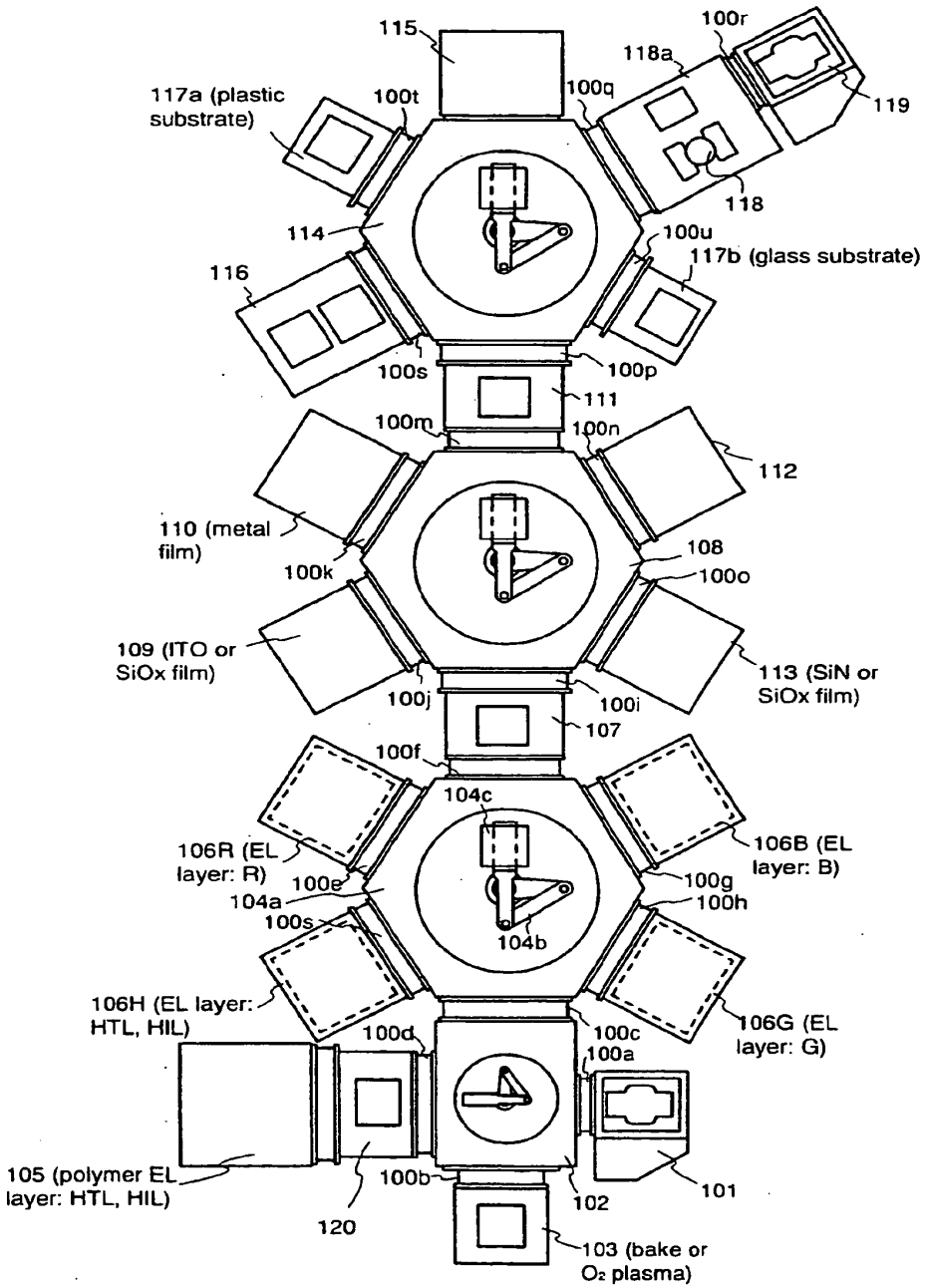
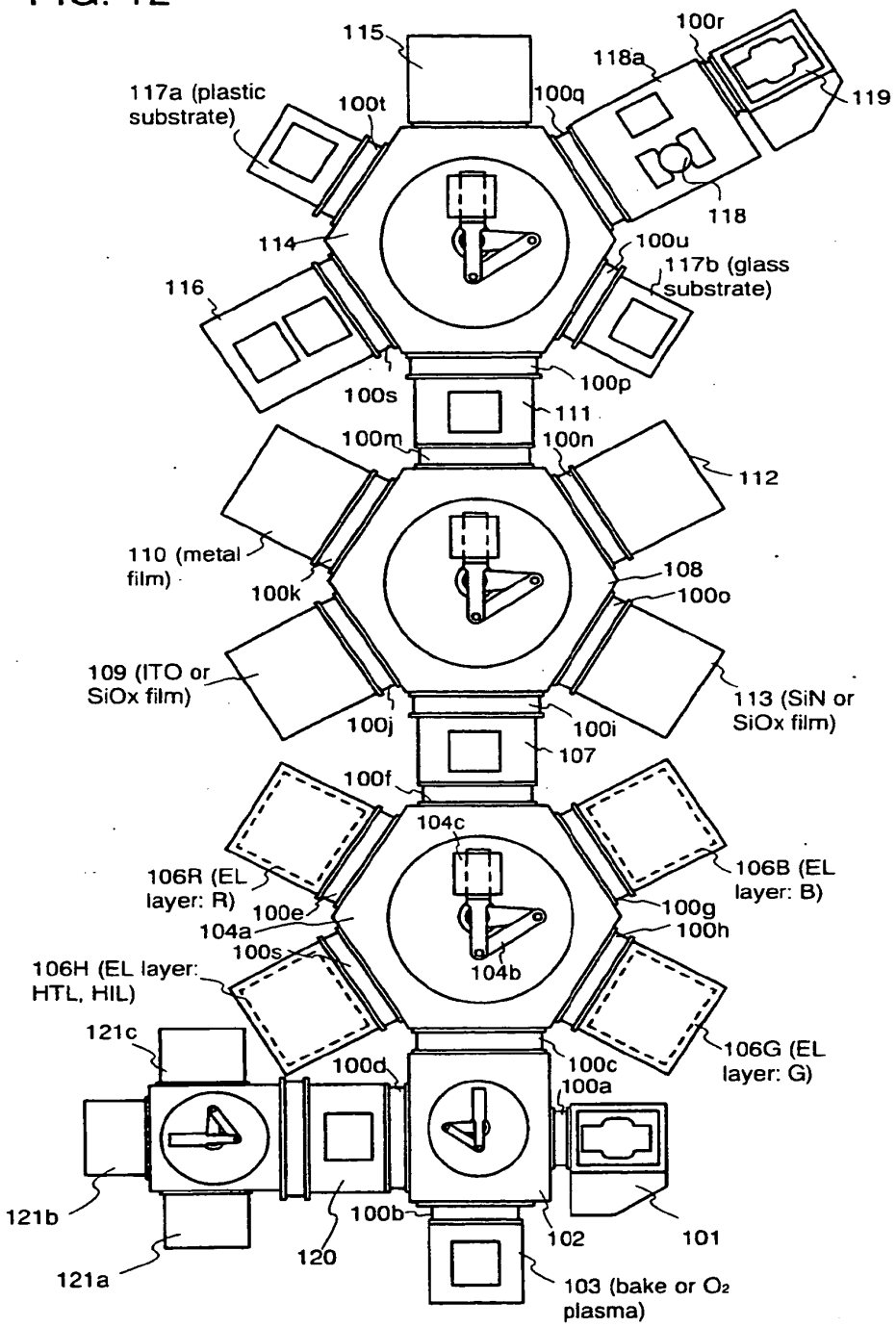


FIG. 12



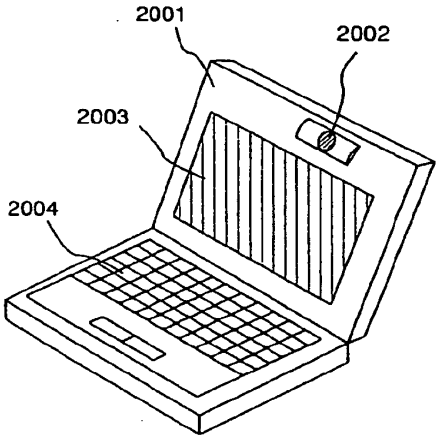


FIG. 13A

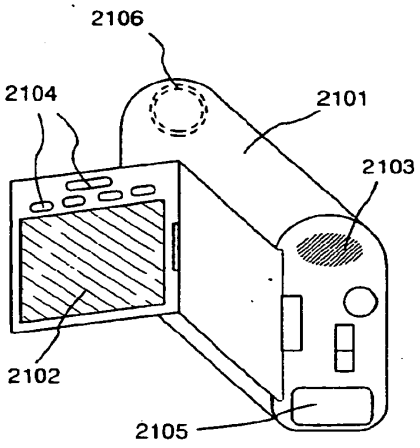


FIG. 13B

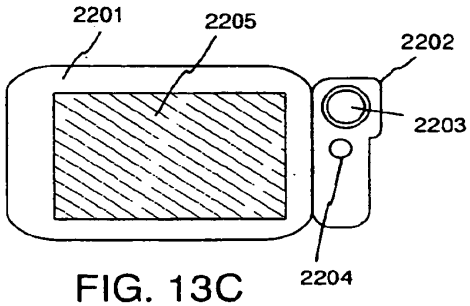


FIG. 13C

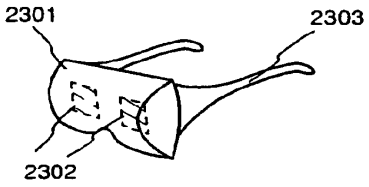


FIG. 13D

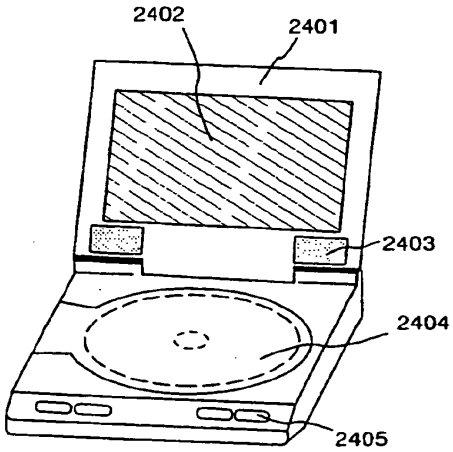


FIG. 13E

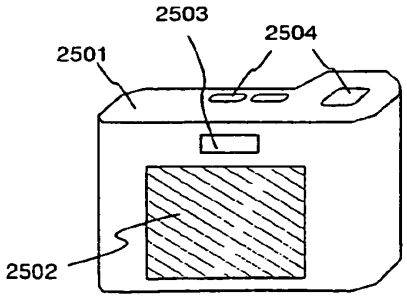


FIG. 13F

FIG. 14A

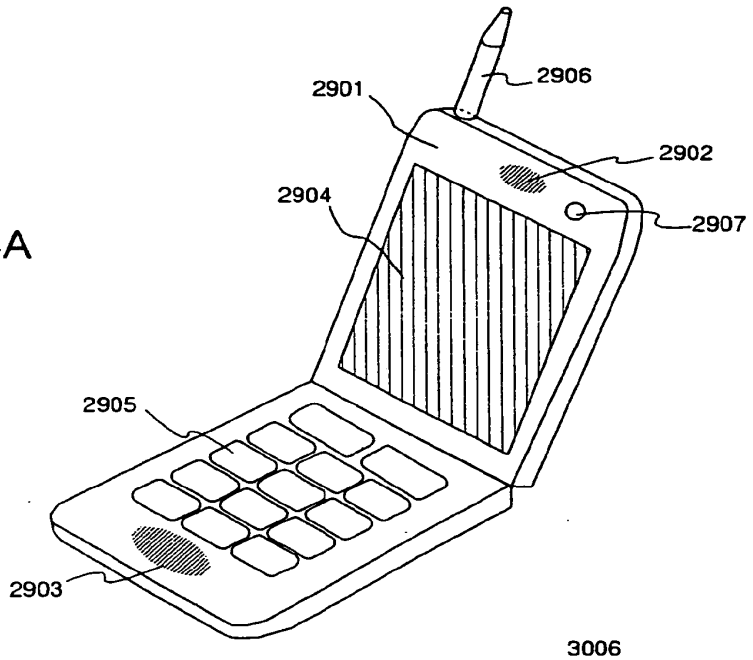


FIG. 14B

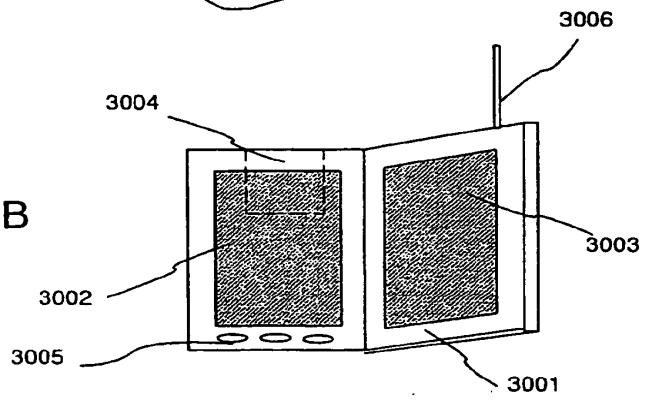
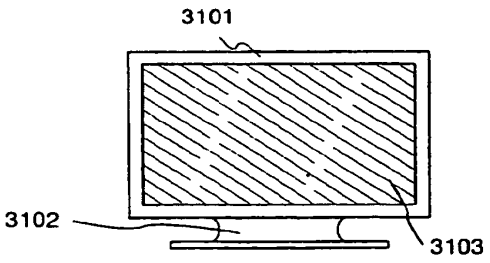


FIG. 14C



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(54) Matrix display device with damascene wiring lines and method for manufacturing same

(57) The present invention provides a structure of a semiconductor device that realizes low power consumption even where increased in screen size, and a method for manufacturing the same. The invention forms an insulating layer, forms a buried interconnection (of Cu, Au, Ag, Ni, Cr, Pd, Rh, Sn, Pb or an alloy thereof) in the insulating layer. Furthermore, after planarizing the surface of the insulating layer, a metal protection film (Ti, TiN, Ta, TaN or the like) is formed in an exposed part. By using the buried interconnection in part of various lines (gate line, source line, power supply line, common line and the like) for a light-emitting device or liquid-crystal display device, line resistance is decreased.

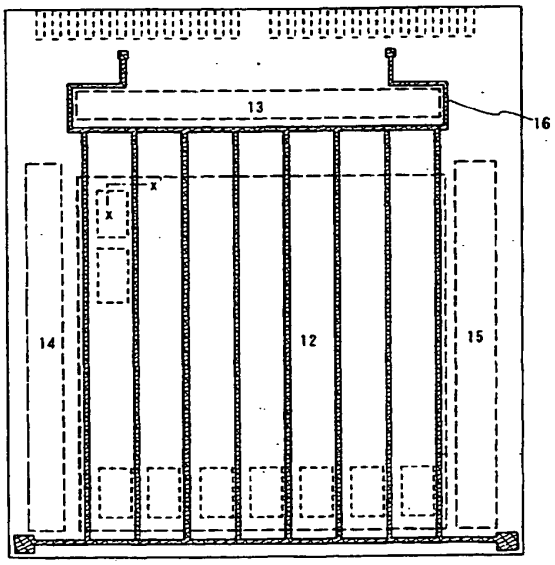

Fig. 3

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Description

BACKGROUND OF THE INVENTION

1. Technical Field of the Invention

[0001] The present invention relates to a semiconductor device having a circuit configured with thin-film transistors (hereinafter, referred to as TFTs) and a method for manufacturing same. For example, the invention relates to an electronic apparatus mounting, as a part, an electro-optical device represented by a liquid-crystal display or a light-emitting device having OLEDs.

[0002] Incidentally, the semiconductor device in this description refers to a device as a whole which is capable of functioning by the utilization of a semiconductor characteristic, i.e. electro-optical devices, semiconductor circuits and electronic apparatuses are all fallen under semiconductor devices.

2. Description of the Related Art

[0003] Recently, attentions are drawn to the art to structure a thin-film transistor (TFT) by the use of a semiconductor film (thickness: approximately several to several hundred nm) formed over a substrate having an insulating surface. Thin-film transistors are broadly used on electronic devices, such as ICs and electro-optical devices. Particularly, development is hurried up for a switching element for an image display device.

[0004] Conventionally, the liquid-crystal display is known as an image display device. There is a tendency of frequent use of the liquid-crystal display of the active-matrix type because of the capability of obtaining an image with definition as compared to the passive-type liquid-crystal display devices. In the active-matrix liquid-crystal display device, a display pattern is formed on the screen by driving the pixel electrodes arranged in a matrix form. Specifically, by applying a voltage to between a selected pixel electrode and a counter electrode corresponding to that electrode, optical modulation is done in the liquid-crystal layer arranged between the pixel electrode and the counter electrode. The optical modulation is recognized as a display pattern by the observer.

[0005] Meanwhile, for the light-emitting devices using OLEDs, TFTs are requisite elements in realizing active-matrix drive scheme. Consequently, the light-emitting device using OLEDs has, on each pixel, at least a TFT functioning as a switching element and a TFT supplying current to the OLED. Light-emitting elements using an organic compound as phosphors, featured in small thickness, light weight, high responsibility, direct-current low voltage drive, are expected for the application to the next-generation display panel. In particular, the display device arranging the light-emitting elements in a matrix form is considered excellent in respect of its wide viewing angle and hence higher visibility as compared to the conventional liquid-crystal display device.

[0006] The luminescent mechanism of a light-emitting element is considered as follows. That is, by applying a voltage to a pair of electrodes sandwiching an organic compound layer, the electrons injected at the cathode and the holes injected at the anode are recombined at luminous centers in the organic compound layer. The molecular exciter, upon retuning to the ground state, gives off energy causing light emission. The excitation state is known as singlet excitation and triplet excitation. Electro-luminescence is considered possible through any of the excitation states.

[0007] For the light-emitting device formed by such light-emitting elements arranged in a matrix form, it is possible to use drive schemes of passive-matrix drive (simple matrix type) and active-matrix drive (active-matrix type). However, in the case with increased pixel density, the active-matrix type having a switch on each pixel (or one dot) is considered advantageous because of the capability of driving at low voltage.

[0008] There are increasing applications of such active-matrix type display devices (representatively, liquid-crystal and light-emitting display devices). With the increasing area in screen size, there are increasing requirements for improving definition, opening ratio and reliability. At the same time, requirements are toward production increase and cost reduction.

[0009] Conventionally, where TFTs are fabricated by using aluminum as a TFT gate interconnection material, there encounter projections, such as hillocks or whiskers, formed by thermal process or TFT poor operation or TFT characteristic reduction due to the diffusion of aluminum atoms into the channel region. To cope with this, in the case of using a metal material resistive to the thermal process, representatively high melt-point metal element, the problem arises that interconnection resistance increases or so with increase in screen area size, incurring increased power consumption.

[0010] Accordingly, it is a problem of the present invention to provide a structure of a semiconductor device that realizes low power consumption even where increased in screen size, and a method for manufacturing the same.

SUMMARY OF THE INVENTION

[0011] In order to solve the problem, the present invention forms an insulating layer, forms a buried interconnection (of Cu, Au, Ag, Ni, Cr, Pd, Rh, Sn, Pb or an alloy thereof) in the insulating layer. Furthermore, after planarizing the surface of the insulating layer, a metal protection film (Ti, TiN, Ta, TaN or the like) is formed in an exposed part. By using the buried interconnection as part of various lines (gate line, source line, power supply line, common line and the like) of light-emitting devices and liquid-crystal display device, line resistance is decreased. The present invention can realize low power consumption even in case screen size is increased in area.

[0012] The structure of the invention disclosed in this description is, as exemplified in Figs. 1A-1E, a light-emitting device comprising, between a first substrate having an insulating surface and a second substrate having light transmission property:

a pixel region having a plurality of light-emitting elements, the light emitting element having a first electrode, a layer containing organic compound provided on and in contact with the first electrode, and a second electrode provided on and in contact with the layer containing organic compound; and
a drive circuit having thin-film transistors;
whereby the pixel region is arranged with a gate line, source line or power supply line made with a buried interconnection.

[0013] In the structure, the buried interconnection is of copper, silver, gold or an alloy thereof which is to be plating-processed. Also, the buried interconnection is provided in a layer lower than the thin-film transistor.

[0014] Also, in the structure, the layer containing organic compound is a material for white light emission and combined with a color filter provided on the second substrate. Otherwise, the layer containing organic compound is a material for single-color light emission and combined with a color change layer or coloring layer provided on the second substrate.

[0015] Also, the structure of the invention for realizing the construction is a method for manufacturing a light-emitting device comprising:

a first step of forming an etching-stop layer having an electric conductivity on an insulating surface;
a second step of forming a first insulating film covering the etching-stop layer;
a third step of etching the first insulating film to open an opening reaching the etching-stop layer;
a fourth step of forming a seed and carrying out plating to form a buried interconnection covering the opening;
a fifth step of carrying out planarization;
a sixth step of forming a second insulating film containing aluminum;
a seventh step of forming a third insulating film on the second insulating film;
an eighth step of forming a semiconductor layer on the third insulating film;
a ninth step of forming a fourth insulating film on the semiconductor layer;
a tenth step of forming a gate electrode on the fourth insulating film;
an eleventh step of forming a line connecting to the semiconductor layer and a line connecting the buried interconnection;
a twelve step of forming a first electrode; and
a thirteenth step of forming a layer containing organic compound on the first electrode and a second electrode on the layer containing organic compound.

[0016] Also, in the structure concerning the manufacturing method, the buried interconnection is a power supply line.

[0017] Also, in the structure concerning the manufacturing method, the buried interconnection is of copper, silver, gold or an alloy thereof.

[0018] Also, the structure of another invention is, as shown in Fig. 12, a liquid-crystal display device comprising, between a first substrate having an insulating surface and a second substrate having light transmission property:

a pixel region having a first electrode, a second electrode and a liquid-crystal material sandwiched between the electrodes; and
a drive circuit having thin-film transistors;
whereby the pixel region is arranged with a gate line or source line made by a buried interconnection.

[0019] Also, in the structure, the buried interconnection is of copper, silver, gold or an alloy thereof. Also, in the structure, the buried interconnection is provided in a layer lower than the thin-film transistor.

[0020] Also, the structure of the invention for realizing the construction is a method for manufacturing a liquid-crystal display device comprising:

a first step of forming an etching-stop layer having an electric conductivity on an insulating surface;
a second step of forming a first insulating film covering the etching-stop layer;
a third step of etching the first insulating film to open an opening reaching the etching-stop layer;
a fourth step of forming a seed and carrying out plating to form a buried interconnection covering the opening;
a fifth step of carrying out planarization;
a sixth step of forming a second insulating film containing aluminum;
a seventh step of forming a third insulating film on the second insulating film;
an eighth step of forming a semiconductor layer on the third insulating film;
a ninth step of forming a fourth insulating film on the semiconductor layer;
a tenth step of forming a gate electrode on the fourth insulating film;
an eleventh step of forming a source line connected to the semiconductor layer and a line connecting between the buried interconnection and the gate line.

[0021] Also, in the structure concerning the manufacturing method, the buried interconnection is a gate line. Also, in the structure concerning the manufacturing

method, the buried interconnection is of copper, silver, gold or an alloy thereof.

[0022] Also, plating may be done using the etching-stop layer as a seed.

[0023] Incidentally, the light-emitting element (EL element) has a layer containing an organic compound to obtain electro-luminescence caused by applying an electric field (hereinafter, described as EL layer), an anode and a cathode. The electro-luminescence in an organic compound includes luminescence of upon returning from a singlet excitation state to the ground state (fluorescence) and luminescence of upon returning from a triplet excitation state to the ground state (phosphorescence). The light-emitting device fabricated by the invention is applicable for the case using any of luminescence.

[0024] The layer containing organic compound is in a lamination structure. Typically, included is a lamination structure having a hole transport layer/light-emitting layer/electron transport layer on the anode. This structure has an extremely high light-emission efficiency. Almost all the light-emitting devices currently researched and developed adopt this structure. Besides, the structure may be a lamination of pole injection layer/hole transport layer/electron transport layer or hole injection layer/hole transport layer/light-emitting layer/light-emitting layer/electron transport layer/electron injection layer in the order. The light-emitting layer may be doped with a fluorescent pigment or the like. These layers may all be formed by using low-molecular materials or all be formed by using high-molecular materials. Incidentally, in the description, all the layers provided between the cathode and the anode are collectively referred to as a layer containing organic compound (EL layer). Accordingly, the hole injection layer, the hole transport layer, the light-emitting layer, the electron transport layer and the electron injection layer are all included in the EL layer. Also, the layer containing organic compound (EL layer) may contain an inorganic material such as silicon.

[0025] Meanwhile, in the light-emitting device of the invention, there is no limitation in drive method for screen display, i.e. dot-sequence drive method, line-sequence drive method or plane-sequence drive method may be used. Typically, line-sequence drive method may be used, and time-division tone drive method or area-tone drive method be properly employed. Also, the video signal to be input to the source line of the light-emitting device may be an analog signal or digital signal. The drive circuit or the like may be properly designed matched to the video signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026]

Figs. 1A to 1E are sectional views each showing a process of the present invention (embodiment);
Figs. 2A and 2B are views each showing a section of a light-emitting element of the invention (example 1);
Fig. 3 is a top view in a manufacturing process of a light-emitting device (example 1);
Fig. 4 is a top view in a manufacturing process of a light-emitting device (example 1);
Fig. 5 is a top view in a manufacturing process of a light-emitting device (example 1);
Fig. 6 is a top view in a manufacturing process of a light-emitting device (example 1);
Figs. 7A to 7C are figures each showing a lamination structure of the light-emitting element (example 1);
Figs. 8A to 8C are typical figures in the case of using white emission light for full-color display (example 1);
Fig. 9 is a figure showing a transmissivity of a coloring layer (example 1);
Fig. 10 is a figure showing a chromaticity coordinate (example 1);
Figs. 11A and 11B are a sectional view and top view of an active-type display device (example 1);
Fig. 12 is a view showing a sectional view of a liquid-crystal display device (example 2);
Fig. 13 is a figure showing a top view in a manufacturing process of a liquid-crystal display device (example 2);
Figs. 14A to 14C are views showing examples of electronic apparatuses; and
Figs. 15A and 15B are views showing examples of electronic apparatuses.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0027] Embodiments of the present invention will now be explained.

[0028] Herein, in Figs. 1A-1E are shown an example to form a buried interconnection and TFT.

[0029] First, an etching-stop layer 102 is formed on a substrate 100 having an insulating surface. The etching-stop layer 102 may use a film, or a lamination thereof, based on an element selected from Ni, Ti, W, WSi_x, Al, Mo, Ta, Cr or Mo, or an alloy or compound material based on the element or elements. The etching-stop layer 102 is to serve as a seed layer (cathode in a plating process) in an electrolytic plating process to be carried out later. Subsequently, an insulating film 101 is formed based on silicon to cover the etching-stop layer 102. (Fig. 1A)

[0030] Then, patterning is made to selectively etch the insulating film 101 thereby forming an opening (trench) reaching the etching-stop layer 102. After forming a first barrier layer 103, an electrolytic plating process is carried out to form a low-resistance metal film having a sufficient thickness in the opening (trench). The electrolytic plating process is a method to flow a direct current in a solution containing the ions of a metal to be formed by

the plating process thereby forming a metal film on a cathode surface. The plating metal can use a material having a low electric resistance, e.g. copper, silver, gold, chromium, iron, nickel, platinum or an alloy of these. The film thickness of a metal film to be formed in an electrolytic plating process can be properly set with controlling a current density and time by a practitioner. Because copper has an extremely low electric resistance, shown herein is an example using copper (Cu) that electrolytic plating is possible in forming a low resistance metal film. Prior to plating, a seed is preferably formed. Meanwhile, the first barrier layer 103 is a diffusion preventing layer against copper having a fast diffusion rate in an insulating film based on silicon oxide, i.e. a barrier metal, preferably using a metal material (WN_x, TaN_x, $TiSi_xN_y$, WSi_xN_y, $TaSi_xN_y$, or the like) having a specific resistance value of 300 - 500 μΩcm or less. Meanwhile, because copper has a poor adhesion to an insulating film based on silicon oxide, it is useful to form a first barrier layer 103 having a good adhesion.

[0031] Then, a planarizing process is carried out, which is represented by the chemical mechanical polish process (hereinafter, referred to as CMP process). Due to this, the copper and first barrier layer is left only in the opening (trench). Unwanted parts are removed away, thereby forming a buried-type interconnection (hereinafter, referred to as buried interconnection) 104a, 104b (Fig. 1B)

[0032] In order to enhance the oxidation resistance of an exposed part of copper, a second barrier layer 106 is formed. The second barrier layer 106 is useful as a diffusion preventing layer against copper having a fast diffusion rate in an insulating film based on silicon oxide, and preferably uses silicon nitride or a metal material (TiN, NbN, WN_x, TaN_x, $TiSi_xN_y$, WSi_xN_y, $TaSi_xN_y$, or the like). Meanwhile, because copper has a poor adhesion to an insulating film based on silicon oxide, it is useful to form a second barrier layer 106 having a good adhesion.

[0033] Subsequently, a layer 107 expressed by AlN_xO_y is formed as an underlying insulating film for prevention against impurity diffusion into a TFT to be formed later. The layer 107 expressed by AlN_xO_y may be deposited by an RF sputter technique using a target of AlN or Al with oxygen, nitrogen or inert gas introduced from the foregoing gas introducing system. Nitrogen may be contained in a range of several atm% or more, preferably 2.5 atm% - 47.5 atm%, in the layer expressed by AlN_xO_y. Oxygen may be 47.5 atm% or less, preferably 0.01 - 20 atm% or less.

[0034] Then, an underlying insulating film 108 is formed by a lamination of insulating films such as a silicon oxide film, a silicon nitride film or a silicon oxynitride film. Although the underlying insulating film 108 herein uses a two-layer structure, it may use a structure having a single layer or a two layers or more of the insulating films. The first layer 108a of the underlying insulating film is a silicon oxide nitride film deposited to 10 - 200 nm (preferably 50 - 100 nm) by a plasma CVD process using a reaction gas of SiH_4, NH_3 and N_2O. Herein, formed is a silicon oxide nitride film (composition ratio: Si = 32%, O = 27%, N = 24% and H = 17%) having a film thickness of 50 nm. The second layer 108b of the underlying insulating film is a silicon oxide nitride film deposited to 50 - 200 nm (preferably 100 - 150 nm) by a plasma CVD process using a reaction gas of SiH_4 and N_2O. Herein, formed is a silicon oxide nitride film (composition ratio: Si = 32%, O = 59%, N = 7% and H = 2%) having a film thickness of 100 nm. (Fig. 1C)

[0035] Subsequently, a semiconductor layer is formed on the underlying film. The semiconductor layer is formed by patterning, into a desired form, a crystalline semiconductor film obtained by forming an amorphous-structured semiconductor film by known means (sputter process, LPCVD process or plasma CVD process) and carrying out a known crystallizing process (laser crystallizing process, thermal crystallizing process or thermal crystallizing process using a catalyst such as nickel). This semiconductor layer is formed in a thickness of 25 - 80 nm (preferably 30 - 60 nm). The material of the crystalline semiconductor film, although not limited in material, is preferably formed of silicon or a silicon-germanium alloy.

[0036] In the case of making a crystalline semiconductor film by a laser crystallizing process, it is possible to use an excimer laser of a pulse-oscillation or continuous-oscillation type, a YAG laser or a YVO_4 laser. In the case of using such a laser, preferably used is a method that the laser light emitted from a laser oscillator is focused by an optical system into a linear form to be irradiated onto the semiconductor film. The condition of crystallization is to be appropriately selected by the practitioner. In the case of using an excimer laser, pulse oscillation frequency is 30 Hz and laser energy density is 100 - 400 mJ/cm^2 (typically 200 - 300 mJ/cm^2). Meanwhile, in the case of using a YAG laser, preferably its second harmonic is used and pulse oscillation frequency is 1 - 10 kHz and laser energy density is 300 - 600 mJ/cm^2 (typically 350 - 500 mJ/cm^2). The laser light focused linear to a width of 100 - 1000 μm, e.g. 400 μm, is irradiated throughout the substrate entirety, whereupon the overlap ratio of linear laser beam may be taken 80 - 98%.

[0037] Then, the surface of the semiconductor layer is cleaned by an etchant containing a hydrogen fluoride, to form a gate insulating film 109 covering the semiconductor layer. The gate insulating film 109 is formed by an insulating film containing silicon having a thickness of 40 - 150 nm by the use of a plasma CVD process or sputter process. This embodiment forms a silicon oxide nitride film (composition ratio: Si = 32%, O = 59%, N = 7% and H = 2%) in a thickness of 115 nm by a plasma CVD process. Naturally, the gate insulating film is not limited to a silicon oxide nitride film but may be made in a single layer or a lamination of layers of insulating films containing other form of silicon.

[0038] After cleaning the surface of the gate insulating film 109, a gate electrode 110 or connection electrode is formed. Before forming a gate electrode 110, a contact hole is formed reaching the buried interconnection 104a, 104b. Thus, electric connection is provided by forming a gate electrode 110 contacted with the buried interconnection 104b or a connection electrode contacted with the buried interconnection 104a.

[0039] Then, a p-type providing impurity element (such as B), boron herein, is added in proper amount to the semiconductor, to form a source region 111 and a drain region 112. After the addition, heating process, intense light radiation or laser irradiation is made in order to activate the impurity element. Simultaneously with activation, restoration is possible from the plasma damage to the gate insulating film or from the plasma damage at the interface between the gate insulating film and the semiconductor layer. Particularly, it is extremely effective to irradiate the second harmonic of a YAG laser at a main or back surface thereby activating the impurity element in an atmosphere at room temperature to 300 °C. YAG laser is preferable activating means because of less maintenance.

[0040] In the subsequent process, after an interlayer insulating film 113 is formed of an organic or inorganic material and hydrogenation is made thereon, a contact hole is formed therein reaching the source region, drain region or connection electrode. Next, a source electrode (line) 115 and a drain electrode 114 are formed to complete a TFT (p-channel TFT) having a buried interconnection. (Fig. 1E) Although the example was herein shown that the buried interconnection and the drain electrode 114 are connected together through a connection electrode simultaneously formed with the gate electrode, a drain electrode may be formed after forming a contact hole reaching the buried interconnection without using a connection electrode.

[0041] The TFT having a buried interconnection 104a, 104b obtained by the above process can be used on various semiconductor devices, e.g. TFTs (current-control TFT) of a light-emitting device as shown in Figs. 2A and 2B, or pixel TFTs of a liquid-crystal display device as shown in Fig. 12.

[0042] Incidentally, although illustrated herein were the buried interconnection 104b connected to the gate electrode and the buried interconnection 104a connected to the drain electrode, the application is possible, without limitation, to various interconnections, e.g. source line, extended line, power supply line, capacitance line or the like, thereby achieving resistance reduction.

[0043] Also, the invention is not limited to the TFT structure of Fig. 1E but, if required, may be in a lightly doped drain (LDD) structure having an LDD region between the channel region and the drain region (or source region). This structure is provided with a region an impurity element is added with light concentration at between the channel region and the source or drain region formed by adding an impurity element with high concentration, which region is called an LDD region. Furthermore, it may be in, what is called, a GOLD (Gate-drain Overlapped LDD) structure arranging an LDD region overlapped with a gate electrode through a gate insulating film.

[0044] Meanwhile, although explanation herein was by using the p-channel TFT, it is needless to say that a p-channel TFT can be formed by using an n-type impurity element (P, As, etc.) in place of the p-type impurity element.

[0045] Also, although explanation herein was on a top-gate TFT, the invention is applicable regardless of the TFT structure, e.g. the invention is applicable to a bottom-gate TFT or a forward stagger TFT.

[0046] The invention configured above will be explained with greater detail by the following embodiment.

EXAMPLE

[Example 1]

[0047] This example shows that the major part of the power supply line of a light-emitting device is made as a buried interconnection, in Figs. 3 to 6.

[0048] At first, according to the above embodiment, an etching-stop layer is formed on a substrate having an insulating surface and a silicon-based insulating film is formed covering the etching-stop layer. The insulating film is selectively etched to form an opening (trench) reaching the etching-stop layer. After forming a first barrier layer, electrolytic plating is carried out to form a low-resistance metal film having a sufficient thickness in the opening (trench). Subsequently, planarization represented by the chemical mechanical polishing (hereinafter, referred to as CMP) is made to leave the copper and first barrier layer only in the opening (trench) but remove away unwanted portions, thereby forming an interconnection in a buried form. The top view in this process stage is shown in Fig. 3, wherein the sectional view taken along the dotted line x-x' therein corresponds to Fig. 1C. In Fig. 3, 12 is a pixel region, 13 is a source drive circuit, and 14, 15 show regions arranging gate drive circuits. As shown in Fig. 3, the power supply line 16 has, at its end, a connection electrode pad provided in a corner of the substrate to flow a current from an external power source when carrying out electrolytic plating. Incidentally, because this example is made in an example having single-color light-emitting elements arranged in a matrix form, the pattern is connected such that the power source line 16 is common between the pixels to make them at the same potential.

[0049] Incidentally, the power source line 16 is shown only eight in the number for simplification sake. In the case there are pixels in the number of m x n (m rows by n columns), the power supply line is actually given m in the number or the number added with one or two spare lines for enhancing the evenness in electrolytic plating.

[0050] Then, a second barrier layer is formed in order to provide an exposed portion of copper with enhanced resistance to oxidation. Furthermore, after forming a layer represented by AlN_xO_y as an underlying insulating film, an underlying insulating film is formed by a lamination of insulating films such as a silicon oxide film, a silicon nitride film or a silicon oxide nitride film. Then, a crystalline semiconductor film is patterned to a desired form to form a semiconductor layer, followed by forming a gate insulating film covering the semiconductor layer.

[0051] After forming a contact hole reaching the buried interconnection, a gate line, a terminal electrode and an extended electrode are formed on the gate insulating film. The extended electrode, provided between the source drive circuit 13 and the pixel region 12, is an electrode arranged such that a source line formed later is not overlapped with the extended line (line connected to a cathode or anode of the light-emitting element) 17. Meanwhile, terminal electrodes are provided in plurality at an end of the substrate, some of which are connected to the power supply line as buried interconnection. The top view in this process stage is shown in Fig. 4.

[0052] Then, the semiconductor is properly added by a p-type providing impurity element (B or the like) or n-type providing impurity element (P, As or the like), to form source and drain regions. Subsequently, in order to activate the added impurity element, heating process, intense light radiation or laser irradiation is carried out. Then, after an interlayer insulating film is formed and hydrogenation is made, contact holes are formed reaching the source region, the drain region, the extended electrode, the terminal electrode or the buried interconnection.

[0053] Subsequently, source electrodes (lines), drain electrodes or connection electrodes are formed to complete various TFTs. In the stage completing the above process, in the pixel region 12, the source region and the power supply line are electrically connected to form a connection electrode contacted with the drain region (not shown herein). Meanwhile, in the drive circuit, formed are a source electrode (line) contacted to the source region and a drain electrode contacted to the drain region. Also, in the terminal region, formed are a source line connected to a certain terminal electrode and an extended line (line connected to a cathode or anode of a light-emitting element) 17 connected to another terminal electrode. Also, between the drive circuit and the pixel region is formed an extended line (line connected to a cathode or anode of a light-emitting element) 17. The top view in this process stage is shown in Fig. 5.

[0054] Then, in the pixel region, the first electrodes 19 are arranged in a matrix form that are connected to the connection electrode contacted to the drain regions. The first electrodes 19 are made into anodes or cathodes of light-emitting elements. Next, formed is an insulator (called bank, partition wall or barrier wall) covering the end of the first electrode 19. Next, in the pixel region, a layer 10 containing organic compound is formed, on which a second electrode 11 is formed to complete a light-emitting element. The second electrode 11 is made into a cathode or anode of the light-emitting element. Incidentally, in a region between the pixel region and the source drive circuit, the second electrode 11 is electrically connected to the extended line 17.

[0055] Then, the substrate and a sealing member (light-transmissive substrate, herein) 30 are bonded together by a sealant 31. The top view in this process stage is shown in Fig. 6. Furthermore, in order to shield from the outside air, a protection film may be formed of silicon nitride, silicon oxide nitride or DLC (diamond-like carbon) on the second electrode 11. Finally, an FPC (flexible print circuit) for connection to an external circuit is bonded to the terminal electrode.

[0056] By the above process, completed is an active-matrix light-emitting device.

[0057] Incidentally, concerning the active-matrix light-emitting device having TFTs, two constructions can be considered according to the direction of light radiation. One is a structure that the light from the light-emitting element is radiated through the second electrode to the eye of an observer. In this case, the observer can recognize an image on the side of the second electrode. The other one is a structure that the light from the light-emitting element is radiated through the first electrode and substrate to the eye of an observer.

[0058] In the case of the structure that the light from the light-emitting element radiates through the second electrode to the eye of an observer as shown in Fig. 2A, it is desired to use a light-transmissive material for the second electrode 11 (electrode 119 in Fig. 2A).

[0059] For example, where the first electrode 19 (electrode 117 in Fig. 2A) is made as an anode, the material of the first electrode 19 uses a metal having a great work function (Pt, Cr, W, Ni, Zn, Sn or In). After an end region is covered by an insulator (called bank, partition wall or barrier wall) 116, a poly (ethylene dioxythiophene)/poly (styrene sulfonic acid) solution (PEDOT/PSS) is applied to the entire surface and baked. Thereafter, after a polyvinyl carbazole (PVK) solution doped with luminescent center pigment acting as a light-emitting layer (1, 1, 4, 4-tetraphenyl-1, 3-buthadiene (TPB), 4-dicyanomethylene-2-methyl-6- (p-dimethylamino-styryl) - 4H-pyran (DCM1), Nilered, coumarine 6, or the like) is applied to the entire surface and baked, a cathode may be formed by a second electrode 11 (electrode 119 in Fig. 2A) having a lamination of a thin film containing a metal having a small work function (Li, Mg or Cs) and a transparent conductive film (ITO (indium oxide tin oxide alloy), indium oxide zinc oxide alloy (In_2O_3-ZnO), zinc oxide (ZnO) or the like) layered thereon. Incidentally, in Fig. 2A, an auxiliary electrode 120 is provided on the insulator 116, in order to reduce the resistance in the cathode. The light-emitting element thus obtained shows white light emission. Incidentally, the PEDOT/PSS, using water as solvent, is insoluble in organic sol-

vent. Accordingly, in the case of applying PVK thereon, there is no fear of re-dissolution. Meanwhile, because solvent is different between PEDOT/PSS and PVK, it is preferred not to use the same one in the deposition chamber. Incidentally, although the example was herein shown that the layer 10 containing organic compound (118 in Fig. 2A) was formed by the application, there is no especial limitation, i.e. may be formed by a deposition process.

[0060] Meanwhile, although the above example showed the example having a lamination of organic compound as shown in Fig. 7B, the organic compound layer can be made in a single layer as shown in Fig. 7A. For example, electron-transporting 1, 3, 4-oxadiazole derivative (PBD) may be dispersed in hole-transporting polyvinyl carbazole (PVK). Meanwhile, 30 wt% of PBD is dispersed as electron-transport agent and four kinds of pigments (TPB, coumarin 6, DCM1, nilered) are dispersed in proper amount, thereby obtaining white light emission. Also, as shown in Fig. 7C, the organic compound layer may be provided by a lamination of a polymer material layer and a low-molecule material layer.

[0061] Incidentally, the organic compound film is formed between the anode and the cathode. By recombining between the holes injected at the anode and the electrons injected at the cathode in the organic compound film, white light emission is obtained in the organic compound film.

[0062] Also, by properly selecting and superposing, for mixing colors, an organic compound film for red light emission, an organic compound film for green light emission and an organic compound film for blue light emission, it is possible to obtain white light emission in the entirety.

[0063] There are various methods of full-color displaying by the use of light-emitting elements for white light. For example, as shown in Fig. 8A, there is a method of passing obtained white light emission through a color filter thereby obtaining red, green and blue light (hereinafter, referred to as color filter method).

[0064] By forming a color filter having a coloring layer (R) absorbing the portion other than red, a coloring layer (G) absorbing the portion other than green and a coloring layer (B) absorbing the portion other than blue in a direction the organic compound film emits white light, the white light from the light emitting element is separated to obtain red light, green light and blue light. Also, in the case of an active-matrix type, the TFTs are structurally formed between the substrate and the color filter. Meanwhile, the color filter has shade layer between the coloring layers. Where the screen is made great, the shade layer preferably includes desiccant.

[0065] The coloring layer (R, G, B) can use, besides a stripe pattern in the simplest form, an oblique mosaic arrangement, a triangular mosaic arrangement, an RGBG four-pixel arrangement or an RGBW four-pixel arrangement.

[0066] Fig. 9 shows an example of a relationship between a transmission ratio and a wavelength on each coloring layer using white light source (D65). The coloring layer constituting the color filter is formed by using a color resist of an organic photosensitive material dispersed with a pigment. Meanwhile, Fig. 10 shows, on a chromaticity coordinate, a color reproduction range in the case of combining white emission light with a color filter. Note that the chromaticity coordinate of white emission light (x, y) = (0.34, 0.35). From Fig. 10, it can be seen that color reproduction as full colors is fully secured.

[0067] Incidentally, in this case, even if there is a difference in obtainable light color, because each is formed by the organic compound film to exhibit white emission light, there is no need to separately apply organic compound films for the emission light colors. Also, it is possible to eliminate the especial need for a circular polarization plate that prevents mirror reflection.

[0068] Now explanation is made on a CCM (color changing mediums) method to be realized by combining a blue light-emitting element having a blue-light-emitting organic compound film with a fluorescent color change layer, with reference to Fig. 8B.

[0069] In the CCM method, the fluorescent color change layer is excited by the blue light emitted from a blue light-emitting element, to carry out color change by each color change layer. Specifically, change of blue to red (B → R) is made by a color change layer, change of blue to green (B → G) is made by a color change layer and change of blue to blue (B → B) is made by a color change layer (note that the change of from blue to blue may be omitted), thereby obtaining light emission of red, green and blue. In also the CCM method, for the active matrix type, TFTs are structurally formed between the substrate and the color change layer.

[0070] Incidentally, in also this case, there is no need to form organic compound films by separate applications. Also, it is possible to eliminate the necessity of the circular polarization plate for preventing mirror reflection.

[0071] Meanwhile, where the CCM method is used, the color change layer is excited by external light because of its fluorescent nature, possibly resulting in a problem of contrast reduction. It is accordingly preferred to raise the contrast by attaching a color filter or so, as shown in Fig. 8C.

[0072] Explanation is herein made on the external appearance of the active-matrix light-emitting device overall, in Figs. 11A and 11B. Fig. 11A is a top view showing the light-emitting device while Fig. 11B is a sectional view taken along A-A' in Fig. 11A. 901 shown by the dotted line is a source signal-line drive circuit, 902 is a pixel region, and 903 is a gate signal-line drive circuit. Also, 904 is a sealing substrate and 905 is a sealant. The interior surrounded by the sealant 905 is defined as a space 907.

[0073] 908 is a line for conveying a signal to be inputted to the source signal-line drive circuit 901 and gate

signal-line drive circuit 903, which receives a video signal or clock signal from an FPC (flexible print circuit) 909 serving as an external input terminal. Although only the FPC is shown, the FPC may be attached with a printed wiring board (PWB). The light-emitting device, in this description, assumably includes, besides the light-emitting device main body, a state an FPC or PWB is attached thereon.

[0074] Explanation is now made on a sectional structure, by using Fig. 11B. Although the substrate 910 is formed thereon with a drive circuit and a pixel region, the source signal-line drive circuit 901 and pixel region 902 is herein shown as a drive circuit.

[0075] The source signal-line drive circuit 901 is formed with a CMOS circuit as a combination of an n-channel TFT 923 and a p-channel TFT 924. The TFTs forming the drive circuit may be formed by a known CMOS circuit, PMOS circuit or NMOS circuit. Although this embodiment shows a driver-integrated type having a drive circuit formed on the substrate, it not necessarily required, i.e. it can be externally formed instead of on the substrate.

[0076] The pixel region 902 is formed with a plurality of pixels each of which includes a switching TFT 911, a current-control TFT 912 and a first electrode (anode) 913 electrically connected to the drain thereof. The current-control TFT 912 has a source electrically connected with a buried interconnection 930.

[0077] Meanwhile, an insulating layer 914 is formed at both ends of the first electrode (anode) 913, while a layer 915 containing organic compound is formed on the first electrode (anode) 913. Furthermore, a second electrode (cathode) 916 is formed on the layer 915 containing organic compound. This forms a light-emitting element 918 comprising the first electrode (anode) 912, the layer 915 containing organic compound and the second electrode (cathode) 916. Because the light-emitting element 918 herein is exemplified to emit white light, there is provided a color filter formed by a coloring layer 931 and a BM 932 (overcoat layer is not shown herein for simplification sake).

[0078] The second electrode (cathode) 916 serves also as an interconnection common to all the pixels, which is electrically connected to the FPC 909 via the connection line 908. Also, a third electrode (auxiliary electrode) is formed on the insulating layer 914, thus realizing the resistance reduction in the second electrode.

[0079] The sealing substrate 904 is bonded by the sealant 905 in order to seal the light-emitting elements 918 formed on the substrate 910. A resin-film spacer may be provided in order to secure a spacing between the sealing substrate 904 and the light-emitting element 918. An inert gas, such as nitrogen, is filled in the space 907 at the inside of the sealant 905. The sealant 905 preferably uses an epoxy resin. The sealant 905 is desirably of a material less permeable of moisture or oxygen. Furthermore, a substance having an effect to absorb oxygen or moisture may be included in the space 907.

[0080] In this embodiment, the material structuring the sealing substrate 904 can use, as a material, a plastic substrate of FRP (fiberglass-reinforced plastics) PVF (polyvinyl fluoride), Mylar, polyester or acryl, besides a glass or quartz substrate. Also, after the sealing substrate 904 is bonded by using the sealant 905, it can be further sealed in a manner covering the side surface (exposed surface) by a sealant.

[0081] By sealing the light-emitting elements in the space 907 as in the above, the light-emitting elements can be completely shielded from the outside. This can prevent a substance such as oxygen or moisture that accelerates deterioration of the organic compound layer from externally intruding. Accordingly, a reliable light-emitting device can be obtained.

[0082] On the other hand, in the case of the structure that the emission light from the light-emitting element is radiated through the first electrode and substrate to the eye of an observer as shown in Fig. 2B, the first electrode 19 (electrode 117 in Fig. 2A) desirably uses a light-transmissive material.

[0083] For example, in the case that the first electrode 19 (electrode 117 in Fig. 2B) is an anode, the material of the first electrode 19 uses a transparent conductive film (ITO (indium oxide tin oxide alloy), indium oxide zinc oxide alloy (In_2O_3-ZnO), zinc oxide (ZnO) or the like). After covering the ends with an insulator (called bank, partition wall or barrier wall) 116, a layer 118 containing organic compound is formed, on which a second electrode 11 (electrode 119 in Fig. 2B) of a metal film (an alloy such as of MgAg, MgIn, AlLi, CaF_2 or CaN, or a film formed by co-deposition of an element belonging to group 1 or 2 of the periodic table with aluminum) may be formed as a cathode. When forming a cathode, a resistance heating method due to evaporation is used. Forming may be selective by the use of an evaporation mask.

[0084] This example can be freely combined with the embodiment.

[Example 2]

[0085] This shows an example that the major part of a gate line of a liquid-crystal display device is made by a buried interconnection, in Figs. 12 and 13.

[0086] At first, according to the above embodiment, an etching-stop layer is formed on a substrate having an insulating surface and a silicon-based insulating film is formed covering the etching-stop layer. The insulating film is selectively etched to form an opening (trench) reaching the etching-stop layer. After forming a first barrier layer, electrolytic plating is carried out to form a low-resistance metal film having a sufficient thickness in the opening (trench). Subsequently, planarization represented by the chemical mechanical polishing (hereinafter, referred to as CMP) is made to leave the copper and first barrier layer only in the opening (trench) but remove

away unwanted portions, thereby forming an interconnection in a buried form.

[0087] Then, a second barrier layer is formed in order to provide an exposed portion of copper with enhanced resistance to oxidation. Furthermore, after forming a layer represented by AlN_xO_y as an underlying insulating film, an underlying insulating film is formed by the layers of a silicon oxide film, a silicon nitride film or a silicon oxide nitride film. Then, a crystalline semiconductor film is patterned to a desired form to form a semiconductor layer, followed by forming a gate insulating film covering the semiconductor layer.

[0088] After forming a contact hole reaching the buried interconnection, a gate electrode and a terminal electrode are formed on the gate insulating film. Incidentally, the gate electrode is connected to the buried interconnection to realize the resistance reduction in the gate line. Also, the terminal electrode is provided in plurality at the end of the substrate.

[0089] Then, the semiconductor is properly added by a p-type providing impurity element (B or the like) or n-type providing impurity element (P, As or the like), to form source and drain regions. Subsequently, in order to activate the added impurity element, heating process, intense light radiation or laser irradiation is carried out. Then, after an interlayer insulating film is formed and hydrogenation is made, contact holes are formed reaching the source region, the drain region, and the terminal electrode.

[0090] Subsequently, source electrodes (lines) 55 or drain electrodes are formed to complete various TFTs. In the stage completing the above process, in the pixel region 52, the drain regions and the respective drain electrodes are electrically connected while source regions and source electrodes (lines) are electrically connected. Meanwhile, in the drive circuit, formed are a source electrode (line) contacted to the source region and a drain electrode contacted to the drain region. Also, in the terminal region, formed are a source line connected to a certain terminal electrode. Then, in the pixel region, the pixel electrodes 59 are arranged in a matrix form that are contacted to the connection electrode contacted to the drain regions. The top view in this process stage is shown in Fig. 13. In Fig. 13, 52 is a pixel region, 53 is a source drive circuit, and 54 shows a region arranging a gate drive circuit. As shown in Fig. 13, the gate line 56 has, at an end, a connection electrode pad provided close to an end of the substrate to flow a current from an external power supply when carrying out electrolytic plating. Incidentally, in this example, the connection electrode pads are provided corresponding to the same number of the gate lines 56. Meanwhile, the gate lines may be formed by connecting the patterns to place all the gate lines in the same potential to carry out a plating process and then cutting them into individual gate lines.

[0091] Then, after forming an orientation film 62a, a rubbing process is carried out. Then, the substrate and a counter substrate 60 are bonded together by a sealant (not shown), to fill a liquid-crystal material 63 between the substrates, followed by being sealed. The counter substrate 60 is previously provided with a counter electrode 61 of a transparent conductive film and an orientation film 62b rubbing-processed. Finally, an FPC (flexible print circuit) for connection to an external circuit is bonded to the terminal electrode. Further, a polarization plate and a color filter are provided.

[0092] By the above process, an active-matrix liquid-crystal display device is completed.

[0093] Incidentally, concerning the active-matrix liquid-crystal display device having TFTs, three constructions (transparent type, reflection type and semi-transparent type) are to be considered. Although there are a transmission type having a pixel electrode made by a transparent conductive film to provide a backlight, a reflection type having a pixel electrode made by a reflection metal film to reflect external light, and a semi-transparent type having a pixel electrode a part of which is made by a transparent conductive film and the other part made by a reflection metal film to properly cause switching, the invention can be applied to any of the structures.

[0094] This example can be freely combined with the embodiment.

[Example 3]

[0095] The drive circuit and pixel region formed by carrying out the invention can complete various modules (active-matrix liquid-crystal module, active-matrix EC module). Namely, the invention can complete an electronic apparatus built it in a display part.

[0096] Such electronic apparatuses include video cameras, digital cameras, head-mount displays (goggle type displays), car navigators, projectors, car stereo sets, personal computers, and personal digital assistants (mobile computers, cellular phones or electronic books). Examples of them are shown in Figs. 14A to 14C and 15A and 15B.

[0097] Fig. 14A is a personal computer, including a main body 2001, an image input part 2002, a display part 2003, a keyboard 2004 and so on.

[0098] Fig. 14B is a mobile computer, including a main body 2201, a camera part 2202, an image receiving part 2203, an operation switch 2204, and a display part 2205.

[0099] Fig. 14C is a player using a recording medium recording a program (hereinafter, referred to as recording medium), including a main body 2401, a display part 2402, a speaker part 2403, a recording medium 2404, and an operation switch 2405. Incidentally, the player uses, as a recording medium, a DVD (Digital Versatile Disc), a CD or the like, enabling music listening, movie viewing or the Internet.

[0100] Fig. 15A is a portable book (electronic book), including a main body 3001, a display part 3002, 3003, a storage medium 3004, an operation switch 3005, and an antenna 3006.

[0101] Fig. 15B is a display, including a main body 3101, a support base 3102, and a display part 3103. The invention can complete a display part 3103 having a diagonal length 10 - 50 inches.

[0102] As in the above, the invention has extremely broad application range, and can complete an electronic appliance in every field. Also, the electronic apparatus of this example can be realized by using a structure in any of combinations of the embodiment and examples 1 and 2.

[0103] According to the present invention, in a semiconductor device represented by an active-matrix light-emitting display device or liquid-crystal display device, even if the pixel region area increases and the screen size increases, favorable display can be realized. Because the line resistance in the pixel region can be greatly decreased, the present invention can cope with a large screen having a diagonal length of 40 or 50 inches.

Claims

1. A light-emitting device comprising:

   a substrate having an insulating surface;
   a second substrate having light transmission property;
   a pixel region having a plurality of light-emitting elements, the light emitting element having a first electrode, a layer containing organic compound provided on and in contact with the first electrode, and a second electrode provided on and in contact with the layer containing organic compound; and
   a drive circuit having thin-film transistors,

   wherein the pixel region is arranged with a gate line, source line or power supply line made with a buried interconnection.

2. A light-emitting device according to claim 1, wherein the buried interconnection comprises at least one material selected from the group consisting of copper, silver, gold and an alloy thereof.

3. A light-emitting device according to claim 1, wherein the buried interconnection is provided in a layer below the thin-film transistor.

4. A light-emitting device according to any one of claims 1, wherein the layer containing organic compound is a material for white light emission and combined with a color filter provided on the second substrate.

5. A light-emitting device according to any one of claims 1, wherein the layer containing organic compound is a material for single-color light emission and combined with a color change layer or coloring layer provided on the second substrate.

6. A light-emitting device according to claim 1, wherein the light-emitting device is incorporated into an electronic apparatus selected from the group consisting of a video camera, a digital camera, a head-mount display, a car navigator, a projector, a car stereo, a personal computer, a personal digital assistant.

7. A liquid-crystal display device comprising:

   a first substrate having an insulating surface;
   a second substrate having light transmission property;
   a pixel region having a first electrode, a second electrode and a liquid-crystal material sandwiched between the first and second electrodes; and
   a drive circuit having thin-film transistors,
   whereby the pixel region is arranged with a gate line or source line made with a buried interconnection.

8. A liquid-crystal display device according to claim 7, wherein the buried interconnection comprises at least one material selected from the group consisting of copper, silver, gold and an alloy thereof.

9. A liquid-crystal display device according to claim 7, wherein the buried interconnection is provided in a layer below the thin-film transistor.

10. A liquid-crystal display device according to claim 7, wherein the liquid crystal display device is incorporated into an electronic apparatus selected from the group consisting of a video camera, a digital camera, a head-mount display, a car navigator, a projector, a car stereo, a personal computer, a personal digital assistant.

11. A display device comprising:

   a substrate having an insulating surface;
   a first insulating film formed over the substrate;
   a gate line buried in the first insulating film;
   a second insulating film formed over the first insulating film; and
   a thin film transistor formed over the second insulating film,

   wherein the gate line is electrically connected to a gate electrode of the thin film transistor.

12. A display device according to claim 11, wherein the gate line comprises at least one material selected

from the group consisting of copper, silver, gold and an alloy thereof.

13. A display device according to claim 11, wherein the display device is incorporated into an electronic apparatus selected from the group consisting of s video camera, a digital camera, a head-mount display, a car navigator, a projector, a car stereo, a personal computer, a personal digital assistant.

14. A display device comprising:

a substrate having an insulating surface;
a first insulating film formed over the substrate;
a source line buried in the first insulating film;
a second insulating film formed over the first insulating film; and
a thin film transistor formed over the second insulating film,

wherein the source line is electrically connected to a source region of the thin film transistor.

15. A display device according to claim 14, wherein the source line comprises at least one material selected from the group consisting of copper, silver, gold and an alloy thereof.

16. A display device according to claim 14, wherein the display device is incorporated into an electronic apparatus selected from the group consisting of s video camera, a digital camera, a head-mount display, a car navigator, a projector, a car stereo, a personal computer, a personal digital assistant.

17. A display device comprising:

a substrate having an insulating surface;
a first insulating film formed over the substrate;
a power supply line buried in the first insulating film;
a second insulating film formed over the first insulating film; and
a thin film transistor formed over the second insulating film.

18. A display device according to claim 17, wherein the power supply line comprises at least one material selected from the group consisting of copper, silver, gold and an alloy thereof.

19. A display device according to claim 17, wherein the display device is incorporated into an electronic apparatus selected from the group consisting of s video camera, a digital camera, a head-mount display, a car navigator, a projector, a car stereo, a personal computer, a personal digital assistant.

20. A method for manufacturing a light-emitting device comprising:

forming an etching-stop layer having an electric conductivity on an insulating surface;
forming a first insulating film covering the etching-stop layer;
etching the first insulating film to open an opening reaching the etching-stop layer;
forming a seed and carrying out plating to form a buried interconnection covering the opening;
planarizing a surface of the buried interconnection;
forming a second insulating film containing aluminum;
forming a third insulating film on the second insulating film;
forming a semiconductor layer on the third insulating film;
forming a fourth insulating film on the semiconductor layer;
forming a gate electrode on the fourth insulating film;
forming a line connecting to the semiconductor layer and a line connecting the buried interconnection;
forming a first electrode; and
forming a layer containing organic compound on the first electrode and a second electrode on the layer containing organic compound.

21. A method for manufacturing a light-emitting device according to claim 20, wherein the buried interconnection is a power supply line.

22. A method for manufacturing a light-emitting device according to claim 20, wherein the buried interconnection comprises at least one material selected from the group consisting of copper, silver, gold and an alloy thereof.

23. A method for manufacturing a liquid-crystal display device comprising:

forming an etching-stop layer having an electric conductivity on an insulating surface;
forming a first insulating film covering the etching-stop layer;
etching the first insulating film to open an opening reaching the etching-stop layer;
forming a seed and carrying out plating to form a buried interconnection covering the opening;
planarizing a surface of the buried interconnection;
forming a second insulating film containing aluminum;
forming a third insulating film on the second insulating film;

forming a semiconductor layer on the third insulating film;
forming a fourth insulating film on the semiconductor layer;
forming a gate electrode on the fourth insulating film; and
forming a source line connected to the semiconductor layer and a line connecting between the buried interconnection and the gate line.

24. A method for manufacturing a liquid-crystal display device according to claim 23, wherein the buried interconnection is a gate line.

25. A method for manufacturing a liquid-crystal display device according to claim 23, wherein the buried interconnection comprises at least one material selected from the group consisting of copper, silver, gold and an alloy thereof.

Fig. 1A

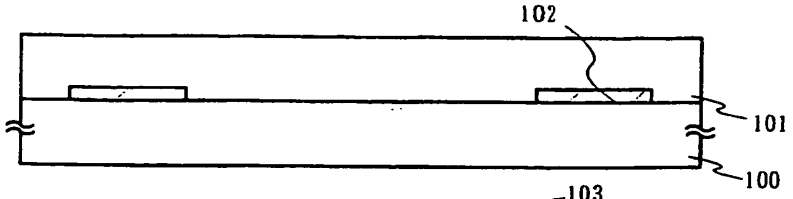


Fig. 1B

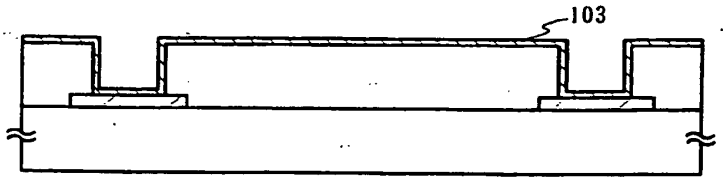


Fig. 1C

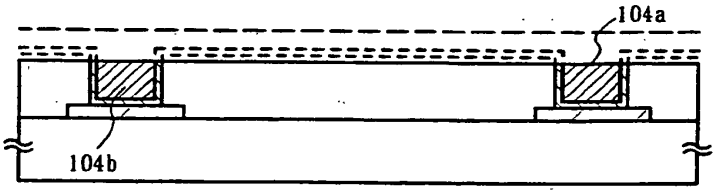


Fig. 1D

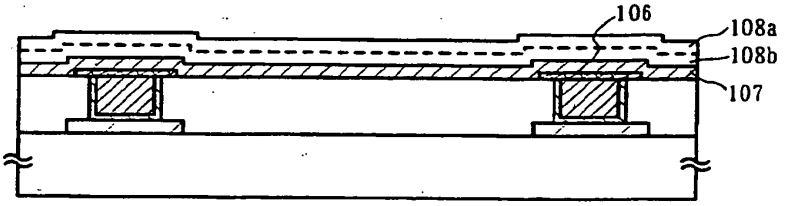


Fig. 1E

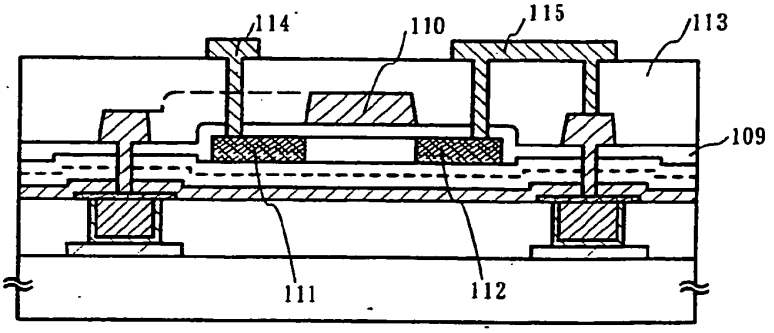


Fig. 2A

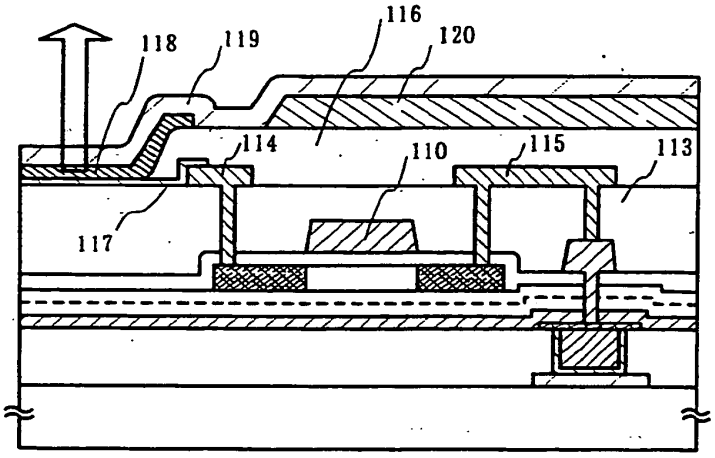
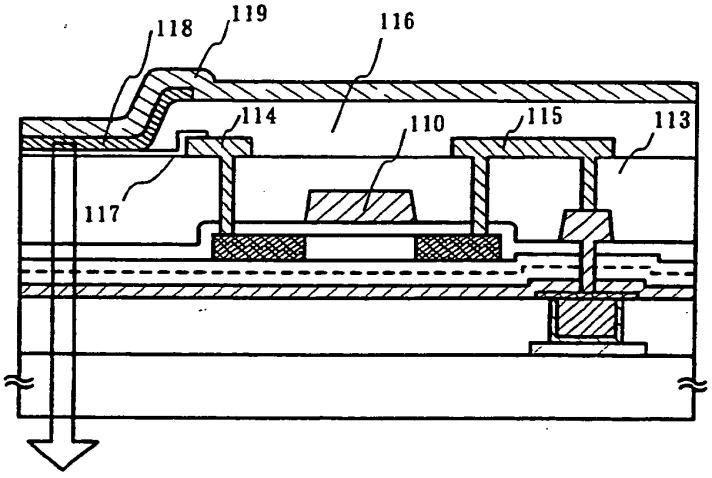


Fig. 2B



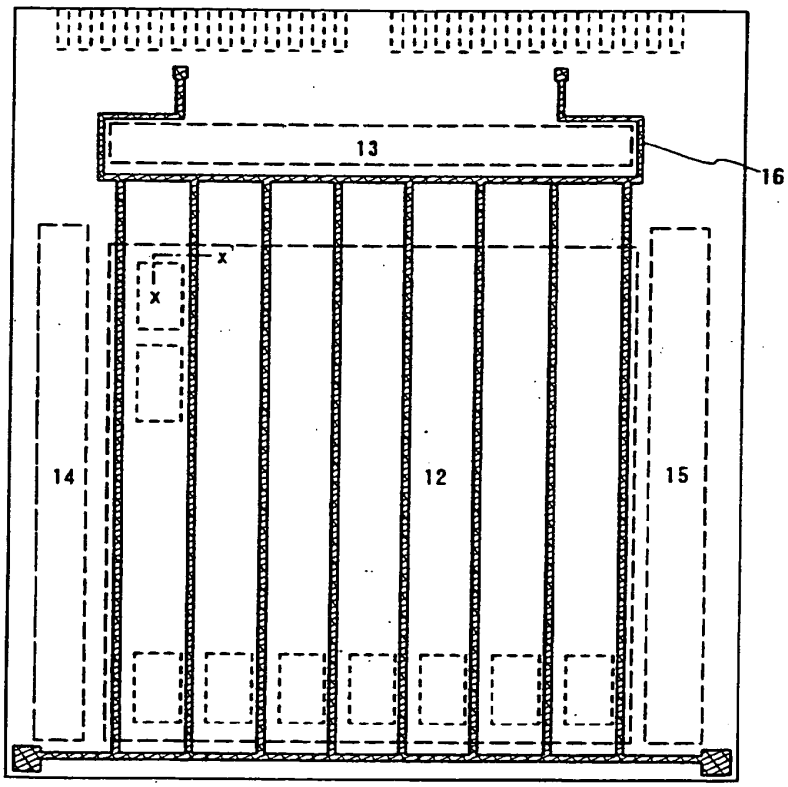


Fig. 3

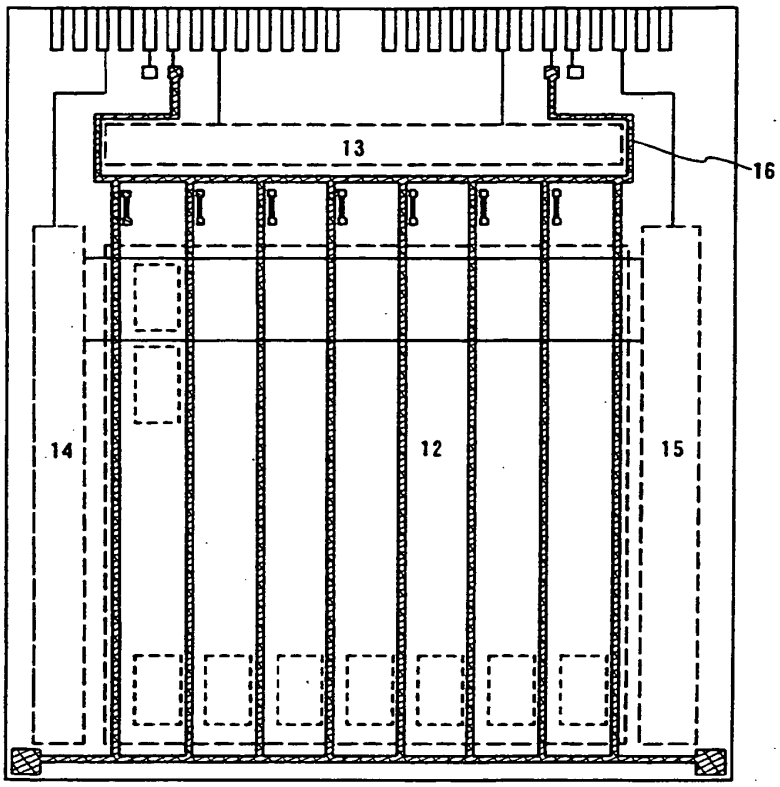


Fig. 4

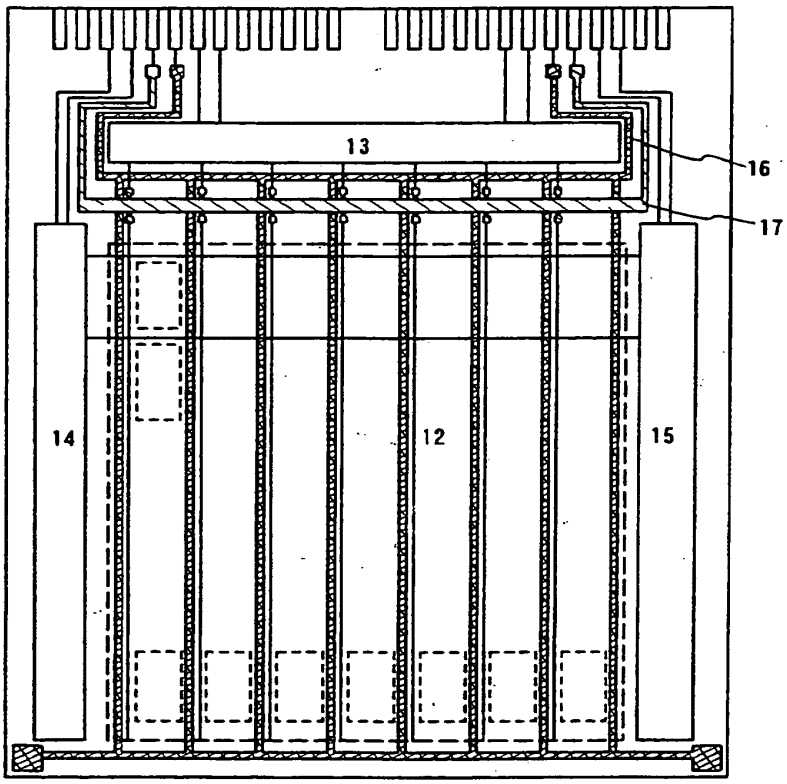


Fig. 5

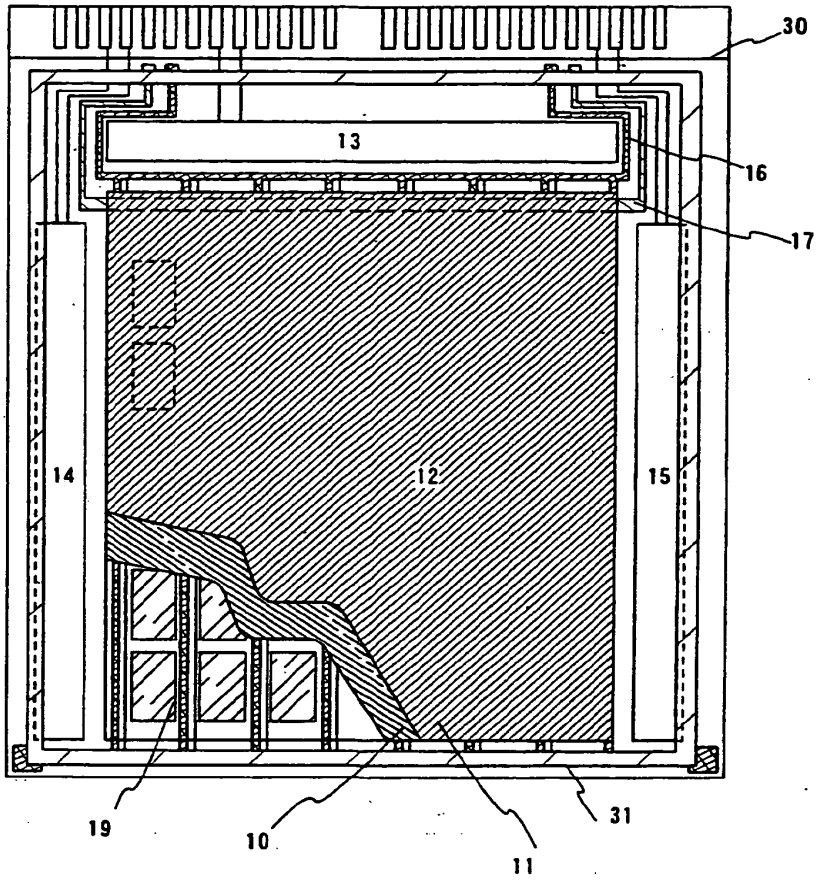


Fig. 6

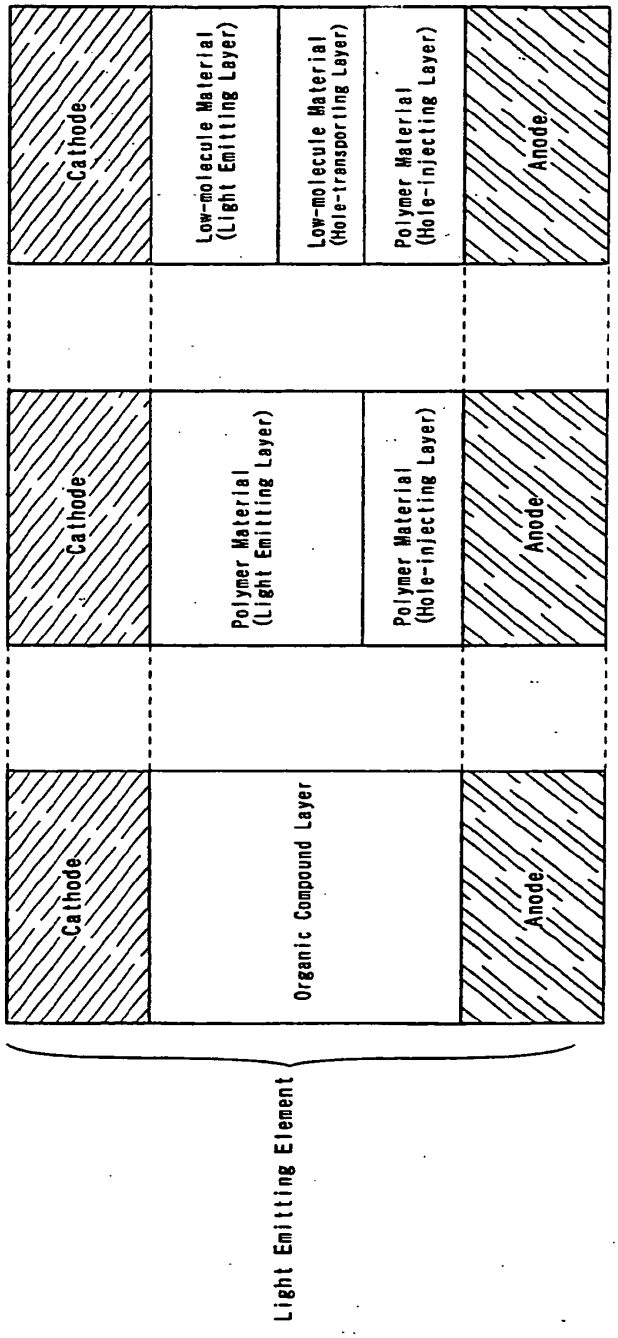


Fig. 7A

Fig. 7B

Fig. 7C

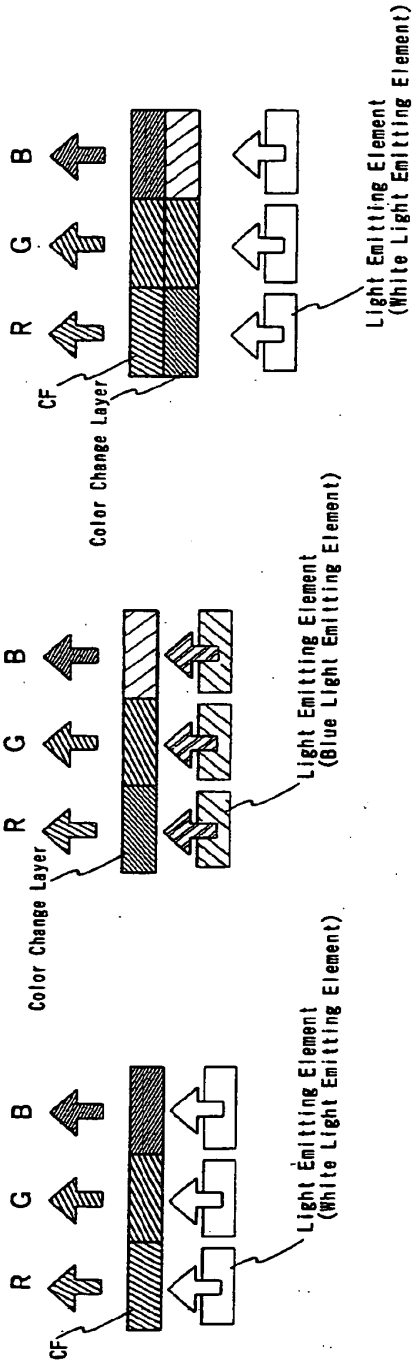


Fig. 8A
(White Color + CF Method)

Fig. 8B
(Blue Color + Color Change Layer)

Fig. 8C
(White Color+Color Change Layer+CF)

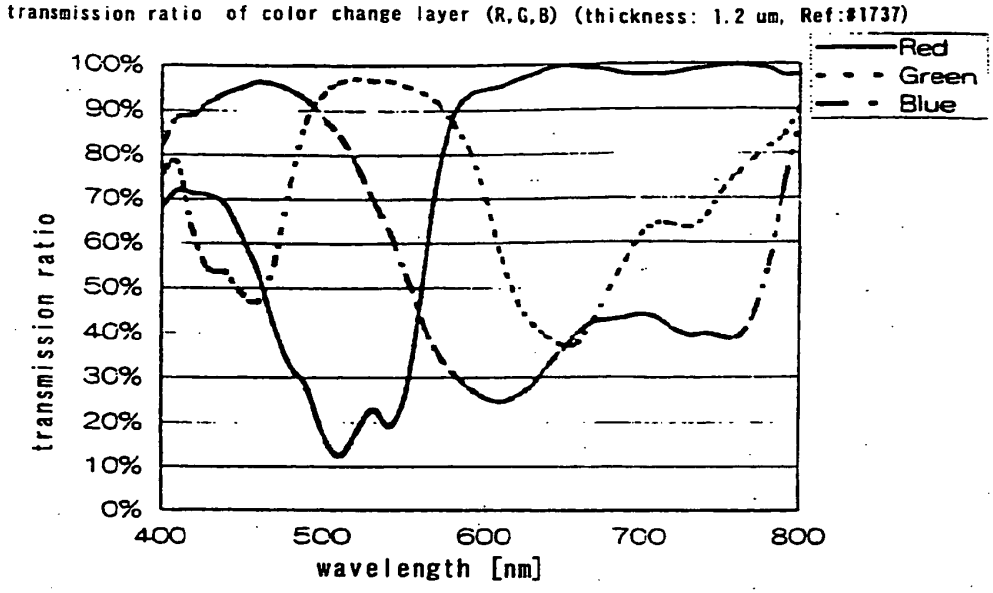


Fig. 9

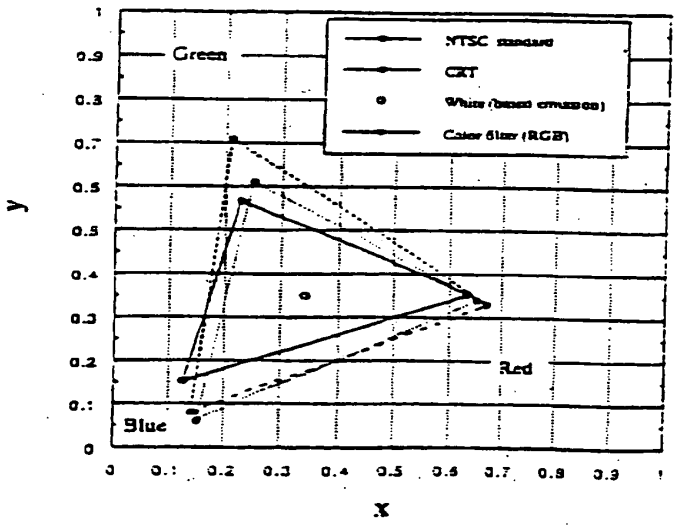


Fig. 10

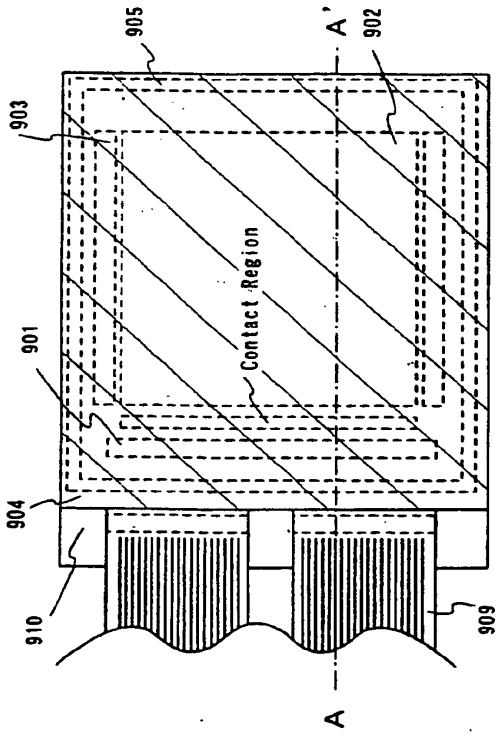


Fig. 11A

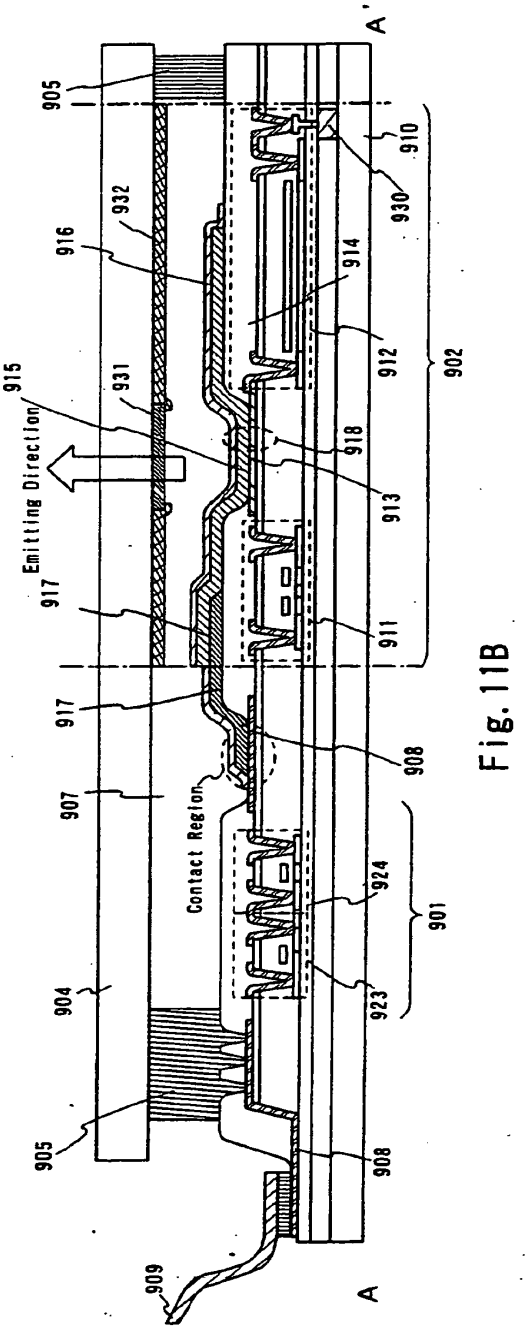


Fig. 11B

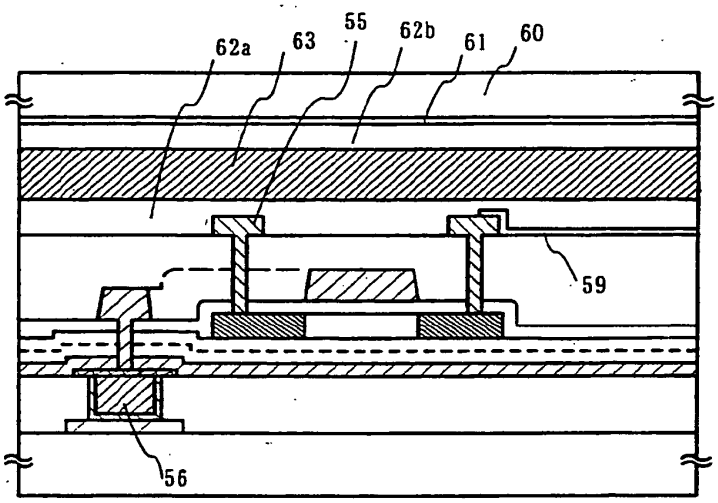


Fig. 12

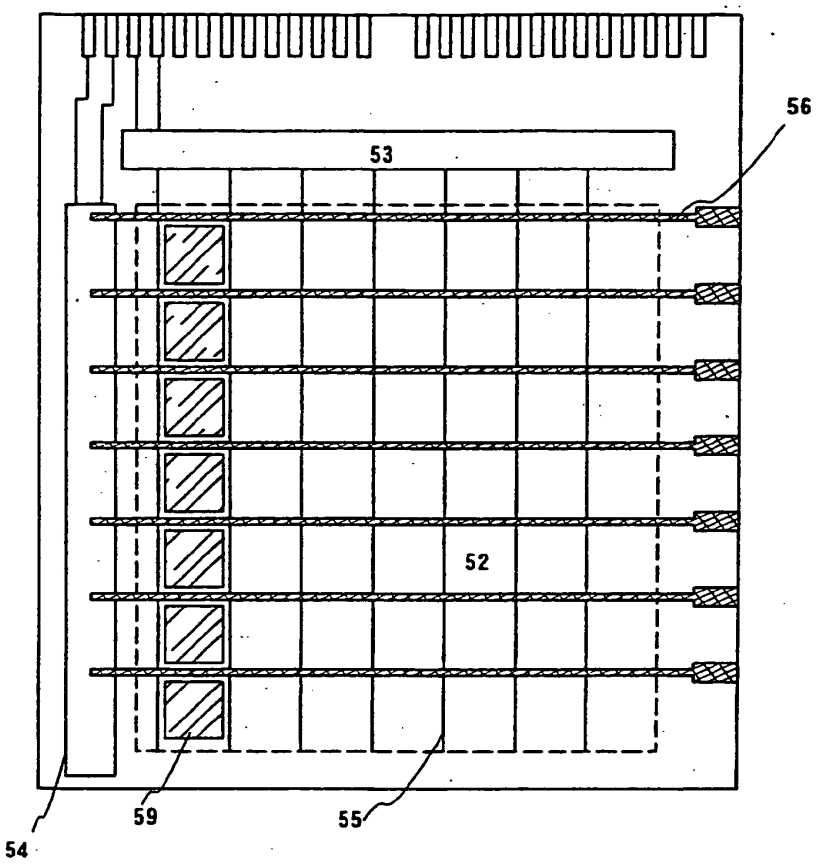


Fig. 13

Fig. 14A

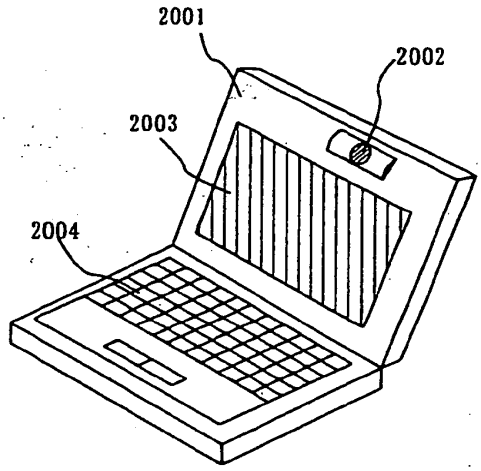


Fig. 14B

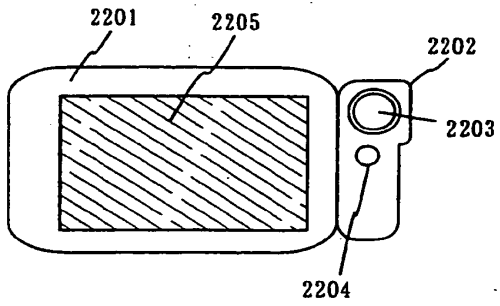


Fig. 14C

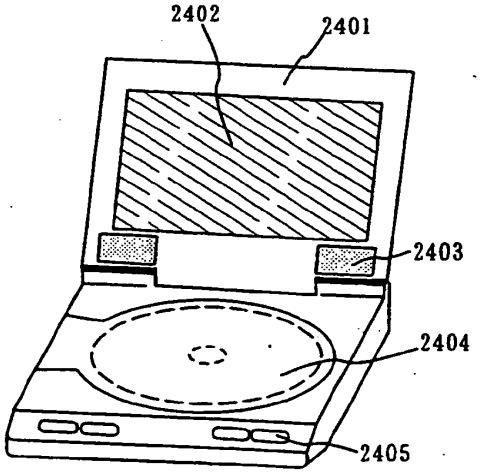


Fig. 15A

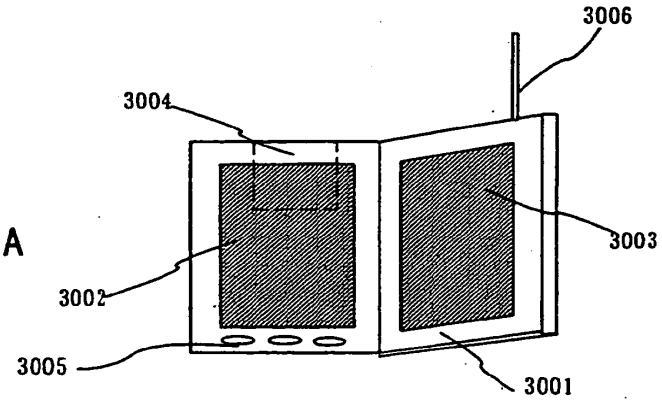
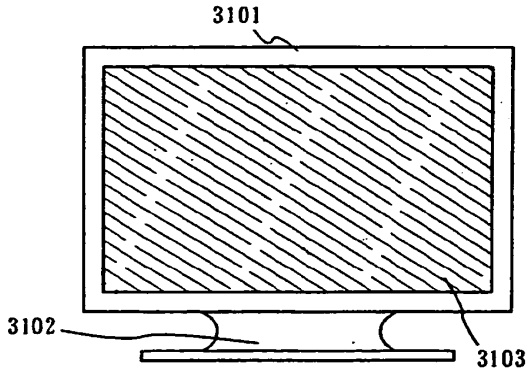


Fig. 15B



European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 03 00 6774

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X Y	US 6 275 275 B1 (HA YONG MIN) 14 August 2001 (2001-08-14) * column 5, line 20 - column 7, line 7; figures 5,6A-6F * ---	1,3,6,7, 9,10 1-25	H01L21/768 H01L21/84 H01L27/12
Y	"TFT/LCD DAMASCENE SCAN LINES" IBM TECHNICAL DISCLOSURE BULLETIN, IBM CORP. NEW YORK, US, vol. 32, no. 3B, 1 August 1989 (1989-08-01), pages 67-68, XP000029920 ISSN: 0018-8689 * the whole document * ---	7-25	
Y	LU M H ET AL: "Amorphous silicon TFT active-matrix OLED pixel" LASERS AND ELECTRO-OPTICS SOCIETY ANNUAL MEETING, 1998. LEOS '98. IEEE ORLANDO, FL, USA 1-4 DEC. 1998, PISCATAWAY, NJ, USA,IEEE, US, 1 December 1998 (1998-12-01), pages 130-131, XP010317344 ISBN: 0-7803-4947-4 * the whole document * ---	1-6, 11-25	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H01L
P,X	US 2003/020065 A1 (HONDA TATSUYA) 30 January 2003 (2003-01-30) * paragraph [0053] - paragraph [0080]; figures 6B,7A,7B,8,9 * * paragraph [0109] - paragraph [0114]; figures 11A-11F * -----	1,3,6-8, 10	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	14 July 2003	Agne, M

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 03 00 6774

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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14-07-2003

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EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

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(25) Filing Language: English

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(74) Agents: **SUZUYE, Takehiko** et al.; c/o SUZUYE & SUZUYE, 7-2, Kasumigaseki 3-chome, Chiyoda-ku, Tokyo 100-0013 (JP).

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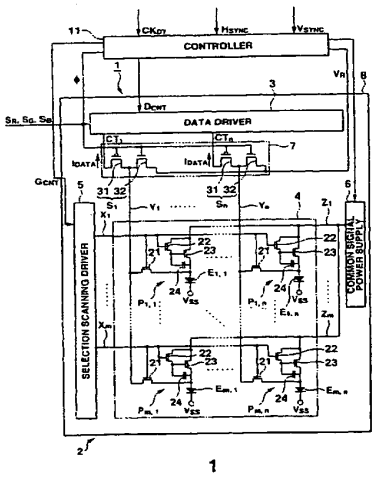
Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

[Continued on next page]

(54) Title: DISPLAY DEVICE AND DISPLAY DEVICE DRIVING METHOD



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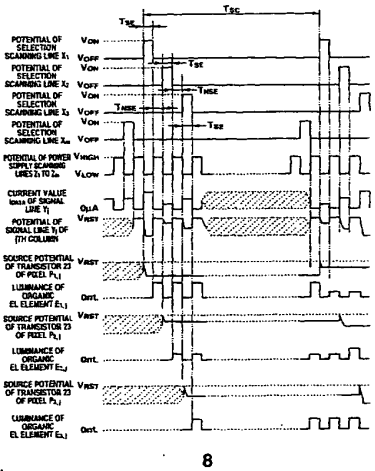

8

(57) Abstract: A display device includes a plurality of scanning lines(X_1- X_m), a plurality of signal lines (Y_1 - Y_n), a scanning driver (5) which sequentially supplies to the scanning lines selection signals that select the scanning lines, a data driver (3) which supplies a designation current to the plurality of signal lines duringwithin a selection period when the scanning lines are being selected, a plurality of pixel circuits which supplies a driving current corresponding to a current value of the designation current that flows to the signal lines, a plurality of optical elements (E1,1 - $E_{m,n}$) which emit light in accordance with the driving current supplied by the plurality of pixel circuits and a power supply (6) which outputs to the plurality of pixel circuits a driving current reference voltage to supply the driving current.

WO 2004/019314 A1

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

DESCRIPTION

DISPLAY DEVICE AND DISPLAY DEVICE DRIVING METHOD

Technical Field

The present invention relates to a display device and a display device driving method.

Background Art

Liquid crystal displays are generally classified into active matrix driving liquid crystal displays and simple matrix driving liquid crystal displays. The active matrix driving liquid crystal display displays an image having a higher luminance, higher contrast, and higher resolution as compared to the simple matrix driving liquid crystal display. In the active matrix driving liquid crystal display, a liquid crystal element which also functions as a capacitor and a transistor which activates the liquid crystal element are arranged for each pixel. In the active matrix driving liquid crystal display, a selection signal is input from a scanning driver serving as a shift register to a scanning line so that the scanning line is selected. At this time, when a voltage having a level representing a luminance is applied from a data driver to a signal line, the voltage is applied to the liquid crystal element through the transistor. Even when the transistor is turned off during a period from

the end of signal input to the scanning line to the next signal input, the voltage level is held until the next signal is input to the scanning line because the liquid crystal element functions as a capacitor. As described above, while the signal is input to the scanning line, the light transmittance of the liquid crystal element is newly refreshed. Light from a backlight passes through the liquid crystal element at the refreshed light transmittance so that the gray level of the liquid crystal display is expressed.

On the other hand, an organic EL (ElectroLuminescence) display which uses organic EL elements as spontaneous optical elements requires no backlight, unlike liquid crystal displays. Hence, the organic EL display is optimum for a thin display. In addition, the organic EL display has no limitation on the angle of field, unlike liquid crystal displays. For this reason, practical utilization of organic EL displays as next-generation display devices is greatly expected.

From the viewpoint of a high luminance, high contrast, and high resolution, voltage-controlled active matrix driving schemes have been developed not only for liquid crystal displays but also for organic EL displays. However, the capacity of an organic EL element is much smaller than that of a liquid crystal element so a current flows to the organic EL element

itself. To hold a voltage, the number of transistors increases. This leads to an increase in complexity of a circuit constituted by transistors.

In a transistor, generally, the channel resistance changes due to a change in ambient temperature or long-time use. For this reason, the gate threshold voltage changes over time or varies between transistors. It is therefore difficult to uniquely designate the current level to be supplied to an organic EL element on the basis of the gate voltage level of a switching transistor by changing the value of the voltage to be applied to the gate electrode of the transistor and thus changing the level of the current to be supplied to the organic EL element. In other words, the level of the current to be supplied can hardly be uniquely designated by changing the value of the voltage to be applied to the gate electrode of the transistor and thus changing the luminance of the organic EL element. That is, even when a gate voltage of the same level is applied to the transistors of a plurality of pixels, the organic EL elements of the plurality of pixels may have different emission luminances. This may cause a variation in luminance on the display screen.

Disclosure of Invention

It is an object of the present invention to provide a display device and a display device driving

method, which allow stable display on the basis of a simple driving principle.

In order to solve the above problems, according to an aspect of the present invention, there is provided a display device comprising:

a plurality of scanning lines (e.g., selection scanning lines X_1 to X_m);

a plurality of signal lines (e.g., signal lines Y_1 to Y_n);

a scanning driver (e.g., a selection scanning driver 5) which sequentially supplies to the scanning lines selection signals that select the scanning lines;

a data driver (e.g., a data driver 3) which supplies a designation current (e.g., a gray level designation current I_{DATA}) to the plurality of signal lines within a selection period (e.g., a selection period T_{SE}) when the scanning lines are being selected;

a plurality of pixel circuits (e.g., pixel circuits $D_{1,1}$ to $D_{m,n}$) which supplies a driving current corresponding to a current value of the designation current that flows to the signal lines;

a plurality of optical elements (e.g., light-emitting elements $E_{1,1}$ to $E_{m,n}$) which emit light in accordance with the driving current supplied by the plurality of pixel circuits; and

a power supply (e.g., a common signal power supply 6) which outputs to the plurality of pixel circuits a

driving current reference voltage (e.g., a voltage V_{HIGH}) to supply the driving current.

In the above device, in accordance with the timing when the power supply outputs the driving current reference voltage, the plurality of pixel circuits supply the driving current in accordance with the current value of the designation current that flows within each selection period. Accordingly, the optical elements emit light.

Hence, when the power supply outputs the driving current reference voltage from the end of the selection period of a predetermined scanning line till the beginning of the selection period of the next scanning line, a driving current corresponding to both an optical element corresponding to the predetermined scanning line and an optical element corresponding to the next scanning line flows. Hence, the optical elements can emit light at a desired luminance.

When the power supply outputs the driving current reference voltage to the pixel circuit at once after all the scanning lines are selected, all the optical elements can emit light.

When a reset voltage is output to the plurality of signal lines within a period when none of the plurality of optical elements are selected, the signal lines reset charges stored in the preceding selection period. For this reason, the parasitic capacitance of the

signal lines can be quickly charged within the next selection period so that even when a designation current having a smaller current value is supplied, the current value of the designation current can rapidly be set in the steady state. Hence, even an optical element such as an organic EL element whose luminance is modulated by a small current on the μA order is allowed to quickly display multiple gray level luminances.

Brief Description of Drawings

FIG. 1 is a view showing an organic EL display applied as a display device according to the first embodiment of the present invention;

FIG. 2 is a plan view showing a pixel shown in FIG. 1, in which an oxide insulating film, channel protective insulating film, and common electrode are omitted to help understanding;

FIG. 3 is a sectional view taken along a line III - III in FIG. 2;

FIG. 4 is a sectional view taken along a line IV - IV in FIG. 2;

FIG. 5 is a sectional view taken along a line V - V in FIG. 2;

FIG. 6 is an equivalent circuit diagram of four adjacent pixels;

FIG. 7 is a graph showing the current vs. voltage characteristic of an N-channel field effect transistor

used in the first embodiment;

FIG. 8 is a timing chart showing the levels of signals in the apparatus according to the first embodiment;

FIG. 9A is a view showing a voltage state when no switching circuit is arranged, and a gray level designation current with the maximum current value is supplied across the drain and source of a transistor and a signal line during the selection period of the ith row;

FIG. 9B is a view showing a voltage state when a switching circuit is arranged, and a gray level designation current with the maximum current value is supplied across the drain and source of a transistor and a signal line during the selection period of the ith row;

FIG. 10 is a view showing an organic EL display applied as a display device according to the second embodiment of the present invention, in which a common signal power supply is arranged in a controller;

FIG. 11 is a view showing an organic EL display applied as a display device according to the third embodiment of the present invention, in which the drain of the transistor of a pixel circuit is connected to a selection scanning line;

FIGS. 12A and 12B are equivalent circuit diagrams showing adjacent pixels in the third embodiment to

indicate current flows in different operation periods; and

FIG. 13 is a timing chart showing the levels of signals in the apparatus according to the third embodiment.

Best Mode for Carrying Out the Invention

Detailed embodiments of the present invention will be described below with reference to the accompanying drawings. The scope and spirit of the display device or panel are not limited to the illustrated embodiments.

[First Embodiment]

FIG. 1 is a view showing an organic EL display to which the present invention is applied. An organic EL display 1 comprises, as a basic arrangement, an organic EL display panel 2, data driver 3, selection scanning driver 5, common signal power supply 6, switching circuit 7, and controller 11.

In the organic EL display panel 2, a display section 4 on which an image is actually displayed is formed on a transparent substrate 8. The data driver 3, selection scanning driver 5, common signal power supply 6, and switching circuit 7 are arranged around the display section 4. The data driver 3, selection scanning driver 5, and common signal power supply 6 may be arranged either on the transparent substrate 8 or on a flexible circuit board arranged around the

transparent substrate 8.

In the display section 4, (m × n) pixels $P_{1,1}$ to $P_{m,n}$ (m and n are arbitrary natural numbers) are arranged in a matrix on the transparent substrate 8. In the column direction, i.e., in the vertical direction, m pixels $P_{1,j}$ to $P_{m,j}$ (j is an arbitrary natural number; $1 \leqq j \leqq n$) are arrayed. In the row direction, i.e., in the horizontal direction, n pixels $P_{i,1}$ to $P_{i,n}$ (i is an arbitrary natural number; $1 \leqq i \leqq m$) are arrayed. That is, a pixel which exists on the ith line (i.e., the ith row) from the upper side in the vertical direction and the jth line (i.e., the jth column) from the left side in the horizontal direction is defined as a pixel $P_{i,j}$.

In the display section 4, m selection scanning lines X_1 to X_m running in the row direction are parallelly arranged in the column direction on the transparent substrate 8. In addition, m common signal supply lines Z_1 to Z_m running in the row direction are parallelly arranged in the column direction on the transparent substrate 8 in correspondence with the selection scanning lines X_1 to X_m. Each common signal supply line Z_k ($1 \leqq k \leqq m-1$) is inserted between the selection scanning lines X_k and X_{k+1}. The selection scanning line X_m is inserted between the common signal supply lines Z_{m-1} and Z_m. In addition, n signal lines Y_1 to Y_n running in the column direction are parallelly

arranged in the row direction on the transparent substrate 8. The selection scanning lines X_1 to X_m, common signal supply lines Z_1 to Z_m, and signal lines Y_1 to Y_n are insulated from each other by intervening insulating films. A selection scanning line X_i and common signal supply line Z_i are connected to $\underline{n}$ pixels $P_{i,1}$ to $P_{i,n}$ arrayed in the row direction. A signal line Y_j is connected to $\underline{m}$ pixels $P_{i,j}$ to $P_{m,j}$ arrayed in the column direction. The pixel $P_{i,j}$ is arranged at a portion surrounded by the selection scanning line X_i, common signal supply line Z_i, and signal line Y_j. The selection scanning lines X_1 to X_m are connected to the output terminals of the selection scanning driver 5. The common signal supply lines Z_1 to Z_m are rendered conductive to each other and connected to the output terminal of the common signal power supply 6. That is, the same signal is output to the common signal supply lines Z_1 to Z_m.

The pixel $P_{i,j}$ will be described next with reference to FIGS. 2 to 6. FIG. 2 is a plan view showing the pixel $P_{i,j}$. To help understanding, an oxide insulating film 41, channel protective insulating film 45, and common electrode 53 (to be described later) are omitted. FIG. 3 is a sectional view taken along a line III - III in FIG. 2. FIG. 4 is a sectional view taken along a line IV - IV in FIG. 2. FIG. 5 is a sectional view taken along a line V - V in

FIG. 2.

FIG. 6 is an equivalent circuit diagram of four adjacent pixels $P_{i,j}$, $P_{i+1,j}$, $P_{i,j+1}$, and $P_{i+1,j+1}$.

The pixel $P_{i,j}$ is constituted by a light-emitting element $E_{i,j}$ which emits light with a luminance (nt. = cd/m^2) corresponding to the current value of the driving current and a pixel circuit $D_{i,j}$ which is arranged around the light-emitting element $E_{i,j}$ and drives the light-emitting element $E_{i,j}$. The pixel circuit $D_{i,j}$ holds the current value of a current that flows to the light-emitting element $E_{i,j}$ during a predetermined light-emitting period on the basis of a voltage signal and current output from the data driver 3, selection scanning driver 5, power supply scanning driver 6, and switching circuit 7. With this operation, the luminance of the light-emitting element $E_{i,j}$ is held at a predetermined value during a predetermined period.

The light-emitting element $E_{i,j}$ is made of an organic EL element. The light-emitting element $E_{i,j}$ has a multilayered structure formed by sequentially stacking a pixel electrode 51, an organic EL layer 52, and the common electrode 53. The pixel electrode 51 functions as an anode on the transparent substrate 8. The organic EL layer 52 has a function of receiving holes and electrons by an electric field and a function of transporting holes and electrons. The organic EL

layer 52 has a recombination region where the transported holes and electrons are recombined and a light-emitting region where light is emitted by capturing excitons generated upon recombination. The organic EL layer 52 functions as a light-emitting layer in a broad sense. The common electrode 53 functions as a cathode.

The pixel electrode 51 is patterned and separated for each pixel $P_{i,j}$ in each surrounded region surrounded by the signal lines Y_1 to Y_n and selection scanning lines X_1 to X_m. The peripheral edge of the pixel electrode 51 is covered with an interlayer dielectric film 54 which has a layer of silicon nitride or silicon oxide that covers three transistors 21, 22, and 23 of the pixel circuit $D_{i,j}$. The upper surface at the center of the pixel electrode 51 is exposed through a contact hole 55 in the interlayer dielectric film 54. The interlayer dielectric film 54 may also have a second layer formed of an insulting film of polyimide or the like on the first layer of silicon nitride or silicon oxide.

The pixel electrode 51 has conductivity and transmittance to visible light. The pixel electrode 51 preferably has a relatively high work function and efficiently injects holes into the organic EL layer 52. For example, the pixel electrode 51 contains, as a principal component, indium tin oxide (ITO), indium

zinc oxide, indium oxide (In_2O_3), tin oxide (SnO_2), or zinc oxide (ZnO).

The organic EL layer 52 is formed on each pixel electrode 51. The organic EL layer 52 is also patterned for each pixel $P_{i,j}$. The organic EL layer 52 contains a light-emitting material (phosphor) as an organic compound. The light-emitting material may be either a polymeric material or a low molecular weight material. The organic EL layer 52 may have, e.g., a two-layered structure in which a hole transport layer 52A and a light-emitting layer 52B in a narrow sense are formed sequentially from the side of the pixel electrode 51, as shown in FIG. 3. The light-emitting layer 52B has a recombination region where holes and electrons are recombined and a light-emitting region where light is emitted by capturing excitons generated upon recombination. Alternatively, the organic EL layer 52 may have a three-layered structure in which a hole transport layer, a light-emitting layer in a narrow sense, and electron transport layer are formed sequentially from the side of the pixel electrode 51. The organic EL layer 52 may have a single-layered structure including a light-emitting layer in a narrow sense. The organic EL layer 52 may also have a multilayered structure formed by interposing an electron or hole injection layer between appropriate layers of the above layer structure. The organic EL

layer 52 may have any other layer structure.

The organic EL display panel 2 is capable of full-color display or multi-color display. In this case, the organic EL layer 52 of each of the pixels $P_{i,1}$ to $P_{i,n}$ is formed of a light-emitting layer in a broad sense, which has a function of emitting one of, e.g., red light, green light, and blue light. That is, when the pixels $P_{i,1}$ to $P_{i,n}$ selectively emit red, green, and blue light, a color tone is displayed by appropriately synthesizing the colors.

The organic EL layer 52 is preferably made of an organic compound that is electronically neutral. In this case, holes and electrons are injected and transported in the organic EL layer 52 in good balance. In addition, an electron transportable substance may be appropriately mixed into the light-emitting layer in a narrow sense. A hole transportable substance may be appropriately mixed into the light-emitting layer in a narrow sense. An electron transportable substance and a hole transportable substance may be appropriately mixed into the light-emitting layer in a narrow sense. A charge transport layer serving as an electron transport layer or a hole transport layer may be caused to function as a recombination region. Light may be emitted by mixing phosphor into the charge transport layer.

The common electrode 53 formed on the organic EL

layer 52 is a single electrode connected to all the pixels $P_{1,1}$ to $P_{m,n}$. Alternately, the common electrode 53 may comprise a plurality of stripe-shaped electrodes connected to the respective columns. More specifically, the common electrode 53 may comprise a stripe common electrode connected to a group of pixels $P_{1,h-1}$ to $P_{m,h-1}$ (h is an arbitrary natural number; $2 \leqq h \leqq n$) in the column direction, a stripe common electrode connected to a group of pixels $P_{1,h}$ to $P_{m,h}$. In this manner, the common electrode 53 comprises a plurality of stripe-shaped electrodes each connected to each column. Alternatively, the common electrode 53 may comprise a stripe common electrode connected to a group of pixels $P_{g-1,1}$ to $P_{g-1,n}$ (g is an arbitrary natural number; $2 \leqq g \leqq m$) in the row direction, a stripe common electrode connected to a group of pixels $P_{g,1}$ to $P_{g,n}$,.... In this manner, the common electrode 53 comprises a plurality of stripe-shaped electrodes connected to each row.

In any case, the common electrode 53 is electrically insulated from the selection scanning line X_i, signal line Y_j, and common signal supply line Z_i. The common electrode 53 is made of a material having a low work function. For example, the common electrode 53 is made of a single element or an alloy containing at least one of indium, magnesium, calcium, lithium, barium, and rare-earth metals. The common electrode 53

may have a multilayered structure formed by stacking a plurality of layers made of the above materials. More specifically, the multilayered structure may include a high purity barium layer which has a low work function and is formed on the side of the interface that is in contact with the organic EL layer 52, and an aluminum layer that covers the barium layer. Alternatively, the multilayered structure may have a lithium layer on the lower side and an aluminum layer on the upper side. When a transparent electrode is used as the pixel electrode 51, and light emitted from the organic EL layer 52 of the organic EL display panel 2 should exit from the side of the transparent substrate 8 through the pixel electrode 51, the common electrode 53 preferably shields the light emitted from the organic EL layer 52. More preferably, the common electrode 53 has a high reflectance against the light emitted from the organic EL layer 52.

As described above, in the light-emitting element $E_{i,j}$ having a multilayered structure, when a forward bias voltage is applied between the pixel electrode 51 and the common electrode 53, holes are injected from the pixel electrode 51 to the organic EL layer 52 while electrons are injected from the common electrode 53 to the organic EL layer 52. The holes and electrons are transported in the organic EL layer 52. When the holes and electrons are recombined in the organic EL layer

52, excitons are generated. The excitons excite the organic EL layer 52. The organic EL layer 52 emits light.

The emission luminance (unit: nt. = cd/m^2) of the light-emitting element $E_{i,j}$ depends on the current value of the current that flows to the light-emitting element $E_{i,j}$. To maintain a predetermined emission luminance of the light-emitting element $E_{i,j}$ during the light-emitting of the light-emitting element $E_{i,j}$ or obtain an emission luminance corresponding to the current value of a gray level designation current I_{DATA} drawn from the data driver 3, the pixel circuit $D_{i,j}$ is arranged around the light-emitting element $E_{i,j}$ of each pixel $P_{i,j}$. The pixel circuit $D_{i,j}$ controls the current value of the light-emitting element $E_{i,j}$.

Each pixel circuit $D_{i,j}$ comprises three transistors 21, 22, and 23 and a capacitor 24. Each transistor is formed of a field effect thin film transistor (TFT) having an N-channel MOS structure.

Each transistor 21 is an MOS field effect transistor constituted by a gate electrode 21g, gate insulating film 42, semiconductor layer 43, source electrode 21s, and drain electrode 21d. Each transistor 22 is an MOS field effect transistor constituted by a gate electrode 22g, gate insulating film 42, semiconductor layer 43, source electrode 22s, and drain electrode 22d. Each transistor 23 is

constituted by a gate electrode 23g, gate insulating film 42, semiconductor layer 43, source electrode 23s, and drain electrode 23d.

More specifically, as shown in FIG. 3, the first transistor 21 is a reverse stagger type transistor comprising the gate electrode 21g, oxide insulating film 41, gate insulating film 42, island-shaped semiconductor layer 43, channel protective insulating film 45, impurity-doped semiconductor layers 44, source electrode 21s, and drain electrode 21d. The gate electrode 21g is made of aluminum and formed on the transparent substrate 8. The oxide insulating film 41 is formed by anodizing aluminum that covers the gate electrode 21g. The gate insulating film 42 is made of silicon nitride or silicon oxide and covers the oxide insulating film 41. The semiconductor layer 43 is formed on the gate insulating film 42. The channel protective insulating film 45 is made of silicon nitride and formed on the gate insulating film 42. The impurity-doped semiconductor layers 44 are made of n^+-silicon and formed at both ends of the semiconductor layer 43. The source electrode 21s and drain electrode 21d are made of a material selected from chromium, a chromium alloy, aluminum and an aluminum alloy, and formed on the impurity semiconductor layers 44.

The second and third transistors 22 and 23 have the same structure as that of the first transistor 21

described above. However, the shapes, sizes, and dimensions of the transistors 21, 22, and 23, and the channel widths and channel lengths of the semiconductor layers 43 are appropriately set in accordance with the functions of the transistors 21, 22, and 23.

The transistors 21, 22, and 23 may be formed simultaneously by the same process. In this case, the gate electrodes, oxide insulating films 41, gate insulating films 42, semiconductor layers 43, impurity semiconductor layers 44, source electrodes, and drain electrodes of the transistors 21, 22, and 23 have the same compositions.

Even when the semiconductor layers 43 of the transistors 21, 22, and 23 are made of amorphous silicon, they can be sufficiently driven. However, the semiconductor layers 43 may be made of polysilicon. The structures of the transistors 21, 22, and 23 are not limited to the reverse stagger type. Even a stagger type or coplanar type structure may be employed.

Each capacitor 24 is constituted by an electrode 24A, electrode 24B, and dielectric body. The electrode 24A is connected to the gate electrode 23g of the third transistor 23. The electrode 24B is connected to the source electrode 23s of the transistor 23. The dielectric body has the gate insulating film 42 interposed between the electrodes 24A and 24B. The

capacitor 24 stores charges between the source electrode 23s and the drain electrode 23d of the transistor 23.

As shown in FIG. 6, in the second transistor 22 of each of the pixel circuit $D_{i,1}$ to $D_{i,n}$ of the ith row, the gate electrode 22g is connected to the selection scanning line X_i of the ith row. The drain electrode 22d is connected to the common signal supply line Z_i of the ith row. As shown in FIG. 5, the drain electrode 23d of the third transistor 23 of each of the pixel circuit $D_{i,1}$ to $D_{i,n}$ of the ith row is connected to the common signal supply line Z_i of the ith row through a contact hole 26. The gate electrode 21g of the first transistor 21 of each of the pixel circuit $D_{i,1}$ to $D_{i,n}$ of the ith row is connected to the selection scanning line X_i of the ith row. The source electrode 21s of the transistor 21 of each of the pixel circuit $D_{1,j}$ to $D_{m,j}$ of the jth column is connected to the signal line Y_j of the jth column.

In each of the pixels $P_{1,1}$ to $P_{m,n}$, the source electrode 22s of the second transistor 22 is connected to the gate electrode 23g of the third transistor 23 through a contact hole 25 formed in the gate insulating film 42, as shown in FIG. 4. The source electrode 22s is also connected to one electrode of the capacitor 24. The source electrode 23s of the transistor 23 is connected to the other electrode of the capacitor 24

and also to the drain electrode 21d of the transistor 21. The source electrode 23s of the transistor 23, the other electrode of the capacitor 24, and the drain electrode 21d of the transistor 21 are connected to the pixel electrode 51 of the light-emitting element $E_{i,j}$. The voltage of the common electrode 53 of the light-emitting element $E_{i,j}$ is a reference voltage V_{SS}. In this embodiment, the common electrode 53 of all light-emitting elements $E_{1,1}$ to $E_{m,n}$ is grounded so that the reference voltage V_{SS} is set to 0 [V].

Protective films 43A formed by patterning the same film as that of the semiconductor layers 43 of the transistors 21 to 23 are arranged between the selection scanning line X_i and the signal line Y_j and between the common signal supply line Z_i and the signal line Y_j as well as the gate insulating film 42.

The controller 11 outputs a control signal group D_{CNT} including a data driver clock signal CK1, start signal ST1 and latch signal L to the data driver 3 on the basis of a dot clock signal CK_{DT}, horizontal sync signal H_{SYNC} and vertical sync signal V_{SYNC}, which are input from the outside. The controller 11 also outputs a control signal group G_{CNT} including a selection scanning driver clock signal CK2 and start signal ST2. The controller 11 also outputs a common signal clock signal CK3 to the common signal power supply 6. The controller 11 also supplies a reset voltage V_{RST} to the

switching circuit 7 and outputs a switching signal ϕ to the switching circuit 7.

More specifically, the data driver clock signal CK1 is a signal to sequentially shift the selected column in synchronism with the dot clock signal CK_{DT}. An 8-bit red digital gray level image signal S_R, green digital gray level image signal S_G, and blue digital gray level image signal S_B are received from an external circuit at the timing of the clock signal CK1. The start signal ST1 is a signal to return the selected column to the first column in synchronism with the horizontal sync signal H_{SYNC}. The latch signal L is a signal to parallelly supply the analog gray level designation current I_{DATA} based on an analog gray level designation signal to the signal lines Y_1 to Y_n. The analog gray level designation signal is obtained by causing the D/A converter in the data driver 3 to D/A-convert the data of one row, i.e., the red digital gray level image signal S_R, green digital gray level image signal S_G, and blue digital gray level image signal S_B which are received in correspondence with the pixels $P_{i,1}$ to $P_{i,n}$.

The selection scanning driver clock signal CK2 is a signal to sequentially shift the selected row in synchronism with the horizontal sync signal H_{SYNC}. The start signal ST2 is a signal to return the selected row to the first row in synchronism with the vertical sync

signal V_{SYNC}.

The common signal clock signal CK3 is a clock signal to output a common signal to the common signal supply lines Z_1 to Z_m.

The data driver 3, selection scanning driver 5, and common signal power supply 6 arranged around the display section 4 will be described next.

The selection scanning driver 5 is a so-called shift register in which m flip-flop circuits are connected in series. The driver 5 outputs a selection signal to the selection scanning lines X_1 to X_m. That is, in accordance with the selection scanning driver clock signal CK2 received from the controller 11, the selection scanning driver 5 sequentially outputs a selection signal of ON level (high level) to the selection scanning lines X_1 to X_m in this order (the selection scanning line X_1 follows the selection scanning line X_m), thereby sequentially selecting the selection scanning lines X_1 to X_m.

More specifically, as shown in FIG. 8, the selection scanning driver 5 individually applies, to the selection scanning lines X_1 to X_m, one of an ON voltage V_{ON} (e.g., much higher than the reference voltage V_{SS}) as a high-level selection signal and an OFF voltage V_{OFF} (e.g., equal to or lower than the reference voltage V_{SS}) as a low-level selection signal, thereby selecting each selection scanning line X_i at a

predetermined period.

During a selection period T_{SE} when the selection scanning line X_i is to be selected, the selection scanning driver 5 applies the ON voltage V_{ON} as a selection signal of ON level (high level) to the selection scanning line X_i. Accordingly, the transistors 21 and 22 (the transistors 21 and 22 of all the pixel circuits $D_{i,1}$ to $D_{i,n}$) connected to the selection scanning line X_i are turned on. When the first transistor 21 is turned on, the current that flows to the signal line Y_j can flow to the pixel circuit $D_{i,j}$. On the other hand, a non-selection period T_{NSE} is present from the end of the selection period T_{SE} of the selection scanning line X_i of the ith row till the beginning of the selection period T_{SE} of the selection scanning line X_{i+1} of the (i+1)th row. When the selection scanning driver 5 applies the OFF voltage V_{OFF} of low level to all the selection scanning lines X_1 to X_m, the transistors 21 and 22 of all the selection scanning lines X_1 to X_m are turned off. When the transistor 21 is turned off, supply of the gray level designation current I_{DATA} to the signal line Y_j is stopped. The period from the start of the selection period T_{SE} of the selection scanning line X_1 of the first row to the start of the next selection period T_{SE} of the selection scanning line X_1 of the first row is defined as one scanning period T_{SC}. The selection

periods T_{SE} of the selection scanning lines X_1 to X_m do not overlap each other.

The common signal power supply 6 is an independent power supply to supply a stable rated voltage to all the common signal supply lines Z_1 to Z_m. The common signal power supply 6 outputs a signal having a phase corresponding to the common signal clock signal CK3 to the common signal supply lines Z_1 to Z_m. While the selection scanning driver 5 is applying the ON voltage V_{ON} to one of all the selection scanning lines X_1 to X_m as a selection signal, i.e., during the selection period T_{SE}, the common signal power supply 6 outputs a low-level voltage V_{LOW} to all the common signal supply lines Z_1 to Z_m as a reference potential for the gray level designation current. During the non-selection period T_{NSE} from the end of the selection period T_{SE} of the selection scanning line X_i of the ith row till the beginning of the selection period T_{SE} of the selection scanning line X_{i+1} of the (i+1)th row, the common signal power supply 6 outputs a high-level voltage V_{HIGH} as a reference potential for a driving current. Hence, when the common signal from the common signal power supply 6 is the voltage V_{LOW}, the selection scanning driver 5 outputs the selection signal of the ON voltage V_{ON} to one selection scanning line X_i of the selection scanning lines X_1 to X_m. The selection scanning driver 5 outputs the selection signal of the

OFF voltage V_{OFF} to the selection scanning lines X_1 to X_m except the selection scanning line X_i. When the common signal output from the common signal power supply 6 drops from the high-level voltage V_{HIGH} to the low-level voltage V_{LOW}, the selection signal output from the selection scanning driver 5 to one of the selection scanning lines X_1 to X_m rises. When the common signal output from the common signal power supply 6 rises from the low-level voltage V_{LOW} to the high-level voltage V_{HIGH}, the selection signal of the ON voltage V_{ON} output from the selection driver 5 to one of the selection scanning lines X_1 to X_m falls.

The low-level voltage V_{LOW} (the reference voltage for the designation current) as the common signal output from the common signal power supply 6 is lower than the reference voltage V_{SS}. However, the low-level voltage V_{LOW} may be equal to the reference voltage V_{SS}. For this reason, even when the third transistors 23 of the pixels $P_{i,1}$ to $P_{i,n}$ are ON during the selection period T_{SE} of the ith row, a voltage of 0 V or a reverse bias voltage is applied between the anode and the cathode of each of the light-emitting elements $E_{i,1}$ to $E_{i,n}$ because the voltage V_{LOW} of the common signal is lower than the reference voltage V_{SS}. Hence, no current flows in the light-emitting elements $E_{i,1}$ to $E_{i,n}$. Light is not emitted. On the other hand, the high-level voltage (the reference voltage for the

driving current) V_{HIGH} output from the common signal power supply 6 is set to be higher than the reference voltage V_{SS}. That is, when the common signal is the voltage V_{HIGH}, the selection scanning driver 5 applies the OFF voltage V_{OFF} to all the selection scanning lines X_1 to X_m. The transistors 21 and 22 of all the pixels $P_{1,1}$ to $P_{m,n}$ are turned off. A forward bias is applied between the light-emitting elements $E_{1,1}$ to $E_{m,n}$ and the transistors 23 connected in series with the light-emitting elements $E_{1,1}$ to $E_{m,n}$.

The voltage V_{HIGH} will be described. FIG. 7 is a graph showing the current vs. voltage characteristic of the N-channel field effect transistor 23. Referring to FIG. 7, the abscissa represents the voltage value between the drain and the source. The ordinate represents the current value between the drain and the source. In the unsaturated region (the region where source-drain voltage V_{DS} < drain saturation threshold voltage V_{TH}: the drain saturation threshold voltage V_{TH} is a function of a gate-source voltage V_{GS} and is uniquely defined in accordance with the source-drain voltage V_{DS} when the gate-source voltage V_{GS} is determined) shown in FIG. 7, when the gate-source voltage V_{GS} has a predetermined value, a source-drain current I_{DS} increases as the source-drain voltage V_{DS} increases. In the saturated region (source-drain voltage $V_{DS} \geqq$ drain saturation threshold voltage V_{TH})

shown in FIG. 7, when the gate-source voltage V_{GS} has a predetermined value, the source-drain current I_{DS} is almost constant even when the source-drain voltage V_{DS} increases.

Referring to FIG. 7, gate-source voltages V_{GS0} to V_{GSMAX} have a relationship given by $V_{GS0} = 0$ [V] < $V_{GS1} < V_{GS2} < V_{GS3} < V_{GS4} < V_{GSMAX}$. That is, as is apparent from FIG. 7, when the source-drain voltage V_{DS} has a predetermined value, the source-drain current I_{DS} increases as the gate-source voltage V_{GS} increases independently of whether it is the unsaturated region or saturated region. In addition, as the gate-source voltage V_{GS} increases, the drain saturation threshold voltage V_{TH} increases.

As described above, in the unsaturated region, when the source-drain voltage V_{DS} changes even slightly, the source-drain current I_{DS} changes. In the saturated region, when the gate-source voltage V_{GS} is defined, the source-drain current I_{DS} is uniquely defined independently of the source-drain voltage V_{DS}.

When the maximum gate-source voltage V_{GSMAX} is being applied to the third transistor 23, the source-drain current I_{DS} is set to the value of the current that flows between the anode 51 and the cathode of the light-emitting element $E_{i,j}$ that emits light at the maximum luminance.

In addition, to make the third transistor 23

maintain the saturated region even when the gate-source voltage V_{GS} of the third transistor 23 is the maximum voltage V_{GSMAX}, the following condition is satisfied.

$$V_{HIGH} - V_E - V_{SS} \geqq V_{THMAX}$$

where V_E is the voltage between the anode and the cathode voltage, which is required by the light-emitting element $E_{i,j}$ for emitting light at the maximum luminance during the light emission life period. V_{THMAX} is the saturation threshold voltage between the source and the drain of the third transistor 23, which corresponds to V_{GSMAX}. The voltage V_{HIGH} is set such that the above condition is satisfied. Hence, even when the source-drain voltage V_{DS} of the third transistor 23 becomes low due to the voltage division of the light-emitting element $E_{i,j}$ connected in series with the transistor 23, the source-drain voltage V_{DS} always falls within the range of the saturated state. For this reason, the source-drain current I_{DS} that flows to the third transistor 23 is uniquely defined by the gate-source voltage V_{GS}.

The data driver 3 will be described next. As shown in FIG. 1, the signal lines Y_1 to Y_n are connected to current terminals CT_1 to CT_n of the data driver 3, respectively. The data driver 3 receives the control signal group D_{CNT} including the data driver clock signal CK1, start signal ST1, and latch signal L

from the controller 11. The data driver 3 also receives the 8-bit red digital gray level image signal S_R, green digital gray level image signal S_G, and blue digital gray level image signal S_B from an external circuit. The received digital signals are converted into analog signals by the D/A converter in the data driver 3. The data driver 3 controls such that the gray level designation current I_{DATA} based on the latch signal L and the converted analog signals flows from the signal lines Y_1 to Y_n to the current terminals CT_1 to CT_n of the data driver 3. The gray level designation current I_{DATA} is a current that is equivalent to the current level (current value) that flows to the light-emitting elements $E_{1,1}$ to $E_{m,n}$ to cause them to emit light at a luminance corresponding to a gray level image signal from an external circuit. The gray level designation current I_{DATA} flows from the signal lines Y_1 to Y_n to the current terminals CT_1 to CT_n.

The switching circuit 7 is formed of switching circuits S_1 to S_n. The switching circuits S_1 to S_n are connected to the signal lines Y_1 to Y_n, respectively. In addition, the current terminals CT_1 to CT_n of the data driver 3 are connected to the switching circuits S_1 to S_n, respectively. Each of the switching circuits S_1 to S_n receives the switching signal ϕ and a reset voltage V_{RST} from the controller 11.

A switching circuit S_j (the switching circuit S_j is connected to the signal line Y_j of the jth column) switches between two operations: an operation in which the gray level designation current I_{DATA} is supplied from the path between the drain 23d and the source 23s of the third transistor 23 and the signal line Y_j to a current terminal CT_j of the data driver 3; and an operation in which the reset voltage V_{RST} having a predetermined voltage level is output from the controller 11 to the signal line Y_j. More specifically, when the switching signal ϕ input from the controller 11 to the switching circuit S_j is at high level, the switching circuit S_j cuts off the current of the current terminal CT_j. The switching circuit S_j also outputs the reset voltage V_{RST} from the controller 11 to the signal line Y_j. On the other hand, when the switching signal ϕ input from the controller 11 to the switching circuit S_j is at low level, the switching circuit S_j supplies the gray level designation current I_{DATA} between the current terminal CT_j and the signal line Y_j to the path between the drain 23d and the source 23s of the transistor 23 and the signal line Y_j. The switching circuit S_j also cuts off the reset voltage V_{RST} from the controller 11.

In the organic EL display 1 having no switching circuit 7 for reset, assume that, e.g., the pixel $P_{i,j}$ of the ith row on the signal line Y_j of the jth column

should emit light at the highest gray level, as shown in FIG. 9A. Assume that, for this purpose, the gray level designation current I_{DATA} having the maximum current value is supplied to the path between the drain 23d and the source 23s of the third transistor 23 and the signal line Y_j during the selection period T_{SE}. At this time, a highest gray level voltage Vhsb of the current terminal CT_j is much lower than the voltage V_{LOW} and reference voltage V_{SS} of the common signal power supply 6. That is, the potential difference between the current terminal CT_j and the voltage V_{LOW} of the common signal power supply 6 is sufficiently large. For this reason, a large current can rapidly be supplied to the path between the drain 23d and the source 23s of the transistor 23 and the signal line Y_j to charge up the parasitic capacitance of the signal line Y_j, and a steady state can quickly be set. Next, assume that the pixel $P_{i+1,j}$ of the (i+1)th row should emit light at the lowest gray level luminance. Assume that, for this purpose, the gray level designation current I_{DATA} having the minimum current value (the current value is not zero) is to be supplied to the signal line Y_j. That is assume that the potential of the current terminal CT_j is to be changed to a lowest gray level voltage Vlsb which has a small potential difference to the voltage V_{LOW} of the common signal power supply 6 by supplying the very small gray level

designation current I_{DATA}, and the gray level designation current I_{DATA} should thus be set in the steady state. At this time, the amount of charges which are stored in the parasitic capacitance of the signal line Y_j when the gray level designation current I_{DATA} for the ith row is supplied is large. For this reason, the potential difference that corresponds to the change in potential of the signal line Y_j per unit time becomes small. A long time may therefore be required until the potential of the signal line Y_j is changed from the highest gray level voltage Vhsb to the lowest gray level voltage Vlsb and set in the steady state. In addition, when the selection period T_{SE} is set to be short, a difference corresponding to a voltage V_{DF} is generated before the potential reaches the lowest gray level voltage Vlsb. Hence, the pixel $P_{i+1,j}$ cannot emit light at an accurate luminance.

The organic EL display 1 of this embodiment has the switching circuit 7. Hence, as shown in FIG. 9B, the switching circuit S_j forcibly switches the potential of the signal line Y_j to the reset voltage V_{RST} much higher than the highest gray level voltage Vhsb during the non-selection period T_{NSE}, i.e., before the gray level designation current I_{DATA} for the (i+1)th row is supplied to the path between the drain 23d and the source 23s of the transistor 23 and the signal line Y_j. During the selection period T_{SE}, the

amount of charges stored in the signal line Y_j serving as a parasitic capacitance quickly changes so the signal line Y_j can rapidly be set at a high potential. For this reason, even when the gray level designation current I_{DATA} for the (i+1)th row has a very small current value corresponding to the lowest gray level, the potential can quickly reach the lowest gray level voltage Vlsb.

The reset voltage V_{RST} is set to be higher than the highest gray level voltage Vhsb. The highest gray level voltage Vhsb is set in the steady state in accordance with charges stored in the signal lines Y_1 to Y_n by the gray level designation current I_{DATA} which has a current value equal to a maximum gray level driving current I_{MAX}. The maximum gray level driving current I_{MAX} flows to the light-emitting elements $E_{1,1}$ to $E_{m,n}$ when they emit light at a maximum gray level luminance L_{MAX} for brightest light during the selection period T_{SE}. More preferably, the reset voltage V_{RST} is set to be equal to or higher than an intermediate voltage that has an intermediate value between the lowest gray level voltage Vlsb and the highest gray level voltage Vhsb. The lowest gray level voltage Vlsb is set in the steady state in accordance with charges stored in the signal lines Y_1 to Y_n by the gray level designation current I_{DATA} which has a current value equal to a minimum gray level driving current I_{MIN}.

The minimum gray level driving current I_{MIN} flows to the light-emitting elements $E_{1,1}$ to $E_{m,n}$ when they have a minimum gray level luminance L_{MIN} (however, the current level is more than 0 A) for darkest light. The reset voltage V_{RST} more preferably has a value equal to or more than the lowest gray level voltage Vlsb.

An example of the switching circuit S_j of the jth column will be described. The switching circuit S_j is constituted by a fourth transistor 31 formed of a P-channel field effect transistor and a fifth transistor 32 formed of an N-channel field effect transistor. The gate electrode of the transistor 31 and the gate electrode of the transistor 32 are connected to the controller 11 so that the switching circuit S_j receives the switching signal ϕ. The source electrode of the transistor 31 is connected to the signal line Y_j. The drain electrode of the transistor 31 is connected to the current terminal CT_j of the data driver 3. The drain electrode of the transistor 32 is connected to the signal line Y_j. The source electrode of the transistor 32 is connected to the controller 11 so that the switching circuit S_j receives the reset voltage V_{RST}. In this arrangement, when the switching signal ϕ from the controller 11 is at high level, the fifth transistor 32 is turned on while the fourth transistor 31 is turned off. On the other hand, when the switching signal ϕ from the

controller 11 is at low level, the transistor 31 is turned on while the transistor 32 is turned off. The transistor 31 may be set to a P-channel type, and the transistor 32 may be set to an N-channel type. In this case, the switching mode of the switching circuit S_j is changed by reversing the phase of the switching signal ϕ.

The period of the switching signal ϕ input to the controller 11 will be described here. As shown in FIG. 8, when the selection scanning driver 5 is applying the ON voltage V_{ON} to one of the selection scanning lines X_1 to X_m, the switching signal ϕ input to the controller 11 is at low level. On the other hand, during the non-selection period T_{NSE} when the selection scanning driver 5 is applying the OFF voltage V_{OFF} to all the selection scanning lines X_1 to X_m, the switching signal ϕ input to the controller 11 is at high level. That is, the switching signal ϕ input to the controller 11 is a pulse signal which changes to high level for each of the $\underline{m}$ non-selection periods T_{NSE} in one selection period T_{SE}.

The switching circuits S_1 to S_n are circuits which switch between two operations: an operation for supplying the gray level designation current I_{DATA} from the signal lines Y_1 to Y_n to the current terminals CT_1 to CT_n in accordance with the switching signal ϕ from the controller 11; and an operation for forcibly

charging the signal lines Y_1 to Y_n to the reset voltage V_{RST}. When the switching signal ϕ input from the controller 11 is at low level, i.e., during the selection period T_{SE} of one of the selection scanning lines X_1 to X_m, each switching circuit turns on the transistor 31 and off the transistor 32. With this operation, the gray level designation current I_{DATA} flows to the current terminals CT_1 to CT_n through the paths between the drain 23d and the source 23s of the transistors 23 and the signal lines Y_1 to Y_n. When the switching signal ϕ input from the controller 11 is at high level, i.e., during the non-selection period T_{NSE} of all the selection scanning lines X_1 to X_m, each switching circuit turns off the transistor 31 and on the transistor 32. At this time, the gray level designation current I_{DATA} does not flow to the drains 23d and sources 23s of the transistors 23 and the signal lines Y_1 to Y_n. Instead, the potentials of the signal lines Y_1 to Y_n are forcibly set to the reset voltage V_{RST}.

Hence, in the selection period T_{SE} of each row, the gray level designation current I_{DATA} flows from the signal lines Y_1 to Y_n to the current terminals CT_1 to CT_n. On the other hand, in the non-selection period T_{NSE} between the rows, the reset voltage V_{RST} is forcibly applied to the signal lines Y_1 to Y_n. The charge amount of the parasitic capacitance of the

signal lines Y_1 to Y_n becomes almost the same as the charge amount when the small gray level designation current I_{DATA} flows, and the steady state is set. For this reason, even when the current value of the gray level designation current I_{DATA} is very small, the steady state can quickly be set.

In the selection period T_{SE} of each row, the data driver 3 generates the gray level designation current I_{DATA} which should flow from the common signal supply lines Z_1 to Z_m to the current terminals CT_1 to CT_n through the transistors 23, transistors 21, signal lines Y_1 to Y_n, and switching circuits S_1 to S_n. The current value of the gray level designation current I_{DATA} is equal to the current value of the driving current which is supplied to the light-emitting elements $E_{1,1}$ to $E_{m,n}$ to cause them to emit light at a luminance gray level corresponding to image data.

A method of causing the data driver 3, selection scanning driver 5, and common signal power supply 6 to drive the organic EL display panel 2 and the display operation of the organic EL display 1 will be described next.

As shown in FIG. 8, on the basis of the selection scanning driver clock signal CK2 received from the controller 11, the selection scanning driver 5 sequentially applies the ON voltage V_{ON} to the selection scanning line X_1 of the first row to the

selection scanning line X_m of the mth row in this order (the selection scanning line X_1 follows the selection scanning line X_m) during each selection period T_{SE} to select the selection scanning line. Accordingly, the selection scanning lines X_1 to X_m are scanned in this order.

Simultaneously when the selection scanning driver 5 sequentially selects and scans the selection scanning lines, the common signal power supply 6 outputs common signals to all the common signal supply lines Z_1 to Z_m. The common signals output to the common signal supply lines Z_1 to Z_m are synchronized with each other. In all pixel circuits $D_{1,1}$ to $D_{m,n}$, the common signal of the voltage V_{LOW} is input to the source electrode 22s of the second transistor 22 and the source electrode 23s of the third transistor 23.

In addition, during the sequential scanning by the selection scanning driver, the data driver 3 receives and latches the 8-bit red digital gray level image signal S_R, green digital gray level image signal S_G, and blue digital gray level image signal S_B from an external circuit on the basis of the data driver clock signal CK1 input from the controller 11. When the selection signal V_{ON} that selects the selection scanning line X_i is output, the switching signal ϕ is synchronously input to the switching circuit 7. The switching signal ϕ turns on the transistor 31 and off

the transistor 32. The gray level designation currents I_{DATA} having current values based on the gray level of the latched signals flow to the current terminals CT_1 to CT_n of the data driver 3 through the common signal supply line Z_i, the paths between the drains 23d and the sources 23s of the transistors 23 of the pixels $P_{i,1}$ to $P_{i,n}$, the paths between the drains 21d and the sources 21s of the transistors 21 of the pixels $P_{i,1}$ to $P_{i,n}$, and the signal lines Y_1 to Y_n.

When the selection signal of ON level V_{ON} is being output to the given selection scanning line X_i, a selection signal of off level is output to the remaining selection scanning lines X_1 to X_m (except X_i). This period is the selection period T_{SE} of the ith row. Hence, for the pixel circuits $D_{i,1}$ to $D_{i,n}$ of the ith row, the first transistor 21 and second transistor 22 are ON. For the pixel circuits $D_{1,1}$ to $D_{m,n}$ (except the pixel circuits $D_{i,1}$ to $D_{i,n}$) of the remaining rows, the first transistor 21 and second transistor 22 are OFF.

That is, when the voltage V_{ON} is applied to the selection scanning line X_i during the selection period T_{SE} of the ith row, the first transistors 21 and second transistors 22 in the pixel circuits $D_{i,1}$ to $D_{i,n}$ are turned on. At this time, the voltage V_{LOW} from the common signal supply lines Z_1 to Z_m is supplied to the drain electrodes 23d of the third transistors 23 and

the drain electrodes 22d of the second transistors 22 of all the pixel circuits $D_{1,1}$ to $D_{m,n}$. Simultaneously, the data driver 3 is going to supply the gray level designation current I_{DATA} to the current terminals CT_1 to CT_n in accordance with the latch signal L. At this time, the switching signal ϕ is input from the controller 11 to the switching circuit 7 to turn on the transistors 31 and off the transistors 32. Hence, the current terminals CT_1 to CT_n are electrically connected to the common signal supply line Z_i. The voltage V_{LOW} of the common signal supply line Z_i is set to be higher than the potentials of the current terminals CT_1 to CT_n. For this reason, a voltage that supplies the gray level designation current I_{DATA} to the path between the source and the drain of the third transistor 23 is applied between the gate 23g and the source 23s and between the source 23s and the drain 23d of the third transistor 23.

The current value of the gray level designation current I_{DATA} is based on the red digital gray level image signal S_R, green digital gray level image signal S_G, and blue digital gray level image signal S_B input to the data driver 3. During the selection period T_{SE}, the data driver 3 stores charges in the capacitor 24 between the gate 23g and the source 23s of the transistor 23 of each of the pixel $P_{i,1}$ to $P_{i,n}$. With this operation, the current value of the gray level

designation current I_{DATA} that flows to the current terminals CT_1 to CT_n of the data driver 3 through the common signal supply line Z_i, the paths between the drains 23d and the sources 23s of the transistors 23 of the pixels $P_{i,1}$ to $P_{i,n}$, the paths between the drains 21d and the sources 21s of the transistors 21 of the pixels $P_{i,1}$ to $P_{i,n}$, and the signal lines Y_1 to Y_n is set in the stead state. That is, the gray level designation current I_{DATA} having a predetermined current value is supplied to the paths between the drains 23d and the sources 23s of the transistors 23 of the pixels $P_{i,1}$ to $P_{i,n}$. After that, the capacitor 24 can hold the charges at least during one scanning period T_{SC} or more. In other words, the transistor 23 is going to supply a driving current having a current value equal to the gray level designation current I_{DATA} at least for a time corresponding to one scanning period T_{SC} or more by the charges in the capacitor 24. That is, the capacitor 24 serves as a storage means for storing the current value of the gray level designation current I_{DATA} that flows during the selection period T_{SE} and flowing a driving current having a current value equal to the gray level designation current I_{DATA} to the light-emitting elements $E_{i,1}$ to $E_{i,n}$ during the non-selection period T_{NSE}.

Hence, during the selection period T_{SE} of the ith row, the first transistors 21 and second transistors 22

of the pixel circuits $D_{i,1}$ to $D_{i,n}$ of the ith row are turned on. Accordingly, the gray level designation current I_{DATA} supplied from the signal lines Y_1 to Y_n to the data driver 3 is stored in the capacitor 24 of each of the pixel circuits $D_{i,1}$ to $D_{i,n}$ of the ith row. In each of the pixel circuits $D_{1,1}$ to $D_{m,n}$ (except the pixel circuits $D_{i,1}$ to $D_{i,n}$) of the remaining rows, the first transistor 21 and second transistor 22 are OFF. Hence, the gray level designation current I_{DATA} is not stored in the capacitors 24 of the remaining rows. That is, the third transistors 23 of the remaining rows cannot flow the gray level designation current I_{DATA}. As described above, during the selection period T_{SE} of the ith row, charges between the gate and the source of the third transistor 23 are received by each of the pixel circuits $D_{i,1}$ to $D_{i,n}$ in correspondence with the gray level designation current I_{DATA}. Accordingly, the charges between the gate and the source of the third transistor 23, which have been stored so far, are refreshed. During the plurality of non-selection periods T_{NSE} after the selection period T_{SE} of the ith row, the pixel circuits $D_{i,1}$ to $D_{i,n}$ supply driving currents (the driving currents have the same level as that of the gray level designation current I_{DATA}) corresponding to the charges stored between the gates and the sources of the third transistors 23 to the light-emitting elements $E_{i,1}$ to $E_{i,n}$, thereby causing

them to emit light.

As described above, the selection scanning driver 5 line-sequentially shifts the selection signal from the first row to the mth row. Accordingly, the gray level designation current I_{DATA} flows sequentially to the pixel circuits $D_{1,1}$ to $D_{1,n}$ of the first row to the pixel circuits $D_{m,1}$ to $D_{m,n}$ of the mth row in accordance with the red digital gray level image signal S_R, green digital gray level image signal S_G, and blue digital gray level image signal S_B input to the data driver 3. With this operation, the charges stored between the gate and the source of each third transistor 23 are refreshed. When such line-sequential scanning is repeated, an image is displayed on the display section 4 of the organic EL display panel 2.

The operation of causing the pixel circuits $D_{i,1}$ to $D_{i,n}$ to receive the gray level designation current I_{DATA} during the selection period T_{SE} of the ith row and the operation of causing the light-emitting elements $E_{i,1}$ to $E_{i,n}$ to emit light on the basis of the received gray level designation current I_{DATA} will be described here in detail.

During the selection period T_{SE} of the ith row, a selection signal of the ON voltage V_{ON} is output from the selection scanning driver 5 to the selection scanning line X_i of the ith row in accordance with the control signal group G_{CNT} including the clock signal

CK2 from the controller 11. Then, the first transistors 21 and second transistors 22 of all the pixel circuits $D_{i,1}$ to $D_{i,n}$ connected to the selection scanning line X_i are set in the ON state during the selection period T_{SE}. At the start of the selection period T_{SE} of the ith row, the common signal changes to the voltage V_{LOW}. During the selection period T_{SE} of the ith row, the voltage V_{LOW} is applied to all the common signal supply lines Z_1 to Z_m. Since the second transistor 22 is ON, a voltage is applied even to the gate electrode 23g of the third transistor 23. Hence, the third transistor 23 is turned on.

Furthermore, when a given column of the light-emitting elements $E_{i,1}$ to $E_{i,n}$ of the selected row is to be caused to emit light during the non-selection period T_{NSE} (to be described later), the data driver 3 controls the potential of one of the current terminals CT_1 to CT_n, which corresponds to the column to be caused to emit light, to be lower than the voltage V_{LOW}. Accordingly, in the column of the pixel circuit $D_{i,j}$, which should emit light, the gray level designation current I_{DATA} flows from the common signal supply line Z_i to the data driver 3. When a given column of the light-emitting elements $E_{i,1}$ to $E_{i,n}$ of the selected ith row is to be inhibited from emitting light during the non-selection period T_{NSE} (to be described later), the data driver 3 controls the

potential of one of the current terminals CT_1 to CT_n, which corresponds to the column that should be inhibited from emitting light, to be equal to the voltage V_{LOW}. Accordingly, in the column of the pixel circuit $D_{i,j}$, which should emit light, the gray level designation current I_{DATA} does not flow from the common signal supply line Z_i to the data driver 3. During the selection period T_{SE} of the ith row, the data driver 3 controls the potentials of the current terminals CT_1 to CT_n to supply the gray level designation current I_{DATA} to the data driver 3 to the signal lines Y_1 to Y_n (the gray level designation current I_{DATA} does not flow for a column which should be inhibited from emitting light). In each of the pixel circuits $D_{i,1}$ to $D_{i,n}$ of the ith row, the first transistor 21 and second transistor 22 are turned on. Hence, the gray level designation current I_{DATA} flows through a path of common signal supply line Z_i → paths between the drains 23d and the sources 23s of the transistors 23 of the pixels $P_{i,1}$ to $P_{i,n}$ → paths between the drains 21d and the sources 21s of the transistors 21 of the pixels $P_{i,1}$ to $P_{i,n}$ → signal lines Y_1 to Y_n → transistors 31 of the switching circuits S_1 to S_n → current terminals CT_1 to CT_n of the data driver 3.

As described above, charges corresponding to the current value of the gray level designation current I_{DATA} are received by the pixel circuits $D_{i,1}$ to $D_{i,n}$.

At this time, in all of the first to nth columns, the current value of the driving current flowing to the light-emitting elements $E_{i,1}$ to $E_{i,n}$ is equal to the current value of the gray level designation current I_{DATA}. The current value is designated by the data driver 3. Hence, the current value of the gray level designation current I_{DATA} which is continuously held during the non-selection period T_{NSE} is constant.

That is, during the selection period T_{SE}, the gray level designation current I_{DATA} flows to the third transistor 23. The voltage across the common signal supply line Z_i, third transistors 23, first transistors 21, signal lines Y_1 to Y_n, switching circuits S_1 to S_n, and data driver 3 is set in the steady state. Accordingly, a voltage at a level corresponding to the level of the gray level designation current I_{DATA} that flows to the third transistor 23 is applied between the gate electrode 23g and the source electrode 23s of the third transistor 23. Charges with a magnitude corresponding to the level of the voltage between the gate electrode 23g and the source electrode 23s of the third transistor 23 are stored in the capacitor 24. During the selection period T_{SE} of the ith row, in each of the pixel circuits $D_{i,1}$ to $D_{i,n}$ of the ith row, the first transistor 21 and second transistor 22 function to supply the gray level designation current I_{DATA} flowing to the signal line Y_j to the third transistor

23. The third transistor 23 functions to convert the current value of the gray level designation current I_{DATA} into the value of the voltage between the gate and the source.

As described above, during the selection period T_{SE} of the ith row, the magnitude of the charges stored in the capacitors 24 of the pixel circuits $D_{i,1}$ to $D_{i,n}$ of the ith row is refreshed from the preceding scanning period T_{SC}. At the same time, the drain-source current level and the source-drain voltage level of the third transistors 23 of the pixel circuits $D_{i,1}$ to $D_{i,n}$ of the ith row are also refreshed from the preceding scanning period T_{SC}.

The potential at an arbitrary point on the path of the third transistor 23, first transistor 21, and signal line Y_j changes depending on the internal resistance of the transistors 21, 22, and 23, which changes over time. However, in this embodiment, the current value of the gray level designation current I_{DATA} that flows through the path of third transistor 23 → first transistor 21 → signal line Y_j is forcibly supplied by the data driver 3. Hence, even when the internal resistance of the transistors 21, 22, and 23 changes over time, the gray level designation current I_{DATA} that flows through the path of third transistor 23 → first transistor 21 → signal line Y_j has a desired level.

During the selection period T_{SE} of the ith row, the common signal supply line Z_i is set to the voltage V_{LOW} that is equal to or lower than the reference voltage V_{SS}. In addition, a zero bias or reverse bias is applied across the anodes and the cathodes of the light-emitting elements $E_{i,1}$ to $E_{i,n}$ of the ith row. Hence, no current flows to the light-emitting elements $E_{i,1}$ to $E_{i,n}$, and they does not emit light.

At the end time of the selection period T_{SE} of the ith row (at the start time of the non-selection period T_{NSE} of the ith row), the selection signal output from the selection scanning driver 5 to the selection scanning line X_i changes from the high-level potential V_{ON} to the low-level potential V_{OFF}. The selection scanning driver 5 applies the OFF voltage V_{OFF} to the gate electrodes 21g of the first transistors 21 and the gate electrodes 22g of the second transistors 22 of the pixel circuits $D_{i,1}$ to $D_{i,n}$ of the ith row.

Hence, during the non-selection period T_{NSE} of the ith row, the first transistors 21 of the pixel circuits $D_{i,1}$ to $D_{i,n}$ of the ith row are turned off. The gray level designation current I_{DATA} that flows from the common signal supply line Z_i to the corresponding signal lines Y_1 to Y_n is cut off. In addition, during the non-selection period T_{NSE} of the ith row, in all the pixel circuits $D_{i,1}$ to $D_{i,n}$ of the ith row, even when the transistor 22 is turned off, charges stored in

the capacitor 24 during the immediately preceding selection period T_{SE} of the ith row are confined by the second transistor 22. For this reason, in all the pixel circuits $D_{i,1}$ to $D_{i,n}$ of the ith row, the third transistor 23 is kept ON during the non-selection period T_{NSE}. That is, in all the pixel circuits $D_{i,1}$ to $D_{i,n}$ of the ith row, the second transistor 22 holds the gate-source voltage level V_{GS} of the third transistor 23 such that the gate-source voltage level V_{GS} of the third transistor 23 during the non-selection period T_{NSE} becomes equal to the gate-source voltage level V_{GS} of the third transistor 23 during the selection period T_{SE}.

During the non-selection period T_{NSE}, the common signal output from the common signal power supply 6 to the common signal supply line Z_i rises to the voltage V_{HIGH}. During the non-selection period T_{NSE}, the cathodes of the light-emitting elements $E_{i,1}$ to $E_{i,n}$ of the ith row are at the reference voltage V_{SS}. The common signal supply line Z_i is at the voltage V_{HIGH} higher than the reference voltage V_{SS}. In addition, charges corresponding to the gray level designation current I_{DATA} flowing during the selection period T_{SE} are stored between the gate 23g and the source 23s of the third transistor 23 connected in series. In this case, a forward bias voltage corresponding to the gray level designation current I_{DATA} is applied to the