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(54) **DISPLAY PANEL**

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U.S.C. 154(b) by 86 days.

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(51) Int. Cl.

H01L 29/04 (2006.01)

(52) **U.S. Cl.** **257/72**; 257/40; 257/79

257/72, 79

See application file for complete search history.

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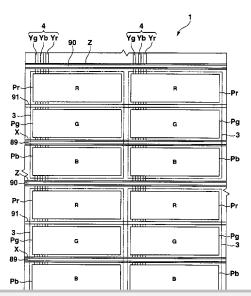
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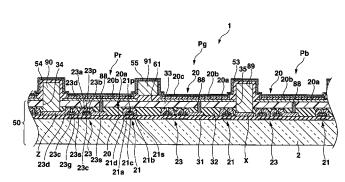
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(57) ABSTRACT

A display panel includes a transistor array substrate which has a plurality of pixels and is formed by providing a plurality of transistors for each pixel, each of the transistor having a gate, a gate insulating film, a source, and a drain. A plurality of interconnections are formed to project to a surface of the transistor array substrate and arrayed in parallel to each other. A plurality of pixel electrodes are provided for each pixel and arrayed between the interconnections on the surface of the transistor array substrate along the interconnections. Each of a plurality of light-emitting layers is formed on each pixel electrode. A counter electrode is stacked on the light-emitting layer.

22 Claims, 13 Drawing Sheets







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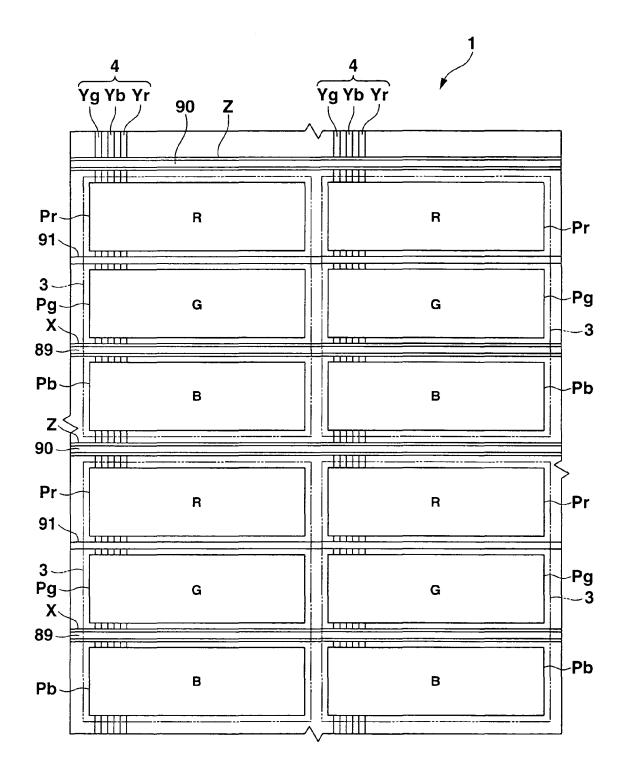


FIG.1



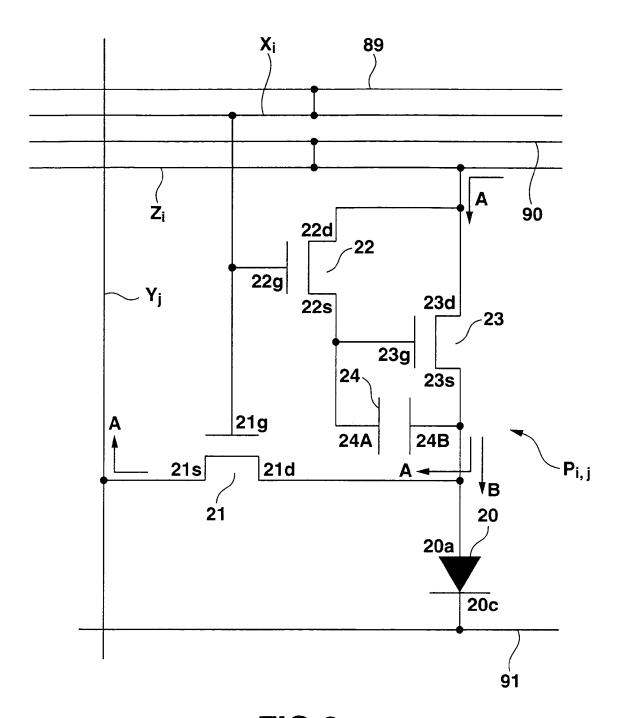
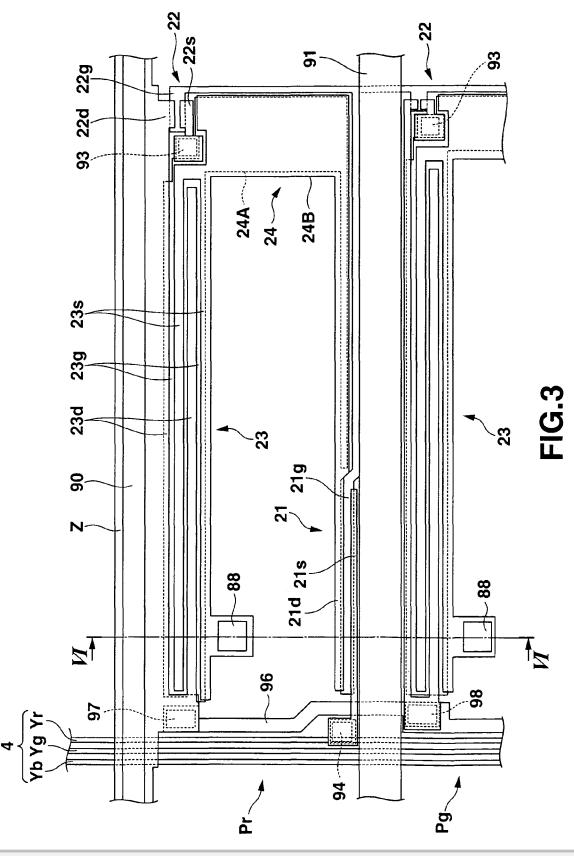


FIG.2







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