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(54) **DYNAMICALLY ALLOCATED CACHE MEMORY FOR A MULTI-PROCESSOR UNIT**

(57) **ABSTRACT**

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The resources of a partitioned cache memory are dynamically allocated between two or more processors on a multi-processor unit (MPU). In one embodiment, the MPU includes first and second processors, and the cache memory includes first and second partitions. A cache access circuit selectively transfers data between the cache memory partitions to maximize cache resources. In one mode, both processors are active and may simultaneously execute separate instruction threads. In this mode, the cache access circuit allocates the first cache memory partition as dedicated cache memory for the first processor, and allocates the second cache memory partition as dedicated cache memory for the second processor. In another mode, one processor is active, and the other processor is inactive. In this mode, the cache access circuit allocates both the first and second cache memory partitions as cache memory for the active processor.

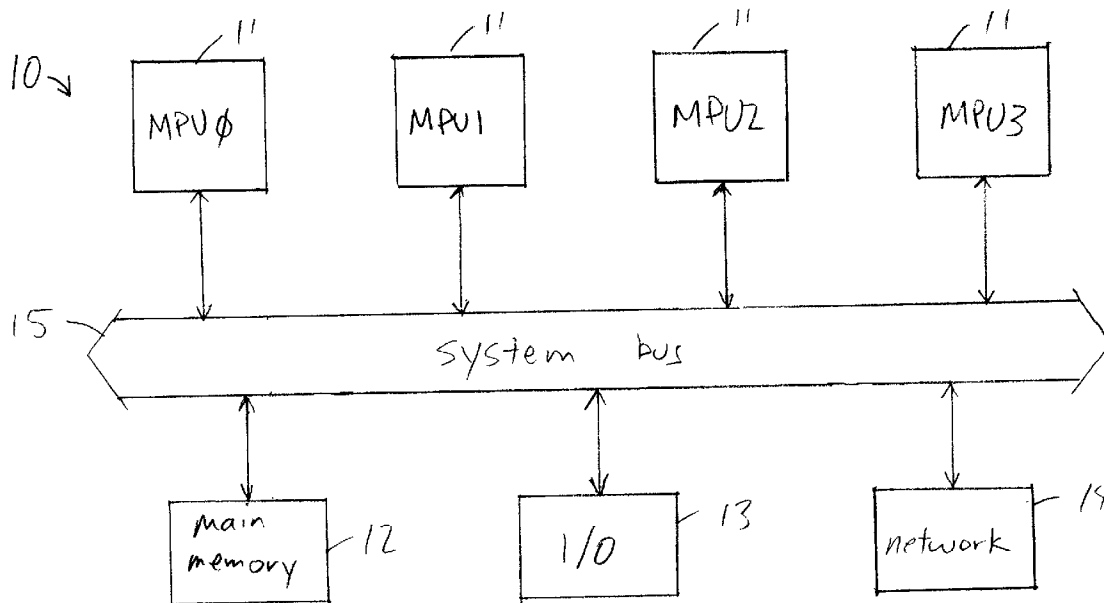
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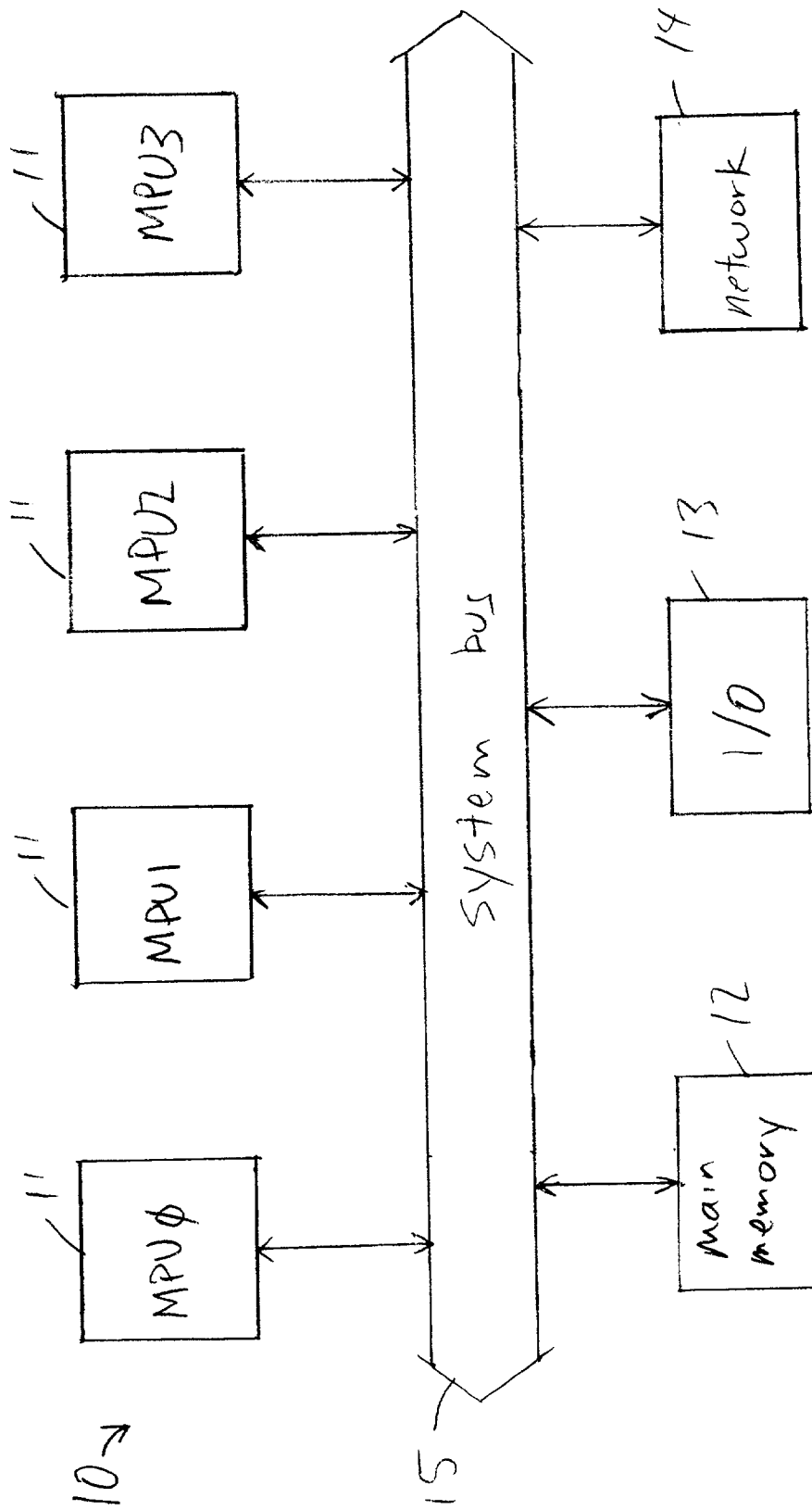
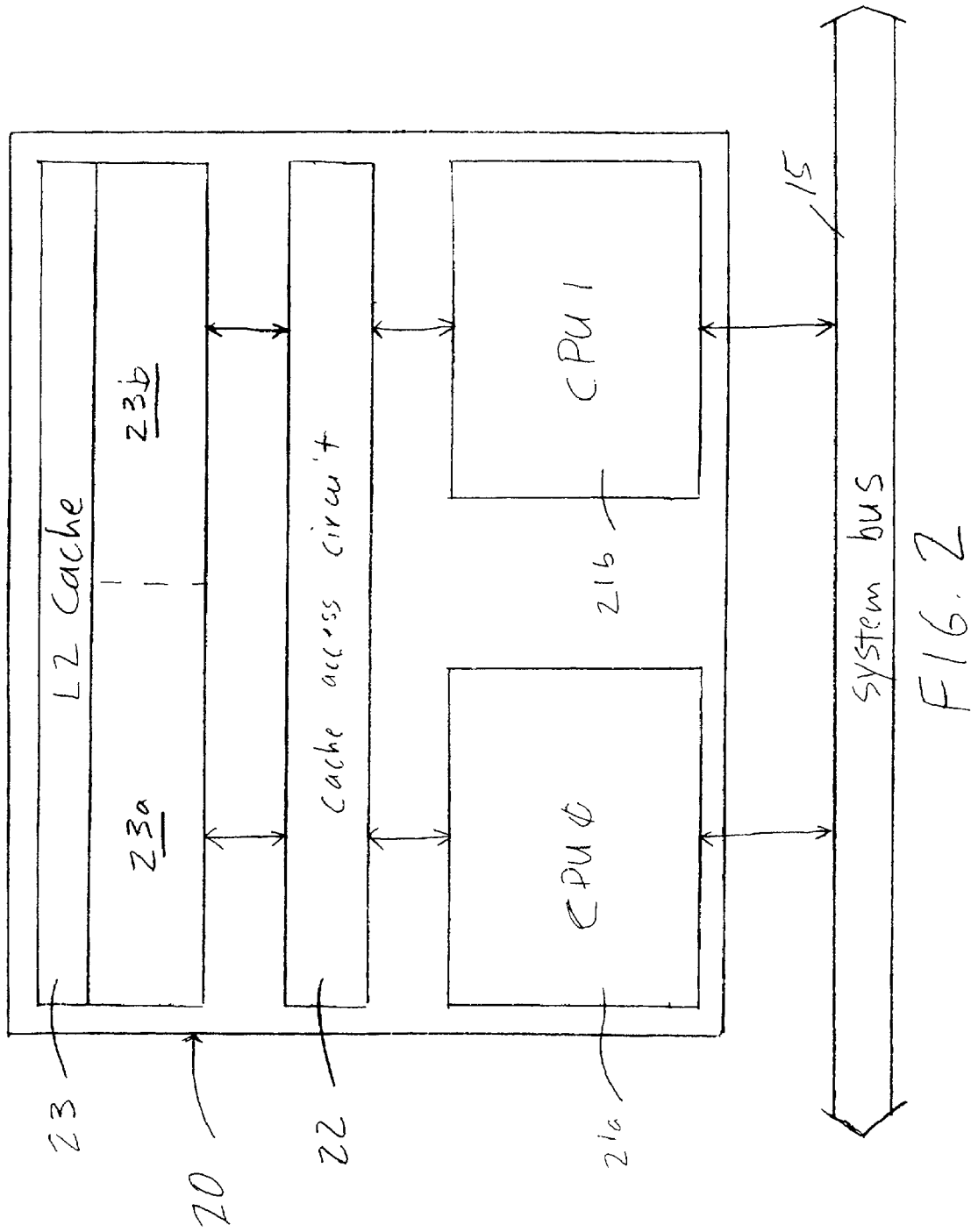


FIG. 1



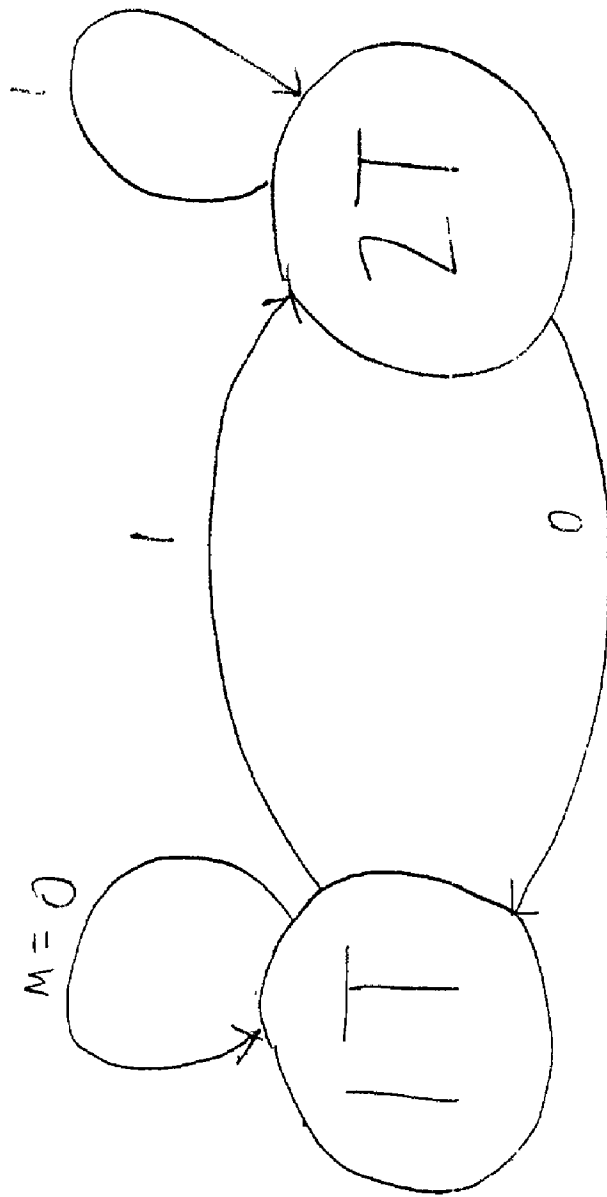


FIG. 3

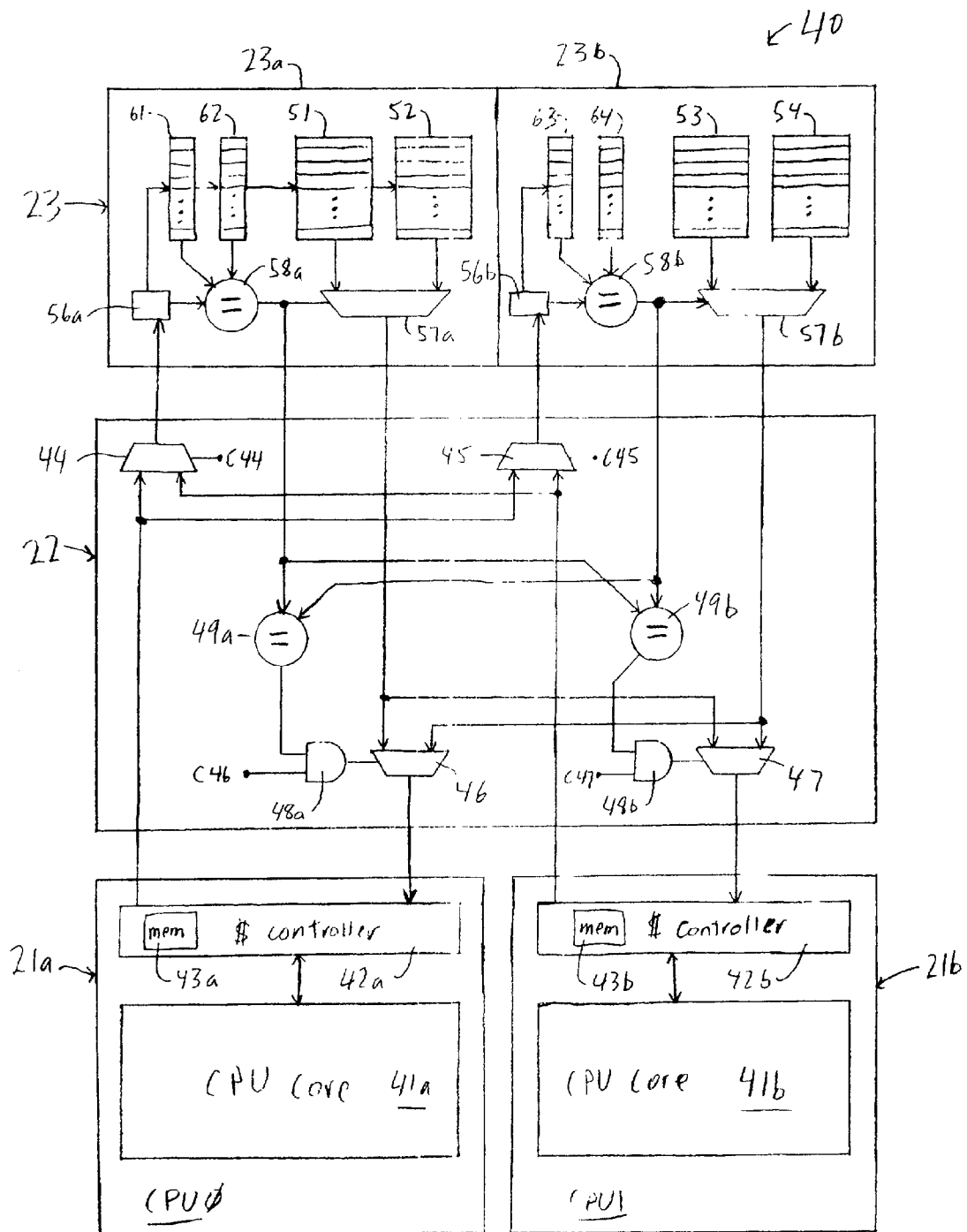


FIG. 4

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