United States Patent [19]

Kawada

[11] **Patent Number:** **4,985,647**

[45] **Date of Patent:** **Jan. 15, 1991**

[54] **CMOS TRANSFER SWITCH FREE FROM MALFUNCTION ON NOISE SIGNAL**

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[73] Assignee: **NEC Corporation,** Tokyo, Japan

[21] Appl. No.: **369,532**

[22] Filed: **Jun. 21, 1989**

[30] **Foreign Application Priority Data**

Jun. 21, 1988 [JP] Japan 63-154419

[51] **Int. Cl.**[5] **H03K 19/94;** H03K 17/687

[52] **U.S. Cl.** **307/449;** 307/573; 307/443; 307/547; 307/572; 307/463

[58] **Field of Search** 307/542, 547–549, 307/242–243, 571–573, 443, 449, 463

[56] **References Cited**

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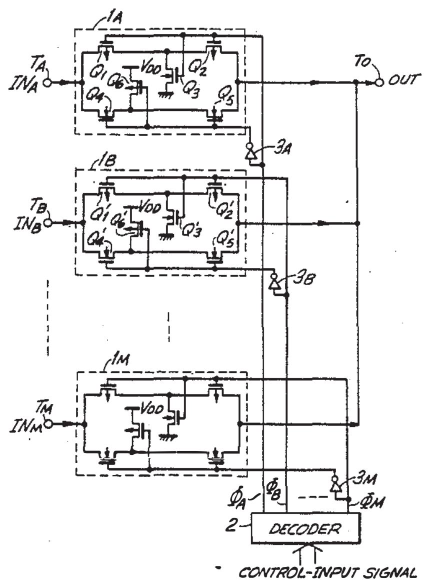
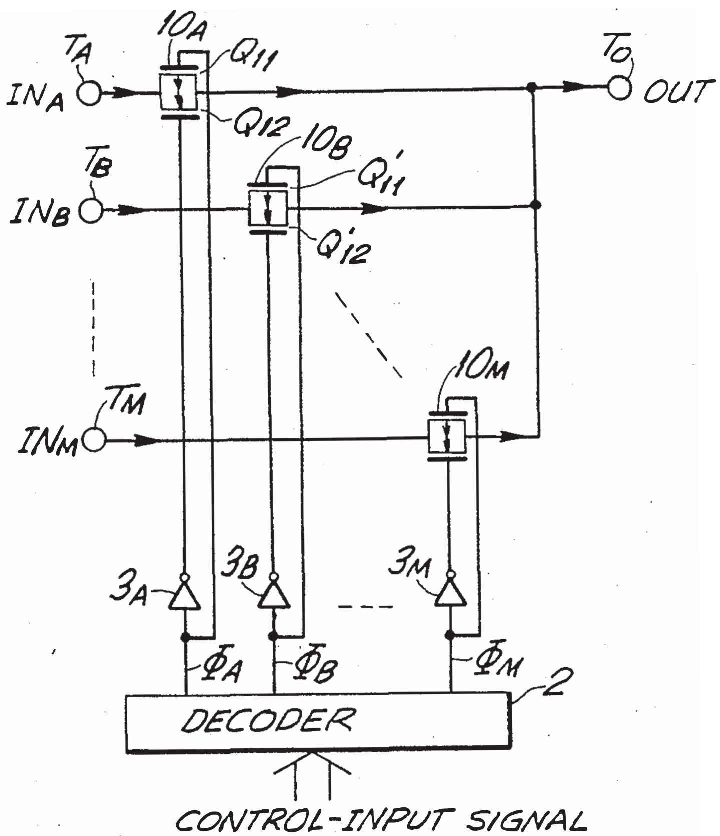
Primary Examiner—Stanley D. Miller
Assistant Examiner—M. Wambach
Attorney, Agent, or Firm—Helfgott & Karas

[57] **ABSTRACT**

An analog switch comprises first and second FET switches connected in series between input and output terminals through a first interconnection point, a third FET switch connected between the first interconnection point and one of power terminals, fourth and fifth FET switches connected in series between input and output terminals through a second interconnection point and a sixth FET switch connected between the second interconnection point and the other of the power terminals, whereby the first, second and sixth FET switches are simultaneously turns on or off in a manner that their operating conditions are kept in phase opposite to the third, fourth and fifth FET switches.

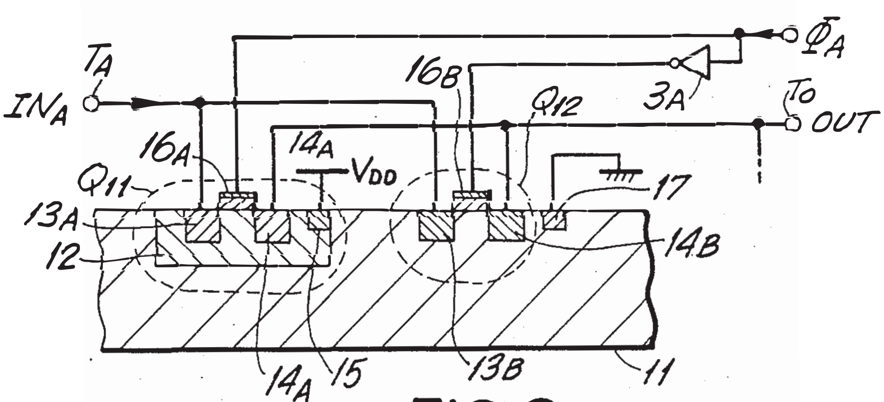
10 Claims, 3 Drawing Sheets





10A
TA
Q11
INA
TO
OUT
Q12
10B
TB
Q'11
INB
Q'12
10M
TM
INM
3A
3B
3M
ΦA
ΦB
ΦM
2
DECODER
CONTROL-INPUT SIGNAL

FIG. 1



ΦA
TA
16B
INA
Q12
3A
TO
OUT
16A
14A
VDD
Q11
17
13A
14B
12
14A
15
13B
11

FIG. 2

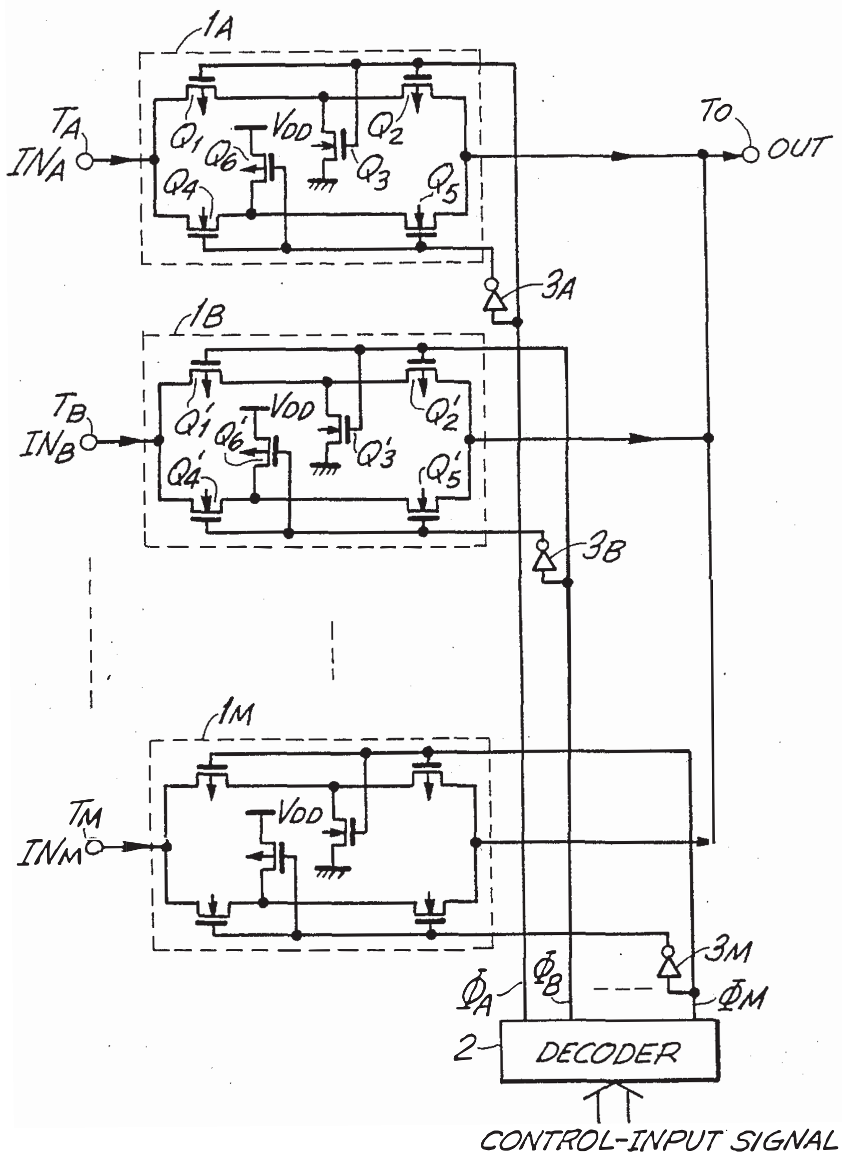

1A
TA
INA
Q1
Q6
VDD
Q2
Q3
Q4
Q5
TO
OUT
3A
1B
TB
INB
Q'1
Q'6
VDD
Q'2
Q'3
Q'4
Q'5
3B
1M
TM
INM
VDD
3M
ΦA
ΦB
ΦM
2
DECODER
CONTROL-INPUT SIGNAL

FIG.3

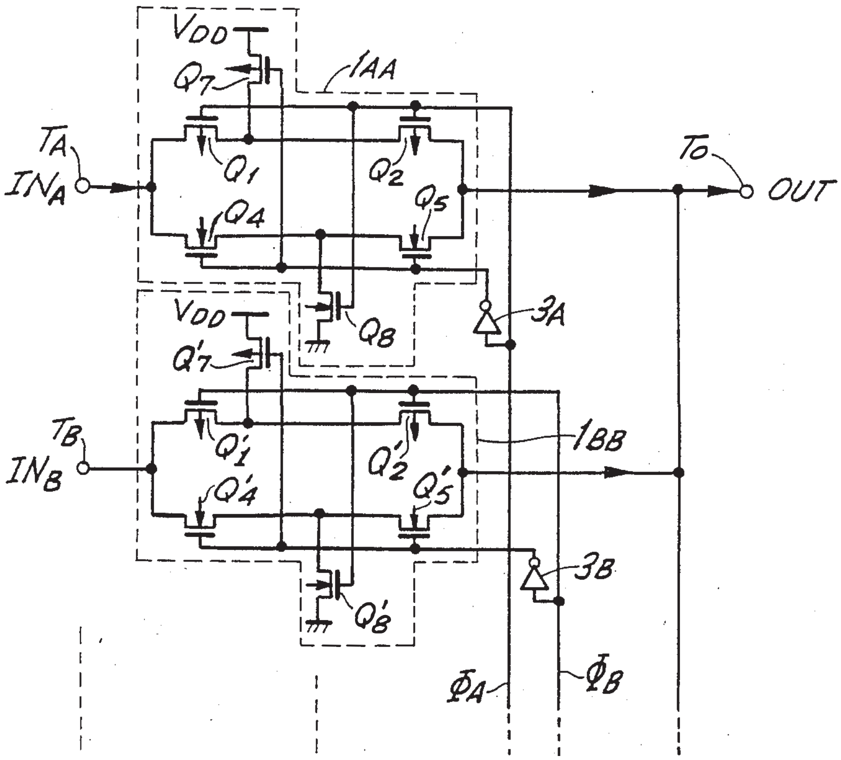

VDD
Q7
1AA
TA
INA
Q1
Q2
Q5
Q4
To
OUT
3A
Q8
VDD
Q'7
TB
INB
Q'1
Q'2
Q'5
Q'4
1BB
3B
Q'8
ΦA
ΦB

FIG.4

CMOS TRANSFER SWITCH FREE FROM MALFUNCTION ON NOISE SIGNAL

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an analog switch circuit and, more particularly, to an analog switch circuit composed of a CMOS structure and being free from malfunction by external noise signal.

2. Related Art

A typical conventional analog switch circuit that is formed on a monolithic integrated circuit to be used in a multiplexer or the like employs a CMOS structure with a view to widening the input voltage range of analog signals.

FIG. 1 shows one example in which a conventional analog switch circuit is applied to a multiplexer.

This circuit has analog switch circuits 10_A to 10_M each comprising a pair of P- and N-type transistors Q_{11} and Q_{12} which are parallel-connected between the corresponding one of the input terminals T_A to T_M and an output terminal T_O and which are respectively supplied at their gate electrodes with the corresponding one of the control signals ϕ_A to ϕ_M from a decoder **2** and an inverted signal formed by respective inverters 3_A to 3_M so that the analog switch circuits 10_a to 10_M turn on/off.

FIG. 2 shows a sectional structure of respective analog switch circuits 10_A to 10_M. An N^{31} -type well region **12** is provided in a P^--type semiconductor substrate **11**. A P-type transistor Q_{11} is formed in the well region **12** with P-type source and drain regions **13A** and **14A** and a gate electrode **16A**, while an N-type transistor Q_{12} is provided directly in the semiconductor substrate **11** with N-type source and drain regions **13B** and **14B** and a gate electrode **16B**. The semiconductor substrate **11** is grounded through a substrate grounding electrode through a substrate grounding region **17**, while the well region **12** is connected to a power supply potential (V_{DD}) terminal through the well-potential supplying region **15**.

The above-described conventional analog switch circuits 10_A to 10_M are each comprised of a pair of P- and N-type transistors Q_{11} and Q_{12}. The N-type transistor Q_{12} of each of the analog switch circuits 10_A to 10_M is formed directly in the P^--type semiconductor substrate **11** supplied with a grounding potential, while the P-type transistor Q_{11} is formed in a well region **12** provided in the semiconductor substrate **11** and supplied with a power supply potential V_{DD}. Therefore, the conventional structure has the disadvantage that, if a noise or the like of a voltage which is out of the range defined by the power supply potential V_{DD} and the ground potential is input to any of the input terminals T_A to T_M, a current flows between the one of input terminals T_A to T_M and the power supply potential V_{DD} terminal through the P-type source region 13A-the well region **12**-the well potential supplying region **15** or the ground potential terminal through the N-type source region **13B**-the substrate **11**-the substrate grounding region **17**. This current flow changes the channel potential of the transistor Q_{11} or Q_{12} so that the noise or the like is transmitted to the output terminal T_O, thus causing an adverse effect on the output signal OUT.

More specifically, it is assumed that a negative overvoltage is applied as a noise to the input terminal T_A in the case where the control signal ϕ_A is at a high level and the transistors Q_{11} and Q_{12} of the analog switch circuit 10_A are in an off-state and therefore the input terminal T_A and the output terminal T_O are not in electrical connection with each other, while another control signal ϕ_B is at a low level and the transistors Q'_{11} and Q'_{12} of the analog switch 10_B are in an on-state and therefore the input terminal T_B and the output terminal T_O are in electrical connection with each other.

In such a case, if the negative overvoltage is applied to the source region 13_A through the input terminal T_A, since the gate electrode 16_A is at a high level, the transistor Q_{11} is not turned on. However, if the negative overvoltage is applied to the source region 13_B, a forward-biased diode is formed between the P^--type semiconductor substrate **11** and the N^+-type source region 13_B, so that the applied negative overvoltage causes a current to flow between the ground potential terminal and the input terminal T_A through the substrate grounding electrode **17**. Further, the transistor Q_{12} which is turned off in the case where the gate electrode 16_B is at a low level, that is, a level substantially equal to the ground potential, and the gate-to-source voltage V_{GS} of the transistor Q_{12} is lower than the threshold voltage V_{TH} is turned on since the source region 13_B is at a negative potential and hence the gate-to-source voltage V_{GS} is higher than the threshold voltage V_{TH} despite the fact that the potential at the gate electrode **16B** is substantially equal to the ground potential. As a result, the negative overvoltage signal applied to the input terminal T_A is undesirably transmitted to the output terminal T_O through the analog switch circuit 10_A which has been set in an off state, thus causing an adverse effect on the output signal OUT.

When a positive overvoltage which is higher than the power supply voltage V_{DD} is applied as a noise to the input terminal T_A, the transistor Q_{11} is turned on in reverse to the above, thus similarly causing an adverse effect on the output signal T_O.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide an analog switch circuit wherein, when the connection between an input terminal and an output terminal is set in an off-state in response to a control signal, this off-state is maintained even if an overvoltage noise or the like which is out of the range defined between the power supply potential and the ground potential, is applied to the input terminal, thus preventing the noise or the like from being transmitted to the output terminal.

The analog switch circuit according to the present invention comprises: first and second transistors of one conductivity type which are series-connected between an input terminal and an output terminal to turn on/off in response to a control signal mutually input to their gate electrodes, thereby closing or opening the circuit between the input and output terminals; a third transistor connected between the node of the series connection of the first and second transistors and a ground potential terminal (or a power supply potential terminal) to perform an on/off operation which is opposite to the on/off operation of the first and second transistors in response to the control signal; fourth and fifth transistors of the opposite conductivity type to said conductivity type which are series-connected between the input and output terminals to turn on/off in response to an inverted signal formed by inverting the control signal,

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