CMOS RF Receiver Design for Wireless LAN Applications

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Abstract

This paper describes design techniques for RF CMOS receivers operating in the 2.4-GHz band. A direct-conversion receiver targetting spread-spectrum wireless LAN applications employs partial channel selection filtering, dc offset removal, and baseband amplification. Fabricated in a 0.6-μm CMOS technology, the receiver achieves a noise figure of 8.3 dB, IP_3 of -9 dBm, IP_2 of +22 dBm, and voltage gain of 34 dB while dissipating 80 mW from a 3-V supply. Dynamic range and linearity requirements of A/D converters used in RF receivers are also presented.

I. Introduction

Wireless local area networks (WLANs) in the 2.4-GHz range have rapidly emerged in the consumer market. Providing flexibility and reconfigurability, WLAN standards allow data rates of several megabits per second and serve as high-speed links in office buildings, hospitals, factories, etc. For high-volume portable applications such as laptop computers, both cost and power dissipation of WLAN transceivers become critical, necessitating compact, efficient solutions.

This paper describes design techniques for RF CMOS receivers to be used in WLAN applications. In order to target realistic specifications, the IEEE 802.11 standard [1] is considered as the framework. Section II reviews the standard and its circuit design implications. Section III presents the architecture and circuit details of a 2.4-GHz receiver designed for this standard and Section IV summarizes the experimental results obtained from the fabricated prototype. Section V deals with the dynamic range and linearity requirements of analog-to-digital converters (ADCs) used in RF receivers.

II. IEEE 802.11 Standard

The IEEE 802.11 RF link incorporates spread-spectrum (SS) techniques in the 2.4-GHz range. The standard offers two SS formats: frequency-hopped with Gaussian minimum shift keying (GMSK) modulation and direct sequence (DS) with quadrature phase shift keying (QPSK) modulation. The receiver reported herein is designed for the latter type.

The DS-SS standard spreads a 2-MHz channel by a factor of 11, generating an output channel 22 MHz wide. The required sensitivity across this bandwidth is -80 dBm for a frame error rate (FER) of 8×10^{-2}, indicating that the sum of the noise figure (NF) and the signal-to-noise ratio (SNR) is: $NF + SNR = 174\text{ dBm} - 10\log(22\text{ MHz}) - 80\text{ dBm} = 20.6\text{ dB}$. Assuming $SNR \approx 10$ dB for the required FER and 2 dB of loss in the front-end band-select filter, we arrive at a noise figure of 8.6 dB for the receiver.

Another specification of the standard is an adjacent channel (blocker) rejection of 40 dB when the desired channel is at -74 dBm. This translates to a 1-dB compression point of roughly -30 dBm.

III. Architecture and Circuit Design

The receiver employs a direct-conversion architecture, a choice particularly suited to the DS-SS standard because of the wide channel bandwidth. The two principal difficulties of direct conversion, namely, dc offsets and flicker noise, are treated so as to impact the performance negligibly. Other issues [2, 3] are resolved by circuit techniques. Note that local oscillator (LO) leakage to the antenna is less troublesome here if it does not desensitize other receivers because it simply appears as a "jammer" and its effect is suppressed by the spread-spectrum nature of the communication scheme.

Fig. 1 shows the receiver architecture. In addition to a low-noise amplifier (LNA) and quadrature downconversion mixers, the circuit incorporates partial channel-selection filtering, ac coupling, and baseband amplification.

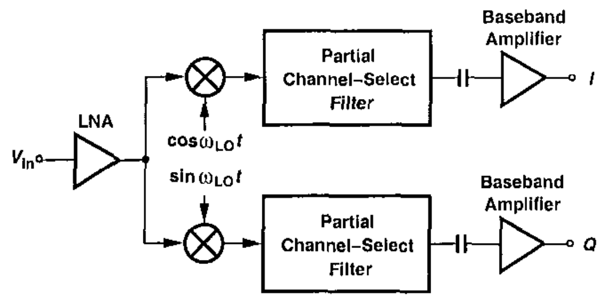

Fig. 1. Receiver architecture.

A. RF Section

The design of the LNA and the mixers is determined by not only noise, linearity, and gain requirements, but also effects related to direct conversion: LO leakage to the antenna and second-order distortion in the RF path. The configuration depicted in Fig. 2 addresses these issues. The cascode LNA reduces the LO leakage while the inductive loading in

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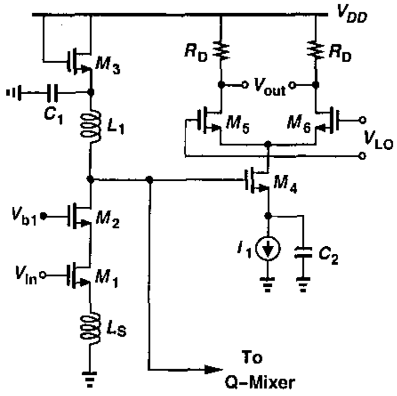

Fig. 2. LNA/mixer circuit.

the LNA and capacitive degeneration in the mixer minimize the products of second-order nonlinearity. The value of C_2 is chosen such that it exhibits a negligible impedance at 2.4 GHz but a relatively high impedance at frequencies below 11 MHz. As illustrated in Fig. 3, if two large interferers accompany the desired signal, then second-order distortion in the RF path creates a low-frequency beat that, in the presence of asymmetries in the mixer, experiences direct feedthrough to the baseband without frequency translation [4]. If the spacing between the interferers is less than 11 MHz, then the direct feedthrough component falls in the baseband, thereby corrupting the downconverted signal. In this design, on the other hand, low-frequency beats generated by the LNA are suppressed by both L_1 and C_2. Furthermore, the input transistor of the mixer, M_4, creates negligible beat components because of the large impedance of C_2 at low frequencies. The effectiveness of these techniques is evident from the measured second intercept point (IP_2) (+22 dBm).

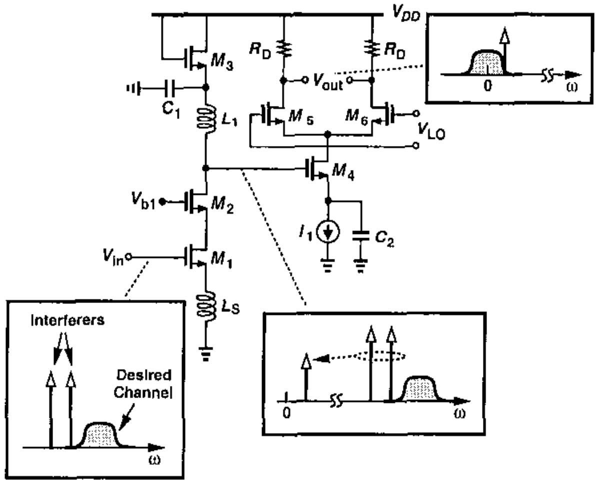

Fig. 3. Effect of second-order distortion in RF path.

B. Baseband Section

The LNA/mixer combination exhibits a gain of approximately 24 dB, mandating high linearity in the baseband amplifiers. To relax this constraint, partial channel selection filtering is interposed between the mixers and the baseband amplifiers, thus lowering the magnitude of adjacent-channel interferers. The channel-select filter must contribute little flicker noise and tolerate several tens of millivolts of dc offset that appears at the output of the mixer due to the self-mixing of the LO. A filter topology satisfying these conditions is the Sallen and Key configuration depicted in Fig. 4(a), where the amplifier is connected in unity gain and can therefore withstand large

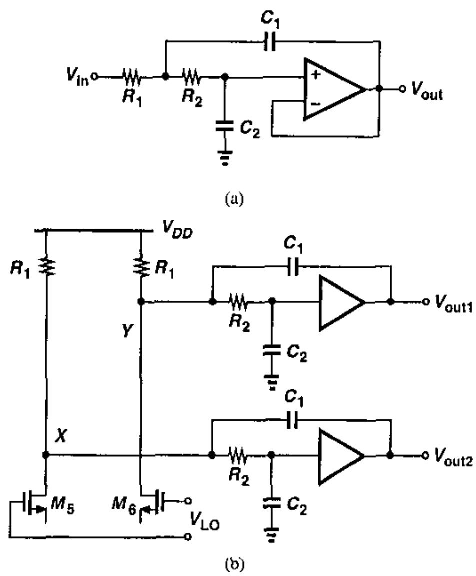

Fig. 4. (a) Simple Sallen and Key filter, (b) filter merged with output of mixer.

dc offsets. The amplifier must introduce few devices in the signal path so as to achieve low flicker noise, but it must also exhibit high linearity. For this reason, the amplifier is realized as a source follower incorporating a relatively large transistor ($W/L = 1000\ \mu\text{m}/1.2\ \mu\text{m}$).

The interface between the mixer and the subsequent filter would typically require a buffer stage with low output impedance so that the filter characteristics remain unaltered, but at the cost of substantial noise and power dissipation due to the buffer. We recognize that, since the output signal of the mixer is available in the current domain, the input network of the filter can be replaced by a Norton equivalent and merged with the mixer. Depicted in Fig. 4(b), this technique obviates the need for interstage buffers. The bottom-plate parasitic of C_1 is placed at nodes X and Y so as to suppress the LO feedthrough, which would otherwise desensitize the source follower.

The dc offsets resulting from the self-mixing of LO must be removed so as to avoid saturating the baseband amplifier. However, since QPSK signals translated to the baseband contain significant energy in the vicinity of zero frequency, the dc notch filter must provide a very low corner frequency, f_C Thus, the choice of f_C is determined by three questions: (1) How does the notch filter affect the downconverted signal? (2) How *high* can f_C be without excessive degradation of the signal? (3) How can a notch filer with such a low f_C be integrated?

The first two questions are answered by simulations of a QPSK signal (with raised-cosine filtering) that is translated to dc and applied to a first-order high-pass RC filter. Shown in Fig. 5, the output waveforms reveal that the dc notch filter

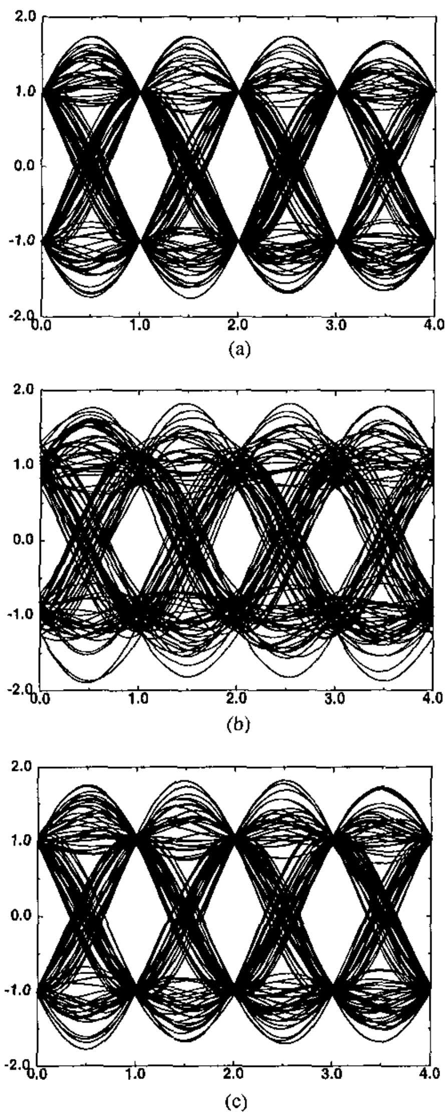

Fig. 5. Effect of high-pass filtering on QPSK data translated to baseband: (a) ideal QPSK waveform, (b) high-pass filtered data with a corner frequency equal to 1/100 of the data rate, (c) high-pass filtered data with a corner frequency equal to 1/1000 of the data rate.

introduces intersymbol interference (ISI), quite excessively if f_C is on the order of $0.01 r_S$, where r_S is the symbol rate. For $f_C \leq 0.001 r_S$, on the other hand, the eye is quite open and the residual ISI can be removed by the equalizer in the digital domain.

This design incorporates a high-pass filter with a nominal f_C of 10 kHz. Setting the maximum allowable value of the coupling capacitor to 10 pF (i.e., a total of 40 pF for differential I and Q signals), we arrive at a resistance of 1.6 MΩ [Fig. 6(a)]. Even using n-well material, such a resistor would suffer from enormous capacitance to the substrate, much greater than 10 pF! To resolve this issue, we employ MOS devices operating in deep triode region with a *well-controlled* gate-source overdrive voltage. Illustrated in Fig. 6(b), the idea is based on the observation that, for long-channel devices, the

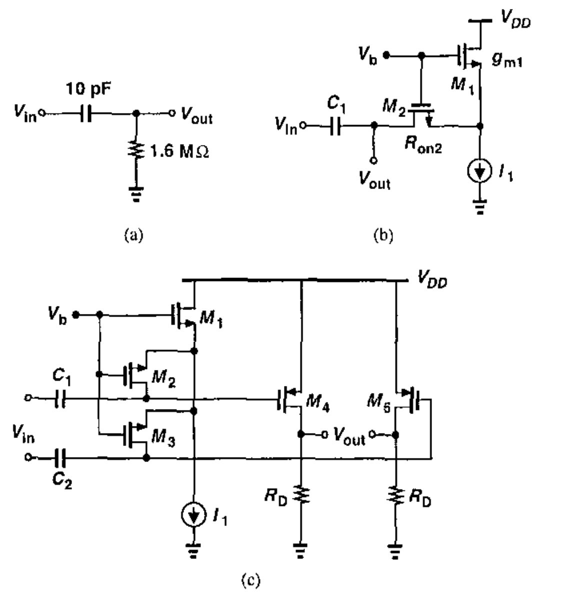

Fig. 6. (a) Simple high-pass filter with corner frequency of 10 kHz, (b) topology yielding $R_{on2} = g_{m1}^{-1}$, (c) high-pass filter along with baseband amplifier.

transconductance of a *saturated* MOSFET (M_1) is expressed by the same equation, $g_{m1} = \mu C_{ox}(W/L)(V_{GS} - V_{TH})$, as the inverse of the on-resistance of a similar device in deep triode region (M_2): $R_{on2}^{-1} = \mu C_{ox}(W/L)(V_{GS} - V_{TH})$. That is, if a saturated device and a linear device have equal overdrive voltages and equal dimensions, the on-resistance of the latter is equal to the inverse transconductance of the former. Since the transconductance of MOSFETs can be defined by means of various analog techniques, this observation makes it possible to achieve a very high on-resistance.

The design of Fig. 6(b) must nonetheless deal with two issues. First, the threshold voltage mismatch between M_1 and M_2 yields some inaccuracy in the definition of R_{on2}. For this reason, an overdrive voltage of 200 mV is chosen for the transistors, suppressing the effect of mismatches. Second, the variation of the on-resistance of M_2 with the input signal level leads to distortion. Fortunately, however, the tolerable *in-channel* distortion is quite high (several percent) because of the nature of the signal waveform, and the out-of-channel distortion is low because the coupling capacitor exhibits a low impedance at adjacent-channel frequencies. Simulated and measured in-channel and out-of-channel two-tone tests of the receiver confirm these results. Fig. 6(c) shows the differential implementation of the high-pass filter and the baseband amplifier. In this design, $(W/L)_1 = 2(1.5\ \mu\text{m}/40\ \mu\text{m})$ and $(W/L)_{2,3} = 1.5\ \mu\text{m}/40\ \mu\text{m}$.

The flicker noise in the baseband section corrupts the down-converted signal. However, since the baseband signal occupies a bandwidth of 11 MHz, flicker noise corner frequencies as high as several hundred kilohertz affect the performance negligibly. With a corner frequency of 200 kHz, we can write: $S_{1/f}(200 \text{ kHz}) = S_{th}$, where $S_{1/f}$ and S_{th} denote the power spectral densities of $1/f$ noise and thermal noise, respectively. Assuming $S_{1/f} = K/f$, where $K = (200 \text{ kHz}) \times S_{th}$, and integrating the total noise from 200 kHz to 11 MHz as in Fig. 7, we have

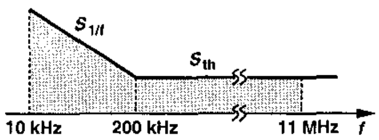

Fig. 7. Contribution of flicker noise to the overall SNR.

$$\overline{V_n^2} = \int_{10 \text{ kHz}}^{200 \text{ kHz}} \frac{K}{f} df + \int_{200 \text{ kHz}}^{11 \text{ MHz}} S_{th} df \qquad (1)$$

$$\approx (11.4 \text{ MHz}) S_{th}. \qquad (2)$$

By contrast, if the circuit suffered from no flicker noise, the total noise power would be $\overline{V_n^2} = (11 \text{ MHz})S_{th}$, only 0.2 dB lower. Note that even if flicker noise frequencies as low as 100 Hz are taken into account, the maximum degradation in SNR is less than 0.6 dB. This is a pessimistic estimate because, owing to the relatively high gain in the RF section, the $1/f$ noise corner in the baseband is expected to be quite lower than 200 kHz.

IV. Experimenal Results

The receiver has been fabricated in a 0.6-μm CMOS technology in an area of 680 μm$\times$980 μm. Both inductors used in the cascode LNA are integrated on-chip with no process modifications. The circuit is tested with a 3-V supply.

Table I summarizes the measurement results. The out-of-channel IP_3 is measured by applying two tones 22 MHz apart such that they fall at 22 MHz and 44 MHz after downconversion and their intermodulation product appears near zero frequency. Fig. 8 plots the measured transfer function of the baseband section, obtained by sweeping the RF input. Note that the corner frequency of the baseband dc notch filter is approximately equal to 7 kHz, confirming the feasibility of the circuit topology shown in Fig. 6(c).

Input Frequency	2.4 GHz
Noise Figure	8.3 dB
IP2	+22 dBm
In-Channel IP3	−9 dBm
1-dB Compression Point	−21 dBm
Out-of-Channel IP3	−4 dBm
Voltage Gain	34 dB
LO Leakage	−47 dBm
Output Offset Voltage	7 mV
Power Dissipation	80 mW

Table 1. Measured performance of receiver at 2.4 GHz.

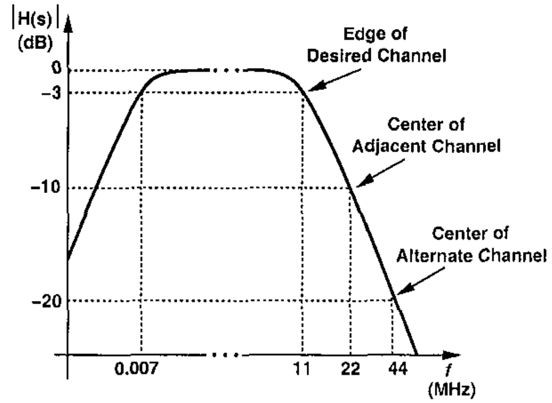

Fig. 8. Measured baseband transfer function. (Axes not to scale)

V. ADC Requirements

The digitization of the received signal can in principle take place at the antenna, at the intermediate frequency (IF), or in the baseband. The required performance of the ADC in each case is determined by the signal dynamic range as well as the number and power of the interferers. Thus, both automatic gain control (AGC) and channel-selection filtering can relax the ADC specifications.

The ADC parameters of interest in an RF receiver include resolution, linearity, full-scale voltage, noise floor (quantization, thermal, and flicker noise), sampling rate, and power dissipation. For our subsequent calculations, we review the definitions of linearity in analog design and RF design.

Assuming a fully-differential architecture for the ADC and representing its input/output characteristic by

$$V_{out}(t) \approx \alpha_1 V_{in}(t) + \alpha_3 V_{in}^3(t), \qquad (3)$$

we define the integral nonlinearity (INL) as the maximum deviation of V_{out} from a straight line passed through the end points of the characteristic (Fig. 9). Here, the end points are given by the full-scale voltage V_{FS}: $(+V_{FS},\ +\alpha_1 V_{FS} + \alpha_3 V_{FS}^3)$ and $(-V_{FS},\ -\alpha_1 V_{FS} - \alpha_3 V_{FS}^3)$. Thus, the straight line can be expressed as

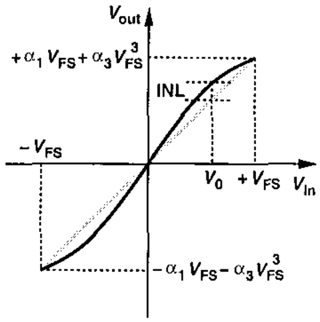

Fig. 9. Definition of INL.

$$V_{out1} = \frac{\alpha_1 V_{FS} + \alpha_3 V_{FS}^3}{V_{FS}} V_{in}. \qquad (4)$$

Subtracting V_{out1} from V_{out} and taking the derivative of the result with respect to V_{in}, we obtain the input level V_{in0} at which the nonlinearity is maximum: $V_{in0} = V_{FS}/\sqrt{3}$, and the maximum nonlinearity as $INL = 2|\alpha_3|V_{FS}^2/(3\sqrt{3})$. Approximating the output full scale by $2\alpha_1 V_{FS}$ and normalizing $|INL|$ to this value, we have:

$$INL_{norm} = \frac{1}{3\sqrt{3}}\left|\frac{\alpha_3}{\alpha_1}\right|V_{FS}^2. \tag{5}$$

Note that the concept of full scale is central to the definition of nonlinearity in analog design but not utilized in RF design.

The most significant effect of (odd-order) nonlinearity from the RF design point of view is intermodulation. If two interferers $V_{int1}(t) = V_{int}\cos\omega_1 t$ and $V_{int2}(t) = V_{int}\cos\omega_2 t$ experience the nonlinearity described by (3), then the intermodulation products are given by

$$V_{out,IM} = \frac{3\alpha_3}{4}V_{int}^3[\cos(2\omega_1 - \omega_2)t + \cos(2\omega_2 - \omega_1)t]. \tag{6}$$

Equations (5) and (6) prove useful in our subsequent derivations.

A. *Digitization at RF*

As a simple case, we first assume the ADC directly digitizes the signal and the interferers at the antenna. In order to compute the resolution, full scale, and linearity, we consider a typical test for GSM receivers. The results can easily be scaled for other standards as well. As shown in Fig. 10, a −98-dBm signal is accompanied by two interferers located two and four channels away. GSM requires that in such a test the signal-to-noise ratio at the end of the receiver be at least 9 dB, restricting both the noise figure and intermodulation behavior of the overall receiver. For simplicity, we assume each interferer has a magnitude of −50 dBm.

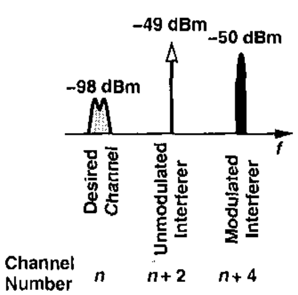

Fig. 10. Intermodulation test in GSM.

ADC Resolution. The resolution is determined by the minimum signal level. To ensure that the ADC corrupts the signal negligibly, we assume the quantization noise must be approximately 20 dB below the signal level, arriving at a resolution of about 3 bits. This yields a least significant bit (LSB) equal to 0.995 μV (in a 50-Ω system).

The thermal noise floor of the ADC is also critical. For a channel bandwidth of 200 kHz in GSM, we calculate the input-referred thermal noise density of the ADC such that the total noise is approximately 20 dB below the minimum signal level. Thus, $10\log(V_{n,in}^2/\Delta f) = -118$ dBm $- 10\log(200$ kHz$) = -171$ dBm/Hz, suggesting that an extremely low noise floor (0.629 nV/$\sqrt{\text{Hz}}$) is required.

The full-scale voltage of the ADC is given by the maximum input level. In the simple test of Fig. 10, the two interferers generate a maximum swing of approximately −50 dBm +6 dB = −44 dBm (3.99 mV$_{pp}$ in a 50-Ω system). Note that this means $2V_{FS} = 3.99$ mV in Fig. 9.

The above calculations reveal that an ADC digitizing a GSM signal along with −50-dBm interferers at the antenna would require an LSB of 0.995 μV and a full-scale voltage of 3.99 mV, i.e., a resolution of approximately 12 bits.

ADC Linearity. In order to determine the linearity required of the ADC, we assume the two interferers must create an intermodulation product at least 20 dB below the signal level. From (6), the signal-to-intermodulation ratio at the output can be expressed as:

$$\frac{\text{Signal}}{\text{Intermodulation}} = \frac{|\alpha_1|V_{min}}{(3/4)|\alpha_3|V_{int}^3}, \tag{7}$$

where V_{min} denotes the peak amplitude of the minimum input signal level, i.e., the receiver sensitivity. Setting (7) equal to 10 yields $\alpha_3/\alpha_1 = 2V_{min}/(15V_{int}^3)$. It follows from (5) that

$$INL_{max} = \frac{1}{3\sqrt{3}}\frac{2}{15}\frac{V_{min}V_{FS}^2}{V_{int}^3} \tag{8}$$

$$= \frac{2}{45\sqrt{3}}\frac{V_{min}V_{FS}^2}{V_{int}^3}. \tag{9}$$

This equation expresses the maximum allowable nonlinearity in terms of the sensitivity, full-scale voltage, and interferer levels. In a 50-Ω system, each of the −50-dBm interferers has a peak amplitude of $V_{int} \approx 1$ mV and the minimum input level has a peak amplitude of $V_{min} \approx 4$ μV. Thus, with $2V_{FS} = 4$ mV, we have $INL_{max} = 4.11 \times 10^{-4}$, i.e., a linearity of approximately 11.3 bits.

An important result of (9) is that the required linearity does not change with preamplification because both the numerator and the denominator scale by the third power of the voltage gain. For this reason, amplifier stages interposed between the antenna and the ADC relax the noise floor and offset requirements but not the linearity requirement.

In summary, our simple GSM example demands an ADC with a resolution of 12 bits, an LSB size of 0.995 μV, a thermal noise floor of 0.629 nV/$\sqrt{\text{Hz}}$, and a linearity of 11.3 bits. While the necessary dynamic range and linearity do not seem prohibitive, the small magnitudes of the LSB and the input-referred noise present great difficulty in the design.

In practice, both the resolution and the linearity may need to be higher than those calculated above. Depending on the type of AGC, the maximum received signal level may demand a greater full scale. Also, more than two interferers may be received, necessitating a higher linearity. This is particularly important in time-division duplexing (TDD) systems such as

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