A 1.5 GHz Highly Linear CMOS Downconversion Mixer

Jan Crols, *Student Member, IEEE* and Michel S. J. Steyaert, *Senior Member, IEEE*

***Abstract*—A CMOS mixer topology for use in highly integrated downconversion receivers is presented. The mixing is based on the modulation of nMOS transistors in the triode region which renders an excellent linearity independent of mismatch. With two extra capacitors added to the classical cross-coupled MOSFET-C lowpass filter structure, GHz signals can be processed while only a low-frequency opamp is required as output amplifier. The downconversion mixer has an input bandwidth of 1.5 GHz. The measured third-order intercept point (IP3) of 45.2 dBm demonstrates the high linearity. The mixer has been implemented in a 1.2 μm CMOS process. It takes up 1 mm^2 of total chip area and its power consumption is 1.3 mW from a single 5 V power supply.**

I. Introduction

THE NEED FOR highly integrated receivers in the 1–2 GHz range has grown considerably with the introduction of new wireless telecommunication services like digital cellular telephone. Key issues in the design of receivers for these applications are the quality of the signal reception, the level of integration, the power consumption and the cost prize. Several realizations of the RF part for these receivers have been presented in the past [1]–[4]. They are all realized in either a GaAs or Si bipolar process. The use of the bipolar technology is often prefered over GaAs for its lower cost prize and equally good performance in the 1–2 GHz range. A further integration, i.e., combining the analog RF, the analog LF and the digital part on one chip, will be the next goal. The analog LF and the digital part are preferably realized in a CMOS technology. Combining these with the RF part would require the use of a BiCMOS technology and although these technologies are ever more used in telecommunication applications, they are not suited for the realization of receivers for frequencies above 1 GHz. The quality of the bipolar devices is in todays BiCMOS processes not sufficient. The value of their f_t and more important of their r_b is not so good as what is available in bipolar only processes. At this time, using CMOS is the only way to obtain a further and full integration. With the ongoing further decreasing of CMOS gatelengths this becomes ever more feasible [5]–[8].

In this paper a full CMOS downconversion mixer is presented. It is a key building block for the realization of a fully integrated CMOS 1 GHz zero-IF receiver. The presented downconversion mixer is not only important for the fact that it is implemented in CMOS, its linearity is also much better than any bipolar or GaAs realization that has been previously presented. A CMOS 1 GHz downconversion mixer has been proposed before [5], but it was based on the use of subsampling. Such a circuit can only cope with smallband input signals, resulting in the need for the use of a high-quality HF filter which can not be realized in an integrated way. The mixer which is presented in this paper is a true double balanced multiplier, capable of downconverting broadband input signals by multiplication with a sinusoidal local oscillator.

The second section of this paper describes the topology of the presented downconversion mixer. The topology is based on the use of four cross-coupled CMOS transistors operated in the triode region and connected to a virtual ground point [6]. Two important capacitors of 25 pF have been added to this topology on the virtual ground points. With these capacitors it becomes possible to realize a very high input bandwidth (as high as 1.5 GHz) with the use of a low-frequency opamp (10 MHz). The third and fourth part of this text describe the design aspects. The fifth and sixth part are respectively on the noise capabilities of the presented structure and the relationschips between linearity, noise and power consumption. The last two parts describe the practical realization and the measurement results.

II. Mixer Topology

The linearity of an RF mixer is in most cases rather limited. The Gilbert topology is the most common used in a bipolar technology [9]. Its operation is based on a translinear configuration, i.e., the use of the exponential voltage to current conversion of the bipolar transistor. Techniques like predistortion and emittor degeneration are necessary to obtain a reasonable linearity. Imperfections in this structure combined with a limited matching will render a third-order intercept point (IP3) which can only be slightly larger than 0 dBm [10]. In CMOS a double balanced structure which cancels out the quadratic term of the MOS transistor can be used [11], [12]. These mixer have not only a limited linearity which highly depends on matching, even more important is their limited frequency range. The input transistors of these mixers can only be biased with a relatively small $V_{GS} - V_T$ in order to keep them in saturation at all times. The result is large input transistors which limits the maximal achievable input bandwidth to about 100 MHz.

A better solution is to use the transistors in the linear region, preferably with a large $V_{GS} - V_t$. In this way a small R_{on} can be realized with a small transistor, allowing a high input bandwidth. This property has been used to realize high frequency GaAs commutating mixers [13]. The

Manuscript received December 20, 1994; revised April 11, 1995.
The authors are with the Katholieke Universiteit Leuven, ESAT-MICAS, Kardinaal Mercierlaan 94, B-3001 Heverlee, Belgium.
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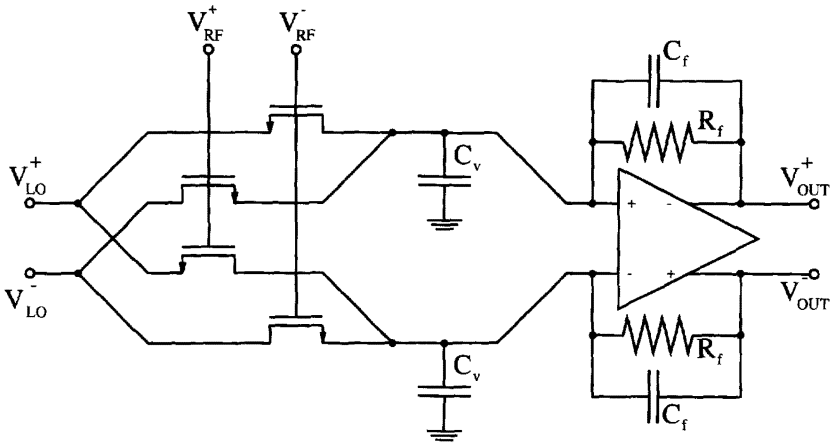

Fig. 1. The mixer topology with the extra capacitor on the virtual ground nodes.

transistors are being used as pass-transistors and the linearity of these mixers does therefore not depend on the voltage to current conversion characteristic of the transistors. The linearity is mainly determined by the speed limitation of the pass-transistor and by the generation of spurious signals during switching. This technique can also be used in CMOS. The output signal after commutation is however still a high-frequency signal and it can therefore not be further processed in CMOS. However, receivers only require a downconversion mixer and this means that the output bandwidth may be limited. A solution based on subsampling with a switched-capacitor structure has been proposed in [5]. The MOS-transistors are used as pass-transistors and an IP3 of 27 dBm has been reported.

A CMOS mixer with very high linearity can be realized by using the linear voltage to current charateristic of the MOS transistor in its triode region [6]. The use of a double balanced structure cancels out the common-mode dc biasing signals and the nonlinear dependence of g_{DS} on V_{DS}. The remaining problem is still the further processing of the high-frequency output current. This limits in [6] the bandwidth to 200 MHz at the cost of a high power consumption and a reduced linearity of the output stage. The mixer presented in this paper is based on this topology (see Fig. 1). There are however two very important capacitors added on the virtual ground nodes of this topology (the capacitors C_v in Fig. 1). Indeed, the output stage, the opamp and the feedback resistors, which convert the output current of the mixing transistors back into a voltage, must, in a downconversion mixer, only be able to produce low-frequency output signals. However, in order to let the input structure operate correctly for all frequencies, there may not be a signal on the virtual ground nodes of the mixer at any time. This is normally done with the feedback structure over the opamp which creates the virtual ground at its inputs. The transistors in the input structure would operate as pass-transistor for high-frequency signals when the frequency capability of the opamp would not be high enough. Therefore the capacitors C_v have been added. They make sure that all high-frequency currents injected to the virtual ground nodes are filtered out and not converted into voltages. The opamp still generates the virtual ground for low-frequencies. By using this structure, it becomes possible to split the design of the input structure and the opamp. The input structure can now be optimized for operation at very high frequencies (more than 1 GHz), while the opamp can be designed for low-frequency operation (a few MHz).

With a perfect virtual ground the currents through the modulated transistors are

$$\begin{aligned}
I_{DS,1} &= \beta_1 \cdot \left(V_{RF}^{+} - V_{LO,DC} - V_{Tn1} - \frac{V_{LO}^{+} - V_{LO,DC}}{2}\right) \\
&\quad \cdot (V_{LO}^{+} - V_{LO,DC}) \\
I_{DS,2} &= \beta_2 \cdot \left(V_{RF}^{-} - V_{LO,DC} - V_{Tn,2} - \frac{V_{LO}^{-} - V_{LO,DC}}{2}\right) \\
&\quad \cdot (V_{LO}^{-} - V_{LO,DC}) \\
I_{DS,3} &= \beta_3 \cdot \left(V_{RF}^{+} - V_{LO,DC} - V_{Tn,3} - \frac{V_{LO}^{-} - V_{LO,DC}}{2}\right) \\
&\quad \cdot (V_{LO}^{-} - V_{LO,DC}) \\
I_{DS,4} &= \beta_4 \cdot \left(V_{RF}^{-} - V_{LO,DC} - V_{Tn,4} - \frac{V_{LO}^{+} - V_{LO,DC}}{2}\right) \\
&\quad \cdot (V_{LO}^{+} - V_{LO,DC}). \qquad (1)
\end{aligned}$$

The bulk effect gives in first order a linear change around the bias point which is cancelled with the double balanced structure [6]. Assuming perfect matching and no bulk-effect, the output signal is then

$$\begin{aligned}
V_{out}^{+} - V_{out}^{-} &= R_f \cdot ((I_1 - I_4) - (I_3 - I_2)) \\
&= \beta \cdot R_f \cdot (V_{RF}^{+} - V_{RF}^{-}) \cdot (V_{LO}^{+} - V_{LO}^{-}). \qquad (2)
\end{aligned}$$

Mismatch between the input transistors has two effects. β and V_T mismatches both result in the appearance of residual dc-offset voltages. These offset voltages either appear directly on the output of the mixer or they result in direct feedthrough of the RF and LO signal to the output caused by multiplication

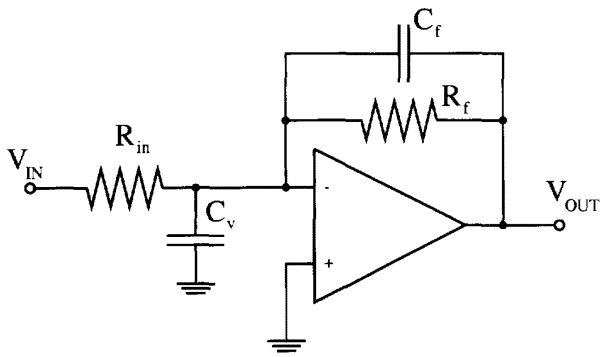

Fig. 2. The negative feedback configuration.

of these signals with the offset voltage. The RF and LO signal are however high-frequency signals. They will therefore be strongly suppressed by the added capacitors C_v. The second effect, caused by β mismatch, is the appearance of a quadratic V_{LO} component in the output signal.

$$V_{\mathrm{out}}^{+} - V_{\mathrm{out}}^{-} = \beta \cdot R_f \cdot (V_{\mathrm{RF}}^{+} - V_{\mathrm{RF}}^{-})(V_{\mathrm{LO}}^{+} - V_{\mathrm{LO}}^{-}) + \Delta\beta \cdot R_f \cdot (V_{\mathrm{LO}}^{+} - V_{\mathrm{LO}}^{-})^2. \quad (3)$$

This explains why the RF signal is best applied to the gates of the modulating transistors. A quadratic V_{RF} component would be highly unwanted. The squared RF signal has frequency components at twice its center frequency and at the baseband. The high-frequency components are filtered out, but the baseband components will degrade the wanted baseband signal. The bandwidth of this parasitic baseband signal is equal to the bandwidth of the RF signal (e.g., 100 MHz), but most of its power will be situated at the lower frequencies, in a band equal to the correlation bandwidth of the RF signal, which is about equal to the bandwidth of a transmission channel (e.g., 200 kHz). The squared LO signal results only in an extra dc component at the output of the opamp. This dc signal can also be a problem. It can be as large as the wanted signal and in that case it will saturate the succeeding filters. There are however techniques available to suppres the dc component without generating to much distortion. One of them is the use of a DSP which measures the dc component and then suppresses it, using a dynamic and nonlinear algoritm [14].

III. Mixer Design

The dc biasing levels of the RF and LO signal must be chosen carefully. There will be a lot of distortion when the modulating transistors are not kept in the triode region at all times. The smallest possible level that can appear at the gates (i.e., $V_{\mathrm{RF,DC}} - V_{\mathrm{RF,AC}}$) must be at least a V_T higher than the largest possible source level (i.e., $V_{\mathrm{LO,DC}}$). Otherwise the transistors will be turned off during a mixing period. Saturation of the modulated transistors will appear when the largest drain-source voltage V_{DS} (i.e., $V_{\mathrm{LO,AC}}$) becomes higher than the smallest $V_{\mathrm{GS}} - V_T$ (i.e., $V_{\mathrm{RF,DC}} - V_{\mathrm{RF,AC}} - V_{\mathrm{LO,DC}} - V_T$). However, saturation does not directly result in distortion. The cross-coupled double balanced structure makes sure that all quadratic components in the voltage to current conversion characteristic of the modulated transistors are cancelled out [9], [10]. The LO dc level is taken to be 1.15 V, making the maximal LO signal that can be applied 4.6 V_{ptp} differential (i.e., 17.2 dBm). An RF dc level of 3.85 V allows an input signal of 4 times $V_{\mathrm{RF,DC}} - V_{\mathrm{LO,DC}} - V_T$, which gives 8 V_{ptp} differential or 22.0 dBm for the 1.2 μm CMOS process which has been used for the mixer which is presented here. These are very high values for an RF mixer, resulting in a topology which renders an excellent linearity. Saturation will occur when $V_{\mathrm{RF}} + V_{\mathrm{LO}} > 8$ V_{ptp}. The applied LO signal is for this reason limited to 2.5 V_{ptp}, so that an RF signal of 5.5 V_{ptp} still can be applied without driving any of the modulated transistors into its saturation region.

IV. Frequency Domain Behavior

The well known negative feedback configuration of Fig. 2 suppresses any signal at the virtual ground node when a perfect opamp is used. An opamp has however always a limited gain-bandwidth GBW and dc-gain A_0. With a limited GBW becomes the transfer function from the input to the virtual ground (A_0, C_f, and C_v are not taken into account)

$$\frac{V_v}{V_{\mathrm{in}}} = \frac{\frac{R_f}{R_{\mathrm{in}}} \cdot j\frac{\omega}{2\pi \cdot \mathrm{GBW}}}{1 + \frac{R_f + R_{\mathrm{in}}}{R_{\mathrm{in}}} \cdot j\frac{\omega}{2\pi \cdot \mathrm{GBW}}} \approx \frac{A \cdot j\frac{\omega}{2\pi \cdot \mathrm{GBW}}}{1 + A \cdot j\frac{\omega}{2\pi \cdot \mathrm{GBW}}}. \quad (4)$$

The transfer function from the input to the output is

$$\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{-\frac{R_f}{R_{\mathrm{in}}}}{1 + \frac{R_f + R_{\mathrm{in}}}{R_{\mathrm{in}}} \cdot j\frac{\omega}{2\pi \cdot \mathrm{GBW}}} \approx \frac{-A}{1 + A \cdot j\frac{\omega}{2\pi \cdot \mathrm{GBW}}}. \quad (5)$$

Normally, the conclusion to be drawn from these equations is that the GBW must be a certain factor higher than the highest frequency component that has to be processed. This is also true if the circuit would be used as lowpass filter with an extra capacitor C_f in the feedback loop. However, here in the mixer topology is the situation different. There is a very large spectrum of input currents to the virtual ground node, basically starting from dc up to twice the LO frequency (more than 2 GHz), but the wanted signal takes up only a few hundred kHz situated at the baseband. The output bandwith BW, given in (5) as GBW/A, only has to be 500 kHz or more. By designing it to be 1 MHz this specification is fulfilled independent of absolute parameter variations. Equation (5) shows that this limited bandwidth can be realized by using an opamp with a small GBW. In combination with a feedback capacitor C_f can the bandwidth be lowered further and can it be positioned more accurately. The use of an opamp with a small GBW poses however a problem. As (4) reflects, beyond the BW is the input signal directly transferred to the virtual ground node. It is not suppressed anymore by the opamp via the feedback construction. The solution for this problem can

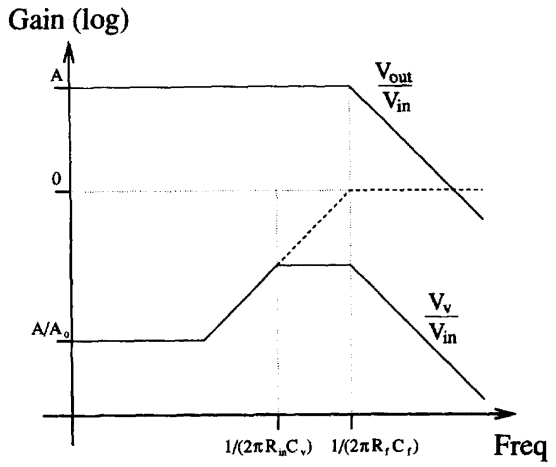

Fig. 3. Transfer function of the mixer used as amplifier.

be found in adding extra capacitance to the virtual ground nodes. This introduces an extra pole in both (4) and (5) situated at $1/(2\pi \cdot R_{in}C_v)$. In order to suppres the signals appearing on the virtual ground without changing the output bandwidth, its value must be positioned between $1/(2\pi \cdot R_f C_f)$ and the BW. Fig. 3 displays the transfer function from the input to the virtual ground and the output.

V. Noise, Power Consumption, and Optimization

The noise figure (NF) of the HF mixer is a very important parameter in receiver design. In a receiver is the mixer positioned directly after the LNA and a mixer with a high NF can only be used in combination with a high-quality LNA. In this case the LNA must have a high gain which, in turn, can only be allowed when the antenna signal is first filtered with a high Q HF filter. The problem with mixers is that its NF can not be made arbritrarely small. Their NF can not even be in the proximity of the NF's that can be achieved with LNA's. This is due to the intrinsic nature of the mixing process.

The two main noise sources in the presented mixer are the modulated input transistors in the triode region and the input stage of the LF opamp. The thermal output noise density generated by these devices is (with the factor 2 introduced by the differential operation)

$$dv_{out}^2 = 2 \cdot 4kT \cdot \left(\frac{2}{3} \cdot \frac{1}{g_{m,in,eq}} \cdot (R_f \cdot 2g_{DS})^2 + 2g_{DS} \cdot R_f^2 \right) \cdot df. \quad (6)$$

Equation (6) gives the output noise density for the mixer biased in its static operation point. The modulated transistors have however, under transient conditions, always the same impedance ($2g_{DS}$) to the virtual ground nodes. For this reason is (6), for the presented topology, also a good measure for the output noise density under transient operation conditions. The equivalent input noise can be found by deviding this expression by the conversion gain G. The conversion gain is defined as the ratio of the output signal over the input signal $(V_{out}^+ - V_{out}^-/V_{RF}^+ - V_{RF}^-)$ and follows from (2):

$$G = \frac{(V_{out}^+ - V_{out}^-)_{ptp}}{(V_{RF}^+ - V_{RF}^-)_{ptp}} = \frac{1}{\sqrt{2}} \cdot \frac{1}{\sqrt{2}} \cdot \beta \cdot R_f \cdot (V_{LO}^+ - V_{LO}^-)_{ptp}. \quad (7)$$

The first $\sqrt{2}$ appears because the multiplication is performed with a sine and not a square wave. This implies that the rms value of the LO signal has to be used. The second $\sqrt{2}$ is necessary because only the low-frequency mixing product is regarded as wanted. Deviding (6) by (7) results in

$$\begin{aligned} dv_{in}^2 = \frac{1}{G^2} \cdot dv_{out}^2 &= \left(\frac{2}{R_f \cdot \beta \cdot (V_{LO}^+ - V_{LO}^-)_{ptp}} \right)^2 \cdot dv_{out}^2 \\ &= 8kT \cdot \left(\frac{4g_{DS}}{\beta \cdot (V_{LO}^+ - V_{LO}^-)_{ptp}} \right)^2 \\ &\quad \cdot \left(\frac{2}{3} \cdot \frac{1}{g_{m,in,eq}} + \frac{1}{2g_{DS}} \right) \cdot df \\ &\equiv 8kT \cdot \left(2 \cdot \frac{2g_{DS}}{\Delta g_{DS}} \right)^2 \cdot \left(\frac{2}{3} \cdot \frac{1}{g_{m,in,eq}} + \frac{1}{2g_{DS}} \right) \cdot df. \end{aligned} \quad (8)$$

The factor $4g_{DS}/\Delta g_{DS}$ is the extra term intrinsic to any mixer or double balanced structure. It is equal to the ratio between the gain of the mixer used as single balanced amplifier and the conversion gain A/G. For low noise, this term should be as low as possible. The noise can also be lowered by using a larger $g_{m,in,eq}$ and g_{DS}, but this is at the expense of a higher power consumption. The minimal value for this extra term is found when the swing of the LO signal is maximal.

$$\frac{A}{G} = 2 \cdot \frac{2g_{DS}}{\Delta g_{DS}} = \frac{4 \cdot \beta \cdot (V_{GS} - V_T)}{\beta \cdot (V_{LO}^+ - V_{LO}^-)_{ptp}} = 4 \cdot \frac{V_{RF,DC} - V_{LO,DC} - V_T}{(V_{LO}^+ - V_{LO}^-)_{ptp}} \quad (9)$$

$$\left(\frac{A}{G} \right)_{min,RF@gates} = \frac{4 \cdot (V_{RF,DC} - V_{LO,DC} - V_T)}{2 \cdot V_{LO,DC}} \quad (10)$$

$$\left(\frac{A}{G} \right)_{min,LO@gates} = \frac{4 \cdot (V_{RF,DC} - V_{LO,DC} - V_T)}{2 \cdot (V_{RF,DC} - V_{LO,DC} - V_T)} = 2. \quad (11)$$

So, according to (11) for the case in which the LO signal is applied to the gates of the modulated transistors, this means that the mixing function adds at least 6 dB to the NF. For the rest is the NF directly determined by the conductivity of a single modulated transistor (g_{DS}) and by the transconductance value of the opamp input stage ($g_{m,in,eq}$), just like in any other amplifier with negative feedback. The noise of the opamp input stage can be made sufficiently small without requiring too much power by using large input transistors (and a small $V_{GS} - V_T$). This is possible because the opamp only has to be LF and there is already standing 25 pF (C_v) at the input nodes. The value of g_{DS} can not be made arbitrarely large because this conductor has to be driven by the LO.

From (10) it might seem that the NF can be made arbitrarely small when the RF signal is applied to the gates by taking $V_{RF,DC} - V_T < 2 \cdot V_{LO,DC}$. This implies however a reduction of the input swing and in this way the dynamic range (DR) at the input is not improved. It is not only necessary to minimize the NF of a mixer. It is the input signal capability (i.e., the DR) which must be compared with the power consumption. A good measure for the performance of a mixer is therefore the DR per Watt. Here this gives

$$\left(\frac{\mathrm{DR}}{P}\right)_{\mathrm{RF@gates}} = \left(\frac{S}{N}\right)^2 \cdot \frac{1}{P} = \frac{(V_{RF,DC} - V_{LO,DC} - V_T)^2}{8kT \cdot \left(\frac{A}{G}\right)^2 \cdot \frac{1}{2g_{DS}} \cdot \mathrm{BW}} \cdot \frac{1}{(V_{LO}^+ - V_{LO}^-)^2 \cdot g_{DS}} = \frac{1}{16 \cdot 4kT \cdot \mathrm{BW}}. \quad (12)$$

Equation (12) takes does not take the power consumption and the noise of the opamp into account. Only a low-frequency opamp is needed and its power consumption and noise can therefore be made sufficiently small. $4kT \cdot$ BW is the intrinsic noise power of a signal with bandwidth BW and the noise of any electronic buiding block with input bandwidth BW can thus never be lower than this value. The factor 1/16 can herefore be defined as the power efficiency for this mixer. It is independant of the choosen input swing, noise level, input bandwidth, or power consumption. In fact, this power efficiency depends, for the presented topology and in first order, only on the topology itself and it can be defined for many other building blocks likes LNA's, amplifiers, filters, A/D converters and any other type of mixer.

$$\eta = \frac{S_{\mathrm{input}}^2}{P_{\mathrm{total}}} \cdot \frac{P_{\mathrm{intrinsic\ noise}}}{N_{\mathrm{input}}^2} \left[\frac{V^2}{\mathrm{Watt}} \cdot \frac{4kT}{V^2/\mathrm{Hz}} = \mathrm{dimensionless}\right]. \quad (13)$$

The power efficiency of a high-quality low-frequency amplifier can be almost 50%. The power efficiency of the presented mixer topology, not taking the power efficiency of the LO signal source into account, is almost 6% and this is, for high-frequency mixers, a very high value.

Equation (12) is slightly different when the LO signal instead of the RF signal is applied to the gates of the modulated transistors

$$\left(\frac{\mathrm{DR}}{P}\right)_{\mathrm{LO@gates}} = \frac{S}{N} \cdot \frac{1}{P} \frac{V_{LO,DC}^2}{8kT \cdot \left(\frac{A}{G}\right)^2 \cdot \frac{1}{2g_{DS}} \cdot \mathrm{BW}} \cdot \frac{1}{4 \cdot V_{LO,DC}^2 \cdot g_{DS}}. \quad (14)$$

And only when A/G is minimal this reduces to

$$\left(\frac{\mathrm{DR}}{P}\right)_{\mathrm{LO@gates}} = \frac{1}{16 \cdot 4kT \cdot \mathrm{BW}}. \quad (15)$$

The main difference is that in this case the efficiency of 6% is only obtained with the maximal LO signal. The efficiency of 6% is in the situation of (12) always obtained, independant of the amplitude of the LO signal. This is caused by the fact that, when the LO signal is applied to the sources of the modulated transistors, a lower conversion gain is compensated by a lower power consumption for the LO signal source. This is another reason why the topology with the RF signal applied to the gates is preferred over the topology in which the LO signal is applied to the gates of the modulated transistors.

VI. Realization

The mixer has been designed and realized in a 1.2 μm CMOS process to illustrate the high linearity and high input frequency capabilities of the proposed topology. The RF and LO signal are externally made differential by means of baluns. They are, as stated in Section III, chosen to be biased at, respectively, 3.85 V (for the RF signal, applied at the gates) and 1.15 V (for the LO signal, applied at the sources and drains) because this renders a $V_{GS} - V_T$ for the modulated transistors of 2.5 V. Such a large value for the $V_{GS} - V_T$ results in an excellent linearity and a high input bandwidth. The applicable voltage swing for the RF input is peak-to-peak four times this $V_{GS} - V_T$. The large $V_{GS} - V_T$ makes it also possible to realize a large g_{DS} with a small transistor, which gives small parasitic capacitances (less than 20 fF) and thus a high input bandwidth. The W/L of the modulated transistors is 6, their g_{DS} is 1 mS. These four modulated transistors are the only high frequency part on the chip and they take up very little area. Because of their small parasitic capacitances is the on-chip RF to LO crosstalk, which is mainly determined by the absolute mismatch between C_{GS} values, also very small. Hence, RF to LO crosstalk is mainly caused by off-chip crosstalk and crosstalk between the bonding wires. The input bandwidth is also completely determined by the bonding pads capacitances and as a result extremely high frequency performances can be achieved.

The opamp topology is shown in Fig. 4. It is a load compensated folded cascode structure succeeded by a source follower which performs buffering and level shifting. The opamp runs on a single 5 V power supply. The output dc level is 1.15 V. It is kept on this level with a standard type common-mode feedback. The GBW of the opamp is 100 MHz, but because of the partial feedback the second nondominant pole is situated at only 30 MHz. The feedback resistors over the opamp are 60 kΩ, which makes the conversion gain very high. The conversion gain is almost 20 dB for a 12 dBm LO signal. An extra lowpass filter of 1 MHz is implemented with the feedback capacitors C_f (2.5 pF). This small output bandwidth and the high conversion gain are required by the zero-IF structure. The extra filtering and amplification that is performed in the output stage of the mixer relaxes the

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