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I. APPENDIX B-1: EXEMPLARY EVIDENCE AND DISCUSSIONS RELATING TO THE INVALIDITY OF THE '068 PATENT IN VIEW OF SHIN, INTERNATIONAL PUBLICATION WO 2004/090853 (“SHIN”)

1. The following includes exemplary evidence and discussions from Shin relating to the asserted claims of the '068 patent.

2. In addition to the exemplary evidence and discussions below, the body of my report contains additional narrative descriptions and exemplary evidence as to Shin that supplements the disclosures below and should be considered part of this Appendix, and vice versa for this and all other appendices.

3. I have reviewed Solas's responses to Defendants' Interrogatory No. 14, and understand that Solas contends that Defendants have failed to show that any limitation of the asserted claims of the '068 patent is disclosed or rendered obvious by Shin, but has not explained any of those positions or provided facts supporting its contentions. Thus, it is not possible to understand or rebut Solas's contentions, which amount to mere conclusions lacking factual support or explanation. However, to the extent that Solas or its expert allege any facts or opinions supporting its contentions that Shin does not disclose and/or render obvious any one or more limitations of the asserted claims of the '068 patent, I may supplement my opinions below to cite additional evidence from Shin, other references, or to supplement or modify my opinions regarding the obviousness of the asserted claims in view of Shin and one or more references.

A. Independent Claim 1

1. [1pre]—“1. A transistor array substrate comprising:”

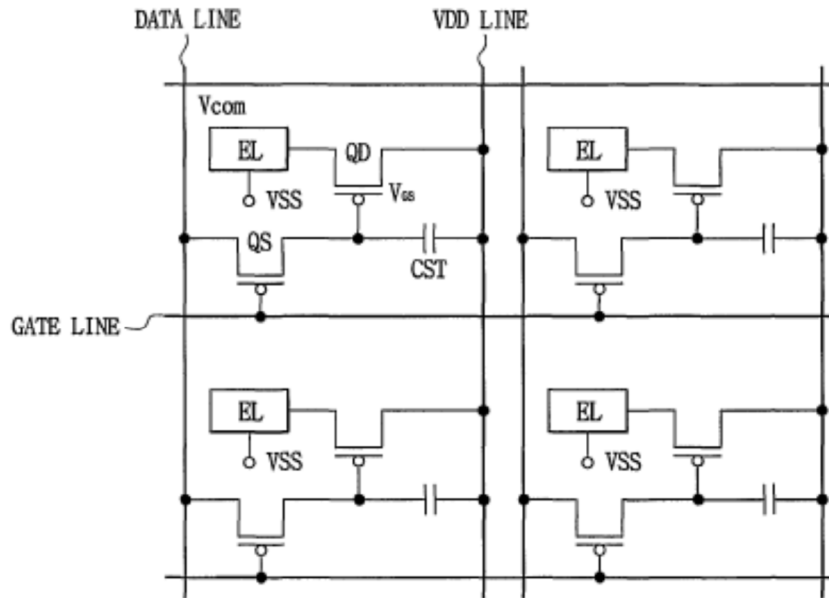
4. To the extent the preamble is limiting, Shin discloses and/or renders obvious [1pre].

5. For example, Shin discloses “an OELD panel capable of decreasing a cross-talk.”

Shin, Abstract. Shin's OELD panel, like any OELD panel, is composed of a plurality of pixels

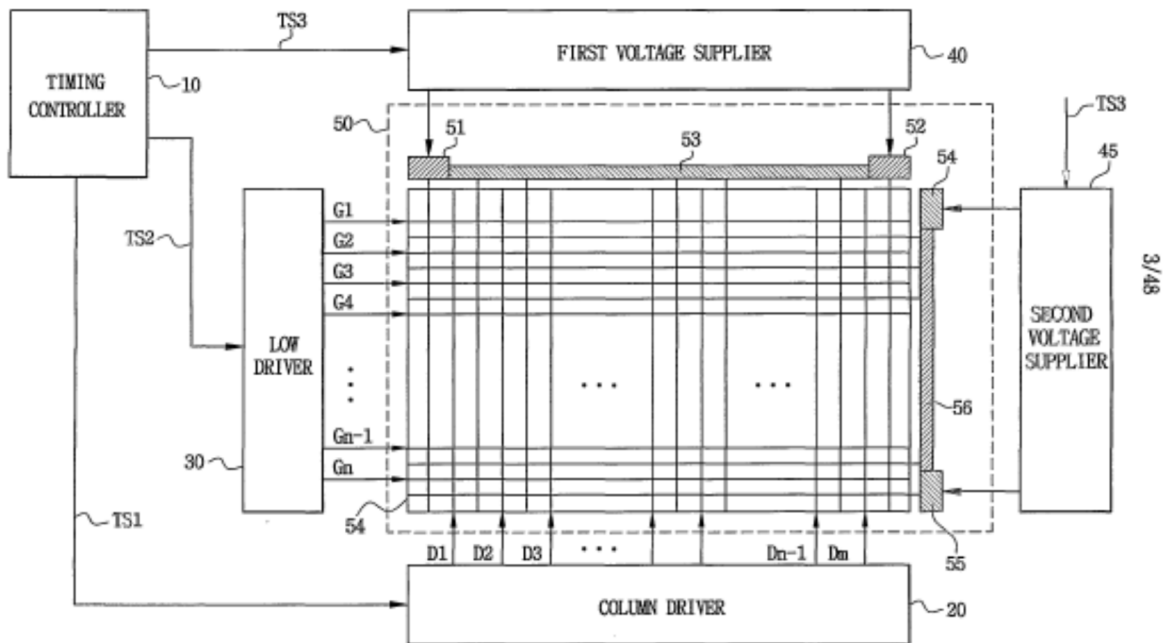
Appendix B-1 to the Expert Report of Douglas R. Holberg Regarding The Invalidity of the '891 patent, '068 patent, and '137 patent

arranged in an array of rows and columns, wherein each pixel has multiple transistors (such as “a driving transistor QD” and a “switching transistor QS”). The claimed transistor array substrate is disclosed throughout the Shin reference, for example:



Shin, Fig. 1;

FIG. 3



Shin, Fig. 3;

In addition, the organic electro luminescent panel 50 includes a plurality of data lines, a plurality of first current supply lines, a plurality of scan lines and a plurality of second current supply lines. Numbers of the data lines, the first current supply lines, the scan lines and the second current supply lines are 'm', 'm', 'n' and 'n', respectively, wherein 'm' and 'n' are positive numbers and are independent from each other. The organic electro luminescent panel 50 displays an image using the image signal that is provided from the column driver 20 in response to the scan signals that are provided from the low driver 30. A switching element (QS, not shown), a driving element (QD, not shown), an organic electro luminescent element (not shown) and a storage capacitor (Cst, not shown) are formed in a region defined by two adjacent data lines and two adjacent scan lines

Shin, 9:8-18;

The organic electro luminescent display apparatus may include a plurality of the pixels, a plurality of the scan lines, a plurality of the horizontal current supply lines, a plurality of the data lines and a plurality of the longitudinal current supply lines. The number of the

pixels that are electrically connected to each of the longitudinal current supply lines may be equal to that of the scan lines.

The p-th longitudinal current supply line (H-Vddp) is extended in the horizontal direction that is substantially in parallel with the scan line. The horizontal current supply line (H-Vddp) is electrically connected to the longitudinal current supply lines (V-Vddg and V-Vddg+1).

Shin, 25:15-23;

FIG. 19 is a plan view showing a unit pixel of an organic electro luminescent display apparatus in accordance with another exemplary embodiment of the present invention. FIG. 20 is a cross-sectional view taken along the line A1-A1' of FIG. 19.

Referring to FIGS. 19 and 20, the organic electro luminescent panel includes a scan line N10, a horizontal current supply line N30, a switching transistor (QS), a driving transistor (QD), a longitudinal current supply line N33, a first ITO pattern N40, a second ITO pattern N42, a partition wall N50, an organic electro luminescent layer N60, a counter electrode layer N70 and a protection layer N80. The organic electro luminescent panel may include a plurality of the scan lines, a plurality of the horizontal current supply lines, a plurality of the switching transistors, a plurality of the driving transistors, a plurality of the longitudinal current supply lines, a plurality of the first ITO patterns, a plurality of the second ITO patterns, a plurality of the partition walls and a plurality of the organic electro luminescent layers.

Shin, 25:24-26:10; *see also id.*, Figs. 1, 7-48 (showing transistors), claim 9 (“plurality of the unit pixels”).

6. With respect to the embodiment described with respect to Figures 18-22, the pixels and their respective transistors are formed on a “substrate N05 including an insulating material, for example, such as a glass, a ceramic, etc.”

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