



(12) **United States Patent**  
**Kawasaki et al.**

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(54) **THIN FILM TRANSISTORS HAVING LDD REGIONS**

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H01L 27/01; H01L 27/12; H01L 31/0392  
(52) **U.S. Cl.** ..... **257/350**; 257/59; 257/72;  
257/344; 257/408  
(58) **Field of Search** ..... 257/59, 72, 350,  
257/344, 392, 408

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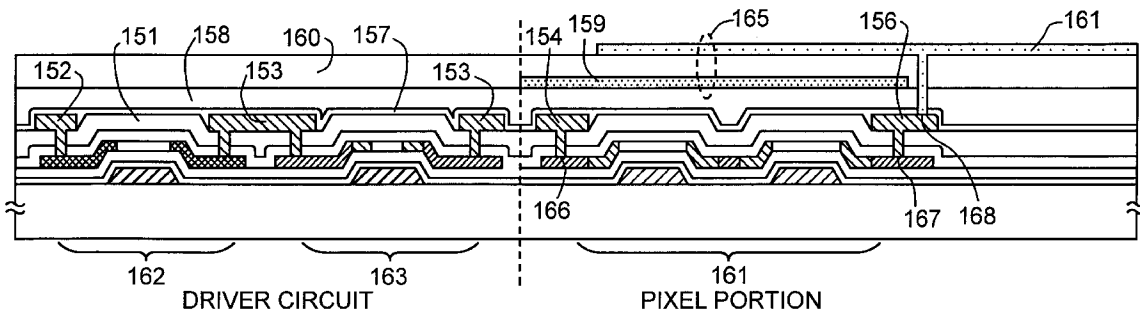
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(57) **ABSTRACT**

To improve the operation characteristic and reliability of a semiconductor device by optimizing the structure of bottom gate type or inverted stagger type TFTs arranged in circuits of the semiconductor device in accordance with the function of the respective circuits. At least LDD regions that overlap with a gate electrode are formed in an N channel type TFT of a driving circuit, and LDD regions that do not overlap with the gate electrode are formed in an N channel type TFT of a pixel matrix circuit. The concentration of the two kinds of LDD regions is differently set from each other, to thereby obtain the optimal circuit operation.

**20 Claims, 16 Drawing Sheets**



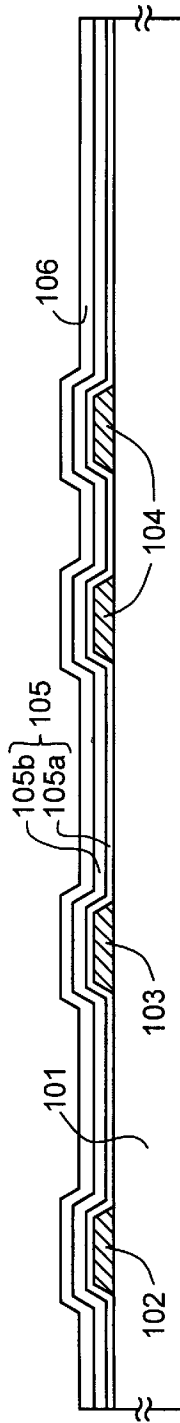


FIG. 1A

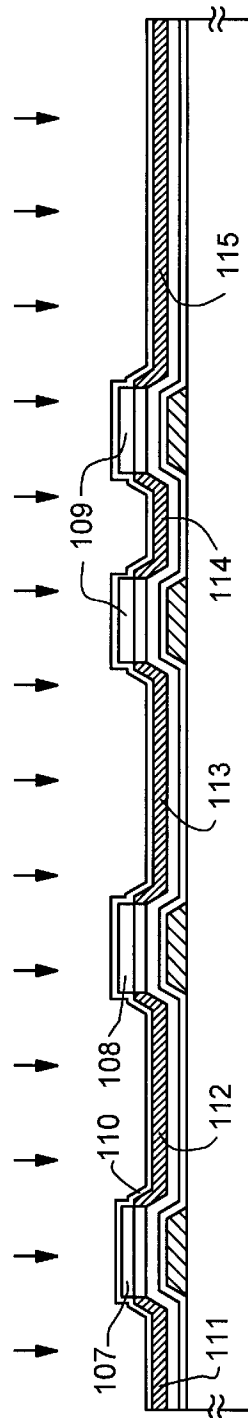


FIG. 1B

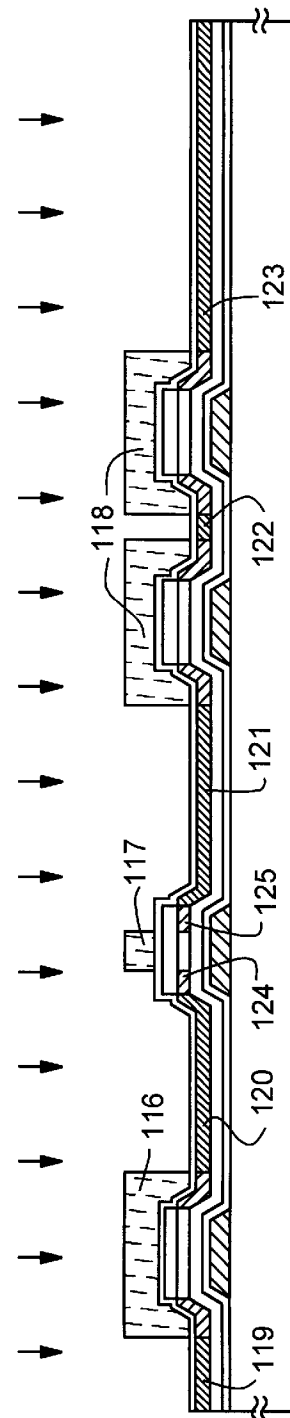


FIG. 1C

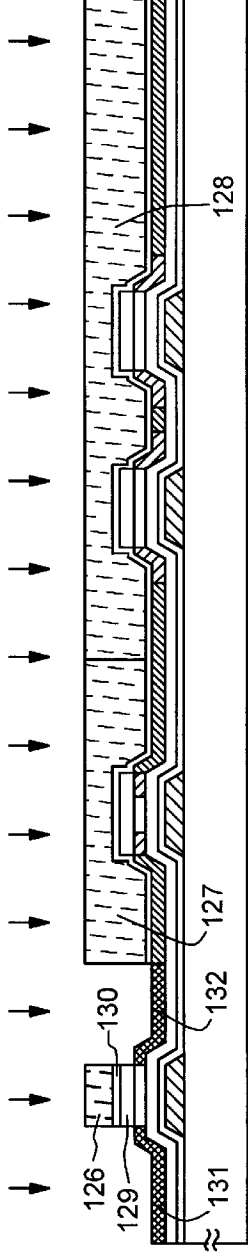


FIG. 2A

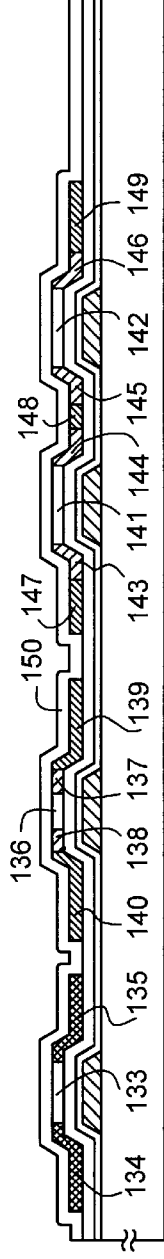


FIG. 2B

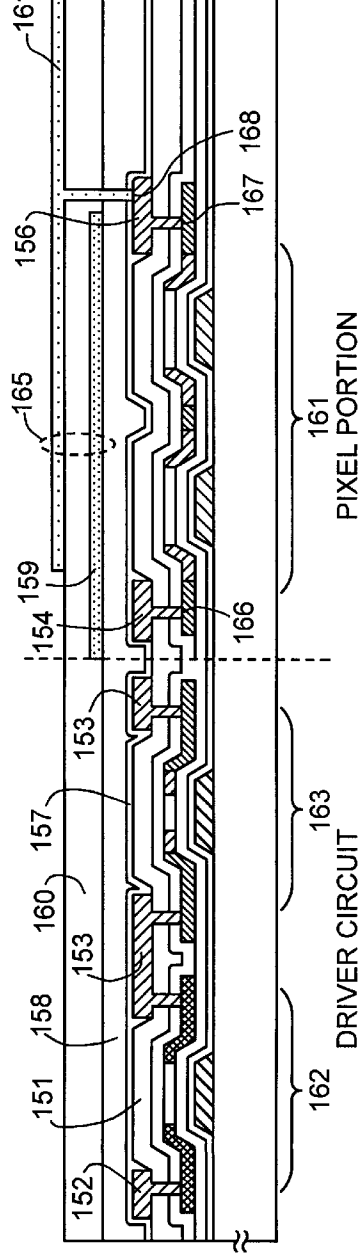


FIG. 2C

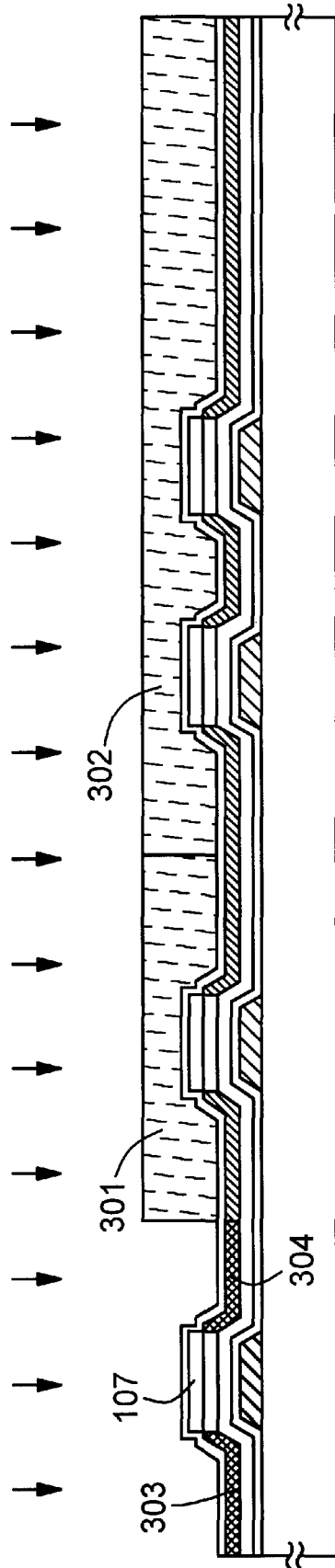


FIG. 3A

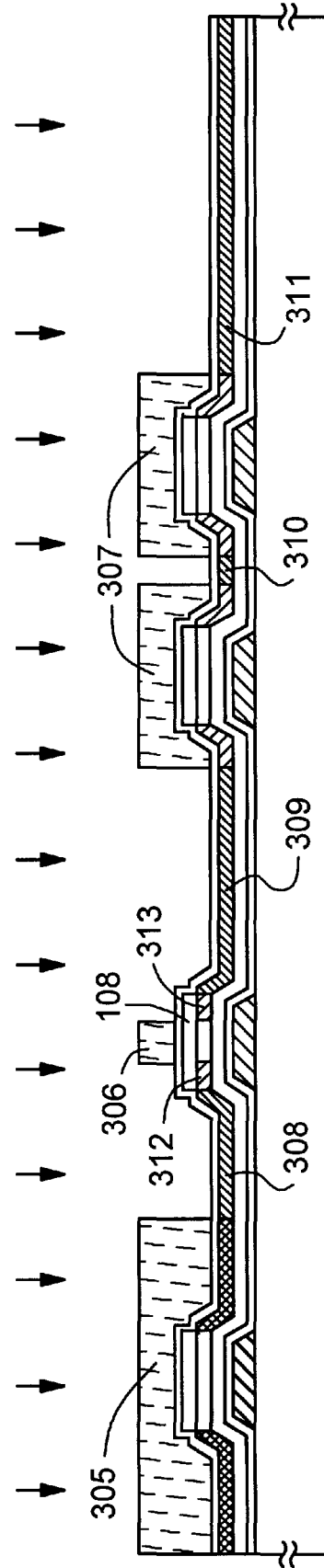


FIG. 3B

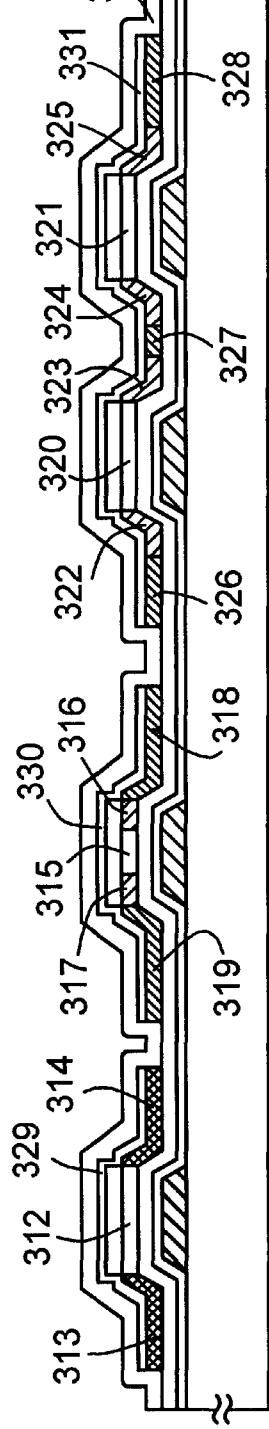


FIG. 4A

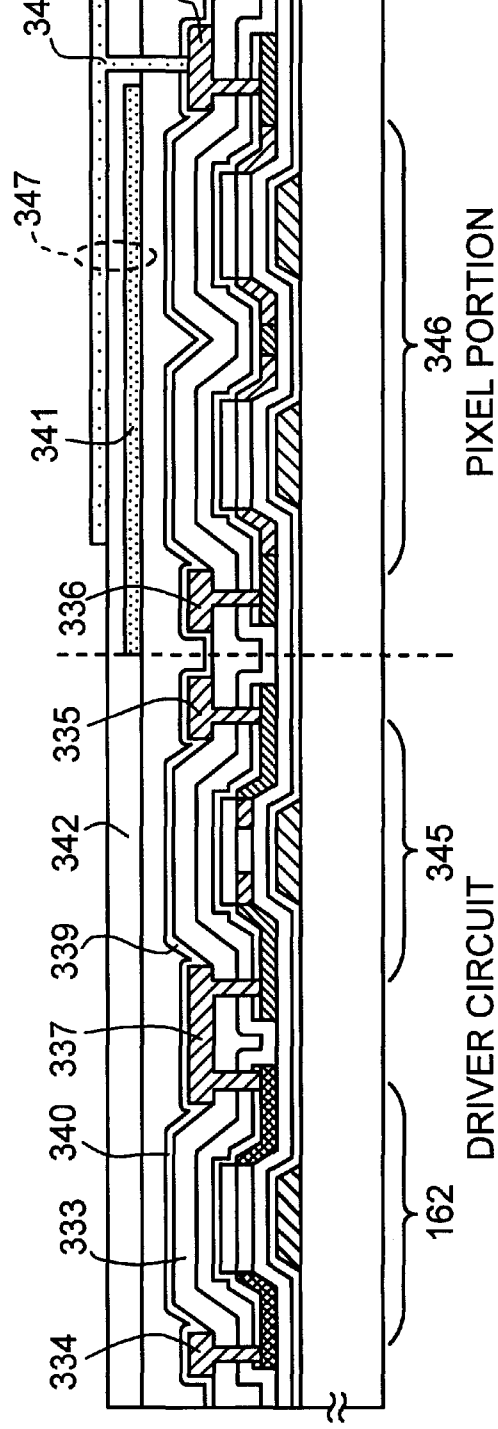


FIG. 4B

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