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(12) United States Patent

Shimoda et al.

54) TRANSISTOR ARRAY SUBSTRATE AND DISPLAY PANEL

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(52) **U.S. Cl.** **257/72**; 257/208; 257/E33.055

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(10) Patent No.: US 7

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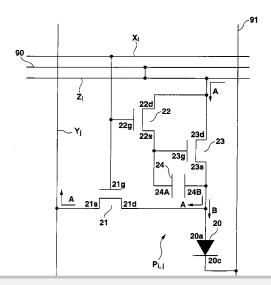
A Japanese Office Action (and English translation thereof) dated Apr. 30, 2008, issued in a counterpart Japanese Application.

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(57) ABSTRACT

A transistor array substrate includes a plurality of driving transistors which are arrayed in a matrix on a substrate. The driving transistor has a gate, a source, a drain, and a gate insulating film inserted between the gate, and the source and drain. A plurality of signal lines are patterned together with the gates of the driving transistors and arrayed to run in a predetermined direction on the substrate. A plurality of supply lines are patterned together with the sources and drains of the driving transistors and arrayed to cross the signal lines via the gate insulating film. The supply line is electrically connected to one of the source and the drain of the driving transistor. A plurality of feed interconnections are formed on the supply lines along the supply lines, respectively.

17 Claims, 27 Drawing Sheets





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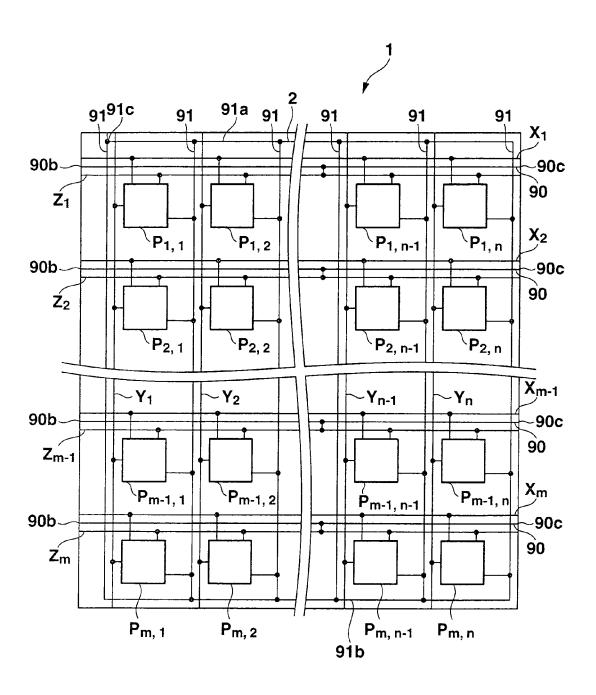


FIG.1

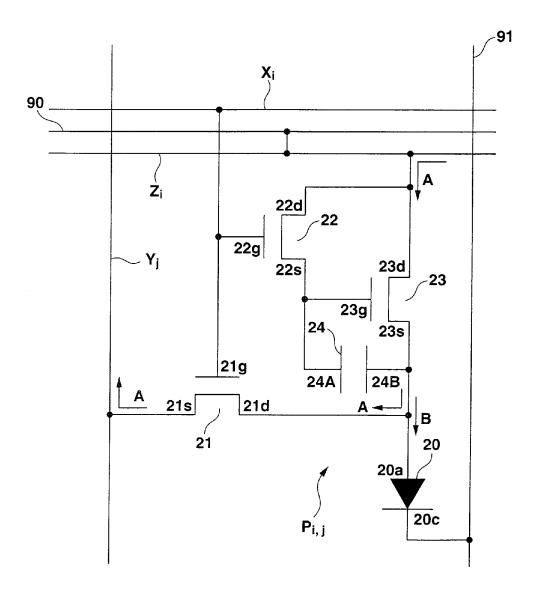
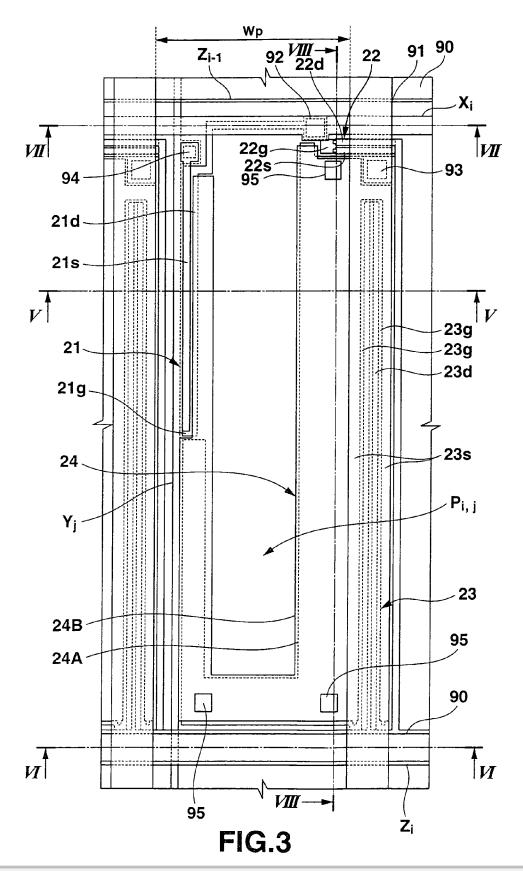


FIG.2

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