

[54] GPS RECEIVER HAVING A LOW POWER STANDBY MODE

5,291,542	3/1994	Kivari et al.	379/58
5,418,537	5/1995	Bird	342/357
5,448,773	9/1995	McBurney et al.	455/343

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[57] ABSTRACT

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[51] Int. Cl.⁶ G01S 5/02; G06F 1/00; H04B 1/16

[52] U.S. Cl. 342/357; 364/707; 455/343; 455/231

[58] Field of Search 342/357; 455/343, 455/230, 231; 364/707

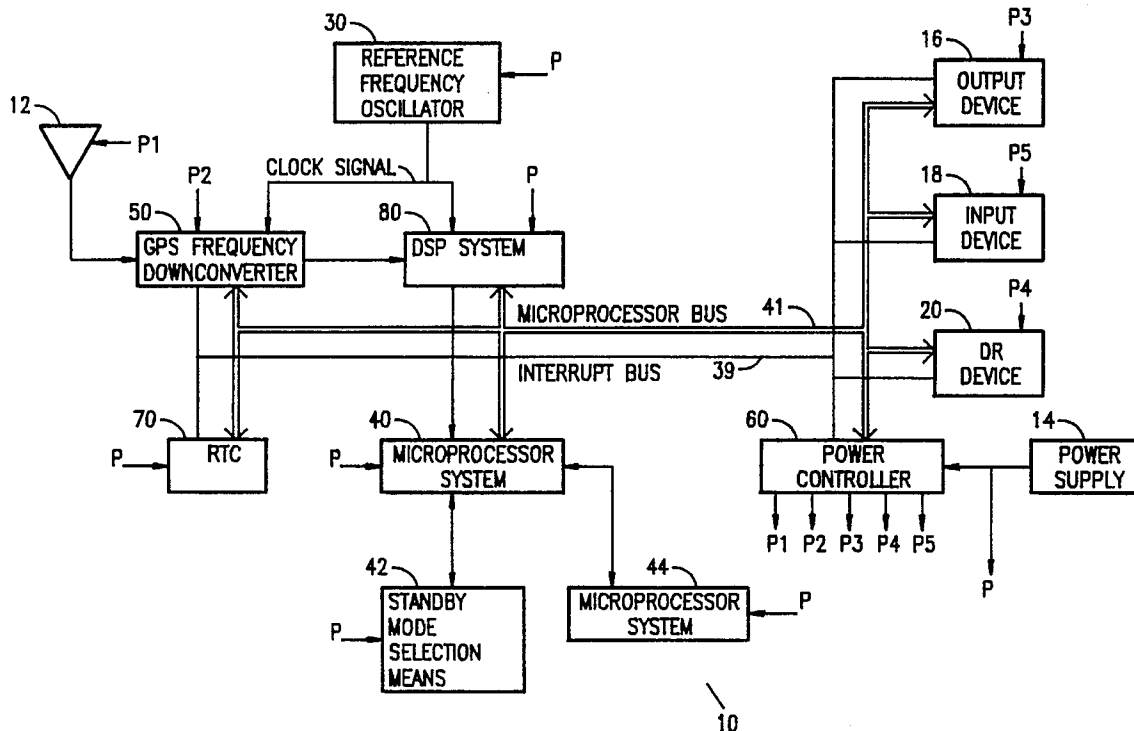
A GPS receiver having a normal mode to receive GPS satellite signals and to provide location information, and a low power standby mode. A microprocessor system in the GPS receiver causes the GPS receiver to alternate between the normal mode and the low power standby mode in order to reduce the average power consumption in the GPS receiver. In the normal mode a GPS antenna receives GPS satellite signals, the GPS frequency downconverter converts the frequency of the GPS satellite signals to an intermediate frequency, a digital signal processing system processes the intermediate frequency to provide GPS satellite signal correlation information. The microprocessor system processes the correlation information and provides location information to a user. In the standby mode, the operating power is inhibited in the GPS antenna and the GPS frequency downconverter, the system clock is inhibited in the digital processing system, and the microprocessor clock is inhibited in the microprocessor system.

[56] References Cited

U.S. PATENT DOCUMENTS

4,449,248	5/1984	Leslie et al.	455/343
5,101,510	3/1992	Duckeck	455/186
5,128,938	7/1992	Borras	455/343

31 Claims, 4 Drawing Sheets



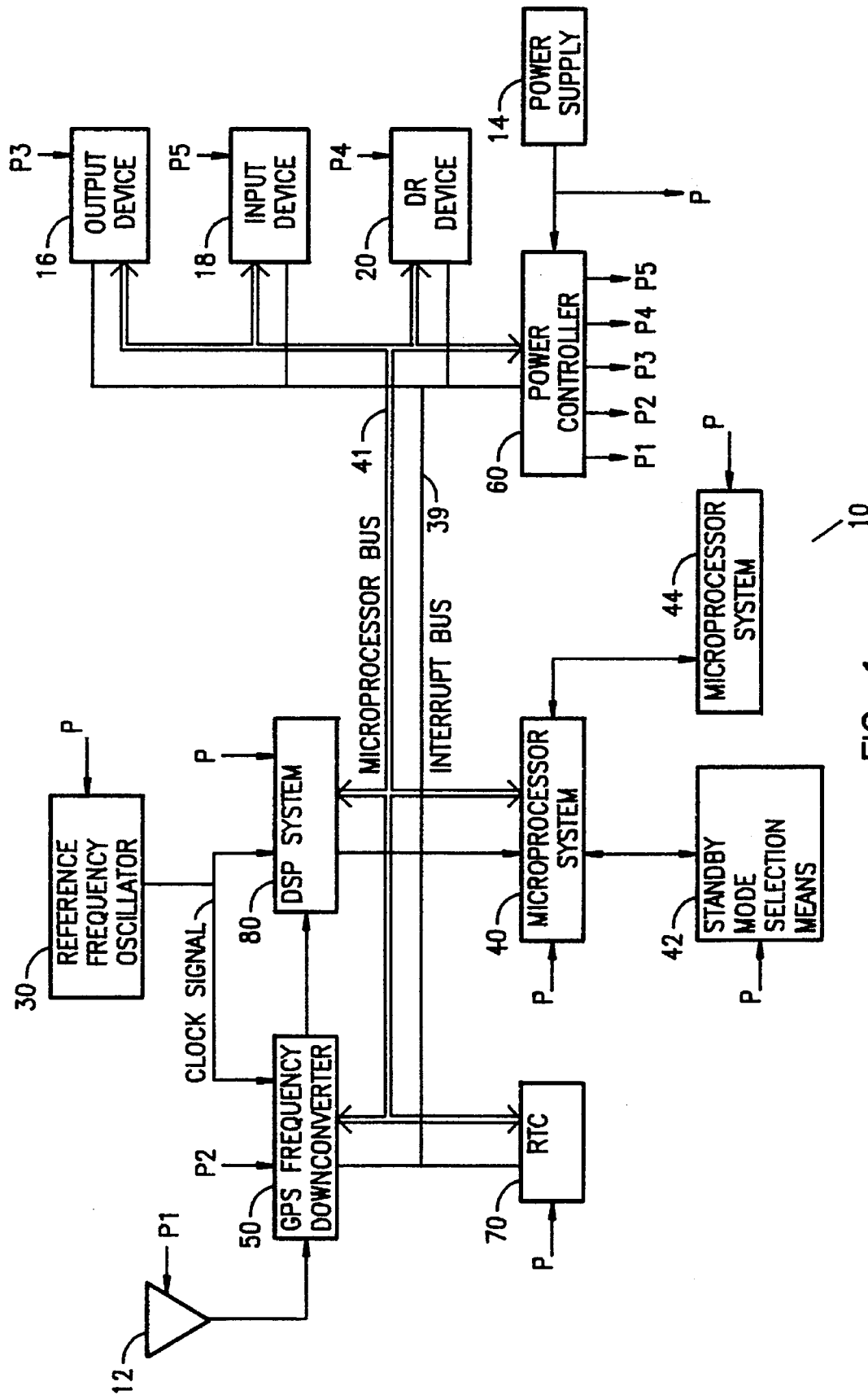


FIG. 1

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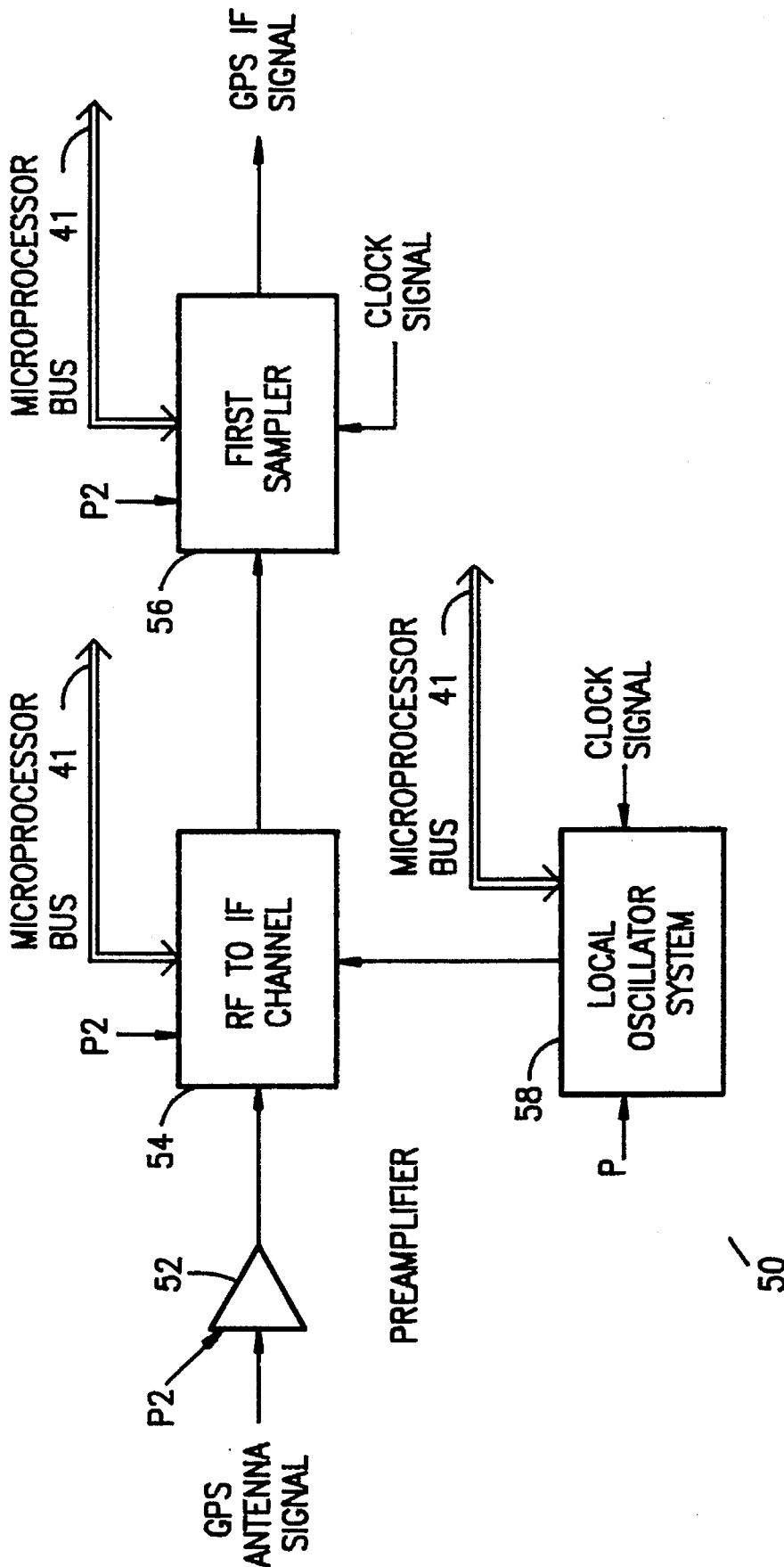


FIG. 2

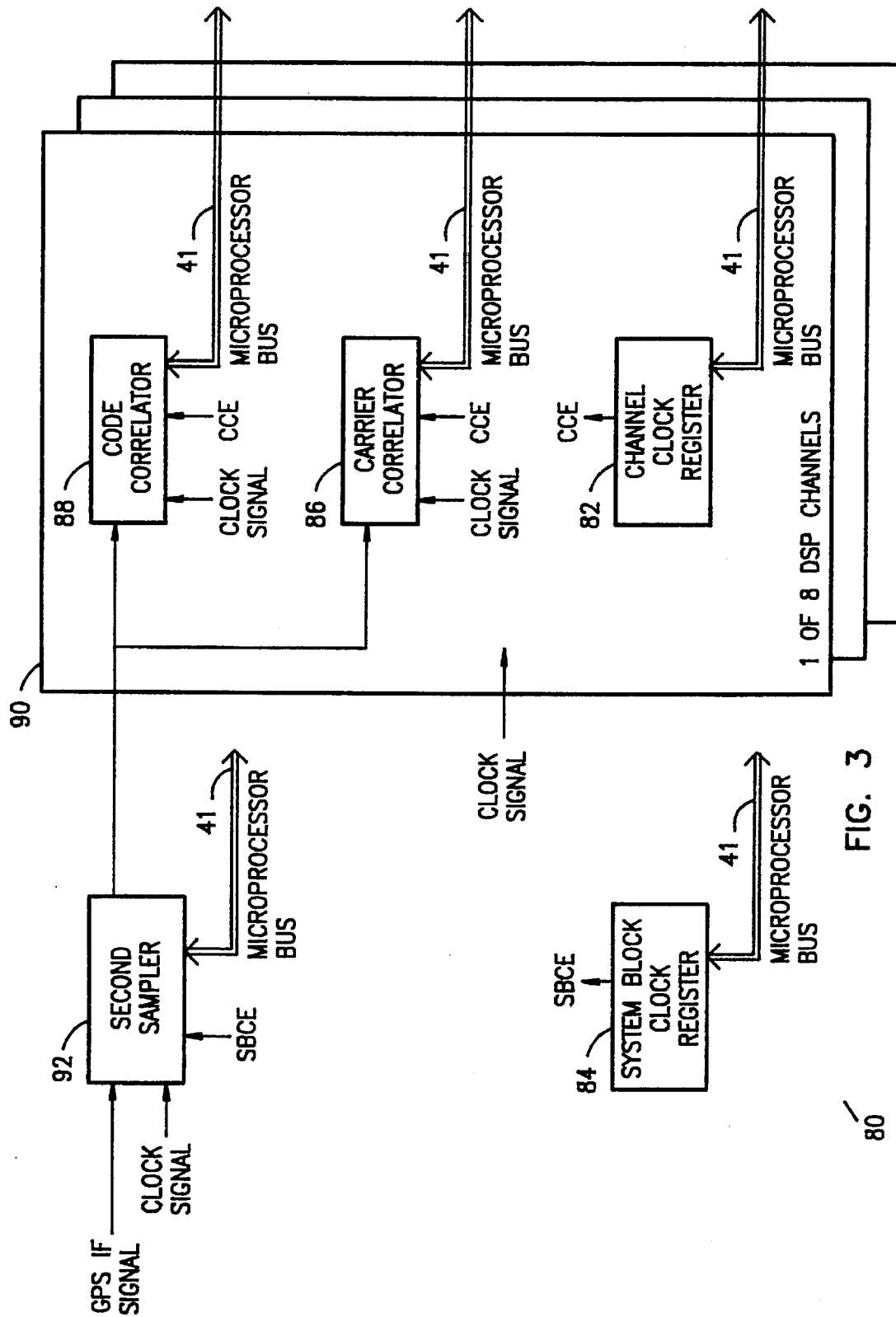


FIG. 3

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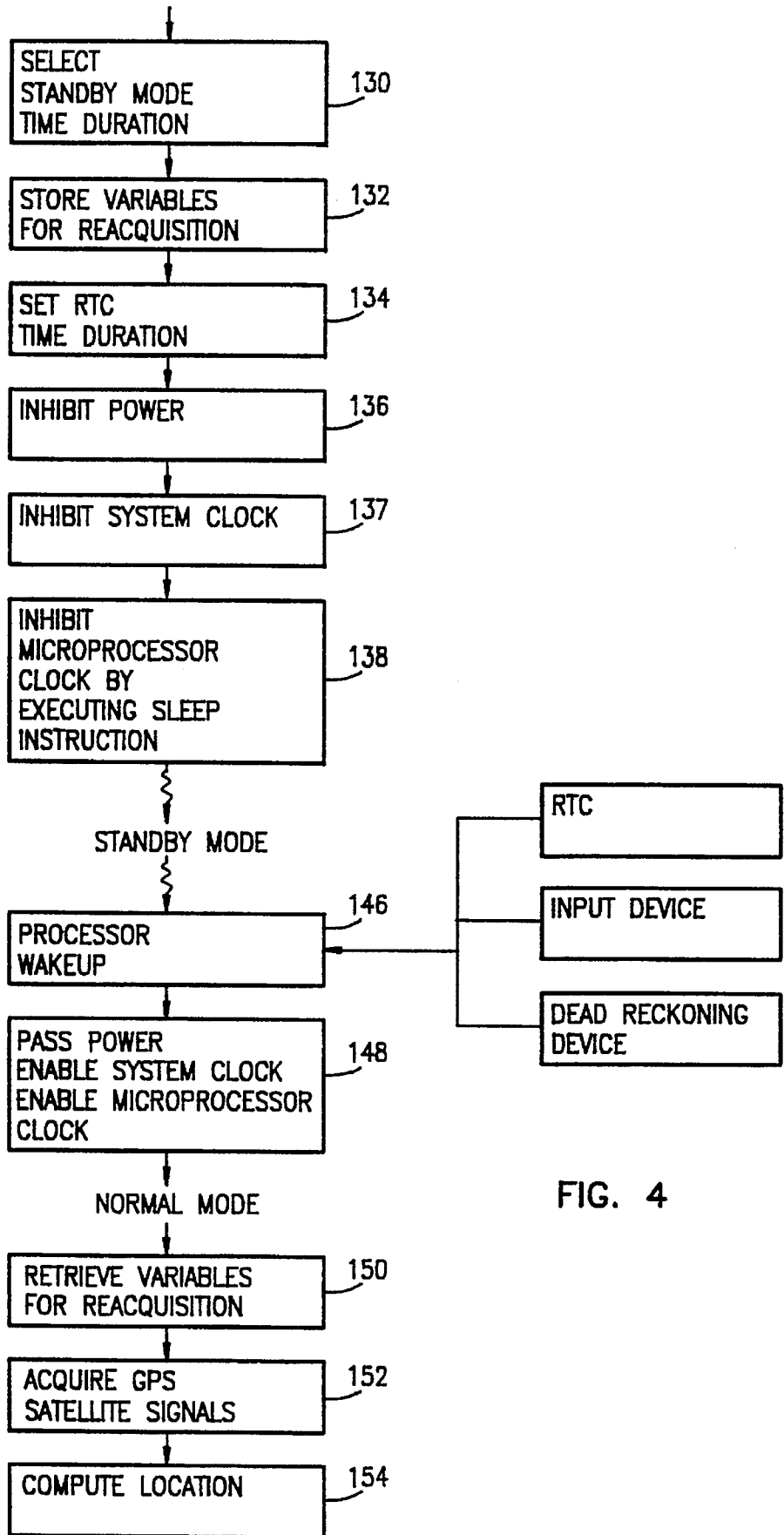


FIG. 4

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