1-MBIT (128K x 8)
BOOT BLOCK FLASH MEMORY

28F001BX-T/28F001BX-B/28F001BN-T/28F001BN-B

- **High-Integration Blocked Architecture**
  - **— One 8 KB Boot Block w/Lock Out**
  - **— Two 4 KB Parameter Blocks**
  - **— One 112 KB Main Block**
- **100,000 Erase/Program Cycles Per Block**
- **Simplified Program and Erase**
  - **— Automated Algorithms via On-Chip Write State Machine (WSM)**
- **SRAM-Compatible Write Interface**
- **Deep Power-Down Mode**
  - **— 0.05 μA I_{CC} Typical**
  - **— 0.8 μA I_{PP} Typical**
- **12.0V $\pm$5% V_{PP}**
- **High-Performance Read**
  - **— 70/75 ns, 90 ns, 120 ns, 150 ns Maximum Access Time**
  - **— 5.0V $\pm$10% V_{CC}**
- **Hardware Data Protection Feature**
  - **— Erase/Write Lockout during Power Transitions**
- **Advanced Packaging, JEDEC Pinouts**
  - **— 32-Pin PDIP**
  - **— 32-Lead PLCC, TSOP**
- **ETOX™ II Nonvolatile Flash Technology**
  - **— EPROM-Compatible Process Base**
  - **— High-Volume Manufacturing Experience**
- **Extended Temperature Options**

Intel's 28F001BX-B and 28F001BX-T combine the cost-effectiveness of Intel standard flash memory with features that simplify write and allow block erase. These devices aid the system designer by combining the functions of several components into one, making boot block flash an innovative alternative to EPROM and EEPROM or battery-backed static RAM. Many new and existing designs can take advantage of the 28F001BX's integration of blocked architecture, automated electrical reprogramming, and standard processor interface.

The 28F001BX-B and 28F001BX-T are 1,048,576 bit nonvolatile memories organized as 131,072 bytes of 8 bits. They are offered in 32-pin plastic DIP, 32-lead PLCC and 32-lead TSOP packages. Pin assignment conform to JEDEC standards for byte-wide EPROMs. These devices use an integrated command port and state machine for simplified block erasure and byte reprogramming. The 28F001BX-T's block locations provide compatibility with microprocessors and microcontrollers that boot from high memory, such as Intel's MCS®-186 family, 80286, i386™, i486™, i860™ and 80960CA. With exactly the same memory segmentation, the 28F001BX-B memory map is tailored for microprocessors and microcontrollers that boot from low memory, such as Intel's MCS-51, MCS-196, 80960KX and 80960SX families. All other features are identical, and unless otherwise noted, the term 28F001BX can refer to either device throughout the remainder of this document.

The boot block section includes a reprogramming write lock out feature to guarantee data integrity. It is designed to contain secure code which will bring up the system minimally and download code to the other locations of the 28F001BX. Intel's 28F001BX employs advanced CMOS circuitry for systems requiring high-performance access speeds, low power consumption, and immunity to noise. Its access time provides no-WAIT-state performance for a wide range of microprocessors and microcontrollers. A deep-powerdown mode lowers power consumption to 0.25 μW typical through V_{CC}, crucial in laptop computer, handheld instrumentation and other low-power applications. The RP# power control input also provides absolute data protection during system powerup or power loss.

Manufactured on Intel's ETOX process base, the 28F001BX builds on years of EPROM experience to yield the highest levels of quality, reliability, and cost-effectiveness.

NOTE: The 28F001BN is equivalent to the 28F001BX.

November 1995 **Order Number: 290406-007**

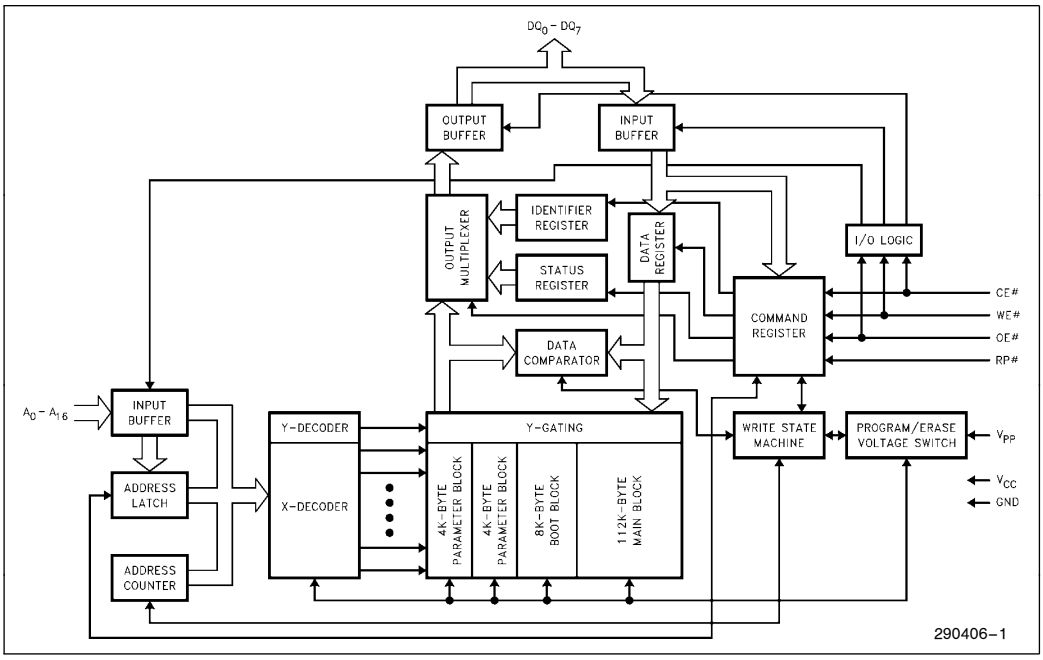

Figure 1. 28F001BX Block Diagram

Table 1. Pin Description

Symbol	Type	Name and Function
A_0–A_{16}	INPUT	**ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a write cycle.
DQ_0–DQ_7	INPUT/ OUTPUT	**DATA INPUTS/OUTPUTS:** Inputs data and commands during memory write cycles; outputs data during memory, Status Register and Identifier read cycles. The data pins are active high and float to tri-state off when the chip is deselected or the outputs are disabled. Data is internally latched during a write cycle.
CE#	INPUT	**CHIP ENABLE:** Activates the device's control logic, input buffers, decoders and sense amplifiers. CE# is active low; CE# high deselects the memory device and reduces power consumption to standby levels.
RP#	INPUT	**POWERDOWN:** Puts the device in deep powerdown mode. RP# is active low; RP# high gates normal operation. RP# = V_{HH} allows programming of the boot block. RP# also locks out erase or write operations when active low, providing data protection during power transitions. RP# active resets internal automation. Exit from deep powerdown sets device to Read Array mode.
OE#	INPUT	**OUTPUT ENABLE:** Gates the device's outputs through the data buffers during a read cycle. OE# is active low. OE# = V_{HH} (pulsed) allows programming of the boot block.
WE#	INPUT	**WRITE ENABLE:** Controls writes to the Command Register and array blocks. WE# is active low. Addresses and data are latched on the rising edge of the WE# pulse.
V_{PP}		**ERASE/PROGRAM POWER SUPPLY** for erasing blocks of the array or programming bytes of each block. Note: With $V_{PP} < V_{PPL}$ max, memory contents cannot be altered.
V_{CC}		**DEVICE POWER SUPPLY:** (5V ±10%)
GND		**GROUND**

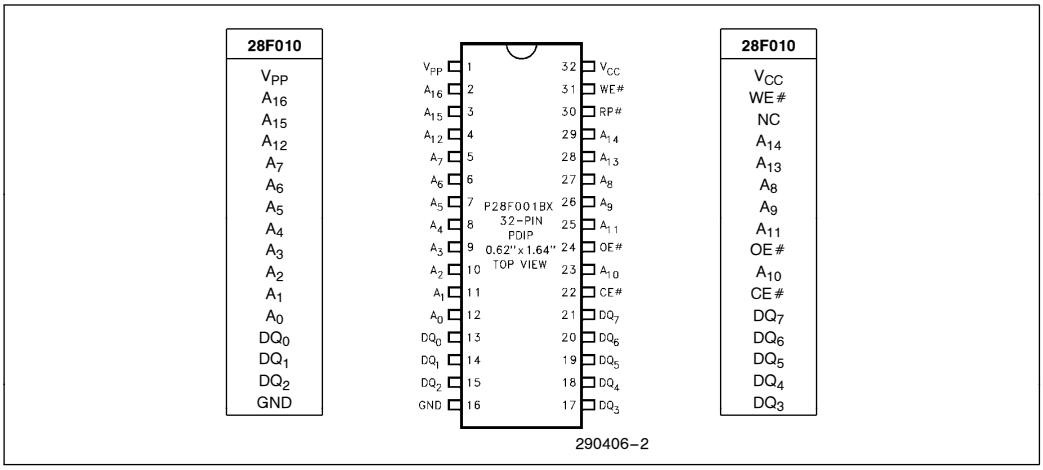

Figure 2. DIP Pin Configuration

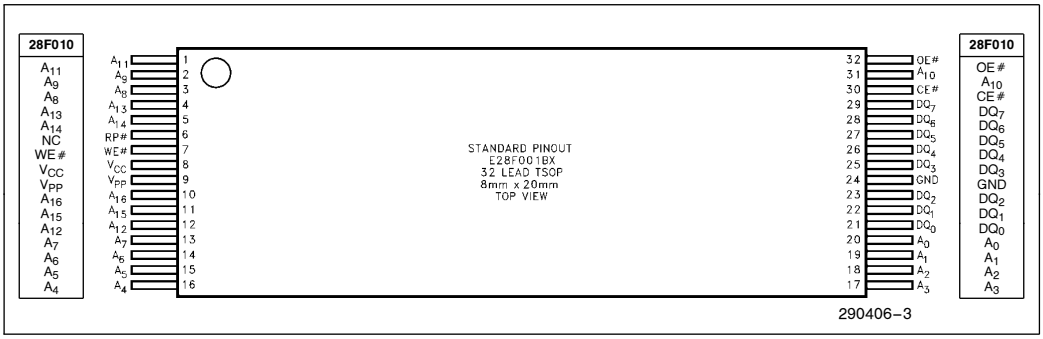

Figure 3. TSOP Lead Configuration

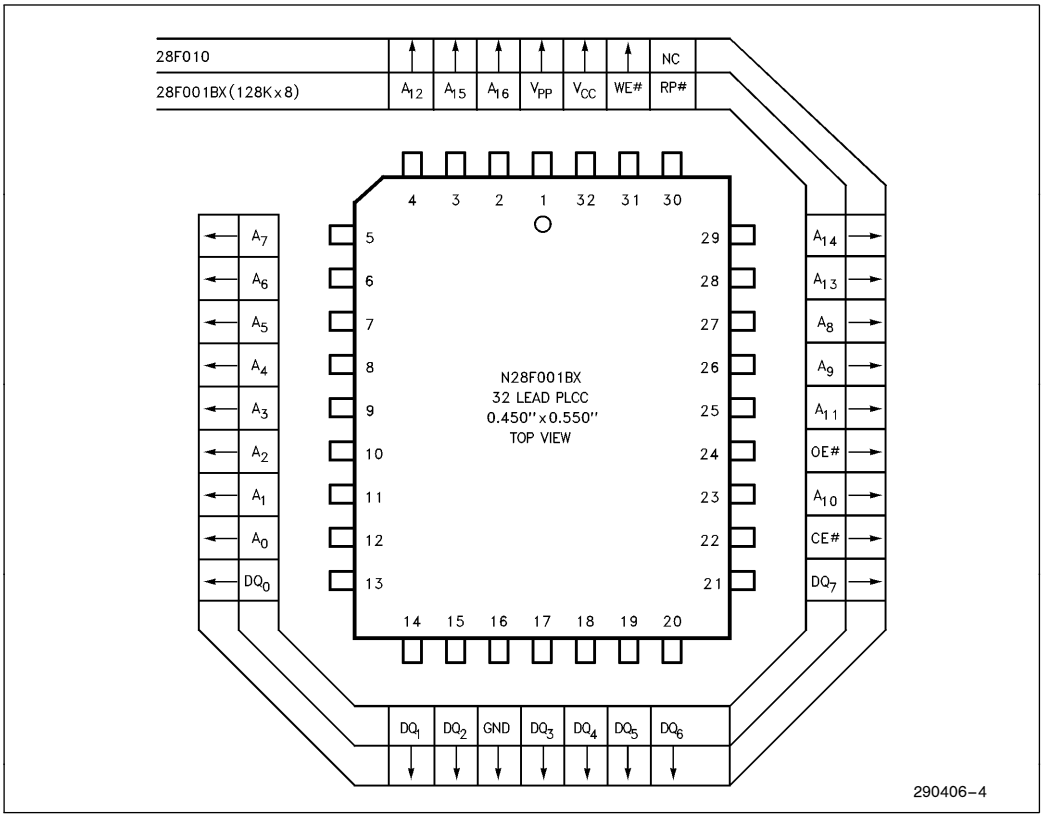

Figure 4. PLCC Lead Configuration

APPLICATIONS

The 28F001BX flash 'boot block' memory augments the non-volatility, in-system electrical erasure and reprogrammability of Intel's standard flash memory by offering four separately erasable blocks and integrating a state machine to control erase and program functions. The specialized blocking architecture and automated programming of the 28F001BX provide a full-function, non-volatile flash memory ideal for a wide range of applications, including PC boot/BIOS memory, minimum-chip embedded program memory and parametric data storage. The 28F001BX combines the safety of a hardware-protected 8-KByte boot block with the flexibility of three separately reprogrammable blocks (two 4-KByte parameter blocks and one 112-KByte code block) into one versatile, cost-effective flash memory. Additionally, reprogramming one block does not affect code stored in another block, ensuring data integrity.

The flexibility of flash memory reduces costs throughout the life cycle of a design. During the early stages of a system's life, flash memory reduces prototype development and testing time, allowing the system designer to modify in-system software electrically versus manual removal of components. During production, flash memory provides flexible firmware for just-in-time configuration, reducing system inventory and eliminating unnecessary handling and less reliable socketed connections. Late in the life cycle, when software updates or code ''bugs'' are often unpredictable and costly, flash memory reduces update costs by allowing the manufacturers to send floppy updates versus a technician. Alternatively, remote updates over a communication link are possible at speeds up to 9600 baud due to flash memory's fast programming time.

Reprogrammable environments, such as the personal computer, are ideal applications for the 28F001BX. The internal state machine provides SRAM-like timings for program and erasure, using the Command and Status Registers. The blocking scheme allows BIOS update in the main and parameter blocks, while still providing recovery code in the boot block in the unlikely event a power failure occurs during an update, or where BIOS code is corrupted. Parameter blocks also provide convenient configuration storage, backing up SRAM and battery configurations. EISA systems, for example, can store hardware configurations in a flash parameter block, reducing system SRAM.

Laptop BIOSs are becoming increasingly complex with the addition of power management software and extended system setup screens. BIOS code complexity increases the potential for code updates after the sale, but the compactness of laptop designs makes hardware updates very costly. Boot block flash memory provides an inexpensive update solution for laptops, while reducing laptop obsolescence. For portable PCs and hand-held equipment, the deep powerdown mode dramatically lowers system power requirements during periods of slow operation or sleep modes.

The 28F001BX gives the embedded system designer several desired features. The internal state machine reduces the size of external code dedicated to the erase and program algorithms, as well as freeing the microcontroller or microprocessor to respond to other system requests during program and erasure. The four blocks allow logical segmentation of the entire embedded software: the 8-KByte block for the boot code, the 112-KByte block for the main program code and the two 4-KByte blocks for updatable parametric data storage, diagnostic messages and data, or extensions of either the boot code or program code. The boot block is hardware protected against unauthorized write or erase of its vital code in the field. Further, the powerdown mode also locks out erase or write operations, providing absolute data protection during system powerup or power loss. This hardware protection provides obvious advantages for safety related applications such as transportation, military, and medical. The 28F001BX is well suited for minimum-chip embedded applications ranging from communications to automotive.

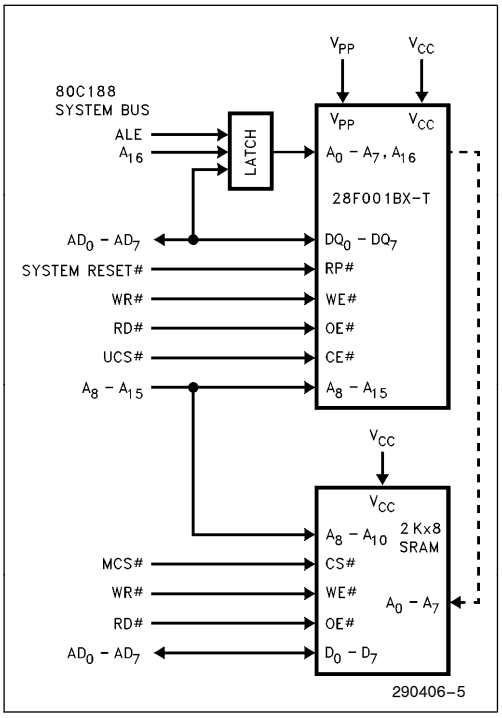

Figure 5. 28F001BX-T in a 80C188 System

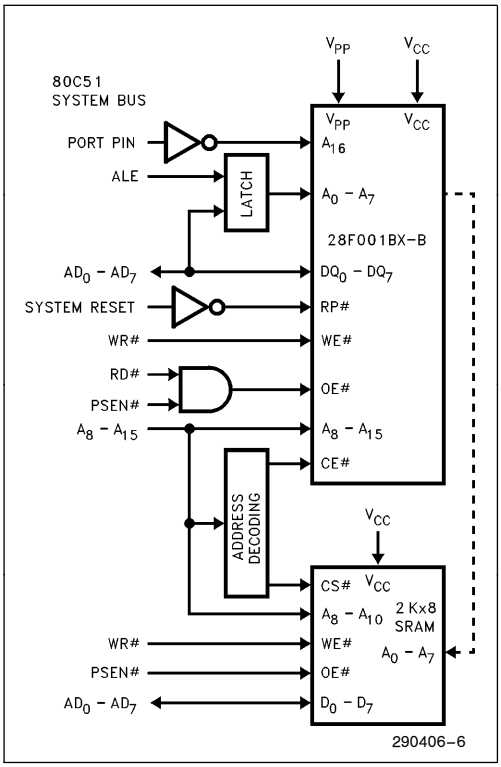

Figure 6. 28F001BX-B in a 80C51 System

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