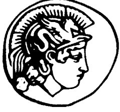

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A review of recent MOSFET threshold voltage extraction methods

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Abstract

The threshold voltage value, which is the most important electrical parameter in modeling MOSFETs, can be extracted from either measured drain current or capacitance characteristics, using a single or more transistors. Practical circuits based on some of the most common methods are available to automatically and quickly measure the threshold voltage. This article reviews and assesses several of the extraction methods currently used to determine the value of threshold voltage from the measured drain current versus gate voltage transfer characteristics. The assessment focuses specially on single-crystal bulk MOSFETs. It includes 11 different methods that use the transfer characteristics measured under linear regime operation conditions. Additionally two methods for threshold voltage extraction under saturation conditions and one specifically suitable for non-crystalline thin film MOSFETs are also included. Practical implementation of the several methods presented is illustrated and their performances are compared under the same challenging conditions: the measured characteristics of an enhancement-mode n-channel single-crystal silicon bulk MOSFET with state-of-the-art short-channel length, and an experimental n-channel a-Si:H thin film MOSFET. © 2002 Elsevier Science Ltd. All rights reserved.

1. Introduction

The threshold voltage (V_T) is a fundamental parameter for MOSFET modeling and characterization [1–6]. This parameter, which represents the onset of significant drain current flow, has been given several definitions [7–9], but it may be essentially understood as the gate voltage value at which the transition between weak and strong inversion takes place in the MOSFET channel. There exist numerous methods to extract the value of threshold voltage [10–41] and various extractor circuits have also been proposed [42–44] to automatically measure this parameter. Recently three books [1–3] and three articles [4–6] have reviewed and scrutinized different available methods.

The greater part of the procedures available to determine V_T are based on the measurement of the static transfer drain current versus gate voltage (I_D–V_g) characteristics [10–35] of a single transistor. Most of these I_D–V_g methods use the strong inversion region [10–27], while only a few consider the weak inversion region [28–31]. Extraction is mostly done using low drain voltages so that the device operates in the linear region [10–33]. However, V_T extraction with the device operating in saturation is also frequently carried out [34,35].

A common feature present of most V_T extraction methods based on the I_D–V_g transfer characteristics is

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the strong influence of the source and drain parasitic series resistances and the channel mobility degradation on the resulting value of the extracted V_T. This situation is highly undesirable because the correct value of the extracted V_T should not depend on parasitic components nor mobility degradation. In order to eliminate the influence of these unwanted effects some methods have been proposed which are based on measuring capacitance as a function of voltage [36,37]. However these C–V methods have the disadvantage of requiring elaborate high-resolution equipment to measure the small capacitances present in MOSFETs, particularly in very small geometry state-of-art devices. Other approaches to eliminate the influence of parasitic series resistances are based on measuring the I_D–V_g transfer characteristics of various devices having different mask channel lengths [38,39], or on measuring several devices connected together [40,41]. Although such multi-device approaches offer interesting solutions to this problem, they require additional work and the availability of several supplementary special devices. Another recently proposed method that requires repeated measurements is based on a proportional difference operator [26,27].

The extraction of V_T in non-crystalline MOSFETs is more conveniently performed using the drain current in saturation, considering that these devices present much smaller currents than single-crystalline devices. Amorphous and polycrystalline thin film transistors (TFTs) introduce the additional difficulty that the saturation drain current in strong inversion is usually modeled by a power law with an exponent which can differ from 2 [45,46]. Because of this behavior, using conventional V_T extraction methods developed for single-crystal devices will generally produce values of V_T that are unacceptable or at least not very accurate. Therefore the extraction method must be capable of extracting the value of the unknown power-law exponent parameter and take it into consideration in the extraction process. To that end, methods have been proposed that are specific for non-crystalline thin MOSFET TFTs [45,46] and thus allow to extract their threshold voltage correctly.

This article will review and scrutinize the following existing I_D–V_g methods for extracting V_T in single-crystal MOSFETs, biased in the *linear region*: (1) constant-current (CC) method, which defines V_T as the gate voltage corresponding to a certain predefined practical constant drain current [1–6,10,11]; (2) extrapolation in the linear region (ELR) method, which finds the gate voltage axis intercept of the linear extrapolation of the I_D–V_g characteristics at its maximum first derivative (slope) point [1–6]; (3) transconductance linear extrapolation (GMLE) method, which finds the gate voltage axis intercept of the linear extrapolation of the g_m–V_g characteristics at its maximum first derivative (slope) point [19,20]; (4) second derivative (SD) method, which determines V_T at the maximum of the SD of I_D with respect to V_g [12]; (5) ratio method (RM), which finds the gate voltage axis intercept of the ratio of the drain current to the square root of the transconductance [13–18]; (6) transition method [33]; (7) integral method [32]; (8) Corsi function method [21]; and (9) second derivative logarithmic (SDL) method, which determines V_T at the minimum of the SD of $\log(I_D)$–V_g [31]; (10) linear cofactor difference operator [22] (LCDO) method, and (11) non-linear optimization [23,24].

This article will also review the following two methods to extract the V_T of single-crystalline MOSFETs, operating in the *saturation region*: (1) extrapolation in the saturation region (ESR) method, which finds the gate voltage axis intercept of the linear extrapolation of the $I_D^{0.5}$–V_g characteristics at its maximum first derivative (slope) point [1,2]; and (2) G_1 function extraction method [34,35].

Finally, we will review and discuss some amorphous TFT specific procedures which have been recently proposed to extract the threshold voltage of these non-crystalline devices [45,46].

2. Extraction from the I_D–V_g curve of MOSFETs biased in the linear region

In order to critically assess and compare the different linear region extraction methods reviewed here, we will apply them all to extract the value of the threshold voltage from the measured transfer characteristics of a state-of-the-art bulk single-crystal silicon enhancement-mode n-channel MOSFET with a 5 μm mask channel width, a 0.18 μm mask channel length, and a 32A gate oxide thickness. For this group of methods the device is biased to operate in the linear regime by applying a drain voltage of 10 mV. Fig. 1 presents the output characteristics of this device for general reference purposes.

2.1. Constant-current method

The CC method [1–6] evaluates the threshold voltage as the value of the gate voltage, V_g, corresponding to a given arbitrary constant drain current, I_D and $V_d < 100$ mV. A typical value [20] for this arbitrary constant drain current is $(W_m/L_m) \times 10^{-7}$, where W_m and L_m are the mask channel width and length, respectively. This method is widely used in industry because of its simplicity. The threshold voltage can be determined quickly with only one voltage measurement, as shown in Fig. 2. In spite of its simplicity, this method has the severe disadvantage of being totally dependent of the arbitrarily chosen value of the drain current level. This is evident by the results in Fig. 2, where different gate voltages can be taken at different drain current values to represent the threshold voltages.

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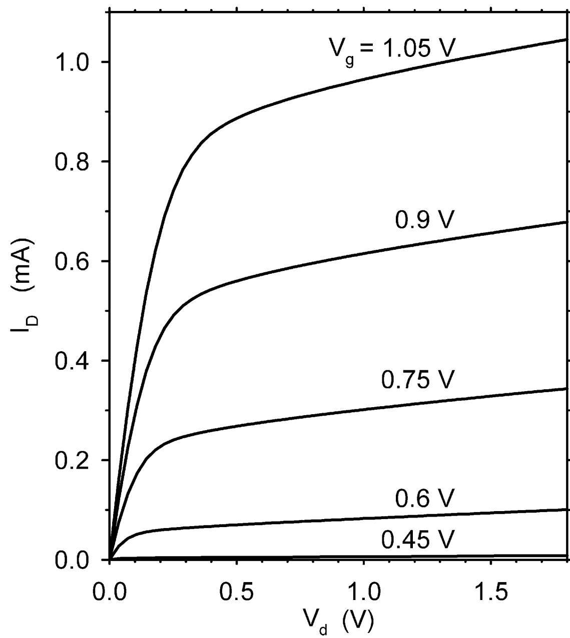

Fig. 1. Measured I_D–V_d output characteristics at five values of gate bias for the test bulk single-crystal n-channel MOSFET with 5 μm mask channel width and 0.18 μm mask channel length.

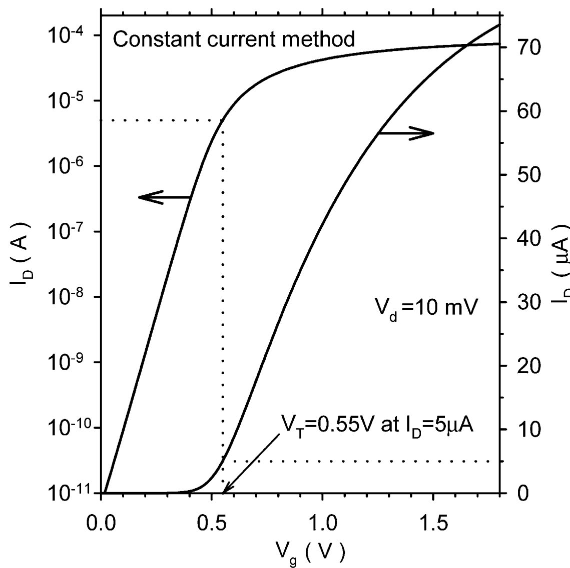

Fig. 2. CC method implemented on the I_D–V_g transfer characteristics of the test bulk device measured at $V_d = 10$ mV. This method evaluates the threshold voltage as the value of the gate voltage corresponding to a given arbitrary constant drain current.

Recently Zhou and his group have proposed [10,11] an improvement to the CC method. It consists on defining the previously arbitrary drain current level used to define the threshold voltage at the drain current where d^2I_D/dV_g^2 presents a maximum. This amounts to a combination of the CC method and the second-derivative method, which will be presented latter.

2.2. Extrapolation in the linear region method

The ELR method [1–6] is perhaps the most popular threshold-voltage extraction method. It consists of finding the gate-voltage axis intercept (i.e., $I_D = 0$) of the linear extrapolation of the I_D–V_g curve at its maximum first derivative (slope) point (i.e. the point of maximum transconductance, g_m), as illustrated in Fig. 3. The value of V_T is calculated by adding $V_d/2$ to the resulting gate-voltage axis intercept, which for the device at hand happens to be 0.51 V. The main drawback of this otherwise useful method is that the maximum slope point might be uncertain, because the I_D–V_g characteristics can deviate from ideal straight line behavior at gate voltages even slightly above V_T, due to mobility degradation effects and to the presence of significant source and drain series parasitic resistances [2]. Therefore, the threshold voltage value extracted using this method, often referred to as the extrapolated V_T, can be strongly influenced by

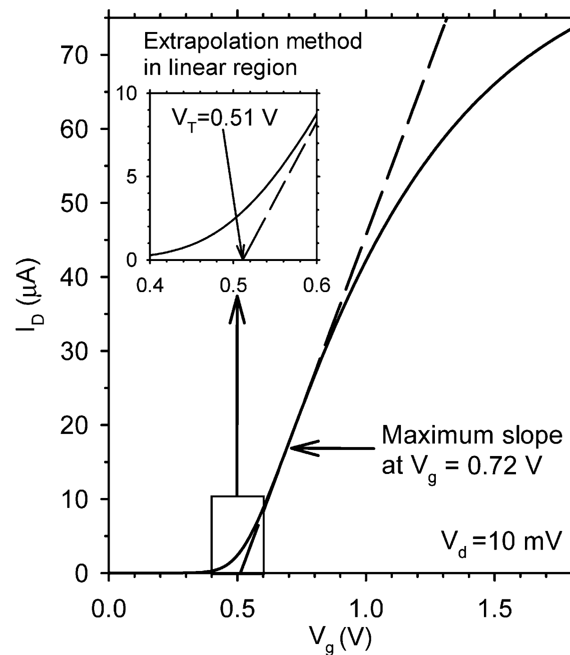

Fig. 3. ELR method implemented on the I_D–V_g characteristics of the test bulk device measured at $V_d = 10$ mV. This method consists of finding the gate-voltage axis intercept (i.e., $I_D = 0$) of the linear extrapolation of the I_D–V_g curve at its maximum slope point.

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parasitic series resistances and mobility degradation effects.

2.3. Transconductance extrapolation method in the linear region

A seldom used method is the transconductance extrapolation method in the linear region (GMLE) which was proposed in 1998 [19,20]. This method suggests that the threshold voltage corresponds to the gate voltage axis intercept of the linear extrapolation of the g_m–V_g characteristics at its maximum first derivative (slope) point. This method is based on the following arguments when the device is biased in the linear region. (1) In weak inversion, the transconductance depends exponentially on gate bias; (2) For strong inversion, if the series resistance and mobility degradation are negligible, the transconductance tends to a constant value; (3) The transconductance decreases slightly with gate bias due to the series resistance and mobility degradation; (4) In the transition region between weak and strong inversion, the transconductance depends linearly on gate bias. Fig. 4 presents the application of this method to the g_m–V_g characteristics producing an apparent value for V_T of only 0.44 V. The following method also based on the maximum slope of the g_m–V_g characteristics offers a better description of V_T.

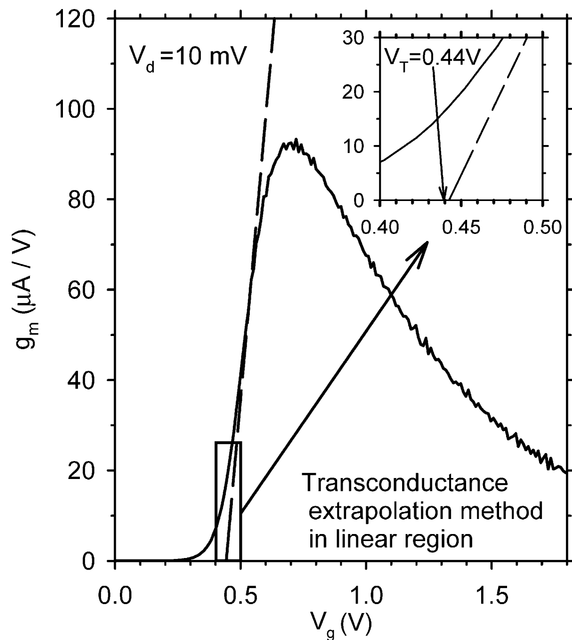

Fig. 4. Transconductance extrapolation method (GMLE) implemented on the $g_m = dI_D/dV_g$ versus V_g characteristics of the test bulk device measured at $V_d = 10$ mV. This method suggests that the threshold voltage corresponds to the gate voltage axis intercept of the linear extrapolation of the g_m–V_g characteristics at its maximum slope point.

2.4. Second-derivative method

The SD method [12], developed to avoid the dependence on the series resistances, determines V_T as the gate voltage at which the derivative of the transconductance (i.e., $dg_m/dV_g = d^2I_D/dV_g^2$) is maximum. The origin of this method can be understood by analyzing the following ideal case of a MOSFET modeled with a simple level = 1 SPICE model, where $I_D = 0$ for $V_g < V_T$ and I_D is proportional to V_g for $V_g > V_T$. Using the previous simplifying assumption, dI_D/dV_g becomes a step function, which is zero for $V_g < V_T$ and has a positive constant value for $V_g > V_T$. Therefore, d^2I_D/dV_g^2 will tend to infinity at $V_g = V_T$. Since for a real device such simplifying assumptions are obviously not exactly true, d^2I_D/dV_g^2 will of course not become infinite, but will instead exhibit a maximum at $V_g = V_T$.

As Fig. 5 indicates, the implementation of this method is highly sensitive to measurement error and noise, because the use of the SD amounts to applying a high-pass filter in the measurement. Notice in this figure that the maximum value of d^2I_D/dV_g^2 occurs at about $V_g = 0.54$ V due to the measurement noise present;

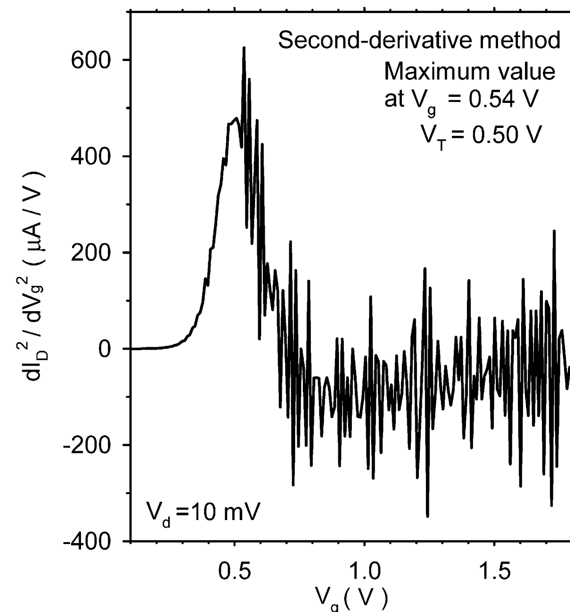

Fig. 5. SD method implemented on the plot of d^2I_D/dV_g^2 versus V_g of the test bulk device measured at $V_d = 10$ mV. This method consists of finding the gate-voltage at which d^2I_D/dV_g^2 exhibits a maximum value.

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whereas if the noise is suppressed the maximum appears to be around $V_g = 0.50$ V.

2.5. Ratio method

The RM [13–18], developed to avoid the dependence of the extracted V_T value on mobility degradation and parasitic series resistance, proposes that the ratio of the drain current to the square root of the transconductance ($I_D/g_m^{0.5}$) behaves as a linear function of gate bias, whose intercept with the gate-voltage axis will equal the threshold voltage. This method was originally published independently in 1988 by Jain [13] and by Ghibaudo [14]. Jain demonstrated that if the mobility degradation were negligible, the function $I_D/g_m^{0.5}$ would be independent of parasitic series resistance [13]. On the other hand, Ghibaudo showed that if the parasitic series resistance were negligible, the function $I_D/g_m^{0.5}$ would not depend on mobility degradation [14]. In 1995, Fikry and his coworkers proved [15] that the function $I_D/g_m^{0.5}$ is independent of mobility degradation, parasitic series resistance and velocity saturation effects. The RM was further improved in 2000 [18] to account for a more general mobility degradation model.

Summarizing the RM developments, the drain current I_D in the linear region can be expressed as [1–3]

$$I_D = \frac{W}{L_{eff}} \mu C_o (V_{GS} - V_T) V_{DS}, \tag{1}$$

where W is the channel width, C_o is the oxide capacitance per unit area, μ is the effective free-carrier mobility, and V_{GS} and V_{DS} are the intrinsic gate–source and drain–source voltages, respectively. The intrinsic voltages can be related to the external gate–source and drain–source voltages (V_g and V_d) by

$$V_{GS} = V_g - I_D R_D \tag{2}$$

and

$$V_{DS} = V_d - I_D(R_S + R_D). \tag{3}$$

Here R_D and R_S represent the drain and source parasitic series resistances, respectively. According to Fikry et al. [15], the velocity saturation effect is imbedded in the following free-carrier mobility model:

$$\mu = \frac{\mu_0}{\left(1 + \theta\left(V_g - V_T\right)\right)\left(1 + \frac{\mu_0 V_d}{L_{eff} v_{sat}}\right)}, \tag{4}$$

where μ_0 is the low-field mobility, θ is the mobility degradation factor due to the vertical field, and v_{sat} is the saturation velocity of the carriers. Using (1)–(4) and the approximation $V_g = V_{GS}$, it can be proved that

$$\frac{I_D}{g_m^{1/2}} = s^{-1/2}\left(V_g - V_T\right), \tag{5}$$

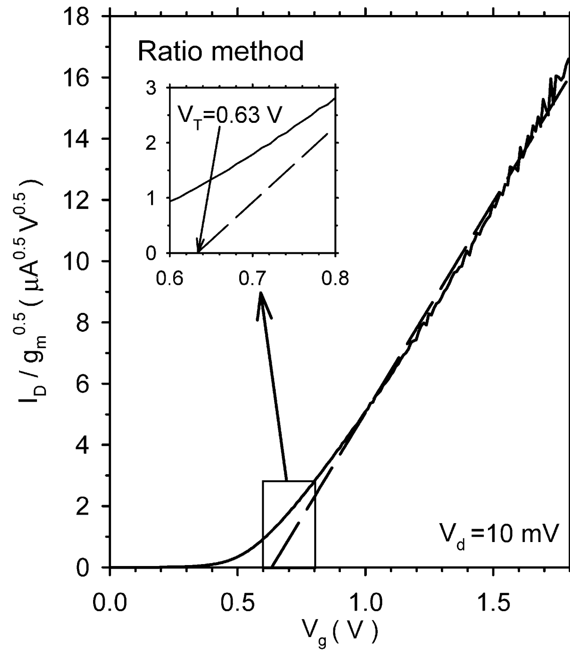

Fig. 6. RM implemented on the plot of the ratio of the drain current to the square root of the transconductance ($I_D/g_m^{0.5}$) versus V_g of the test bulk device measured at $V_d = 10$ mV. This method evaluates V_T from the intercept to the lateral axis of its straight line fit.

where g_m is the transconductance and

$$s = \frac{L_m - \left(\Delta L_{eff} - \frac{\mu_0 V_d}{v_{sat}}\right)}{W \mu_0 C_o V_d}. \tag{6}$$

Then, by plotting the $I_D/g_m^{1/2}$ versus V_g curve the values of V_T and s can be extracted from the intercept and the slope of its straight line fit. Fig. 6 shows the results of applying this method to the present test device. As can be observed, in the present case it is not clear where to do the linear approximation to be extrapolated to the V_g axis to extract the value of V_T. The $I_D/g_m^{1/2}$ versus V_g curve for the present test device shown in Fig. 6 does not appear to totally fulfill this method's assumptions, since it does not clearly behave in the linear manner expected. Therefore, the linear fit shown is just a guess, amidst the evident non-linearity and the noise present, significantly enhanced by dividing the current by the square root of its first derivative (g_m).

2.6. Transition method

This method uses the sub-threshold-to-strong inversion transition region of the MOSFET's transfer characteristics to extract the threshold voltage. It is based on

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