

Case IPR2020-00985
U.S. Patent No. 6,651,134

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.,
Petitioner

v.

MONTEREY RESEARCH, LLC,
Patent Owner

Case IPR2020-00985

U.S. Patent No. 6,651,134

PATENT OWNER'S PRELIMINARY SUR-REPLY

Mail Stop Patent Board
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

AMD criticizes Patent Owner’s discretionary analysis as “misleading” with respect to the substantial similarity of Wada—AMD’s primary reference—and Cowles—a reference that the Patent Office considered during prosecution of the ’134 Patent. (Preliminary Reply, 3.) Specifically, AMD mischaracterizes Wada in exactly the same manner as in its Petition, and incorrectly assumes that a description of Wada’s “‘data burst output’ as ‘uninterrupted’” (Preliminary Reply, 2) applies to individual bursts instead of the periods in between bursts. But AMD is mistaken on both accounts: Wada does not disclose uninterrupted individual data bursts and Wada is substantially similar to Cowles. Therefore, the Board should exercise its discretion and deny the Petition.

AMD incorrectly asserts that Wada “does not limit its teaching [to preventing interruptions in between bursts] and describes its ‘data burst output’ as ‘uninterrupted.’” (Preliminary Reply, 2.) But when Wada describes data burst outputs and increasing data throughput, it does so in the context of preventing “a *data-free period* (an *interruption* in the flow of data output) [which] is bound to occur *between two burst outputs.*” (Ex-1005, 5:50-51; POPR, 31.) All of Wada’s disclosures, including its first and second embodiments and the portion cited by AMD, are thus directed towards preventing interruptions *in between* bursts by providing multiple “output registers” such that one output register outputs data at the same time as other output registers retain new data:

“The SRAM practiced as the second embodiment includes three or more output registers. . . . Of the three output registers, the first register is used to retain fixedly the data read from a specific row of memory cells frequently accessed. The second and third output registers are employed to *carry out the uninterrupted burst output of data discussed in connection with the first embodiment.*” (Ex-1005, 16:11-25.)

Accordingly, Wada merely discloses an architecture that prevents interruptions in *between* bursts, but is *silent* as to preventing interruptions *of* bursts. (Ex-1005, 5:43-53, POPR, 30.) And Wada’s burst procedure may be terminated when the advance signal ADV is not High (Ex-1005, 2:55-60; POPR, 30), just as Cowles’ burst procedure may be terminated when the WE* signal is High. (Ex-1004, ¶0112.)

As such, Wada’s identified problem and alleged technical solutions are substantially similar to those of Cowles’s “continuous burst” device, which accesses a “second row of memory while bursting data out of a first row.” (Ex-1004, ¶¶0107-0108; POPR, 24-25.) AMD’s assertion that these similarities “have nothing to do with the ‘non-interruptible’ claim element Patentee relied upon to gain allowance” (Preliminary Reply, 1) is incorrect. While discussing Cowles, the Applicant confirmed that Cowles’ continuous burst architecture, which nevertheless permits termination of bursts (Ex-1004, ¶0172), “has little or nothing to do with whether a ‘burst’ can be interrupted.” (Ex-1004, ¶¶0107-0108; POPR, 12-13, 24-28.) That criticism of Cowles applies equally to Wada because Wada’s prohibition against

intra-burst interruptions is identical in purpose and operation to the equivalent feature of Cowles.

AMD's reliance on its alternative grounds based on Wada and Barrett fares no better. Barrett does not cure Wada's deficiencies because Barrett is directed towards external data transfers, not generation of internal address signals. (Ex-1010, 4:18-32; POPR, 43.) As such, even the combination of Wada and Barrett fails to disclose generating a predetermined number of internal address signals without interruption. (POPR, 42-43.) And Wada and Barrett are directed towards incompatible goals: Wada seeks to *prevent* interruptions in between bursts (Ex-1005, 5:43-53), while Barrett *ensures* pauses in between bursts (Ex-1010, Abstract, 3:12-22). (POPR, 44-45.) AMD mischaracterizes Barrett's disclosure: Barrett addresses the alleged prior art issue of "allowing a pause at *any* point" (2:39-40) by allowing "pausing *only at pre-determined, fixed intervals of n data transfer cycles.*" (Ex-1010, 3:8-9.) In short, Barrett does not cure Wada's deficiencies, nor does the combination of Barrett with Wada provide any disclosure meaningfully different from that of Cowles.

Because Wada is substantially similar to art the Office already considered, and because AMD's Preliminary Reply continues to mischaracterize Wada, the Board should respectfully exercise its discretion and deny the Petition.

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Dated: October 2, 2020

Respectfully submitted,

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