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United States Patent [19]

Cowles

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[54] **CONTINUOUS BURST EDO MEMORY DEVICE**

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[51] **Int. Cl.**[6] **G11C 8/00**

[52] **U.S. Cl.** **365/236**; 365/238.5; 365/239; 395/496

[58] **Field of Search** 365/236, 238.5, 365/239; 395/496

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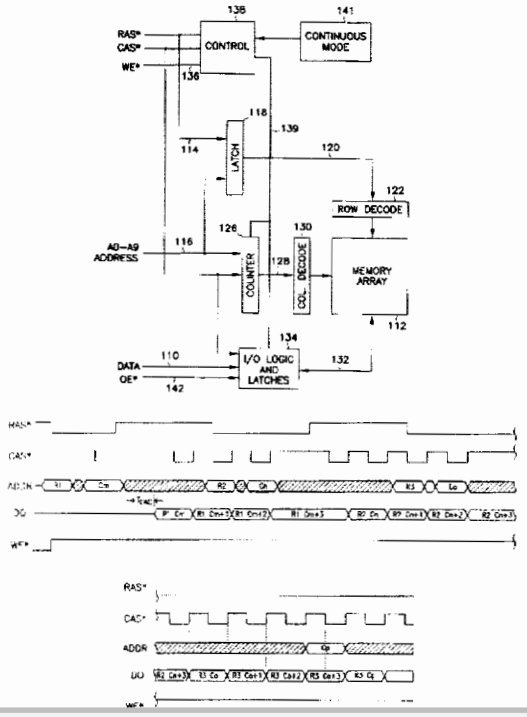
[57] **ABSTRACT**

An integrated circuit memory device is described which can operate at high data speeds. The memory device can either store or retrieve data from the memory in a burst access operation. The burst operations latch a memory address from external address lines and internally generates additional memory addresses. The integrated circuit memory can output data in a continuous stream while new rows of the memory are accessed. A method and circuit are described for outputting a burst of data stored in a first row of the memory while accessing a second row of the memory.

20 Claims, 7 Drawing Sheets



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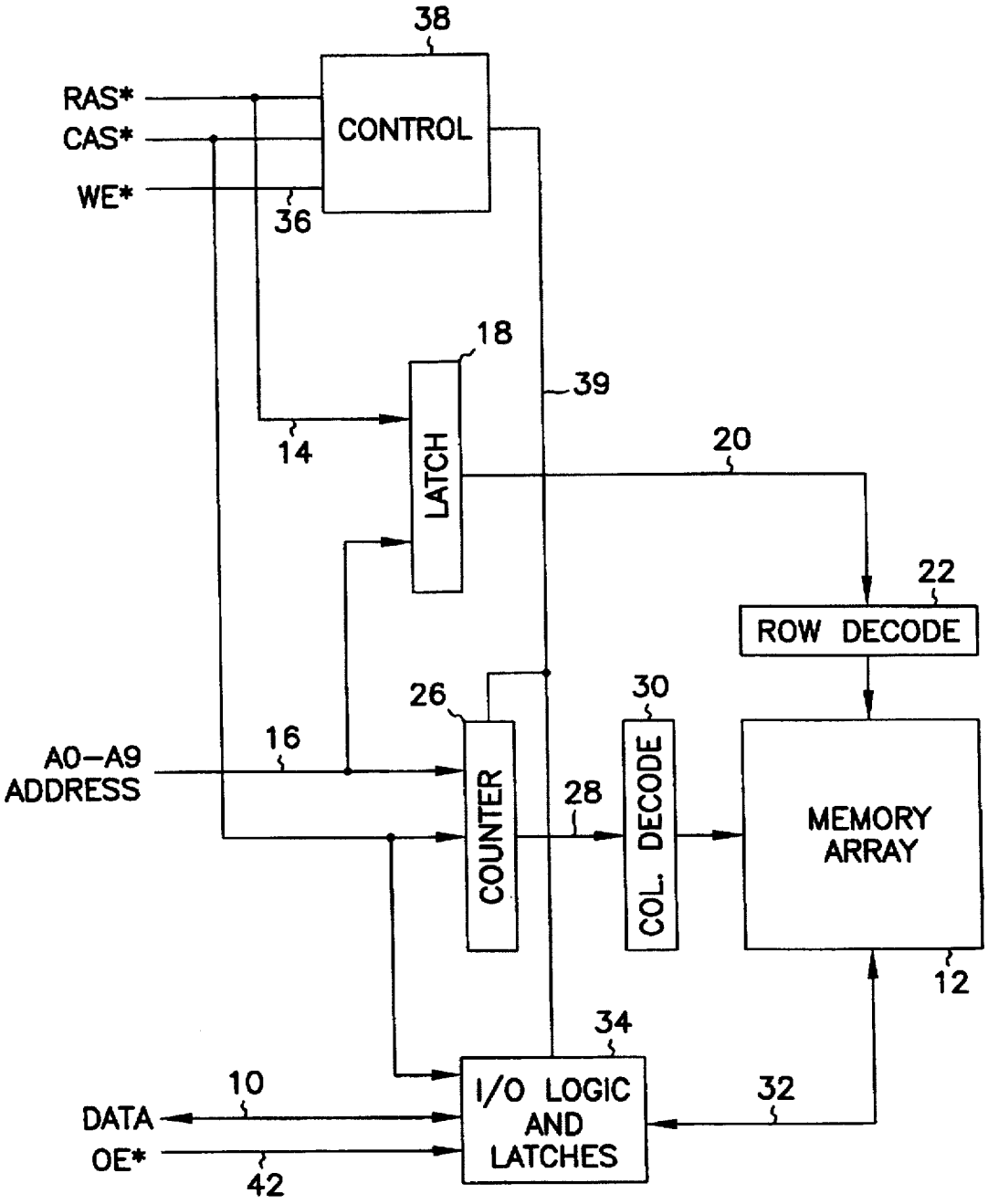

FIG. 1 (PRIOR ART)

Burst Length	Starting Column Address A_2	A_1	A_0	Linear	Interleave
2	V	V	0	0-1	0-1
	V	V	1	1-0	1-0
4	V	0	0	0-1-2-3	0-1-2-3
	V	0	1	1-2-3-0	1-0-3-2
	V	1	0	2-3-0-1	2-3-0-1
	V	1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

FIG. 2
(PRIOR ART)

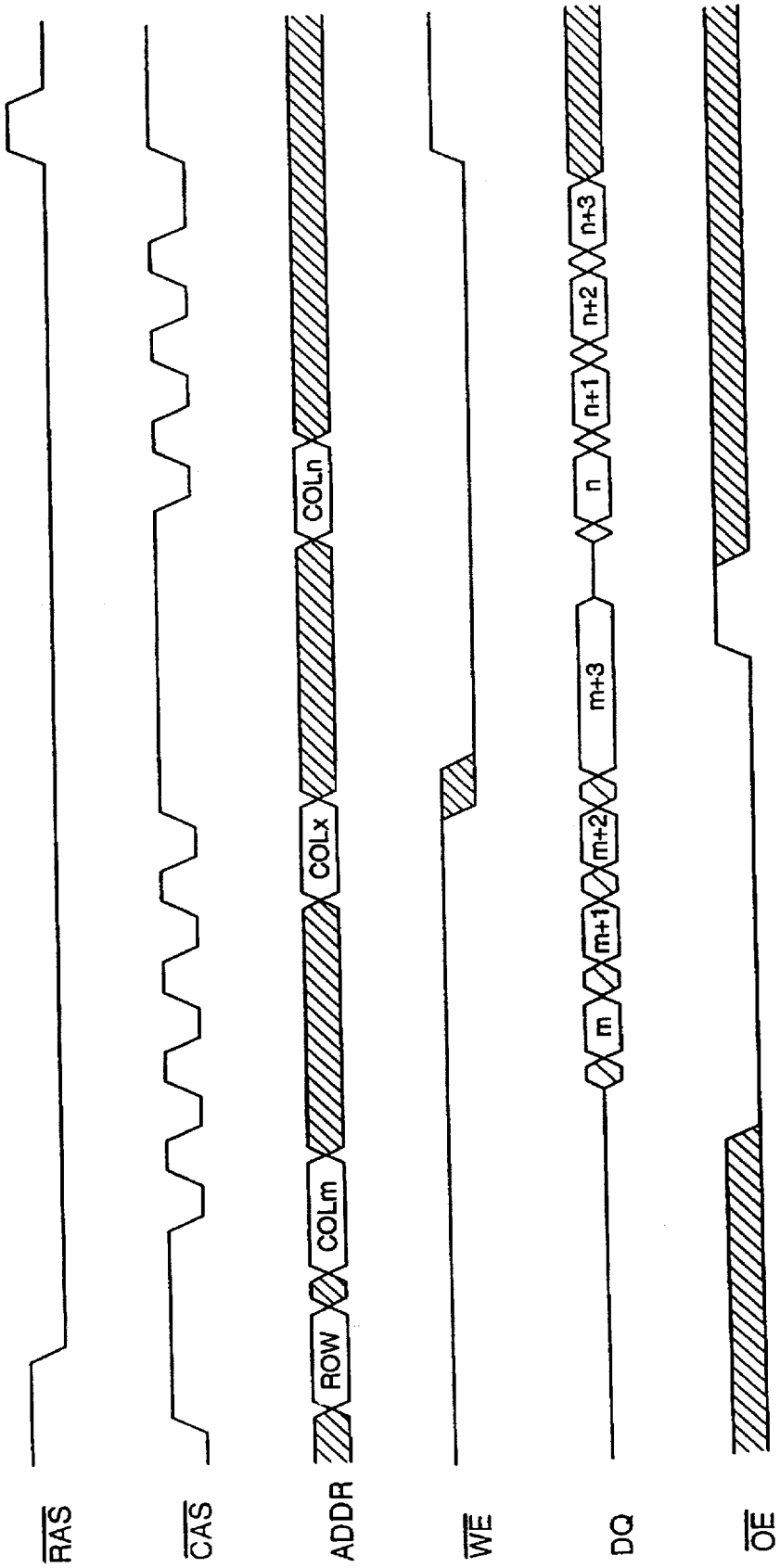

FIG. 3 (PRIOR ART)

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