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United States Patent [19]

Wada

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[54] **SEMICONDUCTOR MEMORY CAPABLE OF BURST OPERATION**

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[73] Assignee: **Mitsubishi Denki Kabushiki Kaisha**, Tokyo, Japan

[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

[21] Appl. No.: **08/833,178**

[22] Filed: **Apr. 4, 1997**

Related U.S. Application Data

[63] Continuation of application No. 08/547,341, Oct. 24, 1995, abandoned.

[30] **Foreign Application Priority Data**

Nov. 1, 1994 [JP] Japan 6-268925

[51] **Int. Cl.**[7] **G11C 7/00**

[52] **U.S. Cl.** **365/78**; 365/236; 365/189.2; 365/230.03

[58] **Field of Search** 365/236, 230.03, 365/189.12, 240, 189.02, 230.02, 78, 233

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[57] **ABSTRACT**

A semiconductor memory for operating in burst mode. The memory has a memory cell array divided into a plurality of memory blocks, a plurality of (e.g., 2) output registers each including a plurality of output data retaining blocks corresponding to the multiple memory blocks, and a burst counter unit. The output registers alternately receive data transferred from the memory cell array. In accordance with the result of counting by the burst counter unit, the data retained in the output registers is output alternately in bursts, whereby the speed of data read operation in the memory is boosted regardless of the operating speed of the memory cell array therein.

12 Claims, 16 Drawing Sheets

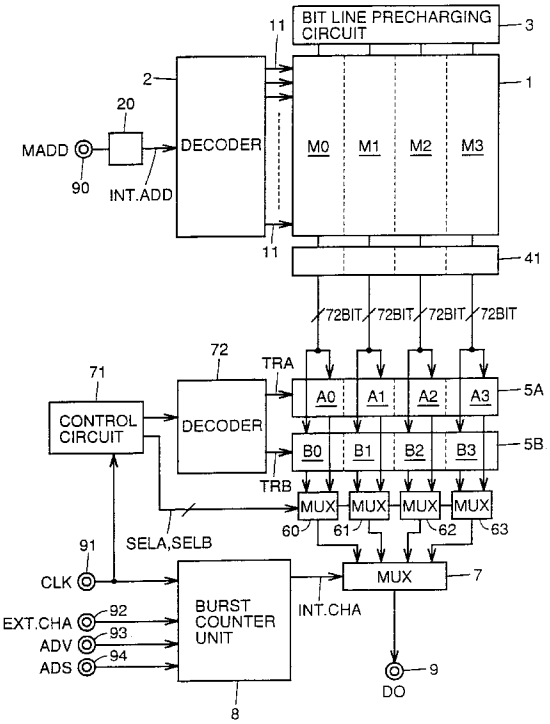
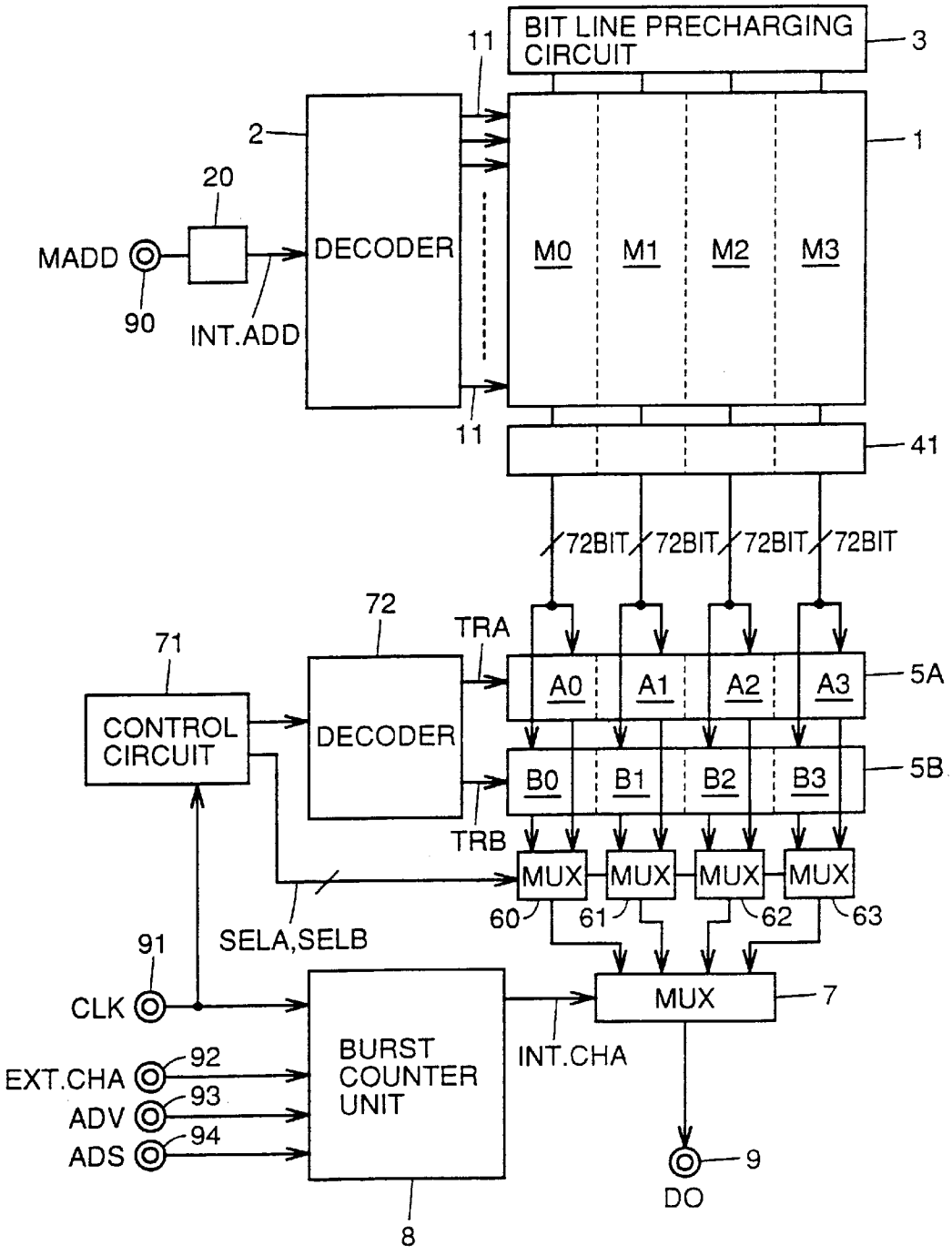


FIG. 1



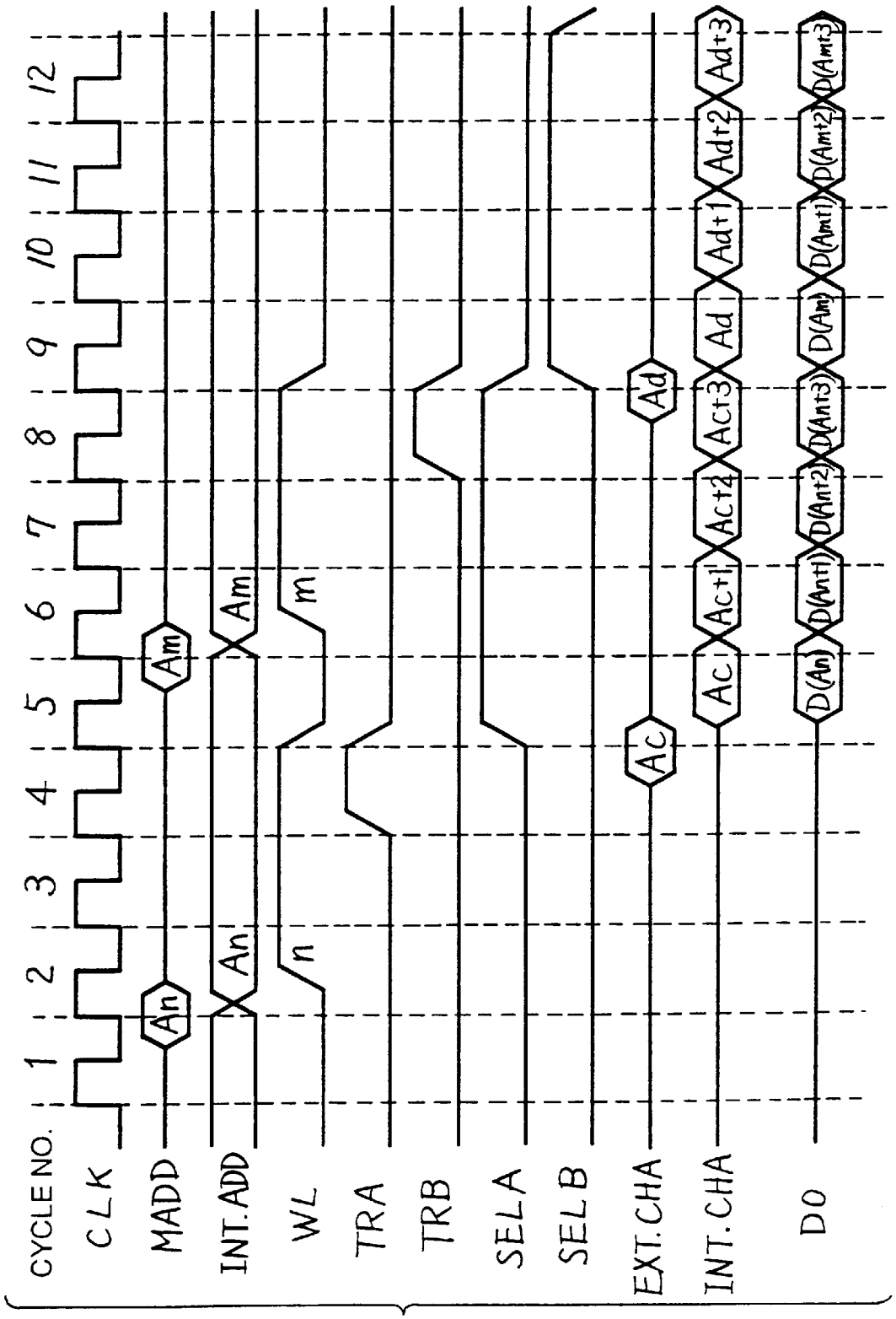
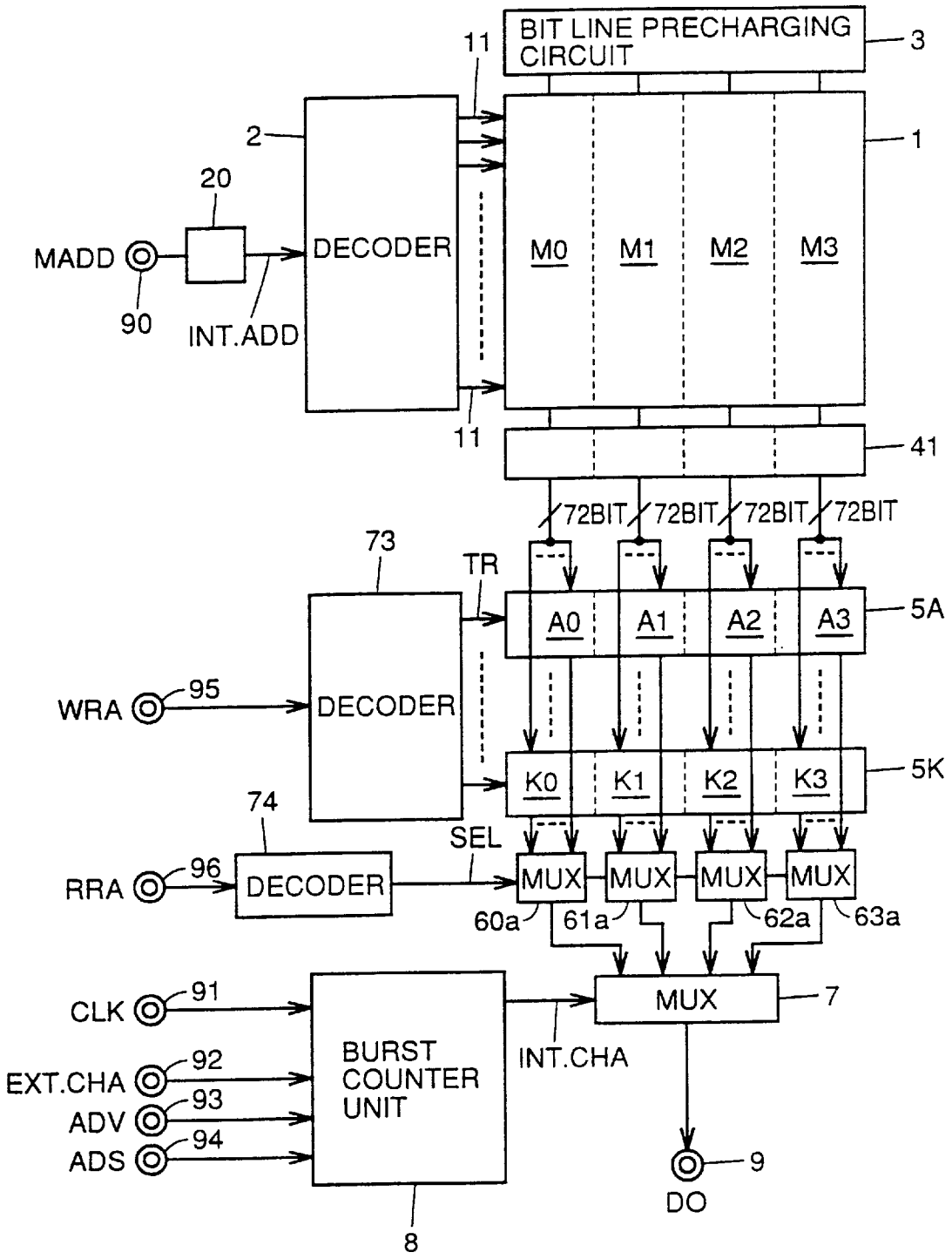


FIG.2

FIG.3



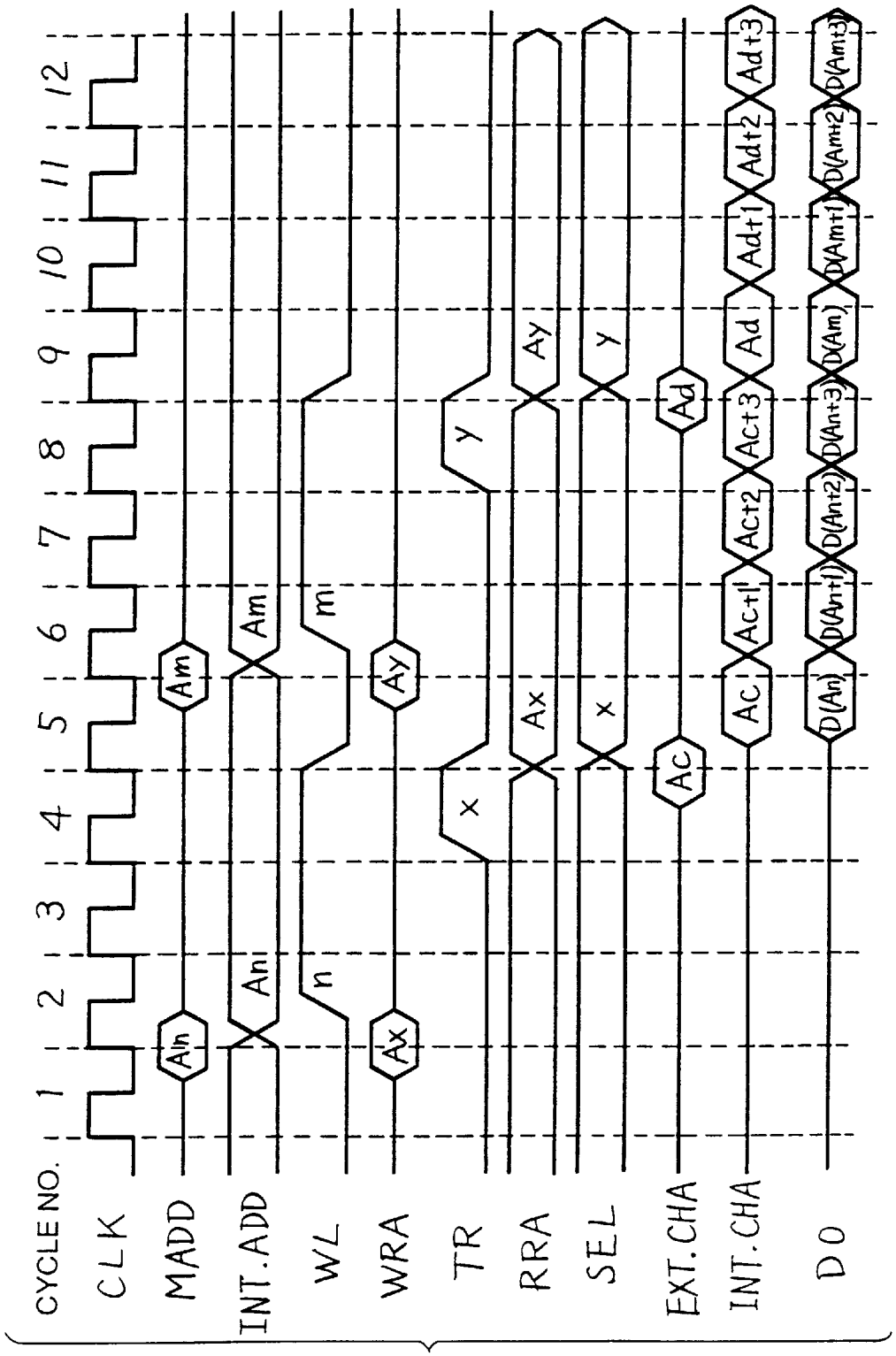


FIG. 4

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