PETITIONER'S DEMONSTRATIVE EXHIBIT 1016

Advanced Micro Devices, Inc. et al.
v.
Monterey Research LLC

Petitioners' Presentation For IPR2020-00985
U.S. Patent No. 6,651,134
September 1, 2021

Overview

- Alleged Invention
- "Non-Interruptible" Limitation
  - Wada
  - Wada + Barrett
  - Patent Owner Fails To Distinguish Prior Art
- "Predetermined Number" Limitation
- No Objective Indicia of Non-Obviousness

Overview

- Alleged Invention
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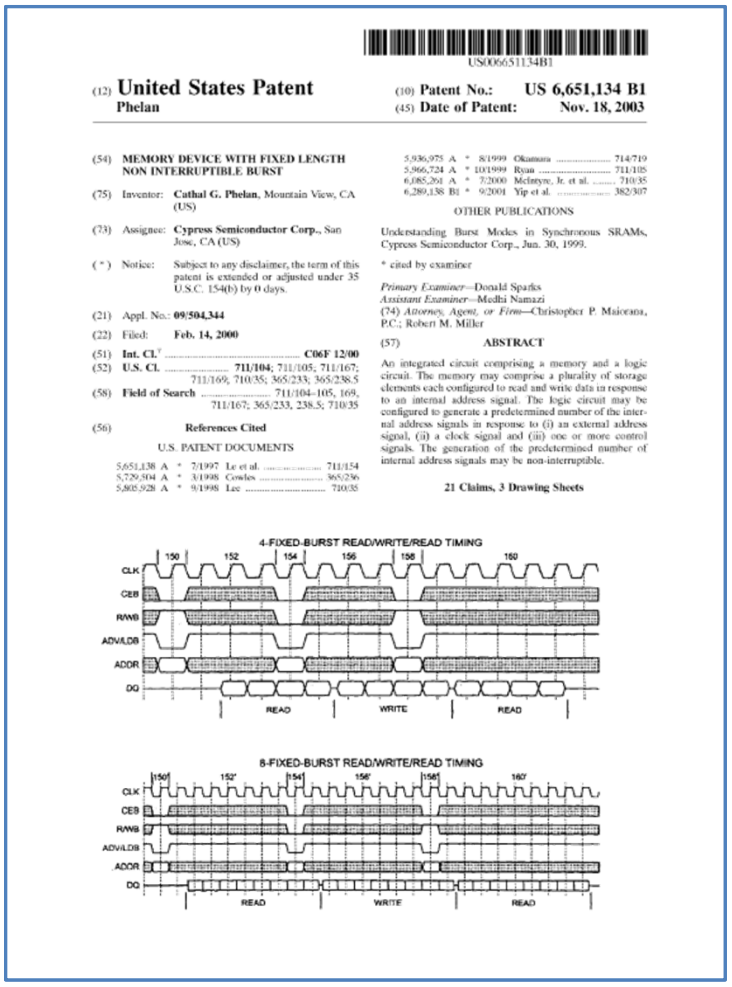
’134 Patent – Non-Interruptible Burst Memory



US006651134B1

(12) **United States Patent**
Phelan

(10) **Patent No.: US 6,651,134 B1**
(45) **Date of Patent: Nov. 18, 2003**

(54) **MEMORY DEVICE WITH FIXED LENGTH NON INTERRUPTIBLE BURST**

(75) Inventor: **Cathal G. Phelan**, Mountain View, CA (US)

(73) Assignee: **Cypress Semiconductor Corp.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/504,344**

(22) Filed: **Feb. 14, 2000**

(51) **Int. Cl.**[7] **C06F 12/00**

(52) **U.S. Cl.** **711/104**; 711/105; 711/167; 711/169; 710/35; 365/233; 365/238.5

(58) **Field of Search** 711/104–105, 169, 711/167; 365/233, 238.5; 710/35

(56) **References Cited**

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6,289,138 B1 * 9/2001 Yip et al. 382/307

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Primary Examiner—Donald Sparks
Assistant Examiner—Medhi Namazi
(74) *Attorney, Agent, or Firm*—Christopher P. Maiorana, P.C.; Robert M. Miller

(57) **ABSTRACT**

An integrated circuit comprising a memory and a logic circuit. The memory may comprise a plurality of storage elements each configured to read and write data in response to an internal address signal. The logic circuit may be configured to generate a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals. The generation of the predetermined number of internal address signals may be non-interruptible.

21 Claims, 3 Drawing Sheets

4-FIXED-BURST READ/WRITE/READ TIMING

8-FIXED-BURST READ/WRITE/READ TIMING

1. A circuit comprising:

a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal; and

a logic circuit configured to generate a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

’134 Patent (Ex-1001) at Cover, claim 1

Demonstrative Exhibit 1016, 0004

Grounds Presented In Petition

Ground	Prior Art and Claims
1	Wada anticipates claims 1-3, 8, 12-13, 16, and 17
2	Wada renders obvious claims 1-4, 8, 12-14, 16, and 17
2a	Wada + Barrett renders obvious claims 1-4, 8, 12-14, 16, and 17
3	Wada + Fujioka renders obvious claims 4-7 and 18-20
3a	Wada + Barrett + Fujioka renders obvious claims 4-7 and 18-20
4	Wada + Reeves renders obvious claims 9-10, 14, and 21
4a	Wada + Barrett + Reeves renders obvious claims 9-10, 14, and 21
5	Wada + Lysinger renders obvious claims 11 and 15
5a	Wada + Barrett + Lysinger renders obvious claims 11 and 15

Petition (Paper 1) at 5

Overview

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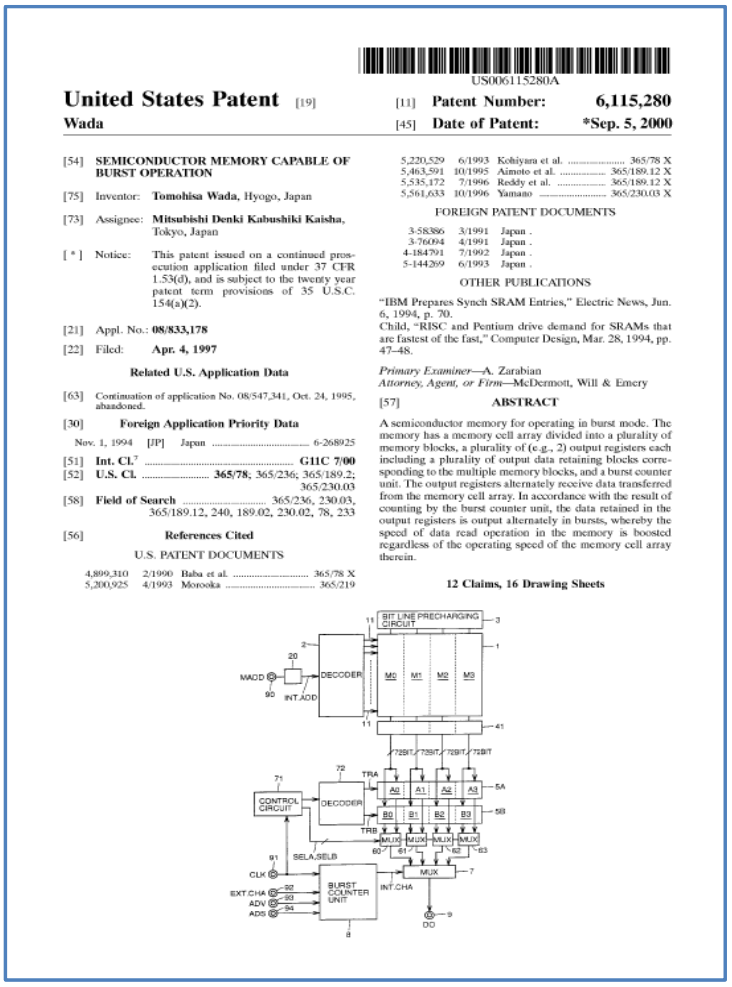
U.S. 6,115,280 ("Wada")



US006115280A

United States Patent [19]
Wada

[11] **Patent Number: 6,115,280**
[45] **Date of Patent: *Sep. 5, 2000**

[54] **SEMICONDUCTOR MEMORY CAPABLE OF BURST OPERATION**

[75] Inventor: **Tomohisa Wada**, Hyogo, Japan

[73] Assignee: **Mitsubishi Denki Kabushiki Kaisha**, Tokyo, Japan

[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

[21] Appl. No.: **08/833,178**

[22] Filed: **Apr. 4, 1997**

Related U.S. Application Data

[63] Continuation of application No. 08/547,341, Oct. 24, 1995, abandoned.

[30] **Foreign Application Priority Data**

Nov. 1, 1994 [JP] Japan 6-268925

[51] **Int. Cl.**[7] **G11C 7/00**

[52] **U.S. Cl.** **365/78**; 365/236; 365/189.2; 365/230.03

[58] **Field of Search** 365/236, 230.03, 365/189.12, 240, 189.02, 230.02, 78, 233

[56] **References Cited**

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"IBM Prepares Synch SRAM Entries," Electric News, Jun. 6, 1994, p. 70.
Child, "RISC and Pentium drive demand for SRAMs that are fastest of the fast," Computer Design, Mar. 28, 1994, pp. 47–48.

Primary Examiner—A. Zarabian
Attorney, Agent, or Firm—McDermott, Will & Emery

[57] **ABSTRACT**

A semiconductor memory for operating in burst mode. The memory has a memory cell array divided into a plurality of memory blocks, a plurality of (e.g., 2) output registers each including a plurality of output data retaining blocks corresponding to the multiple memory blocks, and a burst counter unit. The output registers alternately receive data transferred from the memory cell array. In accordance with the result of counting by the burst counter unit, the data retained in the output registers is output alternately in bursts, whereby the speed of data read operation in the memory is boosted regardless of the operating speed of the memory cell array therein.

12 Claims, 16 Drawing Sheets

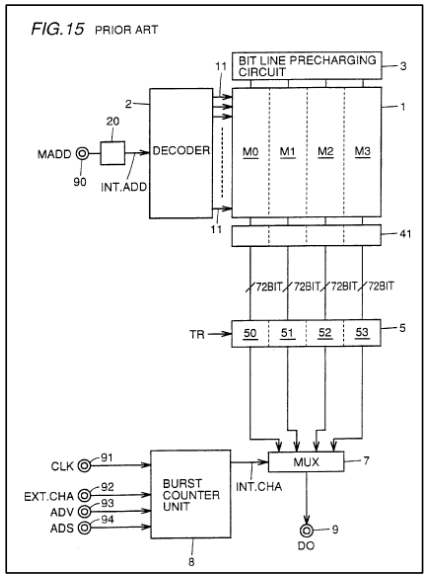
It is another object of the present invention to provide a semiconductor memory working in burst mode for a high-speed read operation irrespective of the operating speed of its memory cell array and without causing data output interruptions.

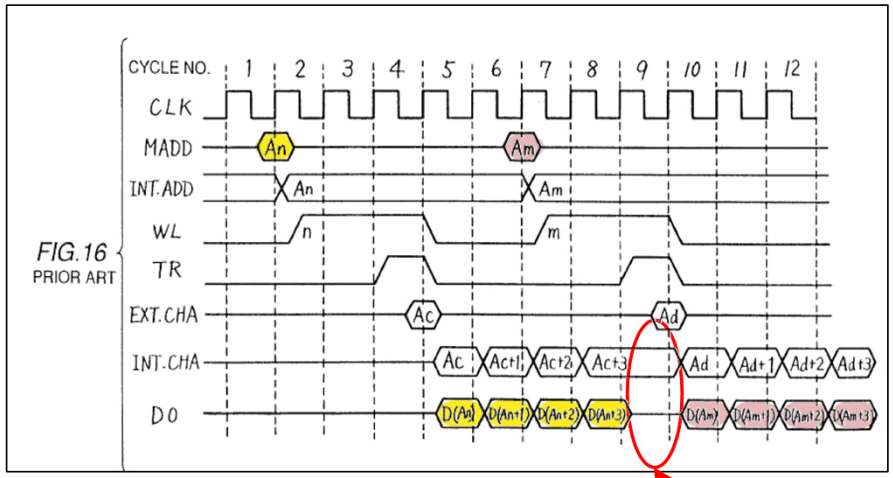
three or more output registers. This constitution provides one advantage identical to that of the first embodiment, i.e., the ability to execute data burst output in uninterrupted fashion.

Wada (Ex-1005) at 6:3-8, 16:12-15; Petition (Paper 1) at 23, 47; Pet. Reply (Paper 21) at 4

An Interruption Anywhere Defeats Wada's Goals

Wada's prior art embodiment of Figures 15-16 is unacceptable





Interruption introduced

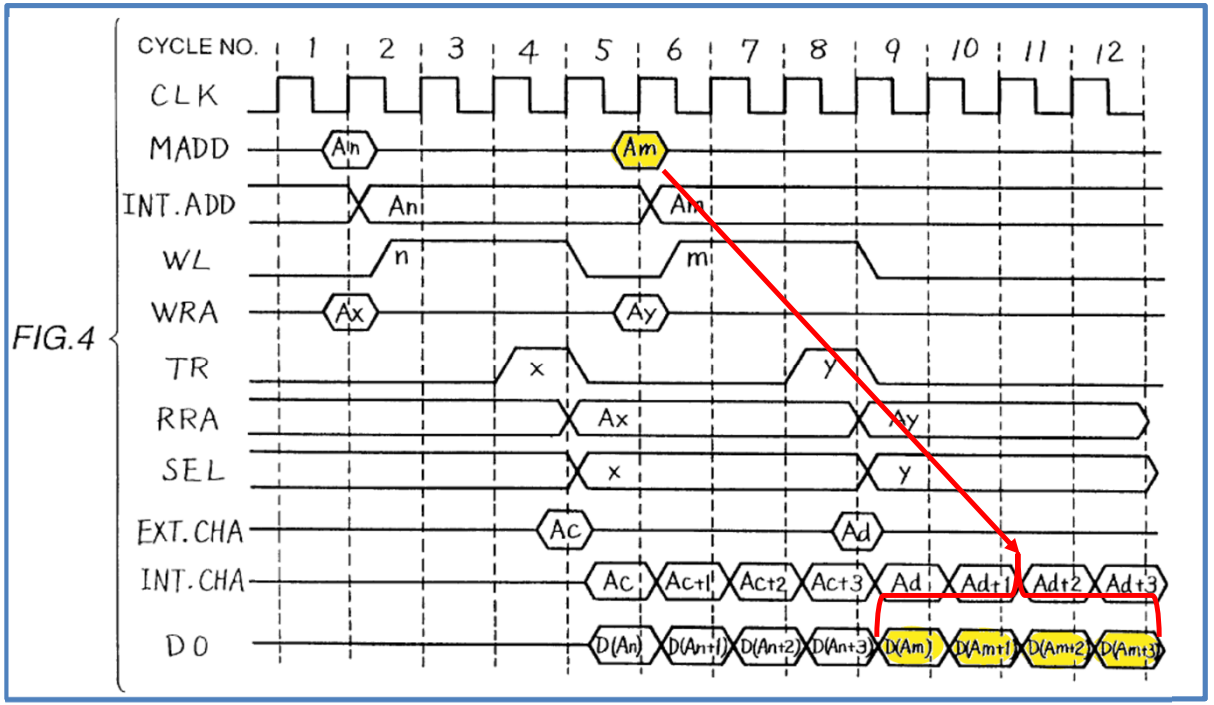
> Thus although the SRAM of FIG. **15** is exempt from the operative delays in the parts of the memory cell array **1**, the memory fails to shorten sufficiently the data transfer period in enhancing its operation speed. As a result, the SRAM of FIG. **15** is incapable of operating at a sufficiently high speed.

Wada (Ex-1005) at 5:59-63, Figs. 15, 16; Pet. Reply (Paper 21) at 2-4

Wada's Bursts Are Not Interruptible

Wada's second embodiment (Figs. 3-4) eliminates interruptions in burst addresses generated corresponding to external address Am.

described actions are carried out continuously. This allows the data corresponding to the address Am to be output uninterrupted in burst mode.



Wada (Ex-1005) at 16:8-10, Fig. 4; Pet. (Paper 1) at 22-23; Pet. Reply (Paper 21) at 5.

Patent Owner's Expert Agrees

Patent Owner's expert agrees "data corresponding to the address Am" is one burst.

described actions are carried out continuously. This allows the data corresponding to the address Am to be output uninterrupted in burst mode.

Wada at 16:8-10

Q. And so the D(Am) to D(Am+3), that's one burst that corresponds to address Am; is that correct?

. . .

A. In this case, if the signals are maintained to not interrupt a burst in this embodiment of Wada, then those four transactions Dm—I'm sorry, D(Am) onward ***would be the burst for the address Am*** in clock cycle 6.

Brogioli Dep. at 211:23-212:7 (emphasis added)

Wada (Ex-1005) at 16:8-10; Brogioli Dep. (Ex-1015) at 211:23-212:7; Pet. Reply (Paper 21) at 5

Board Concurrence Recognized Wada's Overall Goal

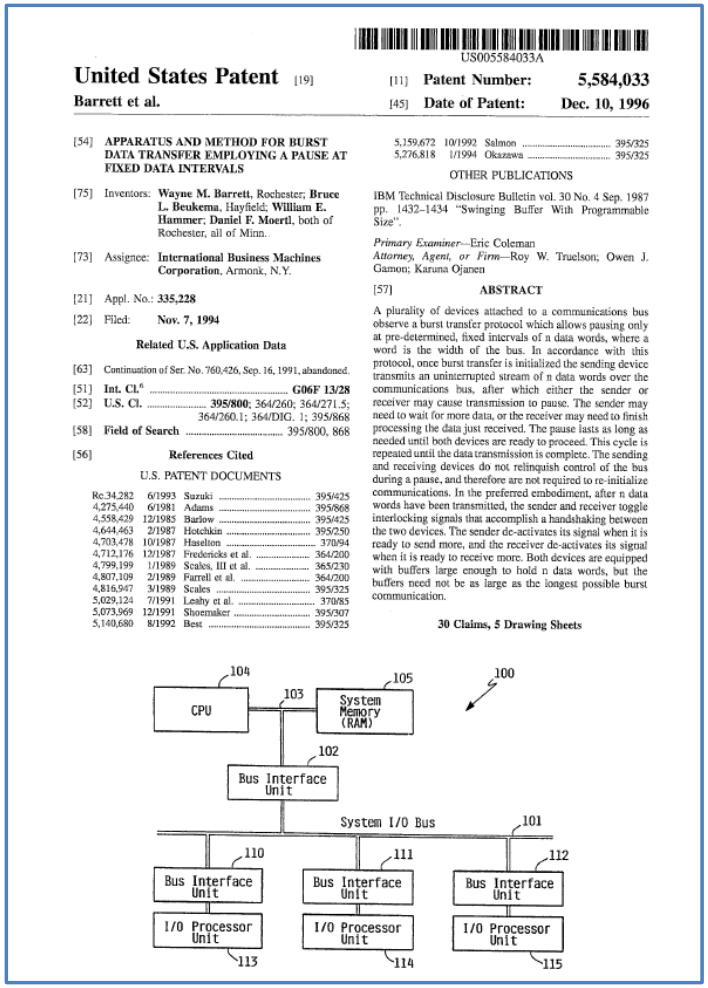
Institution Decision, APJ Horvath, concurring

> Although I agree with the majority that Wada's primary concern is eliminating data output interruptions *between* bursts, I disagree that a person skilled in the art would not read Wada to also teach or suggest eliminating data output interruptions *within* bursts. Indeed, an express object of Wada's invention is a memory circuit that operates in burst mode "without causing data output interruptions," not to operate in burst mode without causing data output interruptions only *between* bursts. Ex. 1005, 6:3–8. As shown in

> uninterrupted in burst mode." Id. at 16:7–10. That is, Wada teaches its Second Embodiment has not only eliminated data output interruptions *between* bursts, but should be operated in a manner having no data output interruptions *within* bursts. *Id.*, Fig. 4.

Institution Decision (APJ. Horvath, concurring) (Paper 13) at 28.

U.S. 5,584,033 ("Barrett")



US005584033A

United States Patent [19]
Barrett et al.

[11] **Patent Number: 5,584,033**
[45] **Date of Patent: Dec. 10, 1996**

[54] **APPARATUS AND METHOD FOR BURST DATA TRANSFER EMPLOYING A PAUSE AT FIXED DATA INTERVALS**

[75] Inventors: **Wayne M. Barrett**, Rochester; **Bruce L. Beukema**, Hayfield; **William E. Hammer**; **Daniel F. Moertl**, both of Rochester, all of Minn.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **335,228**

[22] Filed: **Nov. 7, 1994**

Related U.S. Application Data

[63] Continuation of Ser. No. 760,426, Sep. 16, 1991, abandoned.

[51] **Int. Cl.**[6] **G06F 13/28**

[52] **U.S. Cl.** **395/800**; 364/260; 364/271.5; 364/260.1; 364/DIG. 1; 395/868

[58] **Field of Search** 395/800, 868

[56] **References Cited**

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IBM Technical Disclosure Bulletin vol. 30 No. 4 Sep. 1987 pp. 1432–1434 "Swinging Buffer With Programmable Size".

Primary Examiner—Eric Coleman
Attorney, Agent, or Firm—Roy W. Truelson; Owen J. Gamon; Karuna Ojanen

[57] **ABSTRACT**

A plurality of devices attached to a communications bus observe a burst transfer protocol which allows pausing only at pre-determined, fixed intervals of n data words, where a word is the width of the bus. In accordance with this protocol, once burst transfer is initialized the sending device transmits an uninterrupted stream of n data words over the communications bus, after which either the sender or receiver may cause transmission to pause. The sender may need to wait for more data, or the receiver may need to finish processing the data just received. The pause lasts as long as needed until both devices are ready to proceed. This cycle is repeated until the data transmission is complete. The sending and receiving devices do not relinquish control of the bus during a pause, and therefore are not required to re-initialize communications. In the preferred embodiment, after n data words have been transmitted, the sender and receiver toggle interlocking signals that accomplish a handshaking between the two devices. The sender de-activates its signal when it is ready to send more, and the receiver de-activates its signal when it is ready to receive more. Both devices are equipped with buffers large enough to hold n data words, but the buffers need not be as large as the longest possible burst communication.

30 Claims, 5 Drawing Sheets

The essential feature of burst communication is that the data transfer takes place at high speed and without interruption. This feature places certain constraints on the design of devices to handle the pauses. In effect, allowing a pause at any point defeats the purpose of burst transmission, which is to send data a rapidly as possible in an uninterrupted stream.

Barrett (Ex-1010) at 1:64-67, 2:39-41; Petition (Paper 1) at 50-51, Pet. Reply (Paper 21) at 17

Demonstrative Exhibit 1016, 0012

Board Agreed Wada + Barrett Teaches Non-Interruptible Burst

Institution Decision

> We conclude that, in light of Barrett's teaching that "allowing a pause at any point defeats the purpose of burst transmission, which is to send data a[s] rapidly as possible in an uninterrupted stream" (Ex. 1010, 2:39–41), skilled artisans had reason to modify Wada's conventional embodiment or Second Embodiment to remove the ability to interrupt burst-generation via external signals. Thus, the modified conventional embodiment and Second Embodiment would generate internal address or internal chunk addresses, respectively, such that their generation "cannot be stopped or terminated once initiated until the fixed number of internal addresses has been generated." *See* Pet. 12 (claim construction).

Institution Decision (Paper 13) at 21

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  - Wada + Barrett
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- "Predetermined Number" Limitation
- No Objective Indicia of Non-Obviousness

Patent Owner Fails To Distinguish Prior Art

- Wada's teachings not limited to eliminating interruptions only ***between*** bursts
- Wada's control signals make it no more "interruptible" than those of the '134 Patent
- Wada and Barrett are not directed to opposing goals

Pet. Reply (Paper 21) at 2-3, 8-12, 17; Petition (Paper 1) at 8, 51-53

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- Wada's control signals make it no more "interruptible" than those of the '134 Patent
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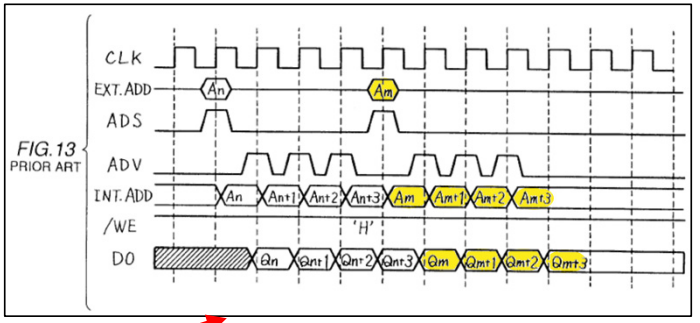
Pet. Reply (Paper 21) at 2-3, 8-12, 17; Petition (Paper 1) at 8, 51-53

Wada Eliminates Interruptions Between And Within Bursts

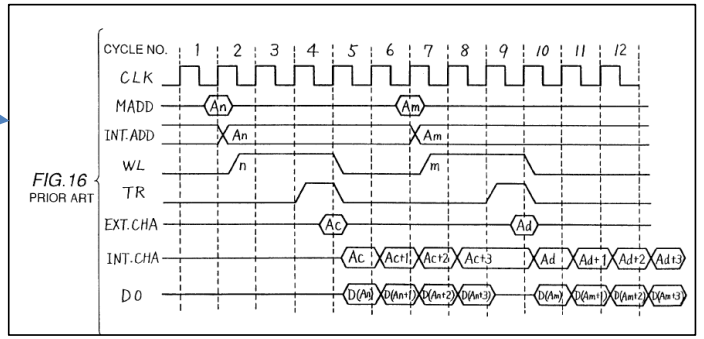
Wada solves all problems preventing high speed operation

It is another object of the present invention to provide a semiconductor memory working in burst mode for a high-speed read operation irrespective of the operating speed of its memory cell array and without causing data output interruptions.

Wada's First Conventional Embodiment



Wada's Second Conventional Embodiment

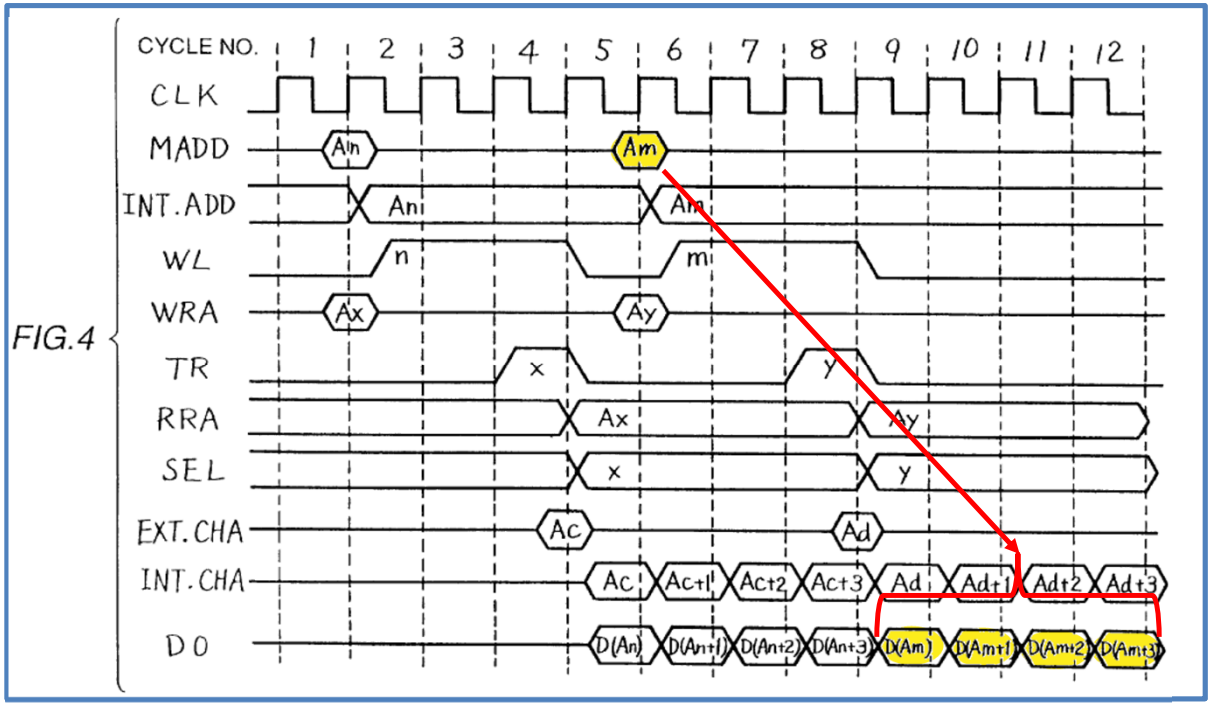


Wada (Ex-1005) at 6:3-7, Figs. 13, 16 (annotated); Pet. Reply (Paper 21) at 2-4

Wada Eliminates Interruptions Between And Within Bursts

Wada's second embodiment expressly teaches eliminating interruptions in the burst addresses corresponding to external address Am.

described actions are carried out continuously. This allows the data corresponding to the address Am to be output uninterrupted in burst mode.



Wada (Ex-1005) at 16:8-10, Fig. 4 (annotated); Pet. (Paper 1) at 22-23

Patent Owner Fails To Distinguish Prior Art

- Wada's teachings not limited to eliminating interruptions only ***between*** bursts
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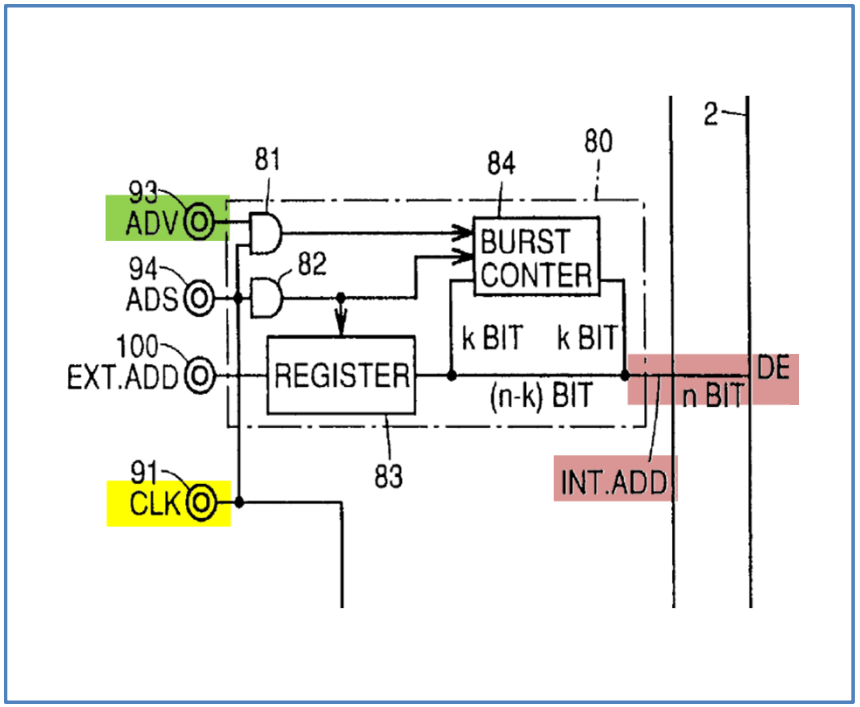
Pet. Reply (Paper 21) at 2-3, 8-12, 17; Petition (Paper 1) at 8, 51-53

Wada Is As "Uninterruptible" As The '134 Patent

Wada, Fig. 12 (excerpt)



'134 Patent, Fig. 2

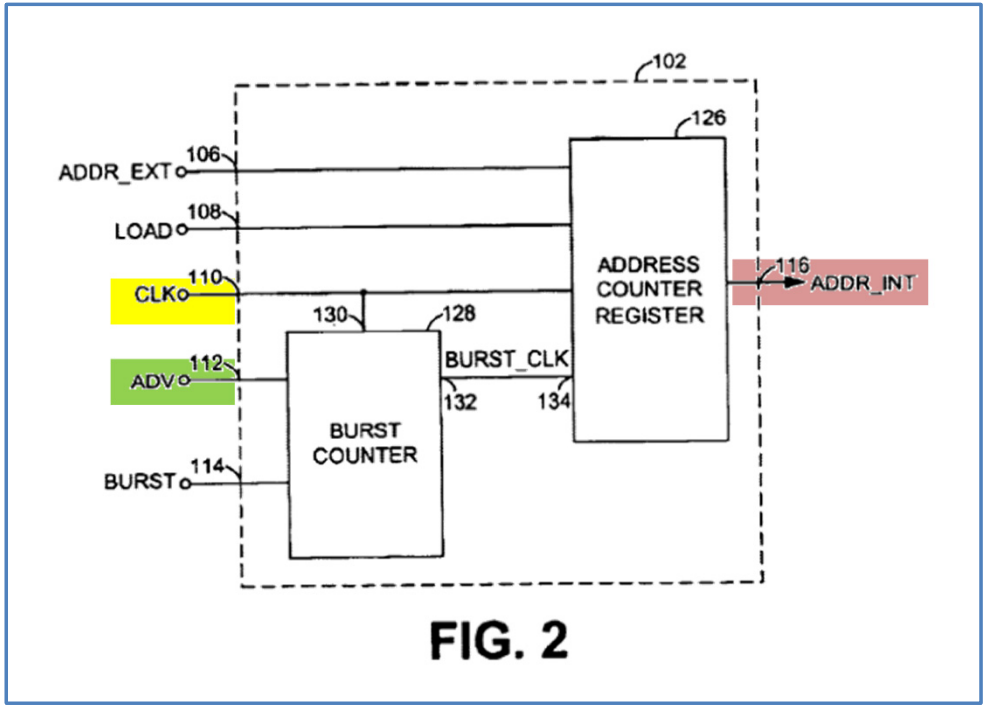


FIG. 2

Wada (Ex-1005) at Fig. 12 (annotated); '134 Patent (Ex-1001) at Fig. 2 (annotated); Pet. Reply (Paper 21) at 8-9; Petition (Paper 1) at 8

Demonstrative Exhibit 1016, 0020

Wada Is As "Uninterruptible" As The '134 Patent

The signals ADV and LOAD may be, in one example, a single signal (e.g., ADV/LDb). The signal ADV/LDb may be a control signal that may be in a first state or a second state. When the signal ADV/LDb is in the first state, the circuit **102** will generally load an address presented by the signal ADDR_EXT as an initial address. When the signal ADV/LDb is in the second state, the circuit **102** may be configured to generate the signal ADDR_INT as a fixed number of addresses in response to the signal CLK. The

When '134 Patent's ADV/LDB signal goes low, next burst is generated

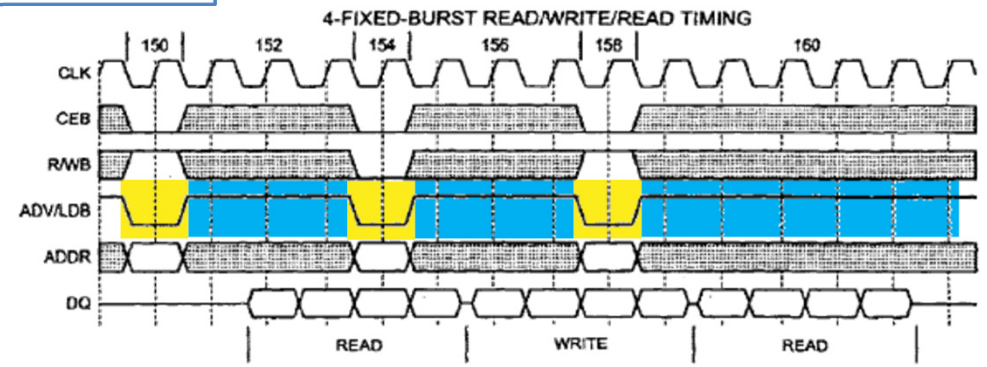


FIG. 5A

'134 Patent (Ex-1001) at 3:14-23, Fig. 5A (annotated); Pet. Reply (Paper 21) at 9-11

Wada Is As "Uninterruptible" As The '134 Patent

Patent Owner's expert agrees that ADV low starts the burst over:

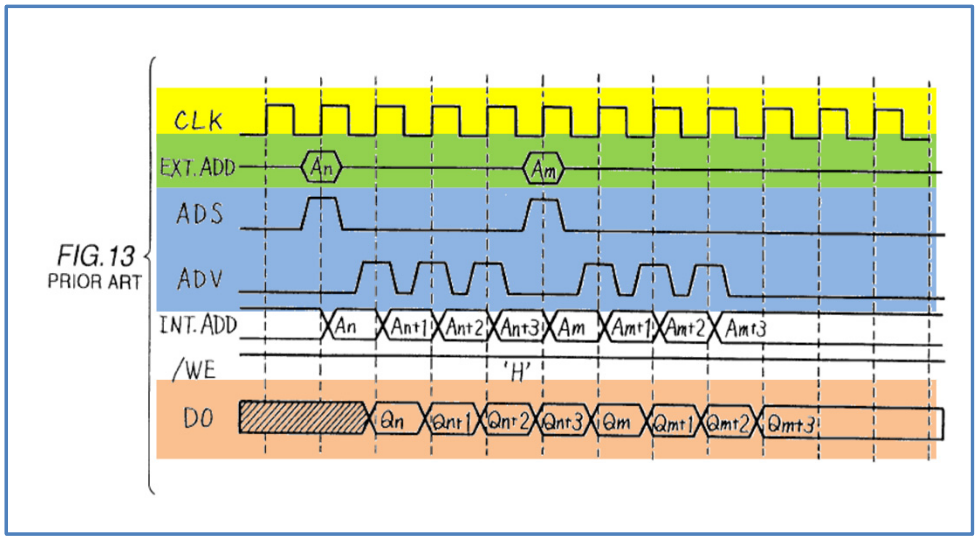
Q. So if the bursts started and the signal ADV/LDb were driven to the first state, wouldn't that load in a new starting address?

A. Let me reread the paragraph. I don't know that that paragraph explicitly states that. It says in that when the signal ADV/LDb is in a first state, the circuit will generally load an address presented by the ADDR_EXT as an initial address. And then the second state happens for ADV/LDb and then you have a non-interruptible burst. I don't know that it says -- ***I guess at some point, down the road if you replace or you reset ADV/LDb back to the first state, you would -- you know, I think that would be part of starting the process over***, for example.

Brogioli Dep. (Ex-1015) at 116:6-24 (emphasis added); Pet. Reply (Paper 21) at 11-12

Wada Is As "Uninterruptible" As The '134 Patent

Wada, Fig. 13



'134 Patent, Fig. 5A

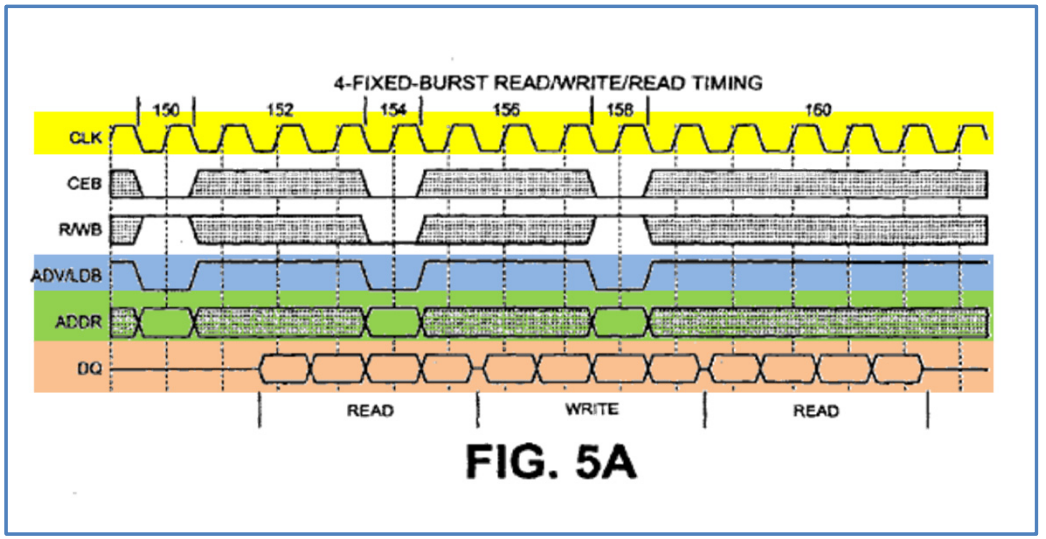


FIG. 5A

Wada (Ex-1005) at Fig. 13 (annotated); '134 Patent (Ex-1001) at Fig. 5A (annotated); Petition (Paper 1) at 28; Pet. Reply (Paper 21) at 10-11

Patent Owner Fails To Distinguish Prior Art

- Wada's teachings not limited to eliminating interruptions only ***between*** bursts
- Wada's control signals make it no more "interruptible" than those of the '134 Patent
- Wada and Barrett are not directed to opposing goals

Pet. Reply (Paper 21) at 2-3, 8-12, 17; Petition (Paper 1) at 8, 51-53

Wada and Barrett's Goals Not Opposed

Barrett and Wada are in similar fields:

Wada

"[T]he present invention [] provide[s] semiconductor memory working in burst mode for a high-speed read operation..." Wada at 6:3-7.

Barrett

"multiple CPUs and memory units communicating with other units via system I/O bus..." Barrett at 4:46-48

Barrett and Wada share goal of high-speed uninterrupted burst data transfer:

Wada

"allows the data corresponding to address Am to be output uninterrupted in burst mode." Wada at 16:8-10

"a semiconductor memory operating in burst mode at a sufficiently high speed irrespective of the operating speed of its memory cell array." Wada at 5:67-6:2.

Barrett

"a burst data transmission comprised of a plurality of uninterruptible streams of n data transfer cycles." Barrett at claim 1.

"allowing a pause at any point defeats the purpose of burst transmission, which is to send data as rapidly as possible in an uninterrupted stream." Barrett at 2:39-41.

Wada (Ex-1005) at 5:67-6:7, 16:8-10; Barrett (Ex-1010) at 2:39-41, 4:46-48, claim 1; Petition (Paper 1) at 51-52; Pet. Reply (Paper 21) at 17

Wada and Barrett's Goals Not Opposed

Patent Owner argues:

> Instead, AMD ignores the complication of changing the control circuitry that sets or resets the ADV signal and also ignores the consequences of its proposed modification, e.g., how to handle overflows of data when the burst output produces more data than can be consumed by the receiving device.

> Barrett, on the other hand, is explicitly directed towards ensuring pauses in between burst data transfers between I/O devices within a computing system—precisely the opposite of Wada's goal. *See, e.g.,* Ex-1010, Abstract, 3:12-22; Ex-

P.O. Sur-Reply (Paper 22) at 13-14

Wada And Barrett Do Not Defeat Each Other's Goals

Barrett

> Because the sending device transmits an uninterrupted stream of n data transfer cycles, it can guarantee that sufficient space will be available in its buffer for the next data transfer cycles stream within a specific time period. As a result, it can overlap the action of obtaining more data (refilling the buffer) with the action of transmitting the current data (emptying the buffer). Furthermore, allowing pauses only at specific intervals simplifies the bus interface circuitry because the number of potential cases (or scenarios) involving pauses is drastically reduced.

Barrett (Ex-1010) at 3:52-61; Pet Rep. (Paper 21) at 19

Overview

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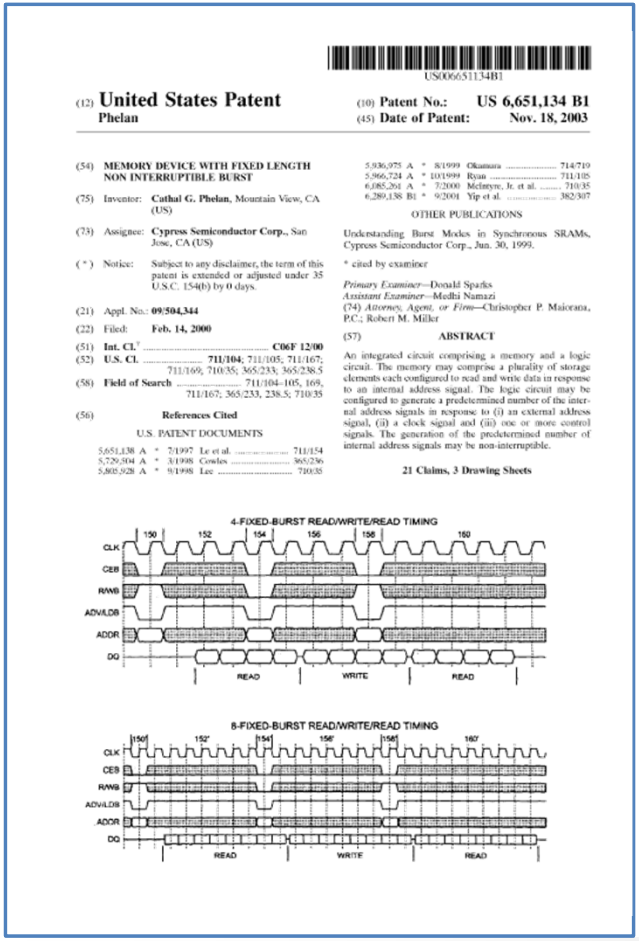
Wada Teaches Predetermined Number of Addresses

’134 Patent



US006651134B1

(12) **United States Patent**
Phelan

(10) **Patent No.: US 6,651,134 B1**
(45) **Date of Patent: Nov. 18, 2003**

(54) **MEMORY DEVICE WITH FIXED LENGTH NON INTERRUPTIBLE BURST**

(75) Inventor: **Cathal G. Phelan**, Mountain View, CA (US)

(73) Assignee: **Cypress Semiconductor Corp.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/504,344**

(22) Filed: **Feb. 14, 2000**

(51) **Int. Cl.**[7] **C06F 12/00**

(52) **U.S. Cl.** **711/104**; 711/105; 711/167; 711/169; 710/35; 365/233; 365/238.5

(58) **Field of Search** 711/104–105, 169, 711/167; 365/233, 238.5; 710/35

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,651,138 A * 7/1997 Le et al. 711/154
5,729,504 A * 3/1998 Cowles 365/236
5,805,928 A * 9/1998 Lee 710/35
5,936,975 A * 8/1999 Okamura 714/719
5,966,724 A * 10/1999 Ryan 711/105
6,085,264 A * 7/2000 McIntyre, Jr. et al. 710/35
6,289,138 B1 * 9/2001 Yip et al. 382/307

OTHER PUBLICATIONS

Understanding Burst Modes in Synchronous SRAMs, Cypress Semiconductor Corp., Jun. 30, 1999.

* cited by examiner

Primary Examiner—Donald Sparks
Assistant Examiner—Medhi Namazi
(74) *Attorney, Agent, or Firm*—Christopher P. Maiorana, P.C.; Robert M. Miller

(57) **ABSTRACT**

An integrated circuit comprising a memory and a logic circuit. The memory may comprise a plurality of storage elements each configured to read and write data in response to an internal address signal. The logic circuit may be configured to generate a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals. The generation of the predetermined number of internal address signals may be non-interruptible.

21 Claims, 3 Drawing Sheets

4-FIXED-BURST READ/WRITE/READ TIMING

8-FIXED-BURST READ/WRITE/READ TIMING

1. A circuit comprising:

a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal; and

a logic circuit configured to generate a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

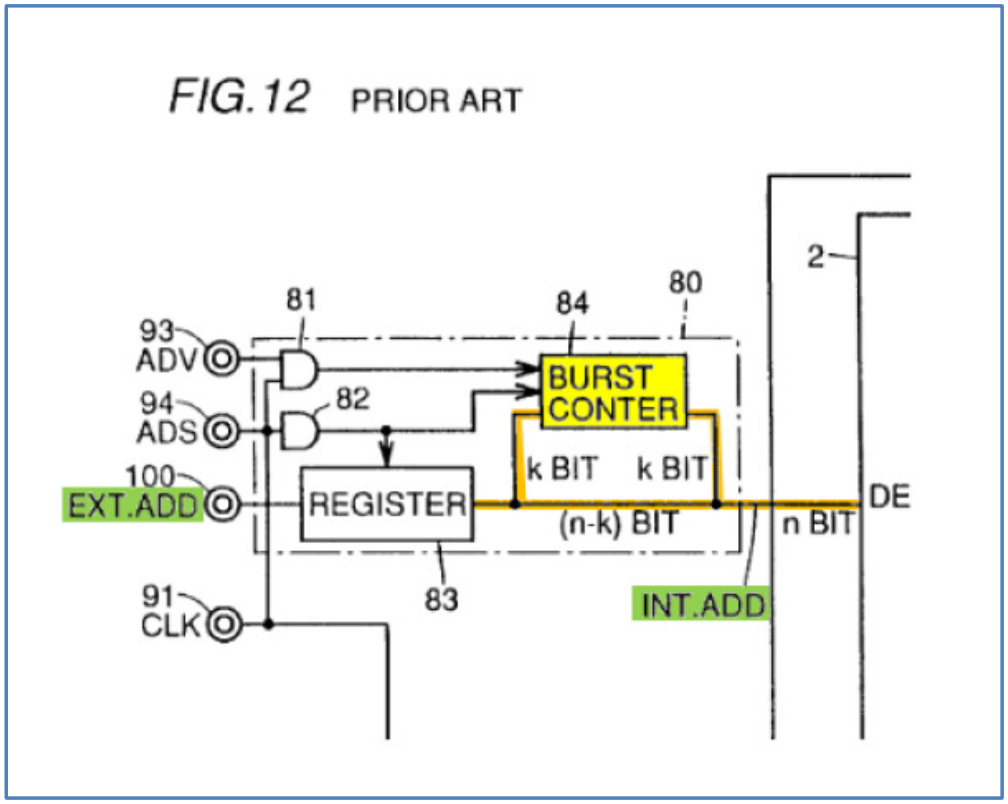
’134 Patent (Ex-1001) at claim 1

Demonstrative Exhibit 1016, 0029

Wada Teaches Predetermined Number of Addresses

Wada's burst counter is configured to generate 2^k internal addresses

Wada



Wada (Ex-1005) at Fig. 12 (annotated excerpt); Pet. Reply (Paper 21) at 7

Wada Teaches Predetermined Number of Addresses

Patent Owner's expert agrees that k bits represent 2^k states:

Q. I'm asking how many different states can be represented in k-bits?

A. States, let's say if you had one bit and it's a binary system, you could have two states. You have two bits, it would be four states, that kind of thing.

Q. In general, k-bits can represent two to the k states; is that correct?

A. If you're talking about a set of bits in a binary system, you could have two—two to k states, states that could be represented at any one instance in time.

Brogioli Dep. (Ex-1015) at 193:16-194:5; Pet. Reply (Paper 21) at 7

Wada Teaches Predetermined Number of Addresses

Institution Decision

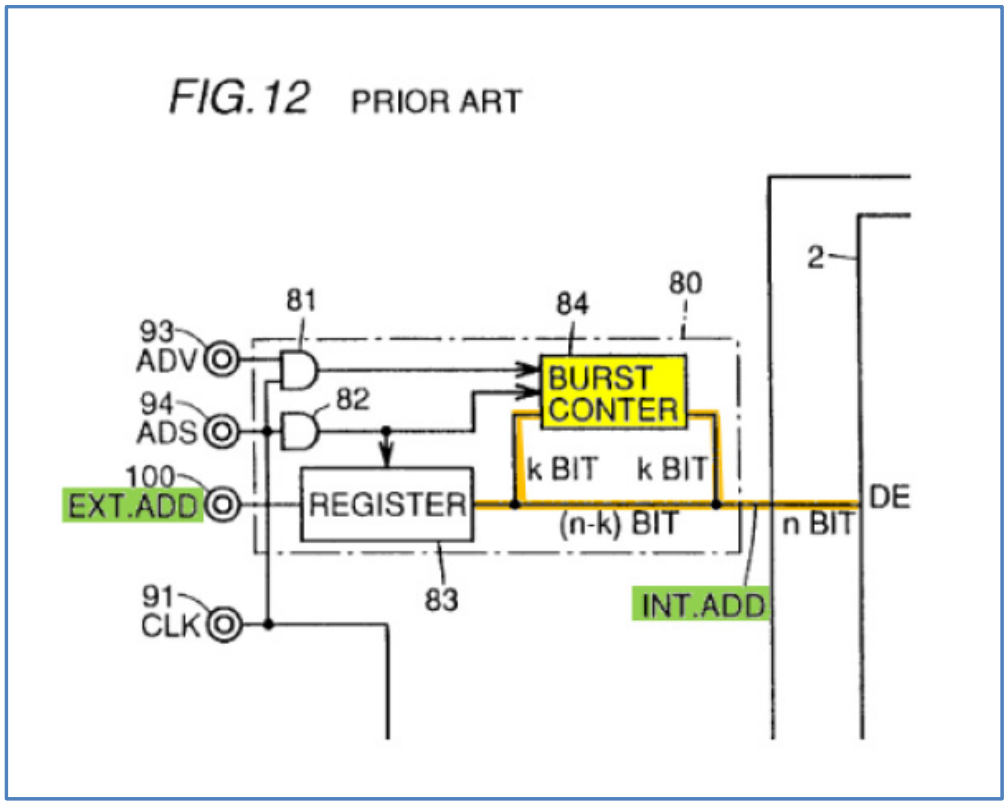
of internal addresses. Indeed, Patent Owner's argument discussed above, that deasserting the ADV signal would interrupt a burst (*see supra* at 16), could not apply upon modifying Wada's system such that continued generation of address signals in a burst is not interruptible by external signals. Accordingly, we do not agree with Patent Owner that, once modified, Wada's system fails to disclose the "predetermined number" limitation.

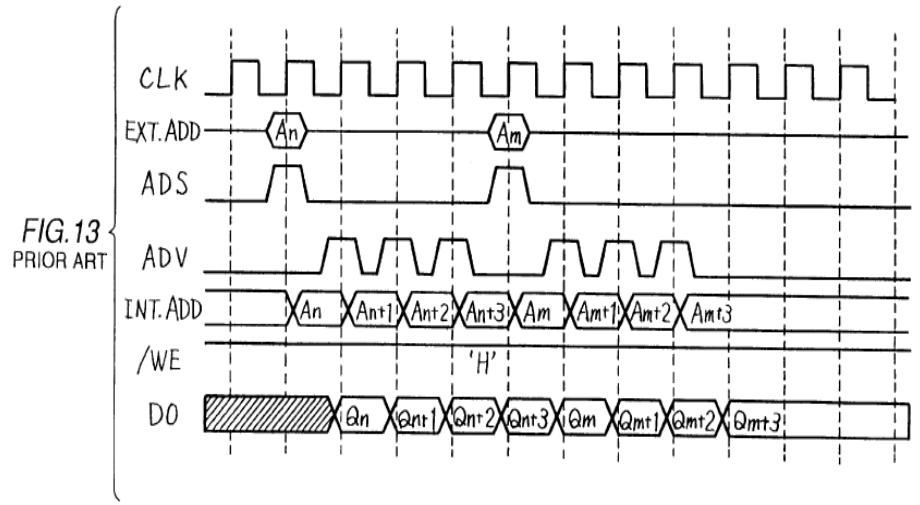
Institution Decision (Paper 13) at 21

Demonstrative Exhibit 1016, 0032

Patent Owner's Argument Fails

Wada





Wada (Ex-1005) at Figs. 12 (annotated excerpt), 13; Pet. Reply (Paper 21) at 7-8

Demonstrative Exhibit 1016, 0033

Overview

- Alleged Invention
- "Non-Interruptible" Limitation
  - Wada
  - Wada + Barrett
  - Patent Owner Fails To Distinguish Prior Art
- "Predetermined Number" Limitation
- No Objective Indicia of Non-Obviousness

No Objective Indicia of Non-Obviousness

Alleged long-felt need to mitigate DRAM/SDRAM refresh requirement fails to show non-obviousness

- No nexus: ’134 Patent claims encompass SRAM, which has no need of refresh
- ’134 Patent does not eliminate need to refresh DRAM
- Mitigation for DRAM refresh had already been solved in the prior art
- Timeline of JDEC specification publications shows opposite of what Patent Owner claims

Pet. Rep. (Paper 21) at 21-26

No Nexus Between Claims And Alleged Long-Felt Need

Patent Owner's alleged "long-felt need" is to mitigate need to refresh DRAM/SDRAM

Patent Owner Response:

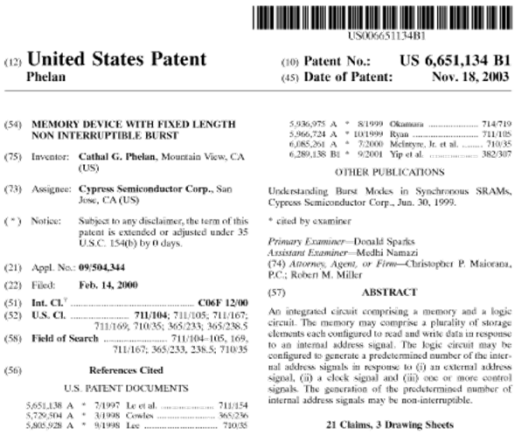
> The claimed invention of the '134 Patent solves a long-felt need, specifically the need to improve read/write rates and efficiency of DRAMs. (Ex-2004, ¶219.) Before the invention of the '134 Patent, DRAM and SDRAM suffered from a susceptibility to interruptions, necessitated by the need to refresh DRAM cells. (See, e.g., Ex-1001, 1:20-25; Ex-2006, 65:11-21; Ex-2003, 19 ("The dynamic nature of DRAM requires that the memory be refreshed periodically so as not to lose the contents of the memory cells."); Ex-2004, ¶219.) Even as the industry transitioned into greater use of SDRAM, and DDR SDRAM, the need to refresh remained. (Ex-2006, 65:22-66:8; Ex-2004, ¶219.)

P.O. Resp. (Paper 19) at 64; Pet. Reply (Paper 21) at 21

Demonstrative Exhibit 1016, 0036

No Nexus: Claims Encompass SRAM

’134 Patent



US006651134B1

(12) **United States Patent**
Phelan

(10) **Patent No.: US 6,651,134 B1**
(45) **Date of Patent: Nov. 18, 2003**

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(73) Assignee: **Cypress Semiconductor Corp.**, San Jose, CA (US)

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(21) Appl. No.: **09/504,344**

(22) Filed: **Feb. 14, 2000**

(51) **Int. Cl.**[7] **C06F 12/00**

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(58) **Field of Search** 711/104–105, 169, 711/167; 365/233, 238.5; 710/35

(56) **References Cited**

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5,729,504 A	*	3/1998	Cowles	365/236
5,805,928 A	*	9/1998	Lee	710/35
5,936,975 A	*	8/1999	Okamura	714/719
5,966,724 A	*	10/1999	Ryan	711/105
6,085,264 A	*	7/2000	McIntyre, Jr. et al.	710/35
6,289,138 B1	*	9/2001	Yip et al.	382/307

OTHER PUBLICATIONS

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* cited by examiner

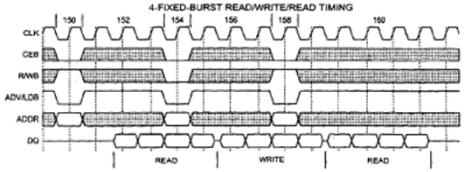
Primary Examiner—Donald Sparks
Assistant Examiner—Medhi Namazi
(74) *Attorney, Agent, or Firm*—Christopher P. Maiorana, P.C.; Robert M. Miller

(57) **ABSTRACT**

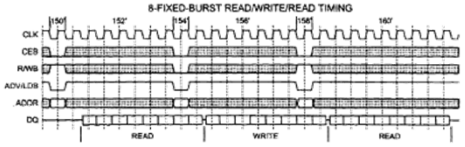
An integrated circuit comprising a memory and a logic circuit. The memory may comprise a plurality of storage elements each configured to read and write data in response to an internal address signal. The logic circuit may be configured to generate a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals. The generation of the predetermined number of internal address signals may be non-interruptible.

21 Claims, 3 Drawing Sheets

4-FIXED-BURST READ/WRITE/READ TIMING



8-FIXED-BURST READ/WRITE/READ TIMING



1. A circuit comprising:

a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal; and

a logic circuit configured to generate a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

8. The circuit according to claim 1, wherein said memory comprises a static random access memory.

‘134 Patent (Ex-1001) at claims 1, 8; Petition (Paper 1) at 33; Pet. Reply (Paper 21) at 13-14, 24

Demonstrative Exhibit 1016, 0037

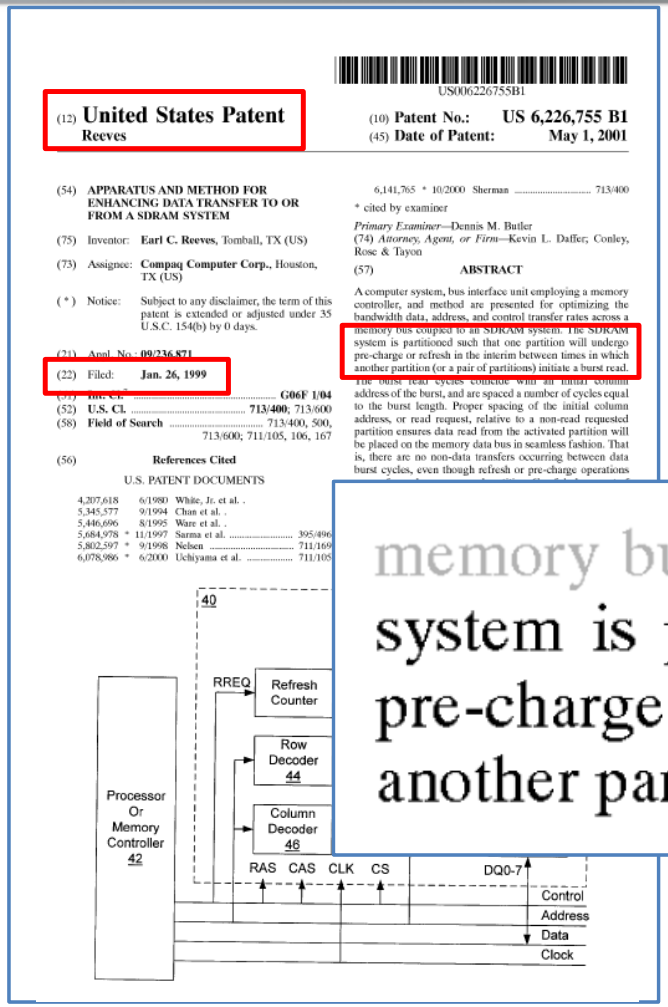
No Nexus: ’134 Patent Does Not Eliminate Refresh

Patent Owner’s expert admits no teaching in ’134 Patent:

> Q. So sitting here today, you are not aware of any teaching about how to eliminate the need to refresh DRAM?
>
> A. In the confines of the patent, I—I don’t recall if it says that from memory. I don’t remember. Maybe there’s a section you can point me to, but I don’t recall that.

Brogioli Dep. (Ex-1015) at 27:12-19; Pet. Rep. (Paper 21) at 14

Mitigation For DRAM Refresh Was Already Known



US006226755B1

(12) **United States Patent**
Reeves

(10) **Patent No.: US 6,226,755 B1**
(45) **Date of Patent: May 1, 2001**

(54) **APPARATUS AND METHOD FOR ENHANCING DATA TRANSFER TO OR FROM A SDRAM SYSTEM**

(75) Inventor: **Earl C. Reeves**, Tomball, TX (US)

(73) Assignee: **Compaq Computer Corp.**, Houston, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/236,871**

(22) Filed: **Jan. 26, 1999**

(51) Int. Cl. **G06F 1/04**
(52) **U.S. Cl.** **713/400**; 713/600
(58) **Field of Search** 713/400, 500, 713/600; 711/105, 106, 167

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,207,618 6/1980 White, Jr. et al. .
5,345,577 9/1994 Chan et al. .
5,446,696 8/1995 Ware et al. .
5,684,978 * 11/1997 Sarma et al. 395/496
5,802,597 * 9/1998 Nelsen 711/169
6,078,986 * 6/2000 Uchiyama et al. 711/105
6,141,765 * 10/2000 Sherman 713/400

* cited by examiner

Primary Examiner—Dennis M. Butler
(74) *Attorney, Agent, or Firm*—Kevin L. Daffer; Conley, Rose & Tayon

(57) **ABSTRACT**

A computer system, bus interface unit employing a memory controller, and method are presented for optimizing the bandwidth data, address, and control transfer rates across a memory bus coupled to an SDRAM system. The SDRAM system is partitioned such that one partition will undergo pre-charge or refresh in the interim between times in which another partition (or a pair of partitions) initiate a burst read. The burst read cycles coincide with an initial column address of the burst, and are spaced a number of cycles equal to the burst length. Proper spacing of the initial column address, or read request, relative to a non-read requested partition ensures data read from the activated partition will be placed on the memory data bus in seamless fashion. That is, there are no non-data transfers occurring between data burst cycles, even though refresh or pre-charge operations

(12) **United States Patent**
Reeves

(22) Filed: **Jan. 26, 1999**

memory bus coupled to an SDRAM system. The SDRAM system is partitioned such that one partition will undergo pre-charge or refresh in the interim between times in which another partition (or a pair of partitions) initiate a burst read.

Reeves (Ex-1008) at Abstract; Petition (Paper 1) at 60-65; Pet. Reply (Paper 21) at 14-15, 21

Demonstrative Exhibit 1016, 0039

Solved Problem Cannot Demonstrate Long Felt Need

> Nike's arguments and evidence on long-felt need focused solely on Nishida and its response to the problem in the art of making cutting waste less expensive, but ignored the teachings of other asserted prior art references. . . . 'any alleged, long-felt need was met by the teachings of at least Schuessler I, namely, knitting textile elements 'without requiring cutting'

Nike, Inc. v. Adidas AG, 955 F.3d 45, 55 (Fed. Cir. 2020)

Pet. Reply (Paper 21) at 21

Patent Owner's Sur-Reply

Patent Owner Argues in Sur-Reply:

issued.. But this solution does not address the '134 Patent's solution to the issue, which ***doesn't need to partition the DRAM in order to achieve non-interruptible bursts***. The '134 Patent meets a long felt need by providing uninterrupted bursts—which also addresses the refresh problem for DRAM—without requiring partitions.

P.O. Sur-Reply (Paper 22) at 16

Demonstrative Exhibit 1016, 0041

JEDEC Specification Timeline Does Not Show Long Felt Need

JESD79F

(Revision of JESD79E, May 2005)

FEBRUARY 2008

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

JEDEC

JDEC DDR at 1

BURST TERMINATE

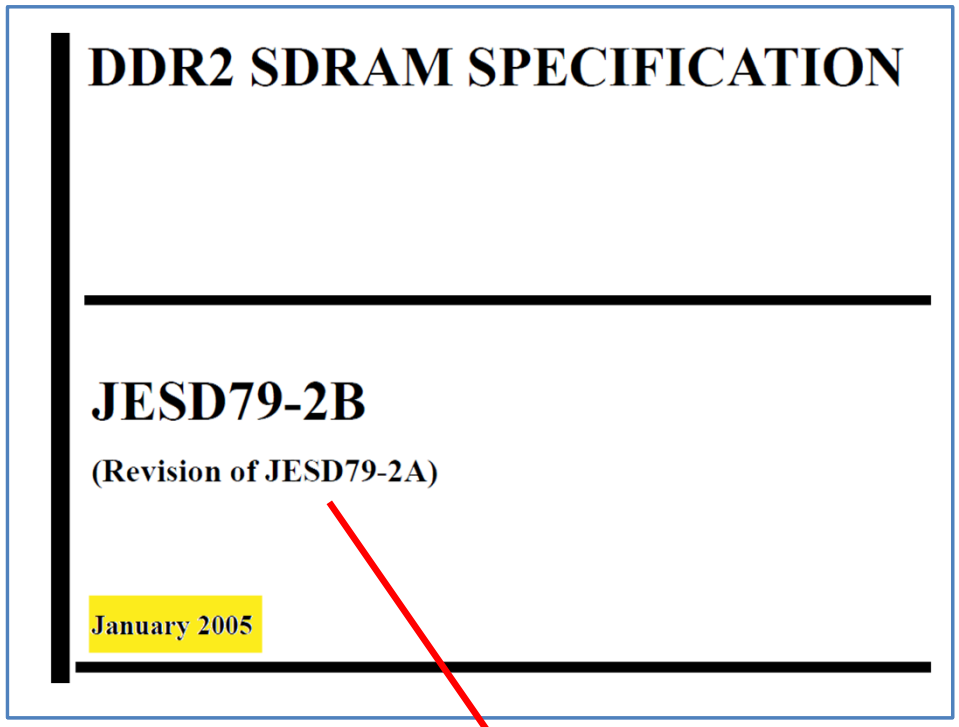
The BURST TERMINATE command is used to truncate read bursts (with autoprecharge disabled).

JDEC DDR at 23

JDEC DDR (Ex-2010) at 1, 23; Pet. Reply (Paper 21) at 22

Demonstrative Exhibit 1016, 0042

DDR2 Specification In 2004 and 2005 Still Specifies Interrupts



JDEC DDR2 at 1

JESD79-2A (January 2004)

JDEC DDR2 at 100

However, in case of BL=8 setting, two cases of interrupt by a new burst access are allowed, one reads interrupted by a read, the other writes interrupted by a write with 4 bit burst boundary respectively.

JDEC DDR 2 at 29-30

JDEC DDR2 (Ex-2011) at 1, 29-30, 100; Pet. Reply (Paper 21) at 22-23

Demonstrative Exhibit 1016, 0043

Back-up / Rebuttal Slides

Claim 16 Means Plus Function Structure Mapping

16[a]: means for reading data from and writing data to a plurality of storage elements in response to a plurality of internal address signals

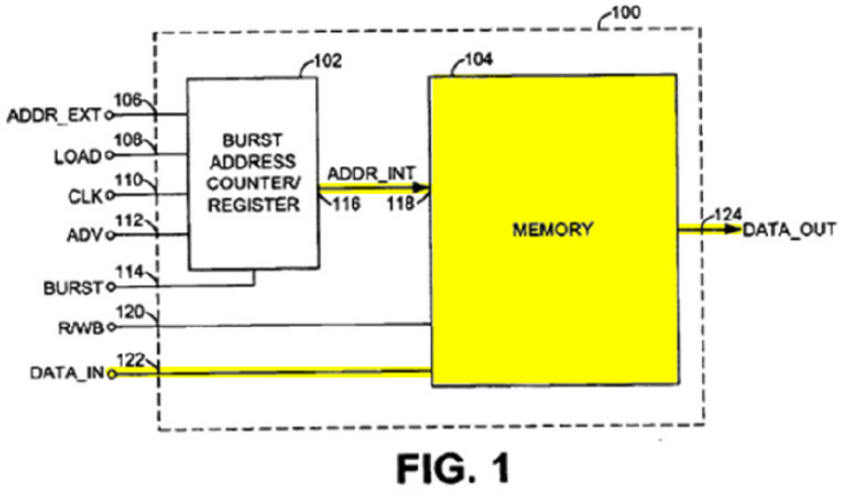
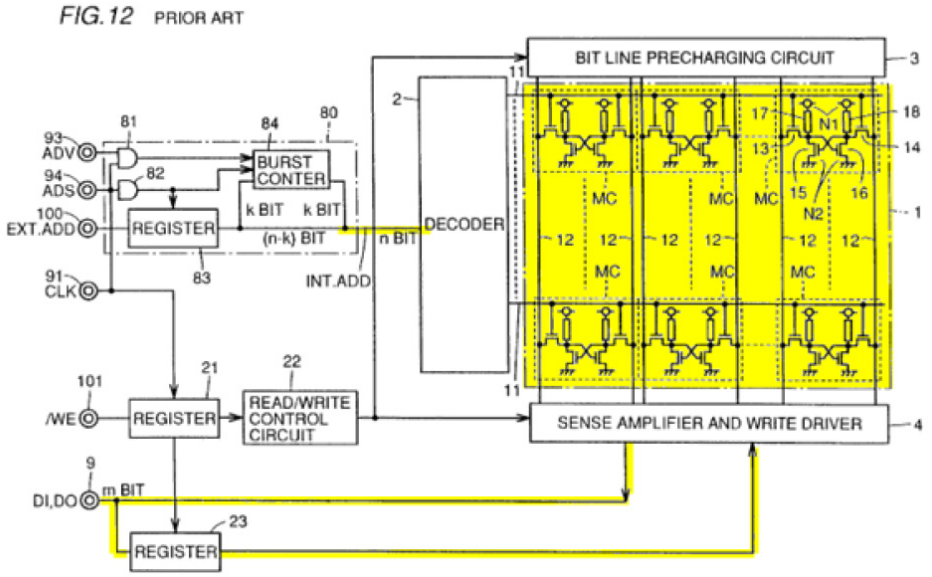


FIG. 1

'134 Patent, Fig. 1



Wada, Fig. 12

'134 Patent (Ex-1001) at Fig. 1 (annotated); Wada (Ex-1005) at Fig. 12 (annotated); Petition (Paper 1) at 40-41

Demonstrative Exhibit 1016, 0045

Claim 16 Means Plus Function Structure Mapping

16[b]: means for generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible

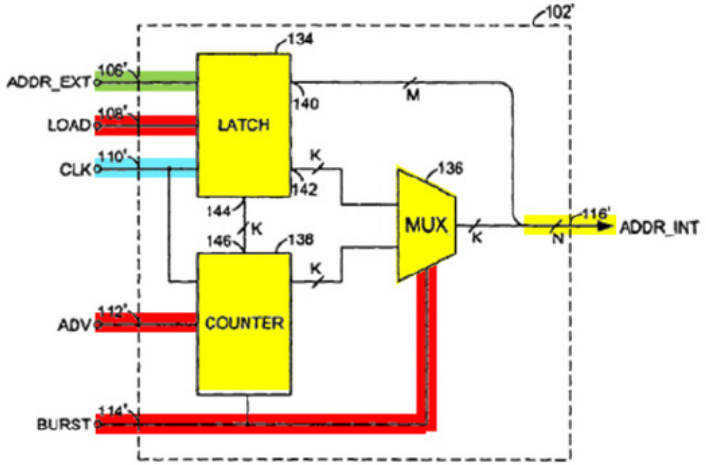
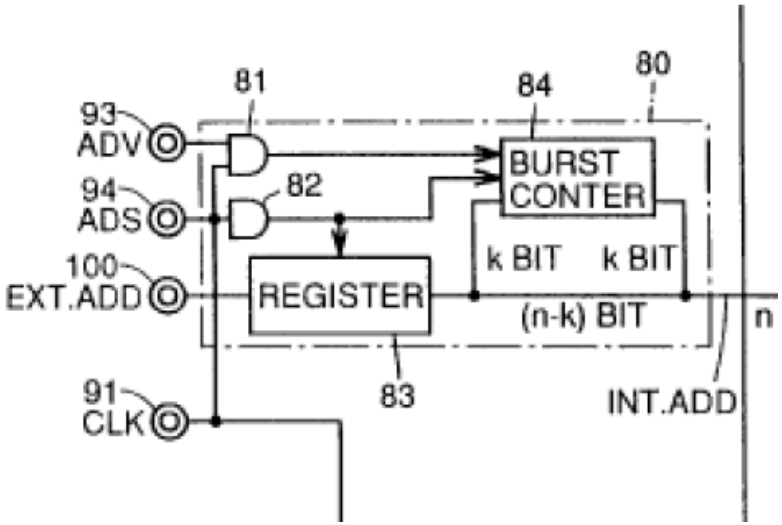


FIG. 3

'134 Patent, Fig. 3



Wada, Fig. 12

'134 Patent (Ex-1001) at Fig. 3 (annotated); Wada (Ex-1005) at Fig. 12 (excerpt); Petition (Paper 1) at 43-44

’134 Patent Solution Was Known In The Art

- Alleged problem of interrupted bursts did not exist for SRAM
- ’134 Patent’s references to refresh cycles apply ***only*** to DRAM, not SRAM

’134 Patent:

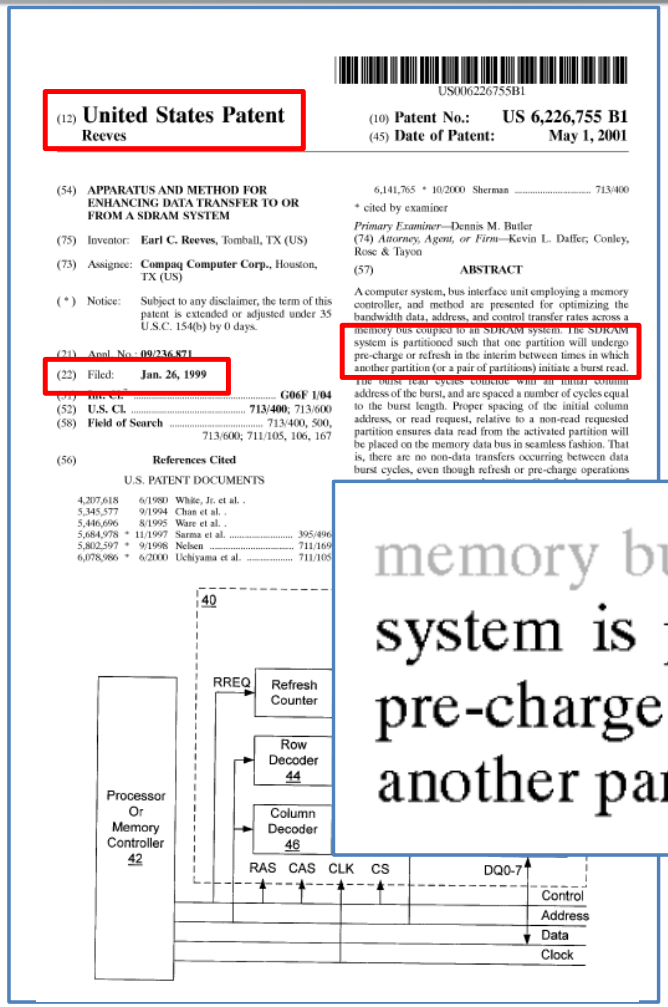
> refreshes. Using a DRAM in a burst application is difficult because of the need to refresh. Completely hiding refresh

- Yet ’134 Patent claims cover ***both*** SRAM and DRAM/SDRAM

Pet. Reply (Paper 21), 13-14

Demonstrative Exhibit 1016, 0047

’134 Patent Solution Was Known In The Art



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Reeves

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5,684,978 * 11/1997 Sarma et al. 395/496
5,802,597 * 9/1998 Nelsen 711/169
6,078,986 * 6/2000 Uchiyama et al. 711/105
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(12) **United States Patent**
Reeves

(22) Filed: **Jan. 26, 1999**

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Reeves (Ex-1008) at Abstract; Petition (Paper 1) at 60-65; Pet. Rep. (Paper 21) at 14-15, 21

Demonstrative Exhibit 1016, 0048

Patent Owner's Sur-Reply

Patent Owner Argues in Sur-Reply:

different advantages. AMD points to U.S. Patent No. 6,226,755 ("Reeves" ("Ex-1008")), which addresses the problem by ***partitioning, such that one partition is pre-charged while the other bursts***. But this solution is the same as the solution disclosed in U.S. Patent No. 5,729,504 to Cowles ("Ex-2001"), which was identified in the '134 Patent's prosecution history. Cowles's—and therefore Reeves's—proposed solution does not address the '134 Patent's solution to the issue, which ***does not need to partition the memory to achieve non-interruptible bursts.***

P.O. Sur-Reply (Paper 22) at 10

Demonstrative Exhibit 1016, 0049

’134 Patent Solution Was Known In The Art

File History, ’134 Patent

"To terminate a continuous burst read operation, the WE* signal merely has to transition high prior to a falling edge of the CAS* signal." (Col. 8, ll. 33-36 of Cowles; emphasis added.)

Therefore, even if we assume for the sake of argument that OE* does not affect the generation of internal addresses, there is still one condition under which the memories of Cowles will interrupt (or prematurely terminate) an access: WE* transitioning. Cowles rather explicitly teaches how such a premature termination can take place.

’134 File Hist. (Ex-1004) at 112; Pet. Prelim. Reply (Paper 10) at 1-2

’134 Patent Solution Was Known In The Art

Patent Owner incorrectly argues
“The ’134 Patent discloses a mechanism to achieve a non-interruptible burst.”

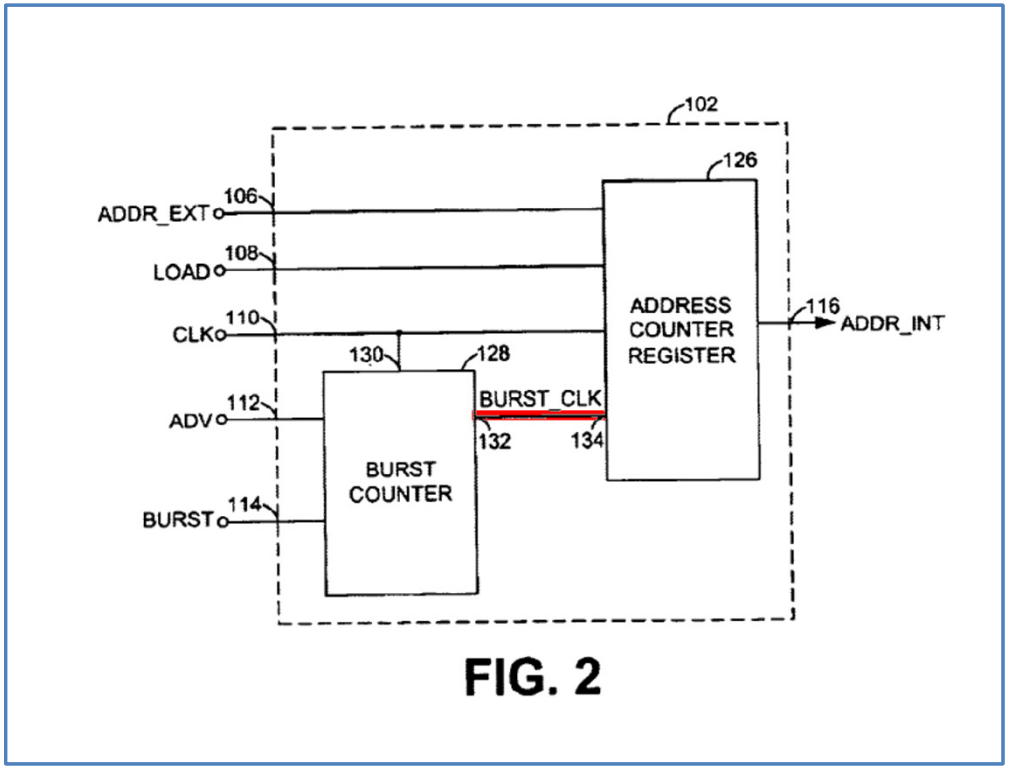

FIG. 2

PO Resp. (Paper 19) at 31; ’134 Patent (Ex-1001) at Fig. 2; Pet. Reply (Paper 21) at 15-16

Demonstrative Exhibit 1016, 0051

’134 Patent Solution Was Known In The Art

Patent Owner’s expert agrees

Q. Okay. And the patent doesn’t describe a particular circuit that will take in a number such as four and generate four pulses in any detail; is that correct?

A. Yeah, I don’t recall that the patent sort of talks about pulse circuit design. That’s something that, you know, the reader would understand and, you know, depending on the use case probably, you know, there’d be different design tradeoffs. But I don’t recall—maybe you can point me to a section if it does, but going from memory, I don’t recall it talking about pulse circuit design. That’s just something a person of skill would understand.

Brogioli Dep. (Ex-1015) at 153:24-154:17; Pet. Reply (Paper 21) at 15-16