Michael C. Brogioli, Ph.D.

Contact Information

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Expertise

Software Analysis, Software Architecture, Embedded Computing, Microprocessor Designs, Software Based Simulation, Computer Hardware Design, Computer Networks, Computer and Network Based Gaming Platforms, High Performance Computing, Digital Signal Processing.

Education

Rice University, Houston, Texas USA

Ph.D., Electrical and Computer Engineering, 2007

- Dissertation Topic: "Reconfigurable Heterogeneous DSP/FPGA Based Embedded Architectures for Numerically Intensive Embedded Computing Workloads."
- Advising Committee: Dr. Joseph R. Cavallaro, Dr. Keith D. Cooper, Dr. Scott Rixner

Rice University, Houston, Texas USA

M.S., Electrical and Computer Engineering, 2003

- Dissertation Topic: "Dynamically Reconfigurable Data Caches in Low Power Computing."
- Advising Committee: Dr. Keith D. Cooper, Dr. Scott Rixner, Dr. Robert Jump

Rensselaer Polytechnic Institute, Troy, New York USA

B.S., Electrical Engineering, Cum Laude - 1999

- Advisor: Dr. William Pearlman

Professional Experience

Polymathic Consulting, TX USA
Managing Director **2011 - Present**
Founder and managing director of Polymathic Consulting, servicing clients ranging from early stage technology start-up endeavors to Fortune 100 and beyond. Clients turn to Polymathic for expansive, proven engineering, research and development, intellectual property and technical leadership to effectively advance their real world business needs.

IEEE and ACM Design Automation Conference, USA
Steering Committee
Conference Chair, Embedded Systems and Software Track **2016 - Present**
Design Automation Conference is the premiere technical conference and trade show specializing in Hardware, Software, Internet of Things, Embedded Systems and related Design Methodologies. Conference chair, responsible for the review, critique, and acceptance of academia and industry based publications in the areas of embedded systems, embedded software, and embedded system design.

Rice University, TX USA
Adjunct Professor, Electrical and Computer Engineering **2009 - Present**
Professor of Ph.D. candidate level courses in wireless telecommunications, embedded computing software, embedded computing hardware, and software/hardware optimization in modern computing systems utilizing modern high level programming languages. Advisor of senior and graduate student based projects revolving around multi-core heterogeneous systems as they pertain to wireless telecommunications, medical and video.

RISC-V Foundation, Berkeley, CA USA

Technical Committee **2018 - Present**

RISC-V is an open CPU instruction set architecture (ISA) based on established reduced instruction set computing (RISC) principles. The RISC-V Foundation is a non-profit consortium chartered to standardize, protect, and promote the free and open RISC-V instruction set architecture together with its hardware and software ecosystem for use in all computing devices.

Freescale Semiconductor, TX USA

Chief Architect, Senior Member Technical Staff **2009 - 2011**

Technical architect of Freescale's DSP compilers and related technology. Responsible for management of technology, engineering roadmaps, design lead on compiler infrastructure and optimizations (high level and low level), next generation ABI definitions and next generation architecture solutions. Technical lead on multi-year engagement with processor architects in design of next generation DSP cores. Developed software infrastructure for migrating OEM competitor software stacks to Freescale solutions, tools generation, software packages, migration strategies and white papers. Technical lead on Tier-1 OEM customer relationships, evaluations of 3rd party technologies for potential partnerships and acquisitions, led various university research collaborations on behalf of Freescale. Development and deployment of internal software engineering policies and practices.

Freescale Semiconductor, TX USA

Senior Compiler Engineer V

High Performance Compiler Design, Processor Architecture **2008 - 2009**

Team leader on compiler engineering effort to provide intuitive, interactive end user experience for DSP compiler tool suite. Designed a framework to guide users in achieving highly optimized compiled VLIW code. Assembly listing reports for optimization failure advice, porting advice when migrating from competitor architectures, advice on code modifications for optimization enablement. Lead designer, engineering effort director, project planning and scoping, release schedule, and drafting of specification. Development of various compiler optimizations for VLIW processing as well as software emulation layers for running competitor software solutions on Freescale silicon.

Advising of next-gen DSP core architecture team in creating a highly orthogonal, compiler targetable multi-clustered VLIW based digital signal processor architecture. Work with future basestation architecture teams on designing next-gen basestation architecture for 4G LTE incorporating control and data plane processing with appropriate programming models.

Method Seven, MA USA

Technical Co-Founder

High Performance Software and Hardware Systems Architecture **2006 - 2007**

Founded Method Seven, a financial engineering company applying biologically inspired machine learning to financial market analysis. Principal software systems architect and hardware systems architect for both research and deployment platforms. Led research and development of platform for scans and overlays covering the NASDAQ, NYSE, and AMEX markets using proprietary technologies.

Texas Instruments, TX USA

Advanced Architecture and Chip Technologies

Microprocessor and Systems Architecture **2005**

System modelling and architectural exploration of Davinci^{TM}system-on-chip (SOC) architecture designed for embedded video processing. SystemC based simulation models of on–chip crossbars, bus arbitration and bridge technology, as well as on–chip and off–chip memory controllers within application specific heterogeneous SOC architectures.

Fulbright and Jaworski LLP, TX USA

Scientific Advisor, Intellectual Property

Electrical, Computer Engineering and Computer Science **2005 - 2007**

Intellectual property consultant and technology advisor on litigation and prosecution work including, but not limited to: CDMA2000 3G wireless standards, wireless communications systems, embedded computing, and large scale modular software systems. Reverse engineering of source code varying from VHDL to high level object oriented applications, as well at patent prosecution and litigation work.

Intel Corporation, CA USA
Microprocessor Research Labs
Compiler Engineering **2000**
Implemented speculative multi–threading support in Intel's IA–64 compiler. Developed new program analysis and back end code generation phases to support speculatively launching threads at runtime. Analyzed the performance potentials of SPEC95 benchmarks with respect to speculatively multi–threaded execution.

Rice University, TX USA
Computer Architecture and Circuit Design (Instructor) **2000 - 2003**
Graduate instructor of graduate and undergraduate curriculim in the areas of Electrical and Computer Engineering, specifically relating to Computer Architecture and Circuit Design. Advised student projects, instructed classes and led laboratory work.

Vicarious Visions, NY USA
Lead Software Engineer **1999**
Principal engineer on Activision's "AMF Extreme Bowling" for Nintendo's Color Gameboy gaming console. Developed PC based audio and graphics development tools suite for use with Color Gameboy game production. Coded innovative, highly optimized assembly routines for real time speech and full motion video on the console's limited Zilog Z80 processor resources.

Stratus Computer, MA USA
Hardware Engineering **1997 - 1998**
Debugged locked step CPU operation and memory management issues in Stratus' fault tolerant UNIX release 3.4. Qualified Hewlett Packard PA–8000 series CPU modules under Stratus' proprietary OS release, VOS 14.0, during alpha and beta test phases. Wrote C code and UNIX shell scripts for recreating documented system failures, and to automate remote kernel updates and OS installs as well as data logging.

Rensselaer Polytechnic Institute, NY USA
Digital Microelectronics Design (Instructor) **1997 - 1998**
Undergraduate instructor of undergraduate courses in digital microelectronics and circuit design. Instructed weekly lessons, computer design labs, graded exams and problem sets.

Rensselaer Electric Motor Sports, NY USA
Hardware and Software Engineering **1995 - 1997**
This project was funded by, and led by, General Motors Corporation and Honda of America. Hardware and software co-design of embedded operating system and hardware platform for electrical vehicle prototypes, running on 16-bit Motorola 68K dual processor platform. Designed power engineering test platform for dynamometers, including hardware and user interface software.

Books and Contributed Chapters

Brogioli, Michael C., and Kraeling, Mark B., *Internet of Things - A Synopsis of the Internet of Things, its History, Application, Technology, Architecture, and Challenges Moving Forward*, Software Engineering for Embedded Systems - Methods, Practical Techniques and Applications, 2nd Edition, Elsevier Publishing, 2019.

Brogioli, Michael C., *Software and Compiler Optimization for Microcontrollers, Embedded Processors and DSPs*, Software Engineering for Embedded Systems - Methods, Practical Techniques and

Applications, 2nd Edition, Elsevier Publishing, 2019.

Brogioli, Michael C., *Embedded and Multicore System Architecture - Design and Optimization*, Software Engineering for Embedded Systems - Methods, Practical Techniques and Applications, 2nd Edition, Elsevier Publishing, 2019.

Leotescu, Florin, and Cristian, Marius and Brogioli, Michael C., *Performance Analysis using NXP's i.MX RT1050 Crossover Processor and the Zephyr Real-Time Operating System*, Software Engineering for Embedded Systems - Methods, Practical Techniques and Applications, 2nd Edition, Elsevier Publishing, 2019.

Wu, Michael and Sun, Yang and Wang, Guohui and Brogioli, Michael C. and Cavallaro, J. R., *Implementation of a High Throughput 3GPP Turbo Decoder on GPU Architectures*, Software Development for Networking Applications – Expert Guides Series, Elsevier Publishing, Atlanta, GA, 2018.

Brogioli, M. C., *On The C++ Programming Language for Embedded Software, Systems, and Platforms*, Software Engineering for Embedded Systems – Expert Guides Series, Elsevier Publishing, Atlanta, GA, 2013.

Brogioli, M. C., *Software Optimizations for Memory Performance in Embedded Systems*, Software Engineering for Embedded Systems – Expert Guides Series, Elsevier Publishing, Atlanta, GA, 2013.

Invited Co-Author, *Signal Processing Systems Handbook, Second Edition*, Springer Publishing Company, 11 West 42nd Street, New York, NY, 2012.

Brogioli, M. C., *Software Programmable DSP Architectures*, Expert Guide DSP for Embedded and Real-Time Systems, pp. 63-75, Elsevier Publishing, Atlanta, GA, 2012.

Brogioli, M. C., *The DSP Hardware / Software Continuum*, Expert Guide DSP for Embedded and Real-Time Systems,, pp. 103-113, Elsevier Publishing, Atlanta, GA, 2012.

Brogioli, M. C., *DSP Optimization - Memory Optimization*, Expert Guide DSP for Embedded and Real-Time Systems, pp. 217-241, Elsevier Publishing, Atlanta, GA, 2012.

Brogioli, M. C. and Dew, Stephen, *Optimizing DSP Software - High level Languages and Programming Models*, Expert Guide DSP for Embedded and Real-Time Systems,, pp. 167-179, Elsevier Publishing, Atlanta, GA, 2012.

Sun, Yang, Amiri, Kiarash, Brogioli, Michael, Wang, Guohui, and Cavallaro, Joseph R., *DSP Hardware Accelerator Architectures for Communication Applications*, Springer Publishing, New York, NY, Spring 2012.

Sun, Yang, and Amiri, Kiarash, and Brogioli, Michael C., and Cavallaro, Joseph, *Application-Specific Accelerators for Communications*, Springer Publishing Company, 11 West 42nd Street, New York, NY, 2010.

Invited Co-Author, *Signal Processing Systems Handbook, First Edition*, Springer Publishing Company, 11 West 42nd Street, New York, NY, 2010.

Publications and Invited Papers

Brogioli, Michael, C., and Games, William, and Moats, Richard, *Current and Future Challenges in Internet of Things (IoT) Development Silos (Part I)*, Embedded Computing Design Magazine, USA, 2020.

Brogioli, Michael, C., and Games, William, and Moats, Richard, *On Solving the IoT Development Silo Problem* IEEE Real-Time and Embedded Technology and Applications Symposium, Tools and Demos Session, Montreal, Canada, 2019.

Moats, Richard, and Games, Bill, and Brogioli, M. C., *Arch - A New Language For The Next Wave of Network-Connected Embedded Development*, Design Automation Conference, Austin, Texas, 2017.

Moats, Richard, and Games, Bill, and Brogioli, M. C., *Network Native - The Next Wave of Connected Embedded Development*, Network Native Inc., Austin, Texas, 2017.

Invited Paper, Arokia I, Brogioli, Michael, Jain, Nitjin and Garg, Umang, *LTE Layer 1 Software Design on Heterogeneous Multicore DSP Platforms*, IEEE 45th Asilomar Conference on Signals, Systems and Computers, Pacific Grove, CA, 2011.

Kyriakopoulous, Konstantinos, Brogioli, Michael C., and Zhang, Ruihao, *Improving Software Systems Quality through Well Defined Development Methodologies*, 2011 Test Methodology and Efficiency Symposium, Freescale Semiconductor, Austin, TX, USA, 2011.

Brogioli, Michael C., and Cavallaro, J.R., *Compiler Driven Architecture Design Space Exploration for Embedded DSP Workloads: A Study in Software Programmability Versus Hardware Acceleration*, IEEE 43rd Asilomar Conference on Signals, Systems and Computers, Pacific Grove, CA, 2009.

Brogioli, Michael C., and Zhang, Ruihao, *Compiler Feedback: Guiding Performance of Compiled C Code*, Freescale Semiconductor White Paper, Austin, TX, 2009.

Brogioli, M.C., and Cavallaro, J., *RISD: A Retargetable Compiler Infrastructure for Scalable Multi-Clustered VLIW DSP Architectures*, IEEE 5th Dallas Circuits and Systems Workshop, Dallas, TX, 2007.

Brogioli, Michael C., Radosavljevic, P., and Cavallaro, J., *A General Hardware/Software Codesign Methodology for Embedded Signal Processing and Multimedia Workloads*, IEEE 40th Asilomar Conference on Signals, Systems, and Computers, Pacific Grove, CA, 2006.

Brogioli, Michael C., Radosavljevic, P., and Cavallaro, J., *Hardware/Software Co-design Methodology for DSP/FPGA Partitioning: A Case Study for Meeting Real-Time Processing Deadlines in 3.5G Mobile Receivers*, 49th IEEE International Midwest Symposium on Circuits and Systems, San Juan, Puerto Rico, 2006.

Brogioli, Michael C., Willmann, P.D., and Rixner, S., *Parallelization Strategies for Network Interface Firmware*, IEEE/ACM 4th Annual Workshop on Optimizations for DSP and Embedded Systems (In Conjunction with IEEE/ACM International Symposium on Code Generation and Optimization), Manhattan, NY, 2006.

Brogioli, Michael C., Gadhiok, M., and Cavallaro, J., *Design and Analysis of Heterogeneous DSP/FPGA Based Architectures for 3GPP Wireless Systems*, IEEE Real-Time and Embedded Technology and Applications Symposium Work-in-Progress Sessions, San Jose, CA, 2006.

Brogioli, Michael C., and Cavallaro, J., *Modelling Heterogeneous DSP-FPGA Based System Partitioning with Extensions to the Spinach Simulation Environment*, IEEE 39th Asilomar Conference on Signals, Systems, and Computers, Pacific Grove, CA, 2005.

Joseph R. Cavallaro, Michael C. Brogioli, Alexandre de Baynast, and Predrag, Radosavljevic, *Reconfigurable Architectures for Wireless Systems: Design Exploration and Integration Challenges*, Wireless World Research Forum, Toronto, CA, 2004.

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