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**Kato**

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- (54) **DIGITAL PLL DEVICE**
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- (\* ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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**H03L 7/06** (2006.01)
- (52) **U.S. Cl.** ..... **327/159; 327/150**
- (58) **Field of Classification Search** ..... None  
See application file for complete search history.

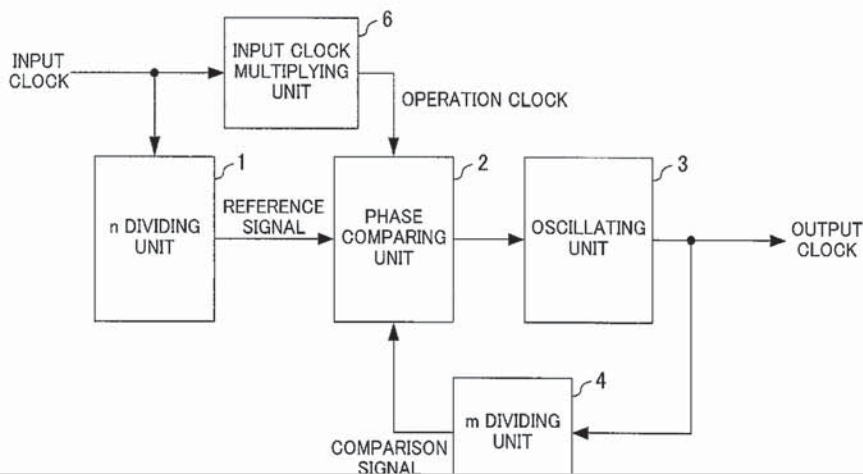
*Primary Examiner* — Cassandra Cox  
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(57) **ABSTRACT**

An input clock dividing unit frequency-divides an input clock, and an input clock multiplying unit frequency-multiplies the input clock. An operation clock selecting unit selects the frequency-divided clock when the input clock is fast and selects the frequency-multiplied clock when the input clock is slow, based on the frequency detection result of frequency detecting unit. The operation clock selecting unit then outputs the selected clock to a phase comparing unit as an operation clock. The phase comparing unit operates according to the frequency-divided or frequency-multiplied clock, and controls an oscillating unit so that the phase difference between a reference signal and a comparison signal becomes zero. The phase of an output clock is thus caused to track the phase of the reference signal.

**11 Claims, 7 Drawing Sheets**



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FIG. 1

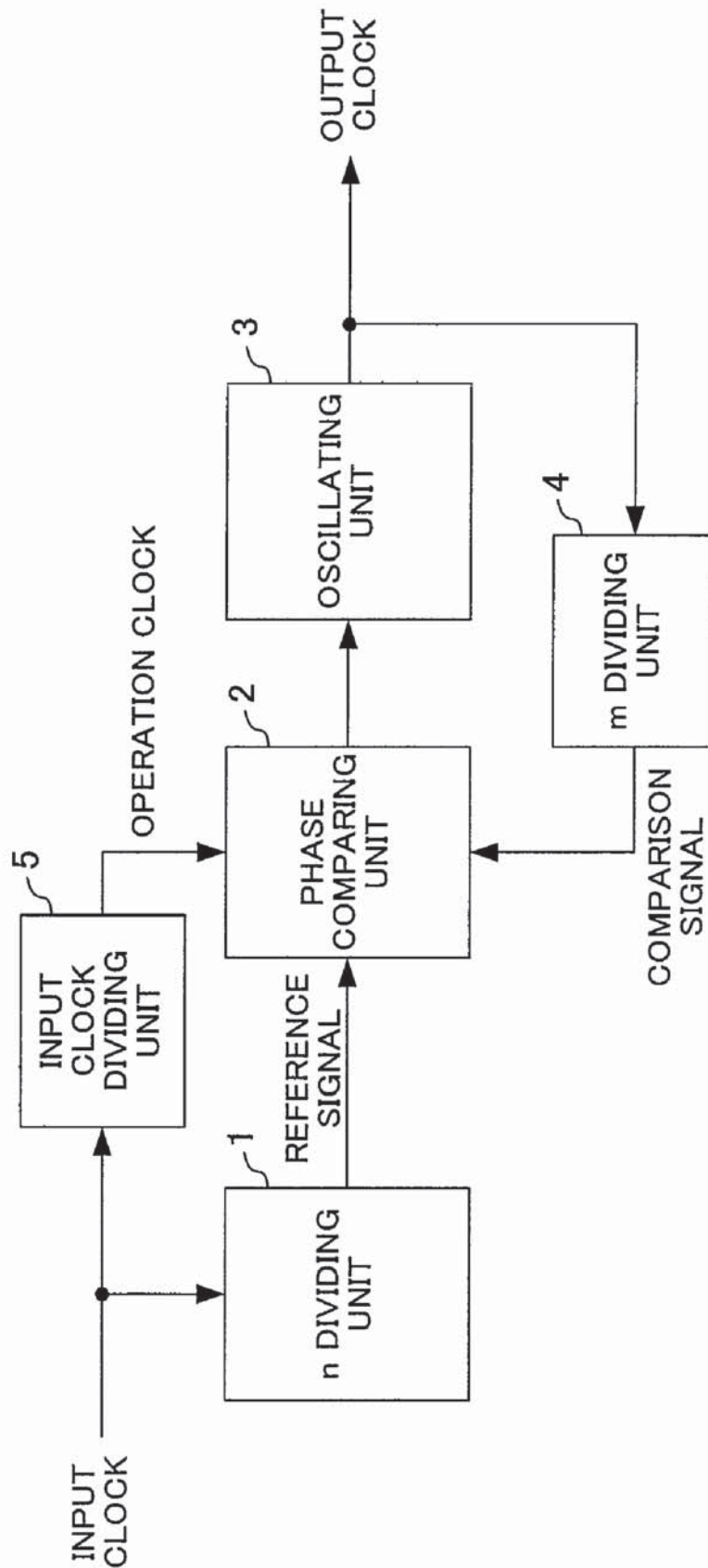
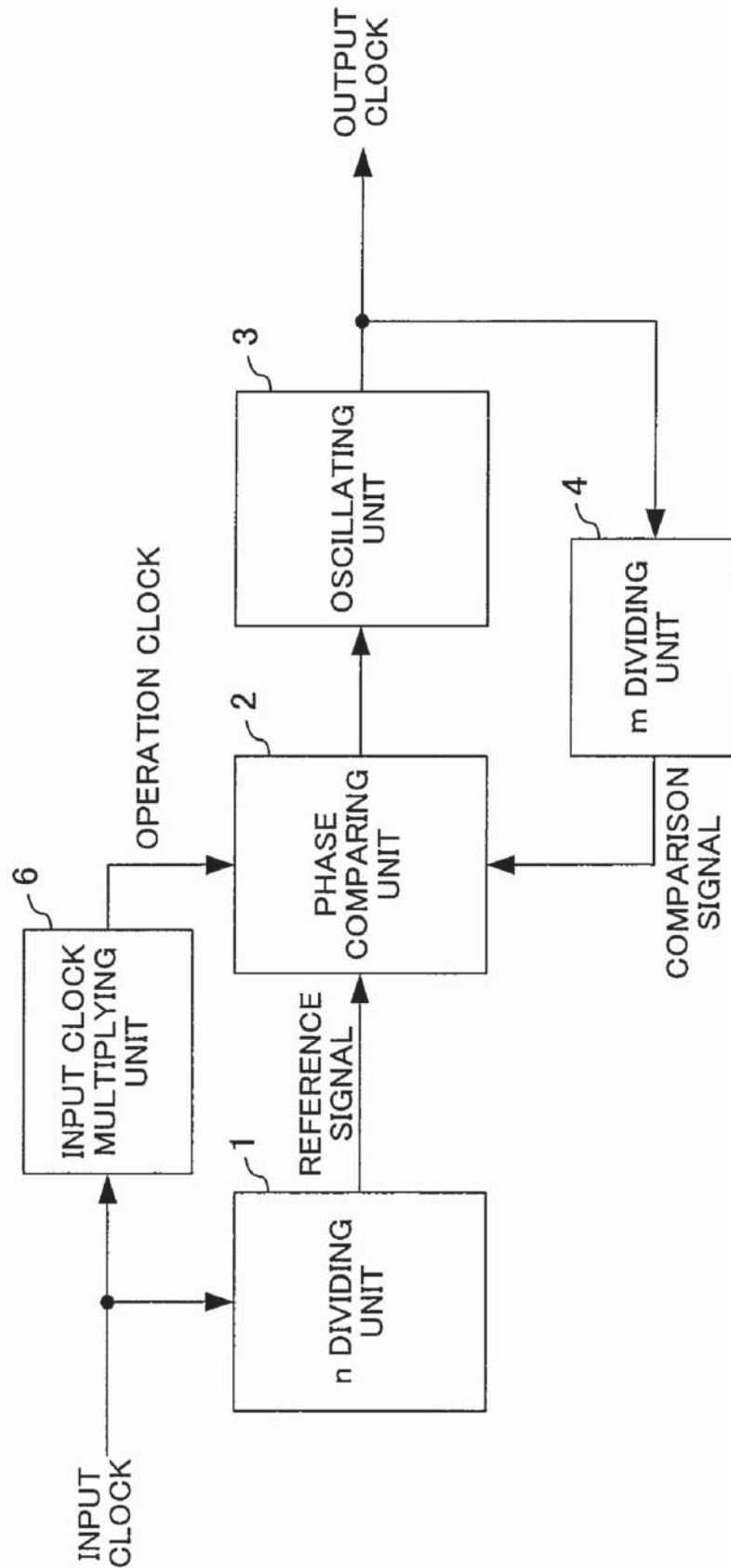


FIG. 2



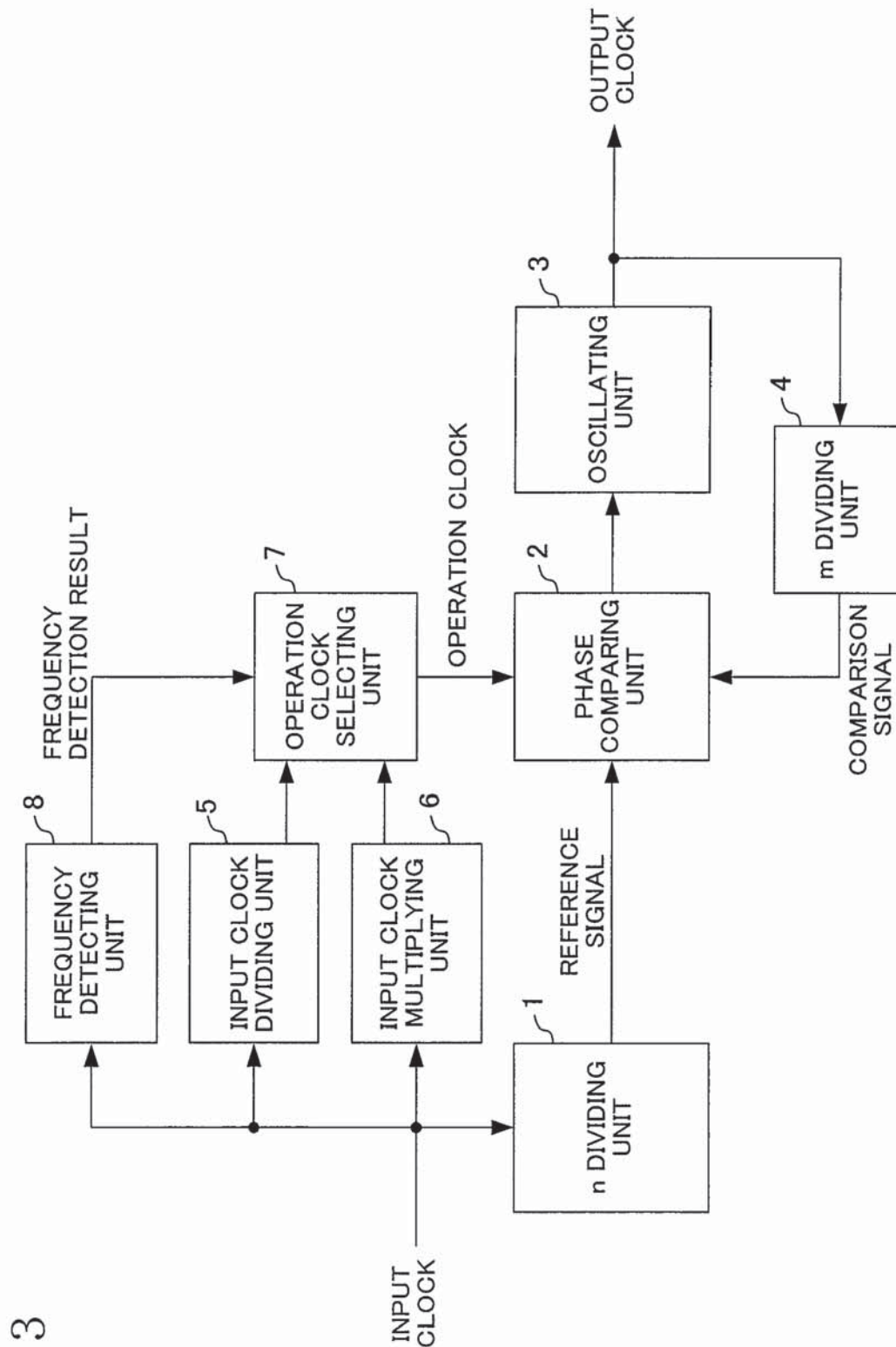


FIG. 3

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