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Balmer

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[54] **SLICED ADDRESSING MULTI-PROCESSOR AND METHOD OF OPERATION**

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[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

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[51] Int. Cl.⁵ **G06F 12/00; G06F 15/00; G06F 7/33; G06F 7/50**

[52] U.S. Cl. **395/400; 395/300; 364/749; 364/786; 364/787**

[58] Field of Search **395/400, 800, 163, 166; 364/749, 786, 787**

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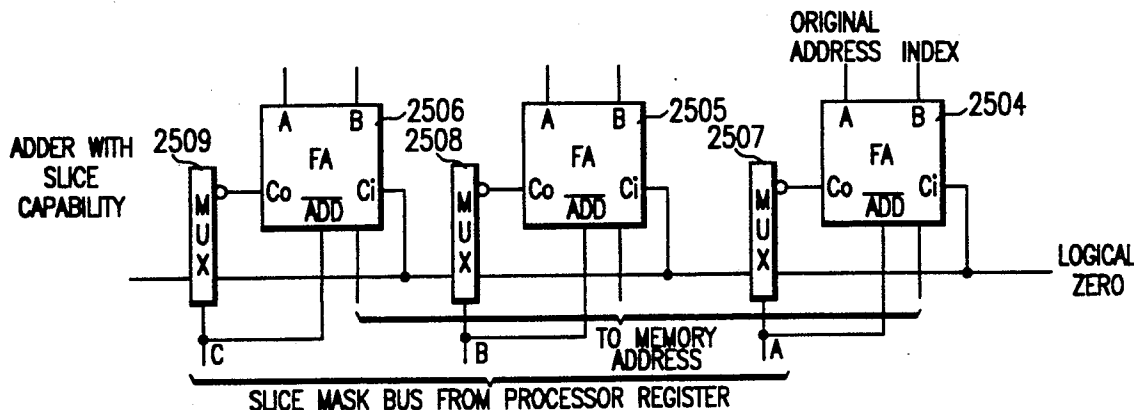
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[57] **ABSTRACT**

A multi-processor system arranged, in one embodiment, as an image and graphics processor. The processor is structured with several individual processors all having communication links to several memories. An addressing scheme, called sliced addressing, is used to spread contiguous related data over several memories so that the data can be concurrently accessed by several processors. A crossbar switch serves to establish the processor memory links. The entire image processor, including the individual processors, the crossbar switch and the memories, is contained on a single silicon chip.

13 Claims, 35 Drawing Sheets



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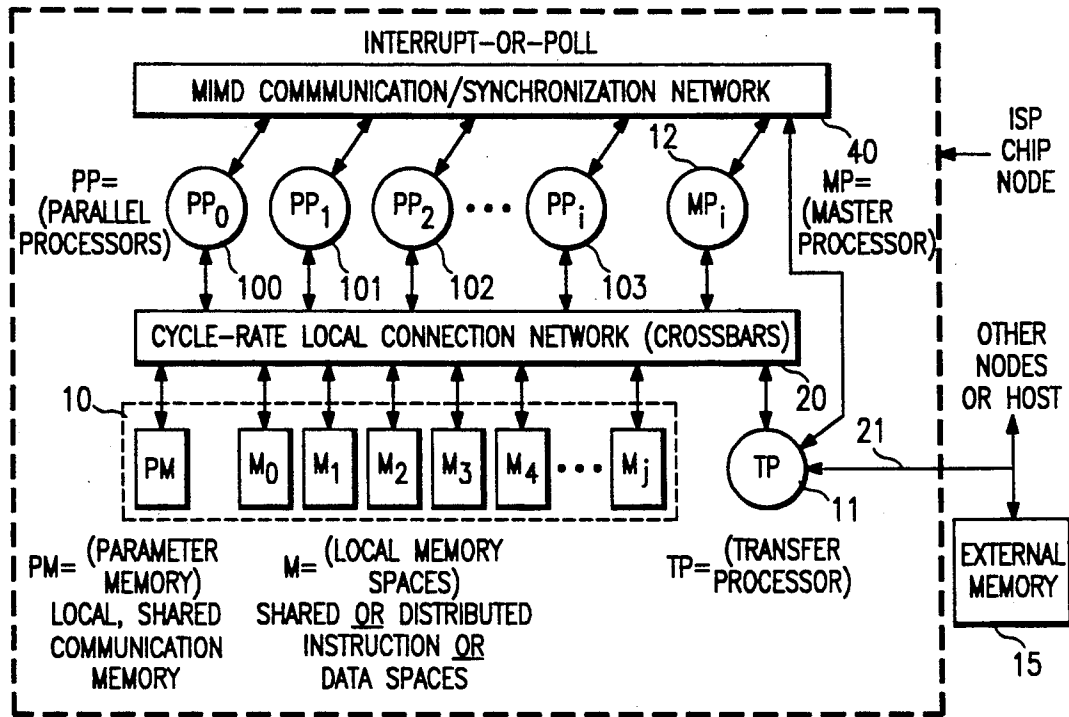


FIG. 1

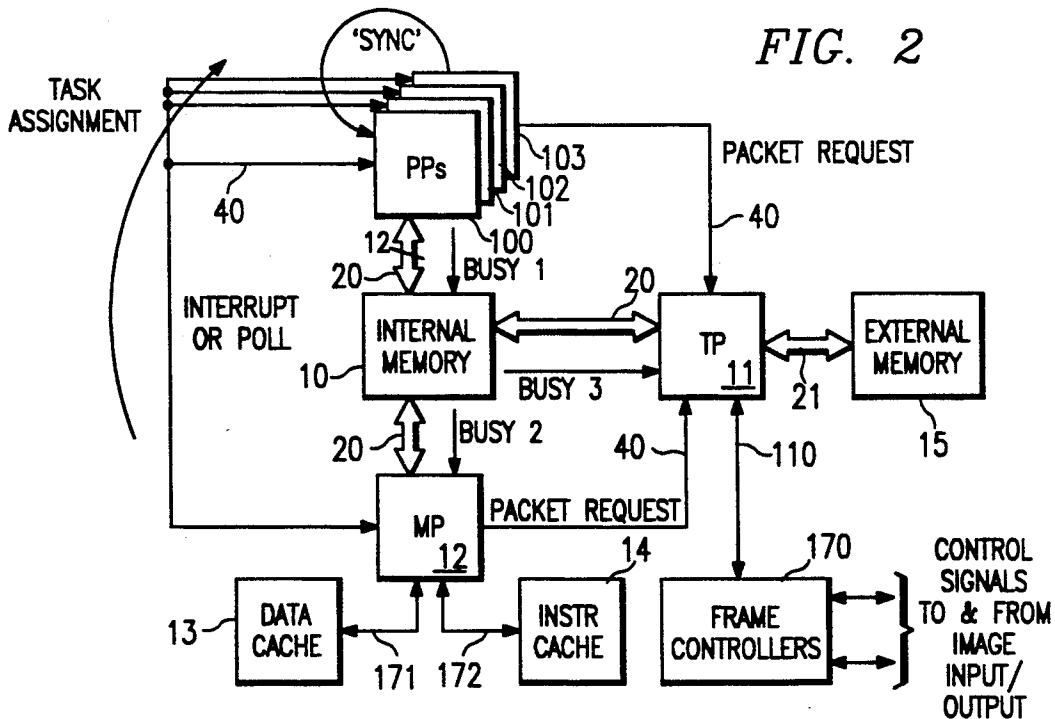
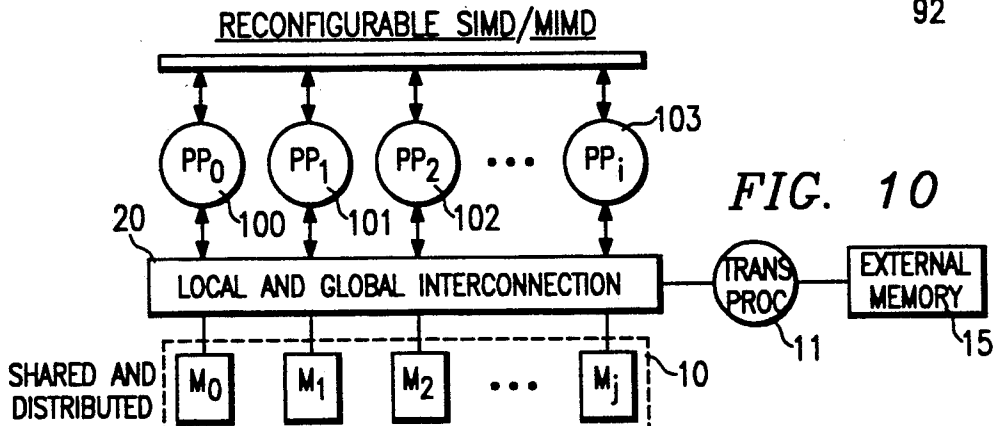
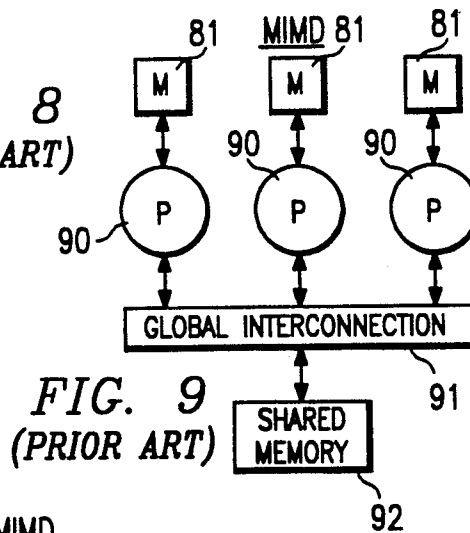
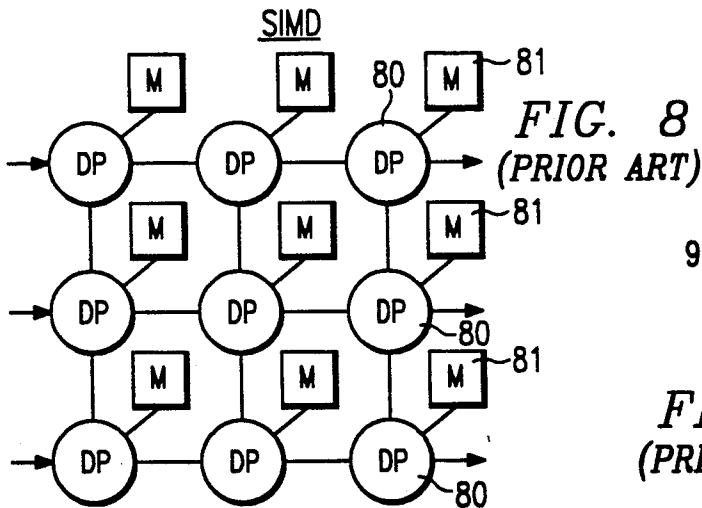
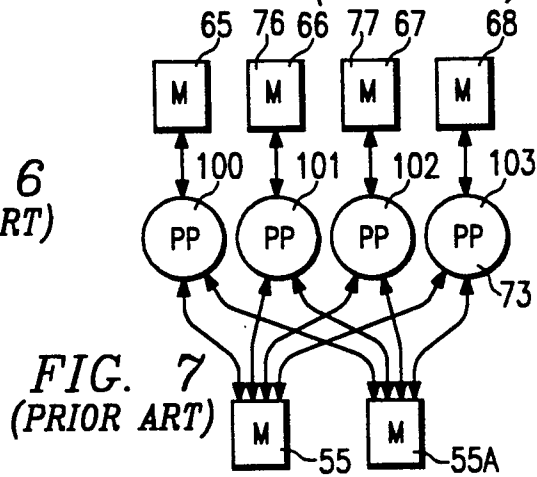
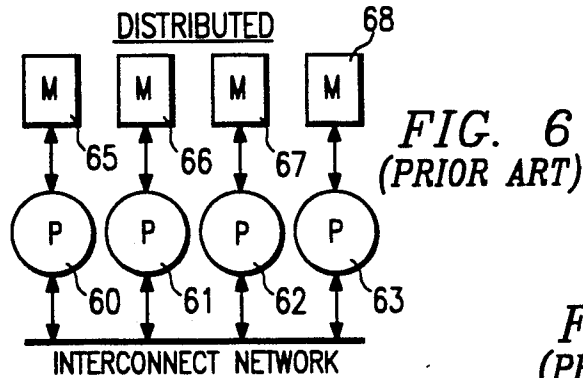
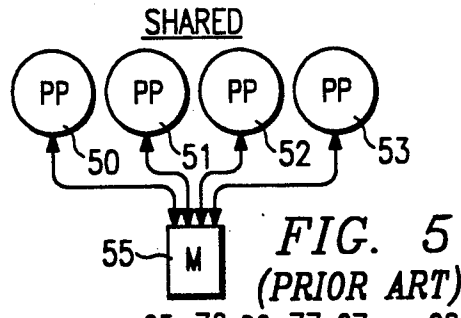
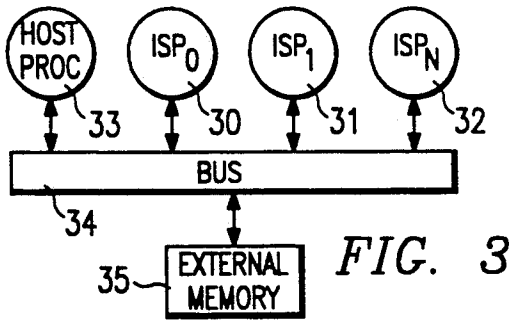
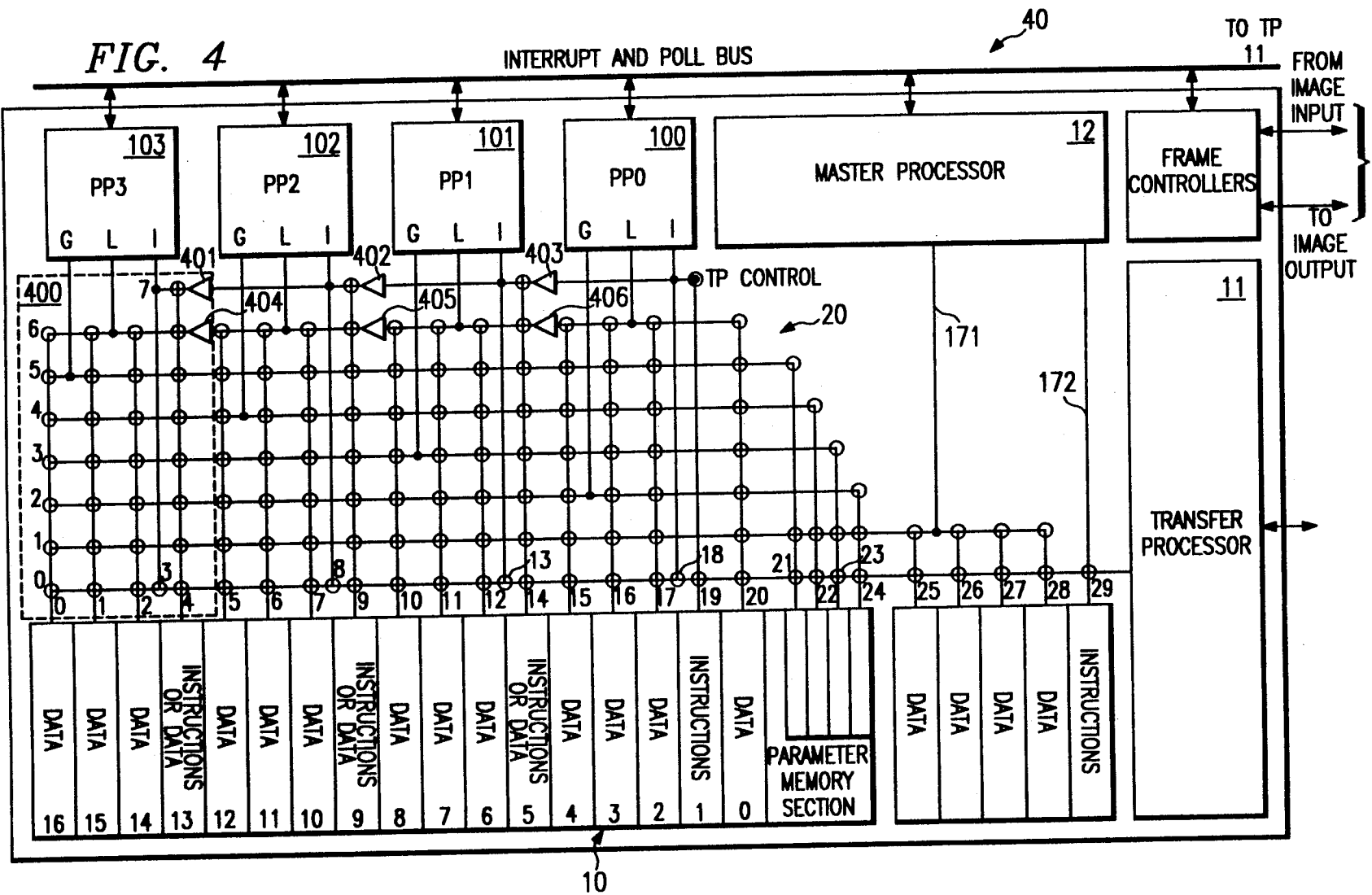


FIG. 2





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