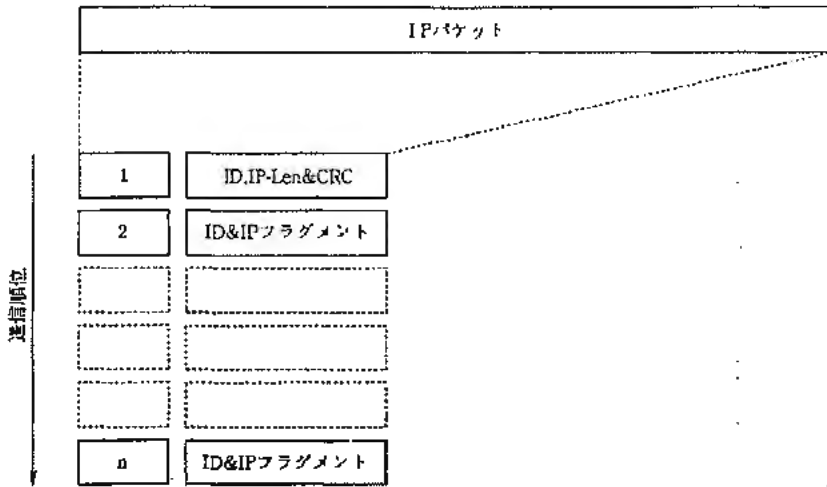
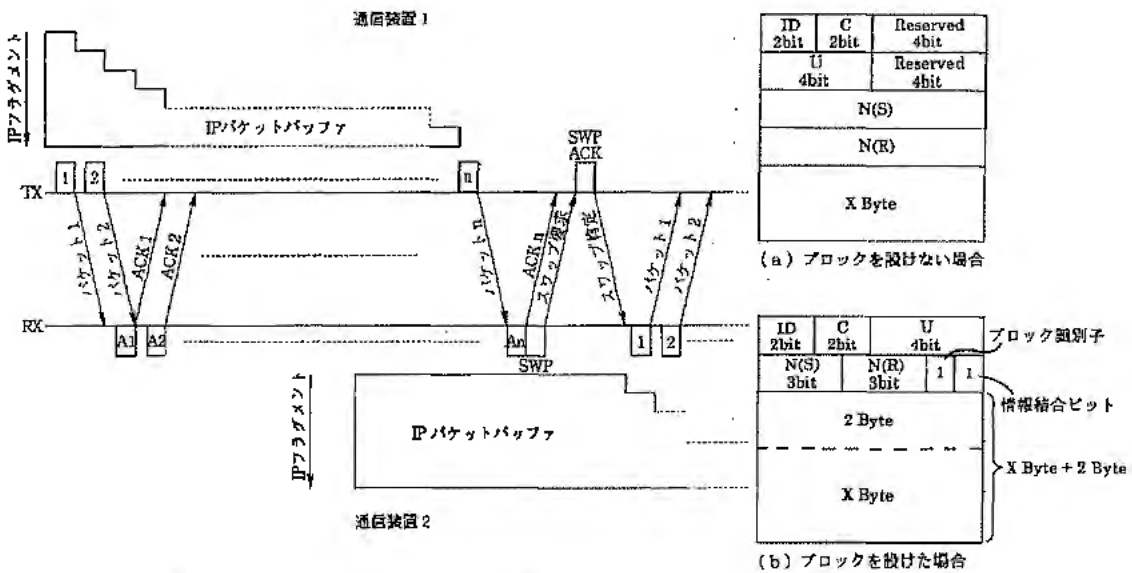


【図2】



【図3】

【図12】

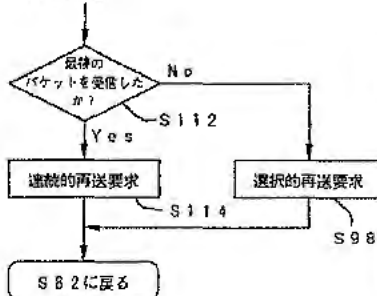


【図10】

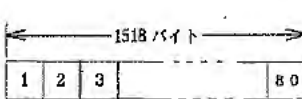
【図13】

【図21】

ステップS84: Yes

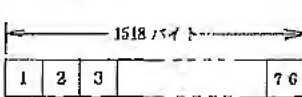


1518バイト ÷ 19バイト = 79.89



a) ブロックを設けない場合

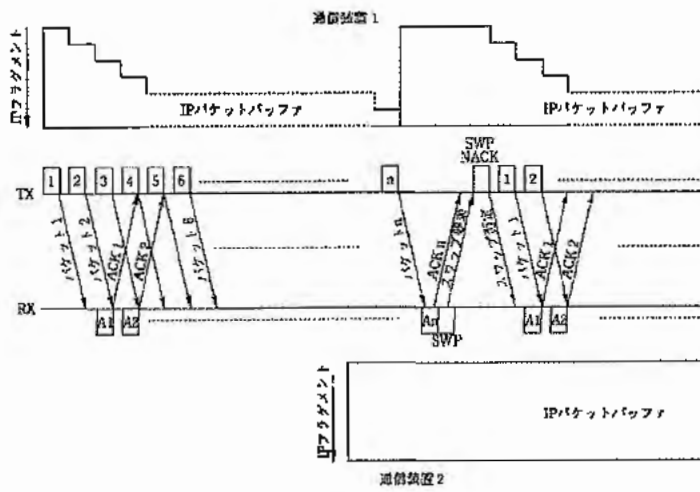
1518バイト ÷ 20バイト = 75.9



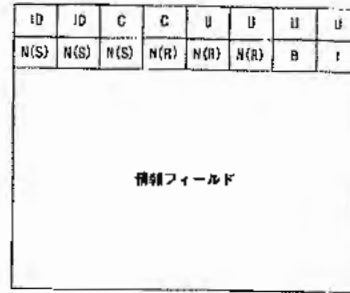
b) ブロックを設けた場合

ID	RD	C	C	0	0	0	0
U	U	U	U	0	0	0	0
N(S)	N(S)	N(S)	N(S)	N(S)	N(S)	N(S)	N(S)
N(R)	N(R)	N(R)	N(R)	N(R)	N(R)	N(R)	N(R)
情報フィールド							

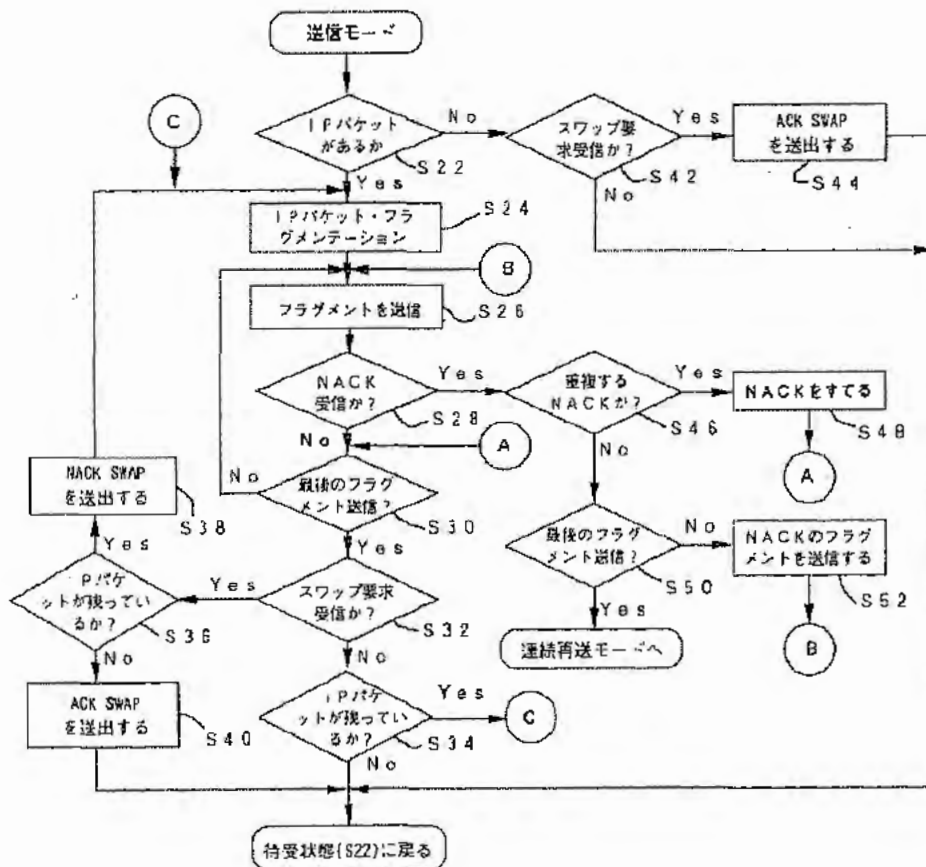
【図4】



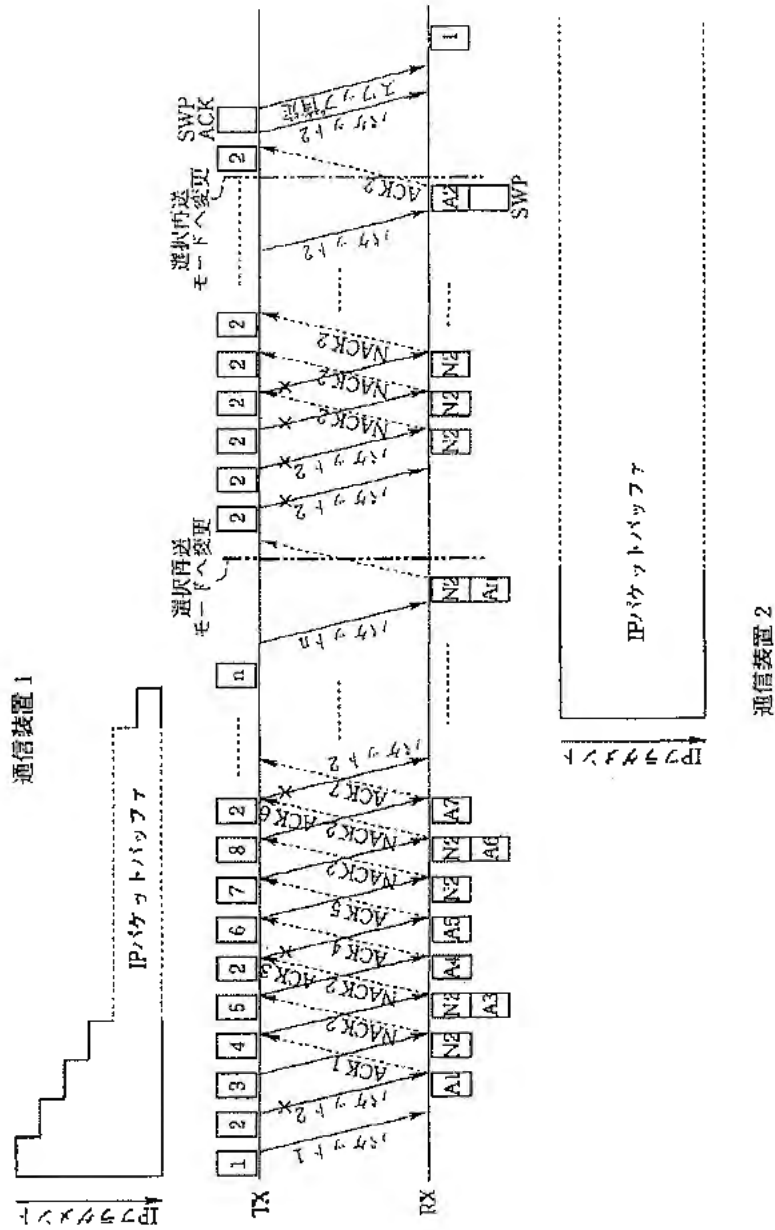
【図22】

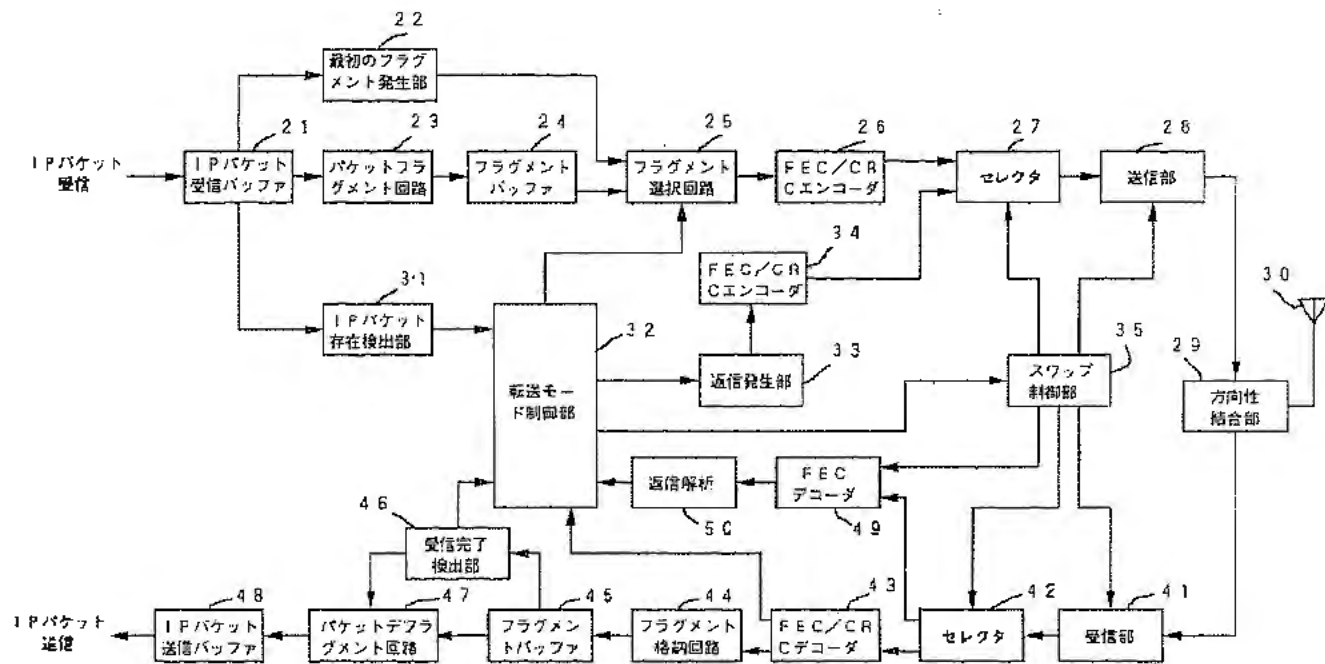


【図7】



【図5】



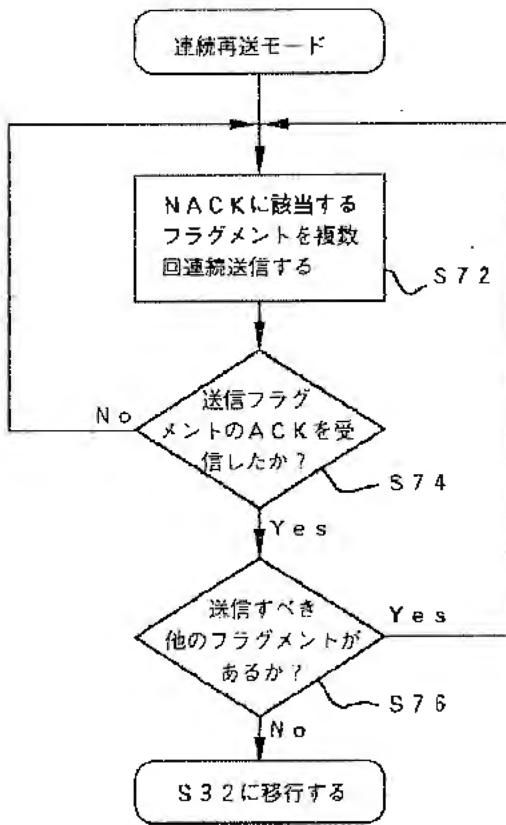


【図6】

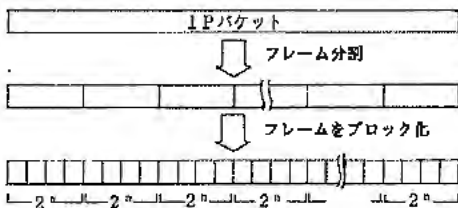
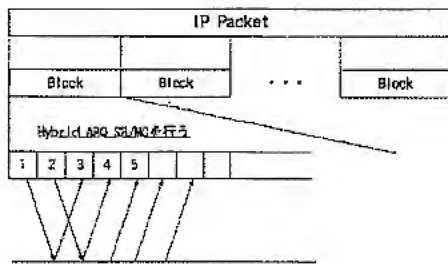
(19)

特開平 11-46187

【図8】



【図11】



IDフィールドコード

ID	Frame Type
00	EMPTY
01	U
10	FCI
11	I

【図26】

Bフィールドコード

B	BLOCK Type
0	BLOCK_0
1	BLOCK_1

Cフィールドコード

C	Control Type
00	EMPTY
01	ACK
10	NACK

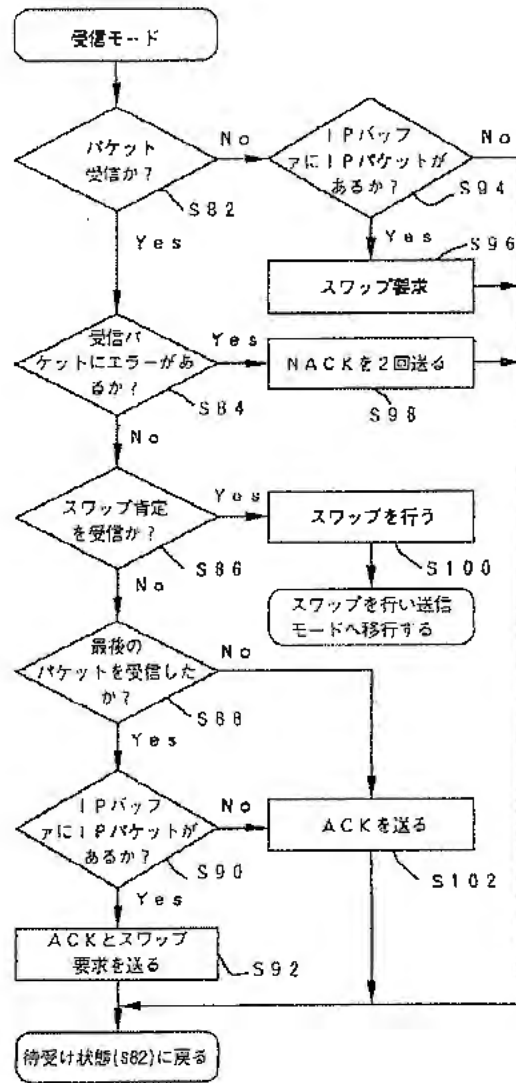
【図24】

【図27】

Iフィールドコード

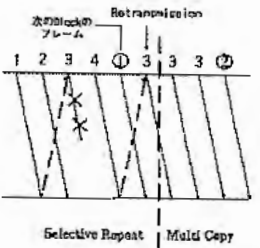
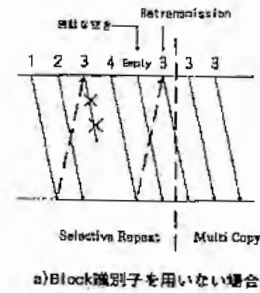
I	I Type
0	CONT
1	DIS_CONT

【図9】

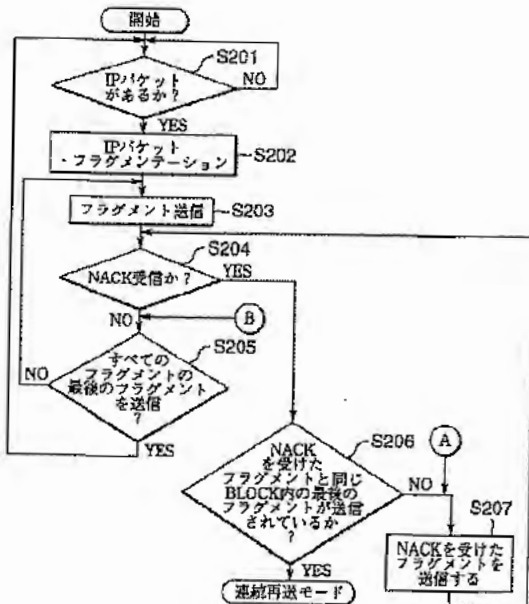


【図23】

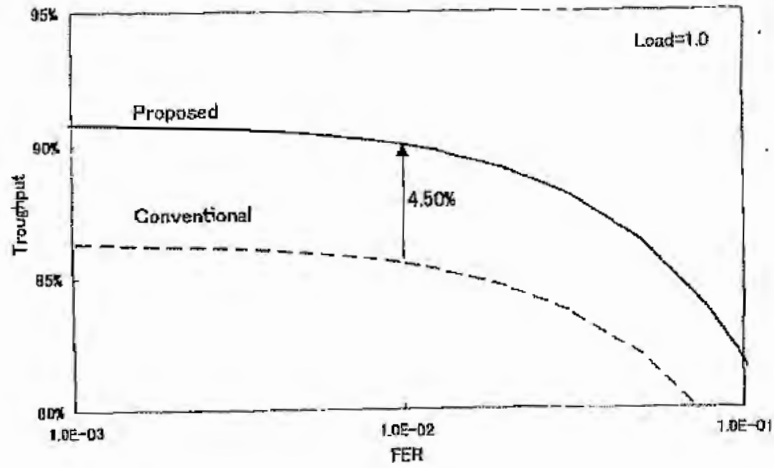
【図14】



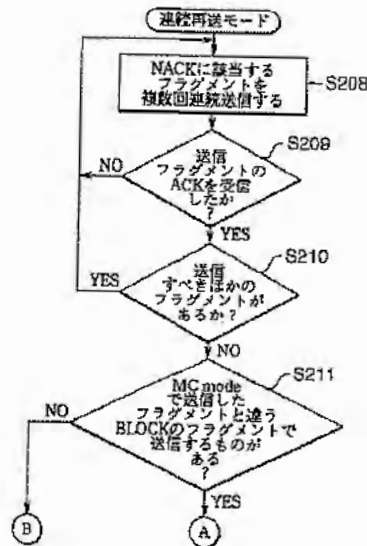
【図17】



【図15】



【図18】

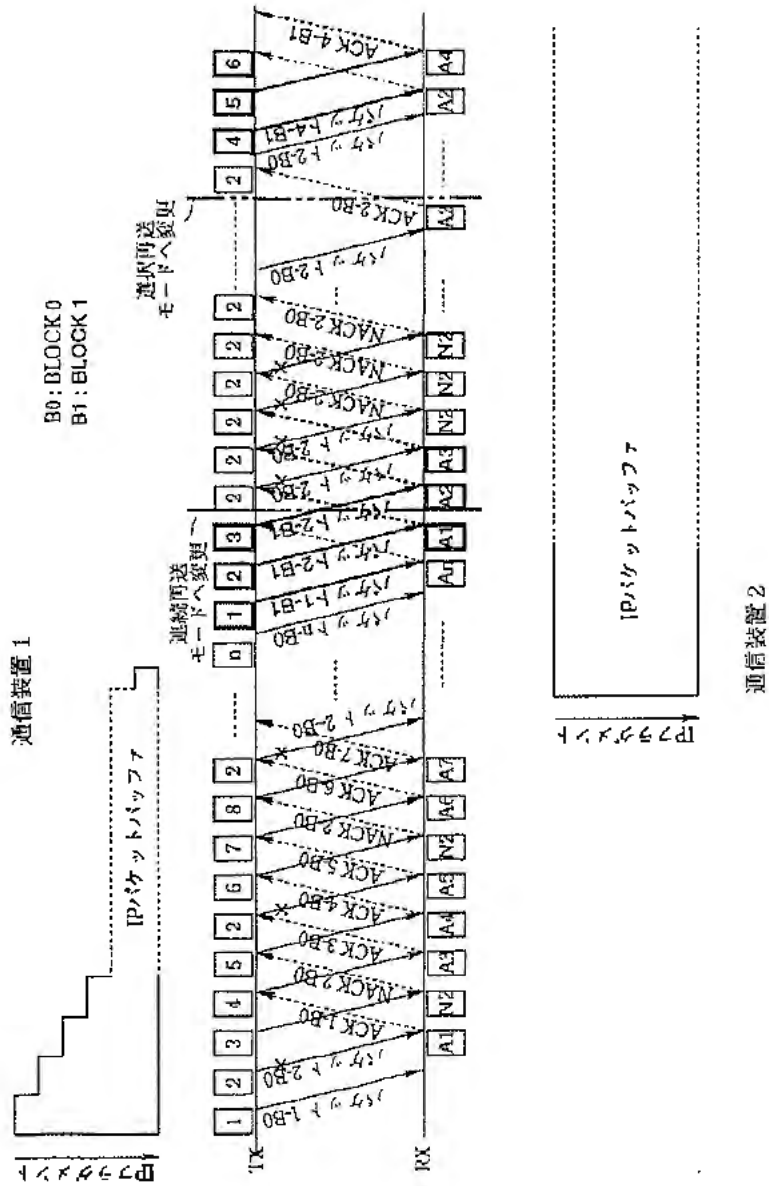


【図25】

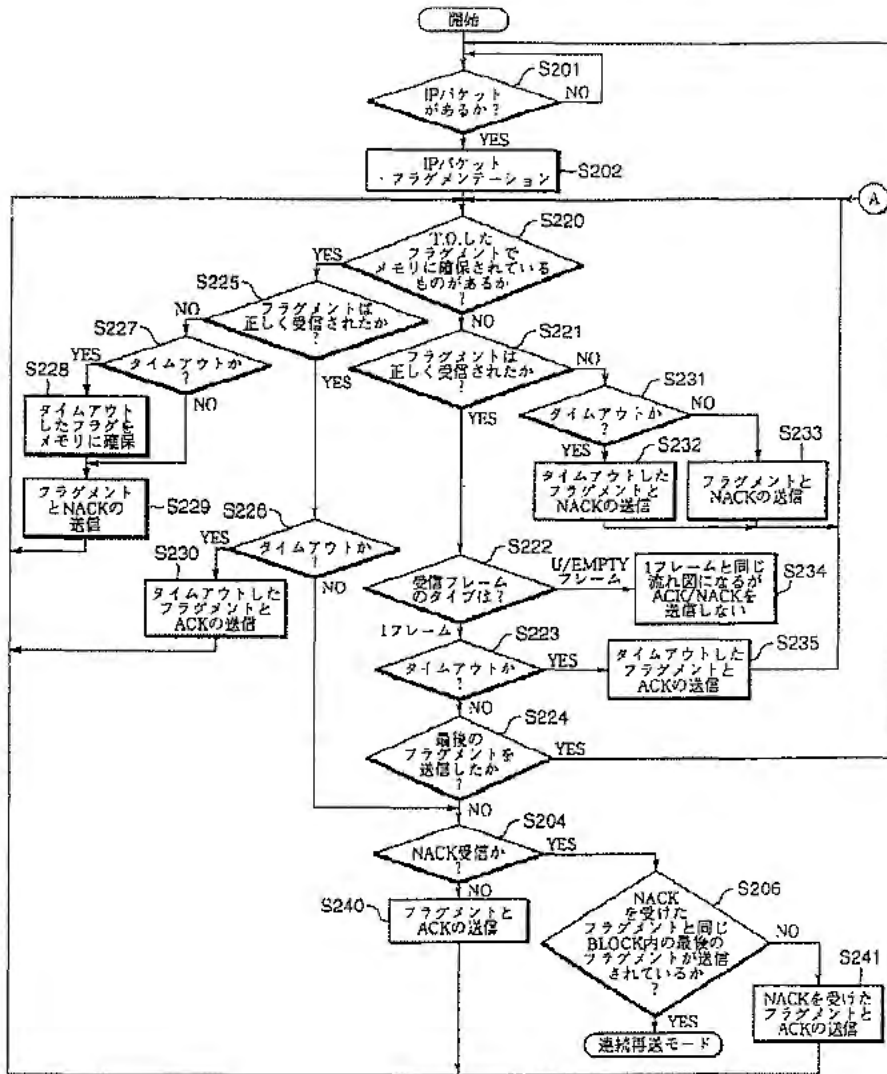
Uフィールドコード

U	U frame type
0001	CHN
0010	UA_CIN
0011	CON
0100	UA_CON
0101	DISC
0110	UA_DISC
0111	RS
1000	RR
1100	BLOCK_0
1101	BLOCK_1

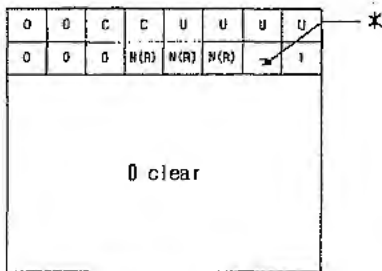
【図16】



【図19】

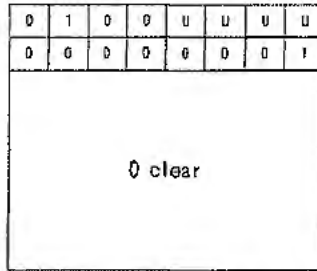


【図28】



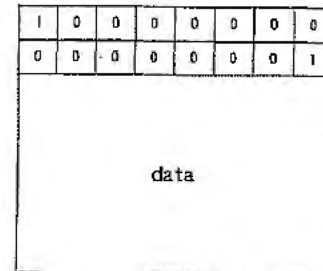
EMPTY フレーム構成図

【図29】



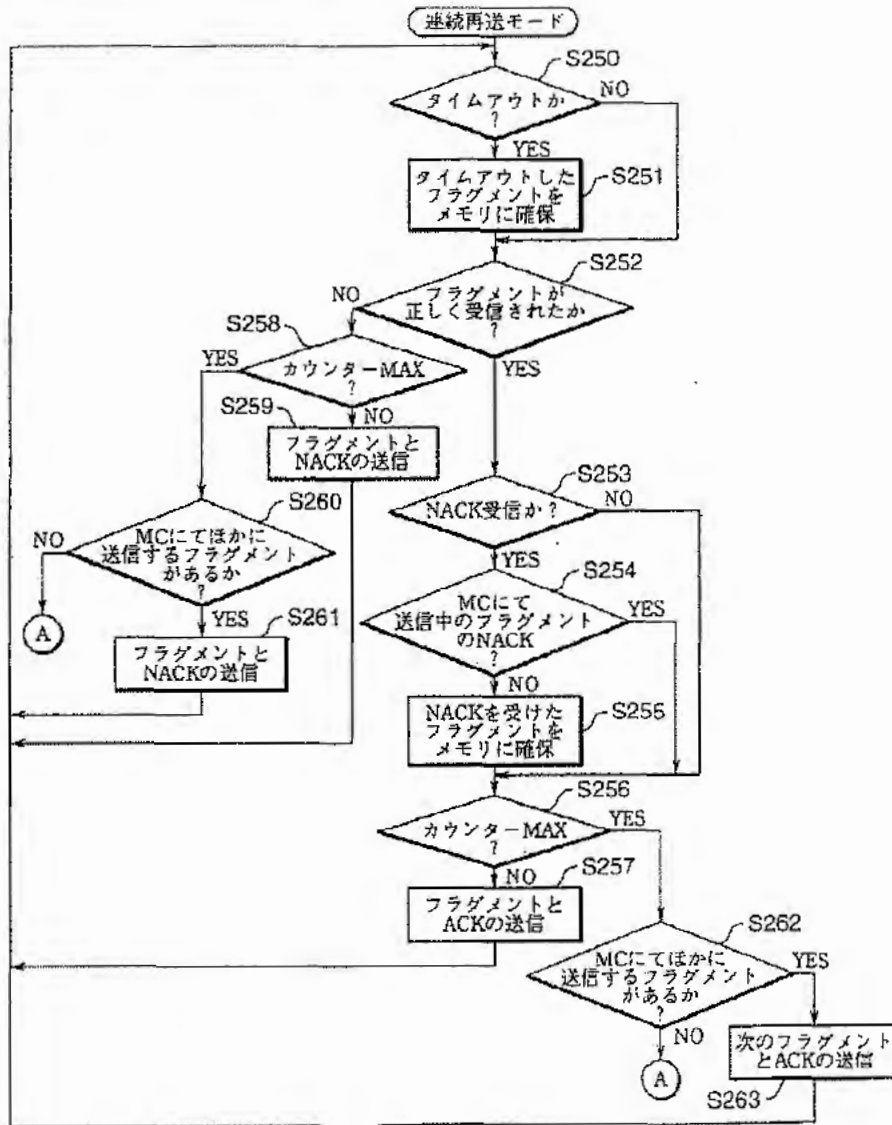
U フレーム構成図

【図30】

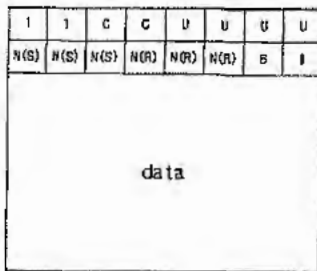


FCI フレーム構成図

【図20】



【図31】



1フレーム構成図

フロントページの続き

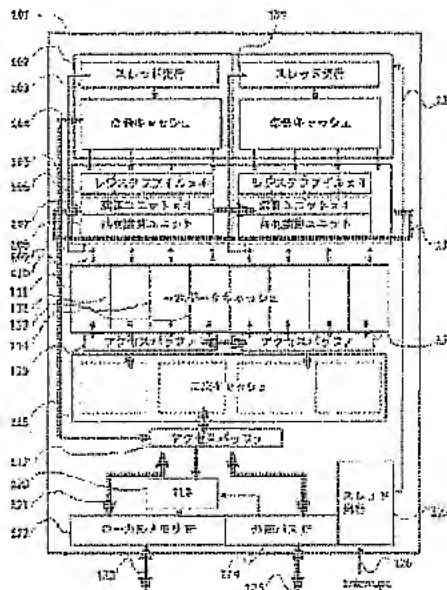
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ン株式会社内

PIPE LINE PARALLEL PROCESSOR USING MULTI-THREAD

Publication number: JP2001236221 (A)
 Publication date: 2001-08-31
 Inventor(s): SHINDO KEISUKE +
 Applicant(s): SHINDO KEISUKE +
 Classification:
 - international: G06F12/08; G06F12/10; G06F12/12; G06F9/30; G06F9/34; G06F9/38; G06F9/46;
 G06F12/08; G06F12/10; G06F12/12; G06F9/30; G06F9/34; G06F9/38; G06F9/46;
 (IPC1-7): G06F12/08; G06F12/10; G06F12/12; G06F9/30; G06F9/34; G06F9/38;
 G06F9/46
 - European:
 Application number: JP20000042696 20000221
 Priority number(s): JP20000042696 20000221

Abstract of JP 2001236221 (A)
PROBLEM TO BE SOLVED: To establish both frequency performance and parallel performance by shortening memory wiring in a system for successively operating plural threads by arithmetic units arranged in a row in a processor using a multi-thread program, and to prevent inter-node data transfer interrupting the parallel processing performance and waiting through synchronization.
SOLUTION: Plural caches for storing data are loaded on a processor carried by patent gazette 1999-287662, and each cache is connected to several arithmetic executing units. The contents of the cache are transferred and duplicated according to the progress of threads. When the contents of the cache can not completely transferred, one thread is executed by a single arithmetic executing unit. Moreover, access to the designated address is detected by using a virtual storage mechanism and the shared mechanism of the caches, and the threads are resumed.



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(19) 日本国特許庁 (JP)

(12) 公開特許公報 (A)

(11) 特許出願公開番号

特開2001-236221

(P2001-236221A)

(43) 公開日 平成13年8月31日 (2001.8.31)

(51) Int.Cl. ⁷	識別記号	F I	テームコード(参考)
G 0 6 F 9/38	3 1 0	G 0 6 F 9/38	3 1 0 E 5 B 0 0 j
	3 5 0		3 1 0 A 5 B 0 1 j
	3 7 0		3 5 0 X 5 B 0 3 j
	3 5 0	9/30	3 7 0 X 5 B 0 9 j
9/30			3 5 0 F

審査請求 未請求 請求項の数31 OL (全 34 頁) 最終頁に続く

(21) 出願番号 特願2000-42696(P2000-42696)

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(22) 出願日 平成12年2月21日 (2000.2.21)

(72) 発明者 進藤 裕介

広島市西区己斐大迫3丁目20番1号

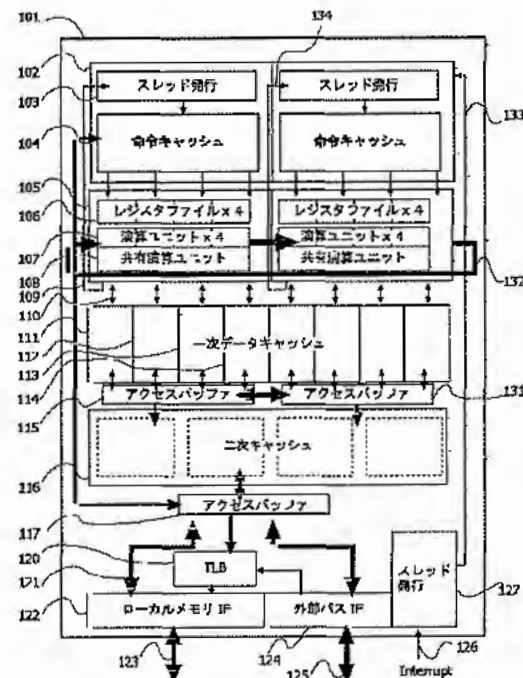
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(54) 【発明の名称】 マルチスレッドを利用するパイプライン並列プロセッサ

(57) 【要約】

【課題】 マルチスレッドプログラムを利用するプロセッサにおいて、一列に並んだ演算ユニットで複数のスレッドを順に動作させる方式において、メモリ配線を短縮して周波数性能と並列性能を両立させる。さらに並列処理性能を阻害するノード間データ転送と、同期による待ちあわせを解決する。

【解決手段】 特許広報平9-287662に記載されたプロセッサに、データを格納するキャッシュを複数搭載し、それぞれのキャッシュを数個の演算実行ユニットと結合する。キャッシュの内容はスレッドの進行にあわせて転送して複製する。キャッシュの内容を転送しきれない場合は、1つのスレッドを単一の演算実行ユニットで実行する。さらに、仮想記憶機構とキャッシュの共有機構を用いて、指定したアドレスへのアクセスを検出してスレッドを再開させる。



【特許請求の範囲】

【請求項1】数値演算ユニット、レジスタファイル、命令メモリ、データキャッシュメモリを複数個内部に有し、複数のスレッドおよびプロセスを同時に利用する事の特徴とするプロセッサにおいて、レジスタファイルが持つ各スレッドごとのレジスタ値等の状態を、常に隣接する演算ユニットに伝達することを特徴とするプロセッサ（以下PMT方式プロセッサと称する）において、プログラムカウンタ、スタックポインタ値、スレッド識別番号、プライオリティ値で構成されるスレッドの情報を示す値を複数格納するスレッド情報格納手段を有し、スレッド情報格納手段から1つのスレッドを選択して、命令メモリおよび演算ユニットにスレッドの情報を伝送するスレッド発行手段を有し、スレッド発行手段において、スレッドの持つプライオリティ値を比較し、最も優先度が高いスレッドの情報を優先的に命令メモリおよび演算ユニットに伝達することを特徴とするプロセッサ。

【請求項2】請求項1の特徴を持つプロセッサにおいて、演算ユニットが実行する命令のプログラムカウンタ値を保存する手段を有し、次に新規に発行する候補のスレッドが同じ命令アドレスを利用するかどうかを比較し、前に実行したスレッドと命令が一致したスレッドを優先的に選択して出力するための手段を有することを特徴とするプロセッサ。

【請求項3】PMT方式プロセッサにおいて、状態を伝達すべき隣接する演算ユニットが別のスレッドの処理を優先的に行うことを感知して、その時だけスレッドの状態を隣接演算ユニットに伝達せずに同一の演算ユニットで処理を行うことを特徴とするプロセッサ。

【請求項4】PMT方式プロセッサにおいて、複数のスレッドがそれぞれ利用するレジスタの値を複数のレジスタバンクに同時に格納するレジスタファイルを有し、各レジスタバンクの内の1つを同時に利用し、スレッドの進行に応じてレジスタバンクの内容を隣接する別のレジスタファイルに転送することを特徴とするプロセッサ。

【請求項5】PMT方式プロセッサにおいて、現在実行しているスレッドを中断し、特機状態のスレッドを実行する操作が必要な際に、実行しているレジスタファイルの値を演算ユニットに伝送する代わりに、レジスタファイルの別のレジスタバンクに格納されている待機状態のレジスタ値を演算ユニットに伝達し、別のスレッドの演算を即座に行うことを特徴とするプロセッサ。

【請求項6】請求項5の特徴を持つプロセッサにおいて、レジスタファイルにレジスタ状態が格納されていないスレッドを実行する際に限り、レジスタファイルの内容をスタックポインタ値の示すメモリから自動的に読み出すことを特徴とし、現在レジスタファイルに格納されていて利用されないスレッドの状態をスタックポインタ値の示すメモリに自動的に書き出すことを特徴とするプロセッサ。

ロセッサ。

【請求項7】PMT方式プロセッサにおける、1つのスレッドが利用するレジスタの値をメモリに保存する特別な分岐命令において、分岐命令の時点のスレッドのレジスタ値をレジスタファイルに保持することを特徴とし、保存されたレジスタの値を読み込む特別な分岐命令において、レジスタファイルに保持されていたスレッドの状態を利用することを特徴とするプロセッサ。

【請求項8】PMT方式プロセッサにおいて、複数のスレッド識別番号及びスタックポインタ値をまとめて格納することを特徴とするスレッド自動発行機構を有し、スレッド発行命令によってスレッドを発行する際に、格納されたスレッド識別番号及びスタックフレームを自動的に割り当てることを特徴とするPMT型プロセッサ。

【請求項9】請求項4に記載された特徴を持つプロセッサにおいて、1つのレジスタファイルが複数の演算ユニットで共有され、レジスタファイルが複数の演算ユニットから1つを選択してデータを伝送することを特徴とする転送手段を有し、レジスタファイルの内容を隣接するレジスタファイルに複数回に分けて転送することを特徴とするプロセッサ。

【請求項10】PMT方式プロセッサの演算ユニットにおいて、値の一部の演算を行う部分演算ユニットを複数個有し、それぞれの部分演算ユニット内部に、部分演算ユニットにおける結果値と完全な演算を行った場合の結果値とが一致しないことを検出するオーバーフロー検出手段を有し、さらに完全な演算を行うための1つの完全演算ユニットを複数の部分演算ユニットに接続し、部分演算ユニットのオーバーフロー検出手段の演算結果の不一致の検出によって、完全演算ユニットに部分演算ユニットで利用した値を転送して演算を再度行うことを特徴とするプロセッサ。

【請求項11】PMT方式プロセッサにおいて、分岐後のプログラムカウンタ値が演算結果によって動的に変更され、分岐後のプログラムカウンタ値が確率的に予測できる条件分岐命令において、分岐後に実行されると予測される命令を格納する命令キャッシュを有し、命令キャッシュに分岐の結果を判別するための情報を有し、実際に分岐が実行された際に予測した分岐結果との一致を確認し、不一致の場合はスレッドを中断してスレッド発行ユニットに正しい分岐結果を転送することを特徴とするプロセッサ。

【請求項12】PMT方式プロセッサにおいて、複数の演算ユニットを複数のブロックに分配し、ブロックごとに専属の一次キャッシュメモリを有し、ブロック内の演算ユニット全てと接続して、データアクセスを行うことを特徴とし、さらに1つ以上の二次キャッシュメモリを有し、複数の一次キャッシュメモリと接続して、互いにデータアクセスを行うことを特徴とするプロセッサ。

【請求項13】PMT方式プロセッサにおいて、スレ

ドが書きこんだメモリ内容をスレッド自身がメモリから読み出して利用する際に、利用するメモリ内容を複数のキャッシュメモリの間で転送することを特徴とし、複数のキャッシュメモリ間の転送はスレッドの進行と同じ方向、速度で伝達することを特徴とし、スレッドの進行にデータの伝達が間に合わない場合はスレッドを停止させることを特徴とするプロセッサ。

【請求項14】PMT方式プロセッサにおいて、プロセッサ内部に1つ以上のキャッシュメモリを有し、個々のキャッシュメモリをさらに複数のメモリバンクに分割し、それぞれのメモリバンクへのアクセス数を制限することを特徴とし、同時にメモリバンクへのアクセスを行うことを特徴とし、さらに、複数のメモリバンクの選択のためにメモリアドレスを利用することを特徴とし、同じキャッシュへの複数のアクセスが存在した場合は、1つのアクセスだけを行い、他のアクセスを保持して後で行うことを特徴とするプロセッサ。

【請求項15】請求項12に記載された特徴を持つプロセッサにおいて、キャッシュメモリ内部に、キャッシュメモリの内容の共有状態を指定するためのディレクトリと呼ばれる情報を有し、個別のキャッシュメモリは、別のキャッシュメモリから内部のデータを読み出された場合に、データのコピーを持つキャッシュメモリを特定する情報をディレクトリに設定することを特徴とし、同時に、別のキャッシュメモリから取得したデータをキャッシュメモリに格納する際に、データのオリジナルを持つキャッシュメモリを特定する情報をディレクトリに設定することを特徴とし、キャッシュメモリへの書き込みの際に、ディレクトリの内容を利用して、同じアドレスのデータのコピーを持つキャッシュメモリにだけデータの書き込みを通知することを特徴とするプロセッサ。

【請求項16】PMT方式プロセッサにおいて、ある命令が利用するデータを別の命令が再度利用する際に、データを再利用する命令を実行する演算ユニットを特定するデータフロー予測情報を命令メモリに格納することを特徴とし、データフロー予測情報を持つ命令が実行されたときに、データフロー予測情報で指定された演算ユニットにデータをあらかじめ転送することを特徴とするプロセッサ。

【請求項17】請求項16の特徴を持つプロセッサにおいて、あるスレッドのデータキャッシュアクセスミスの際に、データの实体のあるデータキャッシュからデータを読み込むと同時に、読み出しを行ったデータキャッシュに要求元の演算ユニットを特定する値を転送し、読み出しを行ったデータキャッシュに対応する命令メモリに、演算ユニットを特定する値を含むデータフロー予測情報を書き込むことを特徴とするプロセッサ。

【請求項18】命令キャッシュメモリを複数有するPMT方式プロセッサにおいて、あるスレッドが、次に実行すべき命令を検索するためにキャッシュメモリにアクセ

スを行い、命令が格納されている命令キャッシュメモリを下位のキャッシュのディレクトリ情報から特定し、前記命令キャッシュメモリに接続された演算ユニットにスレッドを移動することを特徴とし、複数のスレッドが同一の命令キャッシュメモリを利用することを特徴とするプロセッサ。

【請求項19】PMT方式プロセッサにおいて、キャッシュメモリのアドレスを仮想アドレスとすることで、キャッシュメモリ上にはないデータへのアクセスに限って仮想記憶機構にデータを伝送し、仮想アドレスを物理アドレスに変換して物理アドレスメモリに書き戻すことを特徴とするプロセッサ。

【請求項20】PMT方式プロセッサにおいて、アドレス値を入力して、格納されたアドレス値に対する特定のスレッドを生起することを特徴とするデータフロー同期検出ユニットを有し、キャッシュからの読み込み要求に対して、データフロー同期検出ユニットが指定したアドレスとの一致を判定し、一致するアドレスを含む場合はキャッシュに共有状態を示す値を設定することを特徴とするプロセッサ。

【請求項21】請求項20の特徴を持つプロセッサにおいて、データキャッシュ内部で共有状態に設定されているアドレスへのアクセスに対して、ディレクトリの示すユニットにアクセスを通知することで、最終的にデータフロー同期ユニットにアドレス値を伝達することを特徴とし、データフロー同期ユニットが伝達されたアドレス値に対応するスレッドを生起することを特徴とするプロセッサ。

【請求項22】PMT方式プロセッサにおいて、スレッドは同期命令の発行時に停止し、他のすべてのスレッドの、同期命令実行前に行われたストア命令のデータ転送を待ち、すべてのデータが自身のキャッシュに転送された時点でスレッドを再開することを特徴とするプロセッサ。

【請求項23】請求項21のプロセッサにおいて、特定アドレスへのアクセスを検出する命令の発行によって、自分のスレッドの状態をデータフロー同期ユニットに自動的に伝達し、データフロー同期ユニットにおける特定のアドレスへのアクセスの検出によって自分のスレッドを再開することを特徴とするPMT型プロセッサ。

【請求項24】PMT方式プロセッサにおいて、1つのグローバル仮想記憶機構と複数のローカル仮想記憶機構を有し、複数のローカル仮想記憶機構がグローバル仮想記憶の値の一部を有することを特徴とし、グローバル仮想記憶機構の値の改変に対して複数のローカル仮想記憶機構に対して改変を伝達することを特徴とするプロセッサ。

【請求項25】PMT方式プロセッサにおいて、内部のユニット間で伝達する制御信号を、伝送先を示すアドレス値とともにまとめたパケットを利用して転送すること

を特徴とし、複数の制御信号を入力して、複数の制御信号の中から伝送相手に応じて選択して出力するパケットルーターを複数有し、ある演算ユニットからの要求を、パケットに変換して複数のパケットルーターが中継し、目的のユニットに伝達することを特徴とし、1つのユニット間配線を複数の制御信号で共有することを特徴とするプロセッサ。

【請求項26】請求項25に記載された特徴を持つプロセッサにおいて、スレッドが特定のユニットに制御信号を発信して、伝達したユニットから制御信号を受信する制御パケットにおいて、制御パケットをスレッドの進行方向と同一方向のパケットルーターに対して伝達することを特徴とし、制御パケットの伝達がスレッドの進行間に合わないことを検出した場合は、該当するスレッドを即座に停止させることを特徴とするパケットルーター。

【請求項27】請求項25に記載された特徴を持つプロセッサにおいて、特定の制御信号パケットの要求に対して、該当する回路ユニットは要求された内部状態を改変、あるいは読み出して、制御信号を送信したユニットに対して内部状態を転送することを特徴とするプロセッサ。

【請求項28】PMT方式プロセッサを複数個利用して連結するシステムを構築する際に、プロセッサ間の転送方向を固定として、プロセッサのスレッドの状態、データをそのまま別のPMT方式プロセッサに伝送し、システム全体でスレッドを巡回させることを特徴とするPMT方式プロセッサ。

【請求項29】請求項28に記載された特徴を持つプロセッサにおいて、直接連結されていないプロセッサ間で独自にデータ転送を行うためのショートカットバスを設け、遠距離のプロセッサ間の伝送にショートカットバスを用いることを特徴とするプロセッサ。

【請求項30】請求項25に記載された特徴を持つパケットルーターを有し、請求項27に記載された特徴を持つPMT方式プロセッサにおいて、複数のプロセッサの全てのユニットをアドレス値で一意に特定する手段を持ち、スレッドの発行する制御信号パケットを、制御信号パケットの転送先アドレス値に応じて、外部のプロセッサ内部の該当するユニットに伝達することを特徴とするプロセッサ。

【請求項31】請求項30に記載された特徴を持つプロセッサにおいて、それぞれのプロセッサが独自にメモリを接続することを特徴とし、各プロセッサが持つ仮想記憶機構の内部に、指定されたページが外部のプロセッサのデータのコピーを格納していることを示す共有情報を有することを特徴とし、プロセッサ内部からデータを読み込む際に、読み込みアドレスが仮想記憶機構によって共有状態を示す場合には、プロセッサ外にデータ読み込み要求を行うことを特徴とし、プロセッサ内部からデー

タを書きこむ際に、書きこみアドレスが仮想記憶機構によって共有状態を示す場合には、プロセッサ外にデータの書きこみを通知することを特徴とするプロセッサ。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、ソフトウェアによって動的に機能を変更できるプロセッサに属し、特にスレッドと呼ばれる単位で分割されたソフトウェアを利用するプロセッサに属する。

【従来例】(半導体技術の進化とマイクロプロセッサの性能向上)

【0002】半導体技術の進化により、ここ20年はトランジスタ、配線の微細化が常に同じペースで進んできた。DRAMのようにトランジスタ数がそのまま容量につながる素子では、単に微細化によって素子数が増えるだけで、微細化と同じペースで性能を向上できた。

【0003】ところが、マイクロプロセッサに代表される論理LSIに関しては、性能向上には2つの方法がある。1つは動作周波数の向上。そしてもう1つは動作周波数あたりの仕事量である。

【0004】まず、微細化によってトランジスタのスイッチング速度の向上し、前者の動作周波数の向上が可能になった。さらに、後者の動作周波数あたりの仕事量の増加は、利用できるトランジスタの増加により、規模の大きい高速レイテンシ回路、およびスーパースカラなどの並列方式の採用が可能になったことで実現できた。

【0005】これまでは、マイクロプロセッサはこの2つの要素によって飛躍的な性能向上を可能にした。しかし、この2つの要素が、特に後者が限界を迎えつつある。この限界を打破しなければ、今後のマイクロプロセッサの性能向上は見込めない。

【0006】(配線のリスクの相対的増加)

【0007】近年の半導体の微細化技術、プロセスの進歩により、トランジスタの動作速度は飛躍的に増大し、その大きさ、消費電力も飛躍的に減少した。これによって、少なくともトランジスタ単位では、従来では考えられない周波数の動作が可能になった。

【0008】しかし、配線の遅延時間はそれほど改善されてはいない。配線長は、トランジスタのサイズに比例して高速化するわけではない。さらに、微細化された分だけトランジスタの数を増やす場合は配線遅延はかえって増大する。この傾向は深刻に受け止められてきており、配線が最小となるユニット配置を行うことは常識となっている。配線自体のプロセスによる改善も行われている。多層配線やCu配線などがそれである。しかし、それだけでは拡大を続けるトランジスタと配線の速度差を埋めることはできない。

【0009】今後は、配線遅延の増加を押さええて動作周波数の向上比率を維持するためには、常に回路全体に最短配線するという考え方を改め、レイテンシ性能を低下

させてでも最短距離の配線で伝送することが必要となる。

【0010】(データ転送スループットとデータ転送レイテンシ)

【0011】データ転送性能の向上には、データ転送スループットの向上とデータ転送レイテンシの短縮の双方が必要になる。前者のデータの転送スループットの増加は比較的たやすい。それに対して、転送レイテンシは性能低下を押さえるのが精一杯で、数倍以上の改善は見込めない。

【0012】レイテンシ向上の方法としては、キャッシュ、プリフェッチなどによる確率的な方法があるが、それは回路規模を必要とする割にたいした性能向上を果たせない。演算能力と低速なメモリとのレイテンシの開きは拡大の一途をたどり、キャッシュミスにおけるペナルティを相対的に増大させ、最終的には処理時間のほとんどすべてを占めることになる。ということは、なんらかの形でレイテンシを隠蔽することが必須になる。

【0013】そのために現在はアウトオブオーダースーパースカラ、VLIWという方式が存在する。データのロードが終わっていても、データの必要のない命令を先に動作させるプロセッサである。だが、この方式は先に実行させることができる命令を発見する回路が巨大になりすぎ、周波数性能向上に限界がある。

【0014】よって、レイテンシの隠蔽は今後さらに重要になる。だが、アウトオブオーダースーパースカラやVLIWなどの命令レベル並列では、現在以上のレイテンシ隠蔽は不可能である。

【0015】(演算ユニットの使用頻度のばらつきと共有)

【0016】マイクロプロセッサには、加算、論理演算、シフト、分岐、ロードストア、乗算、除算、浮動小数点演算、SIMD型演算、SIMDデータの入れ替え処理など、多くの処理が必要とされる。これらの動作の実現には、それぞれ専用の回路を設けるのが一番効率が良い。ところが、マイクロプロセッサはこれらの全てを同時に必要とするわけではない。稼働率が低いユニットも多く存在する。

【0017】このマイクロプロセッサを同時に複数使用する方式を、マルチプロセッサと呼ぶ。現在のマルチプロセッサでは、これらの演算ユニットが全て複数搭載される。ということは、全体としてはほとんど稼働していない回路が増加することになる。仮に、マルチプロセッサの間であまり使用されない演算ユニットを共有できれば、システム全体の回路の利用効率を高めることができ、本当に数の必要な演算ユニットを増やすことができる。

【0018】(消費電力の増大)

【0019】近年のマイクロプロセッサの動作周波数の向上によって、消費電力は飛躍的に増大した。その増大

を抑制するために、動作電圧を低減させ、低い電圧で性能を維持するための回路技術が開発された。しかし、回路素子数、周波数性能はさらに向上を続けるものと考えられる。さらなる低消費電力の手段が必要になる。

【0020】CMOS回路は、信号のレベルが変化するとき電力を消費する。ということは、信号のレベルの変化の少ない回路がもっとも消費電力の低い回路となる。回路構成のレベルでは、演算ユニットやクロック信号制御など、信号変化を低減する手段が多く利用されている。しかし今後は、さらに上位のアーキテクチャにおいても、最小の電力で演算を行うための手段が必要になると考えられる。

【0021】回路的に考えると、同じ仕事を連続して行うことができれば、回路の状態の変動も最小限となり、動作する回路も最小限となる。そして、トランジスタ数あたりの性能が向上できれば、逆にいえば性能あたりの消費電力が低減できるということである。

【0022】(演算内容の巨大化、分散化)

【0023】前の演算の終了を待ち、その結果を利用して演算を行うことを、データ依存関係と呼ぶ。互いにデータ依存関係のある演算は原理的に同時実行ができず、並列化を阻害する最大の要因である。いかなる方式もこれを解消することはできない。

【0024】ソフトウェアの構造上、このデータ依存関係がもっとも大きいのは連続した命令の近傍であり、現在のスーパースカラやVLIWに代表される、命令レベル並列の対象とされる部分である。すなわち、命令レベル並列はもっとも並列化しにくい部分をあえて並列化する方法であり、性能向上に限界が生じる。

【0025】一般的に仕事の単位をうまく分割できれば、分業が効率が良いのは言うまでもない。そして、巨大なソフトウェアでは、その動作内容が全て密接に結合し、全ての命令、データが同じ確率で利用されるということはあるにない。現に、ソフトウェアは、オブジェクトと呼ばれる独立性の高い単位で分割できることは良く知られている。

【0026】(データスループットの爆発的な増大)

【0027】メディア処理は、巨大なデータ転送能力を要求し、キャッシュの内部で実行できない代表的な処理である。この処理の多くは巨大なデータ転送スループットを要求する。それに対して、メディア処理は全体としてはさしてレイテンシを要求しない。要求されるレイテンシはどんなに小さくても1ミリ秒程度がせいぜいである。レイテンシを犠牲にして並列処理を行うのにこれほど向いた用途はない。

【0028】局所的なレイテンシがそのまま総和される現在のプロセッサの方式では、プロセッサバスのレイテンシがそのまま加算され、全体の性能向上も頭うちになる。それに対して、レイテンシをなんらかの手段で隠蔽することができれば、メモリアクセスの並列化などの方

法によってスループットを確保することができる。そのためにマルチスレッドと呼ばれるソフトウェアモデルを導入して、レイテンシの累積を防止する。スレッド単体のレイテンシが多少大きくてもメディア処理に要求されるレイテンシよりはるかに小さいため、結果的にメディア処理に要求される性能を全て満足することができる。

【0029】(演算の繰り返しの増加)

【0030】長時間動作するプログラムは、その全ての時間に渡ってまったく違う命令を実行することは考えられない。そのため、長い時間の動作の中では、何らかの形で同じコードを再利用して同じ動作を繰り返していることになる。

【0031】この傾向を利用することにより、同じ動作を行う部分を同時にまとめて実行することで、同じ動作で共有される命令メモリ、データメモリなどの資源を共有することができる。しかも、まったく同じ動作を時間的にわずかにずらして実行することにより、同じ資源を同時に利用することも簡単に防ぐことができる。

【0032】(IPユニットの内蔵と、それを結合する性能の要求)

【0033】汎用プロセッサは、32ビットなどの桁の多い数値演算や、大容量メモリ全域を利用した処理、動的に変わる処理に関しては他の手段では実現不可能な性能を発揮できる。しかし、少数の複雑なビット処理演算に関しては依然として弱く、目的に応じて最適化された回路の方が常に性能が上である。ということは、システム全体の性能向上のためには、依然として良く利用されるビット演算を担う回路、IP回路を内蔵することが望ましい。

【0034】ところが、IP回路は、その前後の動作がなければ十分な性能が発揮できない。IP回路同士を直接連結すると、その回路の動作の種類を制限することになる。プログラマブルでかつ高速なアプリケーションの動作を実現するためには、複数の最小限度のIP回路と、IP間のデータの中継を行う十分な演算処理能力が最良の組み合わせである。

【0035】(スーパースカラ、VLIW方式)

【0036】スーパースカラ方式、VLIW方式は、命令レベル並列とよばれ、同時に複数の命令を実行することで、性能を向上させることを狙った方式である。

【0037】まず、スーパースカラ方式は、複数の命令の組み合わせを自動的に抽出してくれる方式である。ところが、自動的に抽出できる命令の範囲、命令ウィンドウは限定されており、特に、条件分岐命令の後に実行される命令の抽出が非常に難しい。そのため、プログラム全体の並列性を生かすことができず、隣接した数個の命令を実行するのがせいぜいである。

【0038】図2に、従来のプロセッサ例としてVLIW方式のプロセッサの構造模式図を示す。VLIW方式は、この命令の抽出の手間をコンパイラに任せ、並列可

能な命令を明示して命令メモリに格納する方法である。しかし、並列化の対象となるのはプログラム内部で隣接した数個の命令であることには変わりない。

【0039】201は複数の命令を同時に格納する命令キャッシュである。命令発行ユニット208は、命令キャッシュ201から同時に複数の命令を読み込み、送られた命令を実行できる演算ユニットにそれぞれ命令を分配する。演算ユニット202、演算ユニット203、分岐ユニット204、ロードストアユニット205は、同時に独立した動作ができる。演算ユニット202、演算ユニット203は、共有レジスタファイル206から複数の値を取り出して演算を行い、結果をレジスタファイル206に返す。分岐ユニット204は、命令キャッシュ201に対してPCアドレスを変更させる。ロードストアユニット205は、データキャッシュ207からレジスタファイル206にデータを読み込む。あるいは逆に、レジスタファイル206の値をデータキャッシュ207に転送する。

【0040】(マルチプロセッサ方式)

【0041】図3に、従来例としてマルチプロセッサ方式を示す。マルチプロセッサ方式は、既存のパイプライン、スーパースカラ、VLIWのいずれかの方式で作成されたプロセッサを複数接続して利用する方法である。飽和しつつある命令レベル並列を補うために用いられる。

【0042】そのために、ソフトウェアをプロセス、あるいはスレッドとよばれる独立した単位に分割して、それぞれのプロセッサに割り当てる。それぞれのプロセッサはそれぞれ独立したスレッドを実行することで、命令レベル並列に対して演算ユニット間の通信を抑制することができる。

【0043】図3にマルチプロセッサの構造を示す。プロセッサ301、302、303、304は、共有バス305に接続される。プロセッサ306、307、308も同様に共有バス309に接続される。共有バス305には二次キャッシュ310が接続され、プロセッサ301のメモリは基本的には二次キャッシュ310から取得する。2つの二次キャッシュ310、311は、共有メモリバス312に接続され、二次キャッシュとメインメモリ313の内容を同一にする。

【0044】プロセッサ301~304、306~308は、それぞれ独自に命令動作を行い、命令、データをメインメモリ313からキャッシュを介して取得する。他のプロセッサと同一アドレスのデータを共有しない限り、プロセッサ間通信は行われない。

【0045】これらのプロセッサ、二次キャッシュ310、311は、半導体のチップに全て搭載することが可能である。半導体チップの微細化によって、同じコストでもより多くの回路の搭載が可能になったため、複数のプロセッサを1つのチップに搭載することで、コストに

対する性能を向上させることになる。

【0046】(従来のPMT方式)

【0047】図4に、命令レベル方式、およびマルチプロセッサ方式の欠点を解消するための従来の方式を示す。以下、この方式をPMT方式と呼称する。PMT方式についての詳細は特許広報平9-287662に記載されている。

【0048】このPMT方式は、前述のマルチプロセッサ方式で利用されるプロセス、スレッドをほぼそのまま用いる。そして、演算ユニット間の通信を最小限にすることにより、演算ユニットの増加に対して周波数性能の低下を抑制し、動作周波数を維持しつつ大量の演算ユニットの搭載を可能にし、飛躍的な性能向上を可能にする。さらに、演算ユニットなどの回路を可能な限り共有することによって、最小の回路規模で最大の並列規模を達成できる。

【発明が解決しようとする課題】

【0049】(VLIW方式の欠点)

【0050】VLIW方式の欠点を示す。まず、命令レベル並列は、プログラムの局所的な領域だけで実行できる命令を選択する方式である。理由は、プログラムはその場の演算結果によって命令の流れが頻繁に変更されるため、演算が終了するまで次に実行すべき命令を特定することはできない。それをある程度克服するために分岐予測と呼ばれる機構があるが、それでも複数の分岐の先を予測することは難しい。そのため、命令キャッシュ301の幅を広げても、同時に実行できる命令をプログラムから大量に選択できないため、性能向上率が飽和する。

【0051】さらに、複数のデータ依存関係が発生するという事は、それらの命令の間のデータの自由な転送が必要になるということである。一般的に、命令実行ユニットのN倍の増加に対して、実行ユニット間の配線の遅延時間はN倍以上、回路規模はNの二乗の規模で増加する。そのため、命令実行を増やしても、それ以上に周波数性能が低下するというデメリットが生じる。

【0052】以上の理由によってVLIW方式は性能向上に限界がある。

【0053】そのため、命令発行ユニット208の幅を広げるのはあきらめて、複数の明示的に独立したスレッドを1つのプロセッサで同時に実行するのも必要と考えられるようになった。そのため、小規模なVLIWを複数搭載し、個々のVLIWで個別のスレッドをそれぞれ動作させるという方法が考案されている。ところがそれでは、次に述べるマルチプロセッサ方式の問題が発生する。

【0054】(マルチプロセッサ方式の欠点)

【0055】次に、マルチプロセッサ方式の4つの欠点を示す。

【0056】まず、マルチプロセッサでは、負荷の高い

プロセッサから負荷の低いプロセッサへプロセス、あるいはスレッドを移すのに非常に時間がかかる(以下、このプロセス、スレッドの移動をプロセス移住、スレッド移住と呼ぶ)。

【0057】次に、マルチプロセッサにはプロセッサ間通信が必要になる。複数のプロセス、スレッドがまったく独立したデータを利用することはまれであるためである。ところが、1つのデータを全てのプロセッサが利用すると、データ通信の量はプロセッサの数にほぼ比例して増加する。そして、通信の量が増えるということは、単体のプロセッサから見てもメモリのアクセスが通信、同期によって制限されることになり、単体のプロセッサにおいても、システム全体においても性能が飽和する。

【0058】次の問題は、プロセッサ間の同期である。あるプロセスがほかのプロセスの特定の処理を待つために停止し、別のプロセスからの処理終了の伝達によって再開するのが同期である。このための最も原始的な手法は、待ち状態のプロセスが定期的に別のプロセスの状態を監視することである(スピンロックと呼ばれる)。しかし、これでは待ち状態のプロセスがプロセッサ、メモリバスなどの資源を占有するために非常に効率が悪い。そのために、OSレベルのソフトウェアで同期処理を管理する方法などがあるが、そのためのソフトウェア処理が大規模な並列における性能向上を阻害するという問題がある。

【0059】最後に、マルチプロセッサは、メモリ、複数の演算ユニットをすべて搭載するプロセッサを、さらに複数搭載する。そのため、それぞれの演算ユニット、メモリの稼働率にもかかわらず、すべてのコピーがプロセッサの数だけ搭載されることになる。そのため、回路規模の点で無駄が多い。

【0060】(従来のPMT方式の欠点)

【0061】PMT方式は、以上で述べた、VLIWに代表される命令レベル方式の性能の限界、およびマルチプロセッサ方式の回路規模的な欠点を解消するための方式である。

【0062】まず、複数のスレッドを常に全てのユニットで巡回させることで、スレッド発行ユニットを演算ユニット間で共有できる。さらに、全てのスレッドを空いた演算ユニットに対して即座に発行することができ、スレッドを中断した場合も、スレッドの移住を行わなくてもその場で再開が可能である。これによって、レイテンシを隠蔽するためのスレッドの切り替えを高速に行うことができる。

【0063】複数のスレッドを動作させる際には、データキャッシュの内容を共有することが多い。そのため、スレッド間で同じデータキャッシュを共有することで、全てのキャッシュへ同じデータを転送する必要がなくなり、ブロードキャスト型のデータの転送を最小限にすることができる。

【0064】同じ種類のスレッドは、同じ命令、データメモリ、演算ユニットを利用する傾向が強い。この性質を利用して、1つの命令キャッシュ、データキャッシュ、特殊演算ユニットを複数のスレッドから共有させることで回路を削減することができる。

【0065】だが、従来例に挙げた図4のPMT方式には、以下の欠点がある。

【0066】まず、コンテキストスイッチのために、メモリにレジスタの値の退避が常に必要になる。キャッシュミスのように、もとの演算ユニットでスレッドを再開できるような処理では、演算ユニットにレジスタを保持しておけば、スレッドの移住は必要ない。そのために、複数のスレッドを同時に管理するレジスタファイルが必要になる。

【0067】次に、分岐命令ごとにコンテキストスイッチが必要になる。理由は、命令アドレスに対して、実行される演算ユニットが常に決定されているために、命令アドレスが昇順に実行されない場合はスレッドの移動が必要になるためである。分岐命令はソフトウェア全体で4分の1を占めるともいわれるため、このようなスレッドの移動は大きく性能を低下させる。ソフトウェアのインライン展開によってある程度分岐を減少させることは可能であるが、汎用的なソフトウェアで性能が出る構造が望ましい。

【0068】次に、命令アドレスによって実行される演算ユニットが決定されるため、命令の配置によっては演算ユニットの稼働率にバラ付きが生じる。同じようにソフトウェアのインライン展開でうまく大半の演算ユニットを利用することはできるが、汎用的なソフトウェアで負荷分散が出来る構造が理想的である。

【0069】従来のPMT方式では、キャッシュ間でデータのコピーを持たせないために、全ての実行ユニットが全てのキャッシュメモリと接続するように配線させる必要がある。そのため、実行ユニットのN倍の増大にしたがってNの二乗で規模が増大する。配線遅延が深刻化する現在では、このような配線は確実に周波数性能を低下させる。ところが、性能向上の為に実行ユニットを増加させることが不可欠である。そのため、キャッシュのコピーを各実行ユニットに持たせる必要があり、キャッシュ間の内容の整合性を取るハードウェアを実装する必要がある。

【0070】従来のPMT方式では、キャッシュのコピーを一切行わないため、全てのキャッシュのアクセスは順序が入れ変わることはない。ところが、キャッシュのコピーを持たせる構造にすると、キャッシュのアクセス順序を保持できなくなる。そのため、新たなハードウェアによる同期機構によって、キャッシュのアクセス順序を保証する必要がある。

【0071】最後に、全てのスレッドは全ての資源に無制限にアクセス可能であり、同時に独立したプロセスを

動作させることができない。そのためには仮想記憶機構によるプロセス間保護の実装が必要である。ところが、キャッシュメモリを分散させると、仮想記憶機構はキャッシュメモリの数だけ必要になる。キャッシュメモリは複数のプロセスが混在するため、単体の仮想記憶の容量も増大する。更に、仮想記憶機構を分散させると仮想記憶の規模が膨大なものになる。

【0072】以上が従来のPMT方式の欠点である。PMT方式の持つ長所を維持しつつ、これらの欠点を解消するのが本発明の目的である。

【課題を解決するための手段】

【作用】

【0073】(コンテキストスイッチ)

【0074】本発明のプロセッサはマルチスレッドを利用する。マルチスレッドは大規模なレイテンシを隠蔽する唯一の方法と言ってよい。このマルチスレッドの管理は、従来のマルチプロセッサなどではOSの仕事となっているが、それがスレッドの数に比例して処理時間を増大させて、マルチスレッドの長所をほとんど発揮できない要因となっている。ハードウェアで極力マルチスレッド動作を実現するのが望ましい。

【0075】図16にマルチプロセッサにおけるマルチスレッドの実行例を示す。スレッドAからスレッドBへの切り替えを行うスケジューリングは、常にプロセッサの資源を消費する。さらに、キャッシュミスの期間には、他のスレッドの動作ができず、各プロセッサはアイドル状態となる。

【0076】図17に、本発明のプロセッサにおけるマルチスレッドの実行例を示す。本発明のプロセッサでは、複数のスレッドがストールしない限り、スケジューリングを全てハードウェアで行うため、常に演算ユニットを実際の動作に利用することができる。キャッシュミスの場合も、別のスレッドがかわりに動作することができる。キャッシュの入れ替え動作が終了した後は、別の任意のスレッドのストールによって、スレッドを再開することができる。

【0077】結論として、本発明のプロセッサは、マルチプロセッサ方式に対してコンテキストスイッチ、スケジューリングの時間が不要である。さらに、本発明のプロセッサはあらゆるスレッドの待ち時間に他のスレッドが動作可能であり、どんなに並列度を上げてでも演算資源をほぼ常時利用することができる。これは、現在の命令レベル並列では、数並列程度でも演算資源の利用率が半分以下であるのと対照的である。

【0078】複数のスレッドを同時に動かす際には、待ち状態のスレッドの中から演算能力に相当する数のスレッドを選択することが必要になる。スレッドには、例外や割り込み要求の応答など、即座に実行を要求されるものと、比較的実行遅延が許されるものとが混在している。このため、スレッドの優先順位を設け、それを自動

的に選択する機構が必要になる。

【0079】本発明のプロセッサにおけるスレッドは16段階のプライオリティーを有する。スレッド発行ユニットは、実行待機状態のスレッドを格納し、スレッドのプライオリティーをハードウェアで判定して選択して、同時に1つのスレッドを発行する。また、既存のスレッドよりもバッファ上のスレッドの優先度が高い場合は、無条件で既存のスレッドを休止して新規のスレッドを発行する。プライオリティーが同一の場合はとくに優先制御、負荷分散制御を行う必要はない。

【0080】なお、実行ユニットの稼働率が高く、新規のスレッドを発行できない場合は、隣接するスレッド発行ユニットに順にスレッド状態を転送する。

【0081】スレッド発行ユニットが発行すべきスレッドを選択する際に、前に実行したスレッドと共通の命令を利用するものが理想的である。理由は、命令が同一であれば利用するデータも同じである確率が高いこと。そして、命令などの状態が等しければ、制御回路などの状態の変更が最小限となり、状態信号が変化しなければCMOS回路の特質上消費電力が最小となるためである。

【0082】そのために、前に発行したスレッドの命令アドレスを控えておく。そして、次に発行するスレッドの命令アドレスと、控えておいた前のスレッドの命令アドレスを比較し、同一であればスレッドを即座に発行する。アドレスが同一でない場合は、今のスレッドとプライオリティーが同一以上のスレッドがない場合に限り用意したスレッドを発行する。

【0083】PMT方式では、そのままではスレッドのライン間の移動によって演算ユニットの間で負荷のばらつきが生じる。そのため、ある演算ユニットは負荷が極端に高く、どうしてもほかのスレッドの要求を受け付けられない状態が発生する。そういう場合は、空いた1つの演算ユニットを有効活用するために、その演算ユニットを単一プロセッサとみなしてスレッドの実行を行う（今後、この動作を局所SMP実行モードと称する）。こうして、PMT方式とSMP方式を混在させて、スレッドが充填されない演算ユニットを最大限に活用する。プライオリティーの高い別のスレッドの要求によって、局所SMP実行モードは解除される。

【0084】スレッド発行ユニットが4つの演算ユニットで共有される場合は、局所SMP実行モードは4つの演算ユニットを順に利用して行う。この場合、4つのスレッドが同時に動作することになるが、相互の演算ユニット間のレジスタ、データ転送は不要である。

【0085】コンテキストスイッチを高速化するために、従来のPMT方式にあったレジスタのメモリへの待避の必要性をなくす。そのために、レジスタファイルには複数のスレッドの情報を共存させ、そのうちの1つだけを利用する。コンテキストスイッチは、利用するレジスタファイルのバンクを切り替えるだけで良く、即座に

スレッドを切り替えることができる。

【0086】PMT方式では、スレッドは基本的には一定方向に移動する。しかし、命令、データの共有を実現するためには、すでに命令が保持してある演算ユニットにスレッドを移すことが望ましい。あるいは、すでに負荷の高い演算ユニットに到達したときは、負荷の低いラインに移動する必要がある。そのために、演算ユニット間でスレッドを移動させる、スレッド移住機構を設ける。スレッド移住は以下の手順で行う。

【0087】(1) 実行ユニットからストール要求。同時にレジスタバンクを別のスレッドに切り替える。

【0088】(2) スレッド発行ユニットは待機してあるスレッドを供給。

【0089】(3) データキャッシュにレジスタの内容を退避。直接二次キャッシュに対して送られる。

【0090】(4) 目的のノードにスレッド情報転送。

【0091】(5) データキャッシュ階層を通して、目的のノードに近い二次キャッシュからレジスタの読み込みを行う。データキャッシュ間の転送は、後述のキャッシュコヒーレンシ機構を用いる。

【0092】なお、本発明では、負荷分散のためのスレッドの移住は基本的には不要である。待ち状態のスレッドは一定場所にとどまっていれば、いつかは他のスレッドが使用していない空いたパイプラインが流れてくるためである。

【0093】図22に、スレッド移住における動作を示す。横軸は演算ユニットの列であり、縦軸は時間経過である。斜線が個別のスレッドの実行を示す。

【0094】7番の演算ユニットへのスレッドの移住によって、7番から10番の演算ユニットはメモリからレジスタを読み込む。11番の演算ユニットから実際のスレッドが再開される。

【0095】プライオリティーの低いスレッドは、7番の演算ユニットがプライオリティーの高い別のスレッドによって占有されたことを検出して、2番の演算ユニットの時点でスレッドを停止させる。3番から6番の演算ユニットではレジスタ状態をメモリに待避する。7番の演算ユニットから別のスレッドの移住が始まる。

【0096】一般的にサブルーチンコールでは、それまでのレジスタをスタックに保持して、リターン直前に退避したレジスタを読み込む操作が必要になる。本発明のプロセッサでは、サブルーチンコールはレジスタを隣接転送する際に、元のレジスタを破壊せずに、サブルーチンコールを実行した演算ユニットのレジスタバンクに保持しておくだけで実現できる。そしてリターンはその保持されていたレジスタバンクを再利用して、帰り値を示す1つのレジスタだけを代入すれば良い。

【0097】図20に、サブルーチンコールの動作例を示す。CALL命令がサブルーチンへの分岐、RET命令がサブルーチン終了を示す命令である。

【0098】CALL命令のように、元の命令アドレスに戻り、元のスタックの値を利用する処理においては、CALL命令の位置にレジスタ値を残しておくだけで良い。レジスタはコール先の命令にも複製されて継承される。

【0099】RET命令の実行によって、帰り値だけがCALL命令に送られる。それ以外のレジスタは、元のレジスタの値をそのまま利用すればよい。

【0100】保持してあるレジスタバンクをほかのスレッドが利用するときは、前述のスレッド移住機構におけるレジスタ同期機構によって、自動的にメモリへの退避が行われる。

【0101】割り込みユニットやTLBは、蓄積されたスレッドIDをスレッド発行ユニットに伝達し、指定されたスレッドを動作させることができる。

【0102】そして、TLBからのスレッド生起は、ページフォルトなどのTLB例外によるコンテキストスイッチを高速化するとともに、OSカーネルサービスの並列化を実現する。

【0103】本発明のプロセッサは大量のスレッドを利用する。そのためには、現在進行しているスレッドの演算能力を極力利用せずに、大量のスレッドを発行しなくてはならない。そのために、スレッドが必要なスレッドID、スタックなどの情報（スレッド構造体と呼ぶ）はハードウェアで管理して、スレッドの生成によって自動的に転送する。実装としては、まとめてスレッドIDとスタックポインタを格納するバッファだけを設ける。バッファの内容の管理はまとめてソフトウェアで行う。

【0104】スレッドを発行する場合は、スレッドバッファから空き状態のスレッド構造体を要求する。スレッドバッファにスレッド構造体が無い場合は、現在のスタックポインタをそのまま返し、これ以上マルチスレッドで実行できないことをプログラムに通達する。

【0105】こうして、スレッド発行命令は新規のスレッド構造体を取得する命令だけで済むようになり、スレッド発行におけるソフトウェアオーバーヘッドを削減できる。

【0106】（演算パイプライン）

【0107】本発明のプロセッサは、レジスタファイルを隣接する複数の演算ユニットで共有する。4つの演算ユニットでレジスタファイルを共有する場合は、4つのレジスタファイルと4つの演算ユニットとの間で自由にアクセスするためのクロスバ接続バスを設ける。

【0108】こうして、従来のPMT方式が常にすべてのレジスタの値を隣接するユニットに転送を必要としたのに対して、隣接するレジスタファイルへの転送を数クロックに1回に抑制することができる。

【0109】レジスタファイルには複数のスレッドの情報混在するが、一度に送るのは1つのスレッドのさらに4分の1の内容で十分となり、実行ユニット全体で

も、1つのスレッド分のレジスタ転送だけで良い。

【0110】なお、同一の命令を利用するスレッドを連続して動作させている場合は、転送する信号の変化はスレッド間のレジスタ値の違いだけとなる。この違いだけがCMOS回路における消費電力となる。

【0111】本発明のプロセッサは浮動小数点演算ユニットを搭載することができるが、このユニットは整数演算に比べてレイテンシが大きくなるという特徴がある。その間、依存関係のない別の整数演算命令を実行することで、浮動小数点演算のレイテンシを隠蔽できる。

【0112】同一の命令を用いるスレッドを連続動作させる場合では、長レイテンシ演算も1つのユニットを使いまわすことになる。この場合は、1クロック分の演算が終了した時点で、隣接する別の長レイテンシ演算ユニットに中間値を渡し、並行して演算を行う。こうして、長レイテンシ演算のスループットを向上させる。

【0113】本発明のプロセッサは、一般的なパイプラインプロセッサと同じく、パイプラインを停止するパイプラインストールを発生する機能を有する。ただし、パイプラインプロセッサと違う点は、ストールする対象が単独のスレッドに限られ、ほとんどの種類のストールの間に待ち状態の別のスレッドを再開できる点である。

【0114】パイプラインストールは、一般的にはあるスレッドの要求する演算ユニット、あるいは転送バスなどの資源を取得できなかった場合に発生する。そして、ストール状態のスレッドは、その原因が解決された時点で、プライオリティの低い別のスレッドの動作を中断することができる。

【0115】パイプラインストールは、すでに実行してしまった演算内容を1、2命令分キャンセルする必要がある。たとえばロード命令に対して、ロード命令が利用するキャッシュへのインバリッドの伝達が間に合わなかった場合、そのロード命令を無効にする必要がある。

【0116】図21は、パイプラインストールの動作例である。スレッドAのEXステージの実行が失敗して、別のEX'ステージによる実行が必要になる。スレッドAの待避したパイプラインスロットには、前にパイプラインストールを起こした別のスレッドが入り込み、結果を格納する。

【0117】EX'の具体的な動作は64ビット演算や浮動小数点除算などである。演算自体は数クロックで終了し、再開待ち状態となる。スレッドEのパイプラインストールによって、スレッドEのかわりにスレッドAが入り込み、スレッドAの命令を終了させる。

【0118】パイプラインストールごとにスレッドを切り替えることによって、パイプラインを間断無く動作させることができる。ただし、パイプラインストールが発生した命令が、前にパイプラインストールが発生した命令より後である場合は、パイプラインに空きが生じる。ただしその幅は最大4クロックである。しかも、同一命令

を利用するスレッドを連続動作させる場合は、パイプラインストールを起こす命令も同一である確率が高いため、大きなペナルティにはならない。

【0119】(ディレクトリ方式階層キャッシュ)

【0120】大量の演算ユニットを搭載するには、それに対応するだけのデータ転送能力が必要になる。ところが、1つのメモリから大量のデータを供給することは不可能である。何らかの形でメモリを分散するしかない。ところが、本発明の方式では、全ての演算ユニットから全てのメモリを高速に参照する必要がある。そのために、分散したメモリの間でコピーを持つ必要がある。

【0121】分散されたメモリは、本来のメモリのコピーを自動的に格納するキャッシュの形態を取る。このとき、キャッシュ間で同じデータのコピーを持つ場合は、あるキャッシュへの書きこみを、別のキャッシュへと転送しなくてはならない。このコピー間のデータの整合性を取る機構を、キャッシュコピーレンシ機構と呼ぶ。

【0122】ところが、キャッシュの数が増大すると、キャッシュの間の転送量も増大し、配線の量、遅延時間も増大する。キャッシュ間で接続されるバス信号の数を最小限度にし、かつキャッシュ間の転送スループットを確保するために、階層型キャッシュ構造を取る。

【0123】演算ユニットには専用の一次キャッシュが接続され、複数の一次キャッシュに対して1つの二次キャッシュが接続される。遠距離の一次キャッシュへの転送に関しては、二次キャッシュを介して転送される。一次キャッシュと二次キャッシュの間のデータバスの接続はクロスバ接続であり、転送スループットを確保する。ただし、クロスバ接続の組みあわせは4つ程度に限定し、配線規模の増大を防ぐ。

【0124】本発明のプロセッサにおいては、隣接しないキャッシュ間の転送は即座には行われず、二次キャッシュにいったん格納されてから伝達される。

【0125】ここで、データの書きこみを行ったスレッド自身が同じデータを読み込む場合を考える。キャッシュ間の転送が間に合わなければ、自分自身のデータも読めないことになる。しかし、キャッシュ間の転送はスレッドの進行に間に合えば良いため、多少のレイテンシの遅れは許される。

【0126】特に、二次キャッシュ間の長距離配線、大容量の二次キャッシュは動作レイテンシが遅くなる傾向がある。ところが、二次キャッシュアクセスを長距離の演算ユニットの間の転送に用いれば、その距離の間のスレッドの進行に間に合えば良いため、キャッシュ動作レイテンシを隠蔽できる。

【0127】異なるスレッド間では、スレッド間の同期を行わない限りデータの即座な転送を保証する必要はない。同期を行う場合は後述する。

【0128】二次キャッシュは複数の一次キャッシュ、そして隣接する二次キャッシュ、三次キャッシュからの

要求をすべて受理することになる。これらの転送スループットは膨大なものとなり、同時に複数の要求を受理しなくてはならない。しかし、同時に複数の要求を完全に受理できる、マルチポートのメモリ回路は規模も大きく、速度も遅い傾向がある。

【0129】そのために、一次キャッシュは複数のロードストアユニットに接続する。逆に1つのロードストアユニットからは、複数の一次キャッシュをアドレスによって選択する。二次以上のキャッシュは複数のバンクに分割し、同様にアクセスするアドレスによってバンクを選択する。同時に同じバンクへのアクセスが重なった場合は、片方のアクセスを停止させる必要がある。ただし、本発明のプロセッサのキャッシュ間のデータ伝送は、スレッドの進行に間に合えば良いため、多少の衝突による遅れは許容される。この機構によって、確率的に多ポートのキャッシュに近いスループットを確保できる。

【0130】データのコピーを持つ別のキャッシュを特定するためには、バススヌープ方式とディレクトリ方式の2つの方法がある。バススヌープ方式は、共有の可能性のあるデータを共通のバスに出力し、全てのプロセッサが共有状態かどうかを判定する方式である。このバススヌープ方式の利点は、共有判定のための外部回路が単純であること、複数のプロセッサへの同時転送が可能であることである。欠点は、すべての外部メモリアクセスがメモリバスを占有して、全体の転送スループット性能を低下させる点と、すべてのプロセッサが自身のキャッシュをアクセスしてコピーを持つかどうかのチェックを行う必要があるという点である。市販されているスーパースカラ型マイクロプロセッサはバススヌープ方式を採用することが多い。

【0131】これに対して本発明のプロセッサは、データの転送スループットが重要であり、かつデータの転送相手を限定する必要がある。そのため、共有するプロセッサを明示的に指定するディレクトリ方式を採用する。ディレクトリ方式は、キャッシュの内部にデータの共有相手を特定するための情報を持つ。

【0132】図23にディレクトリ方式階層キャッシュのロードにおける挙動を示す。演算ユニットからのロードの場合、一次キャッシュ内部にデータがない場合に限り、二次キャッシュから一次キャッシュに向けてデータを転送し、二次キャッシュに共有状態を設定する。すでに二次キャッシュのデータが共有状態となっている場合は、ディレクトリビットの示す一次キャッシュに対して共有状態を設定する。

【0133】図24は、ディレクトリ方式階層キャッシュのストアにおける挙動である。一次キャッシュへの書きこみの際に、一次キャッシュのエントリが共有状態となっている場合は二次キャッシュに書きこみを通過する。二次キャッシュはディレクトリビットの示す共有相

手に対してのみ、直接キャッシュエントリの無効化（インバリッド）を通知する。

【0134】ディレクトリの指定により、一次キャッシュには確実にデータのコピーがあることが判明するため、一次キャッシュのタグの比較を行う必要なく、直接書き込みを行うことができる。ただし、セットアソシアティブキャッシュの場合は、ディレクトリビットは単体のキャッシュ内部のどのバンクにデータが格納されているかを指定する必要がある。

【0135】同じ命令を利用するスレッドは、たとえアクセスするアドレスが異なっても命令間のデータの流れは等しい場合が多い。レジスタの場合は明示的にプログラムで示されるが、メモリに対しても同じことが言える。特に、スタック、ヒープなどを利用する命令では、アドレスは異なっても命令間のデータの流れは等しい場合が多い。

【0136】本発明のプロセッサでは、同一スレッド内部でのキャッシュミスと極力減らすために、たとえキャッシュの共有情報がなくても、ストアされたデータを可能な限り事前にロード命令に渡す必要がある。

【0137】そのために、命令アドレスに対してデータフロー予測情報と呼ぶ情報を設ける。データフロー予測情報がマークされた命令は、ロード、ストア命令で使用したのデータを自動的に次のロード命令に伝達する。そのために、データフロー予測情報には、伝達先のキャッシュを特定する値が格納される。データフロー予測情報は、命令によって明示的に組み込むことも、自動的にプロセッサが書きこむことも可能である。

【0138】データフロー予測情報は、プログラムで明示的に記述するのが簡単だが、既存のソフトウェアとの互換性、そして条件によってデータアドレスが動的に変更される場合に対処するために、ハードウェアで自動的に設定するのが望ましい。

【0139】図19に、データフロー予測情報の書きこみ動作を示す。ロードストアユニット1907における、最初の命令実行でキャッシュミスを起こした命令は、キャッシュの共有状態からデータの実体の位置を知る。そして、データの実体のあるキャッシュ1904からデータを取得すると同時に、データの実体を持つキャッシュ1904に向けて、自分の演算ユニット1906を示す値を送る。こうして、データの実体のあるキャッシュ1904は命令キャッシュ1901にデータフロー予測情報を書きこむ。

【0140】（命令キャッシュ）

【0141】本発明のプロセッサでは、複数のスレッドが同じ命令を利用し、同じ命令は同じ演算ユニット、データキャッシュを利用するのが望ましい。そのためには、発行されたスレッドがプログラムカウンタから命令キャッシュの場所を特定し、自由にスレッドを移動させることが必要になる。

【0142】図18は、分岐によるスレッド移住の方法を示す模式図である。一次キャッシュ1803などに格納された命令は、二次キャッシュ1801に格納されたディレクトリに共有状態を設定する。命令キャッシュ1808の命令キャッシュミスか、分岐命令1806による要求によって二次キャッシュ1801にアクセスしたスレッドは、ディレクトリビットによって該当する命令が格納されている命令キャッシュ1802の位置を知り、その命令キャッシュに向けてスレッドを移住させる。

【0143】どの命令キャッシュにも命令が格納されていない場合は、スレッドの情報を動かさずに、分岐命令の直後、あるいはキャッシュミスを起こしたキャッシュ1808に対してスレッドを再発行を行う。二次キャッシュ1801あるいは外部メモリから取得した命令は、命令キャッシュ1808に格納されて、スレッドを再開する。次に同一の命令を実行する場合には、命令キャッシュ1808にすでに分岐先の命令が格納されていて、分岐のペナルティーも発生しない。

【0144】スレッド管理ユニット1807が、他の優先順位の高いスレッドが充填していて空きがない場合は、やはりスレッドの移住を行う。その場合は、スレッド管理ユニットからの通信で、スレッドの負荷の低いスレッド管理ユニット1809を探し出し、スレッドを移住させる。

【0145】この機構によって、同一命令を最大限に再利用することができる。さらに、従来のPMT方式と異なり、スレッドは命令アドレスにかかわらず、自由に演算ユニットに分配できる。

【0146】本発明のプロセッサは、厳密な分岐命令にスレッドの移住が必要であるため、分岐命令の実行の頻発を避ける必要がある。分岐はマルチスレッドによって隠蔽は可能であるが、スレッドの発行能力には上限があるためである。

【0147】そのために、命令アドレスとは無関係に命令を配置する。格納される命令の順序は、確率的に命令が実行されると予測される順序である。そして、予測された分岐方向を示す分岐予測情報をキャッシュのタグメモリに配置する。分岐予測情報は演算ユニットに送られ、分岐命令の実行結果と照合されて不一致の場合はスレッドを停止させる。

【0148】キャッシュのタグメモリに次の命令アドレスを示す値を置くことで、分岐命令の実行前に隣接する命令キャッシュから命令を取得させることもできる。この機構によって、PC相対分岐だけではなく、レジスタの示すアドレスへの分岐を予測することもできる。

【0149】同時に、前述のデータフロー同期情報も命令キャッシュのタグメモリに格納する。これによって、同じ命令を利用する限りは、すべてのスレッドから1つの分岐予測、データフロー予測情報を共有することがで

きる。

【0150】図13に、本発明の命令キャッシュにおけるタグメモリの構造を示す。命令キャッシュにはそれぞれ命令ごとに数ビットの分岐予測情報、あるいはデータフロー予測情報が格納されている。発行された命令が分岐命令の場合は、分岐予測情報として使用し、発行された命令がロードストア命令の場合は、データフロー予測情報として利用する。命令ごとの予測情報のビット幅は、実行ユニットの数から決定される。データフローユニットが目的とする実行ユニットを特定するためである。

【0151】また、分岐命令の実行とは独立して次の命令キャッシュのアドレスを特定するために、次の命令アドレスを示す値が格納されている。この値によって、条件分岐だけではなく、オブジェクト指向言語の仮想関数に代表される、レジスタ値への分岐も予測することができる。

【0152】(仮想記憶と同期)

【0153】仮想記憶ユニットは、可能であれば全ての演算ユニットから共有することが望ましい。理由は、複数のプロセスが共存する場合は、要求される仮想記憶のエントリの数も増大するためである。更に、仮想記憶ユニットが分散した場合は、その内容のほとんどが重複するためである。

【0154】本発明のプロセッサは、内蔵するキャッシュをすべて仮想空間で管理する。メモリへのアクセスの時だけ、物理アドレスに変換するためにグローバルTLBを用いる。

【0155】仮想キャッシュは、複数のプロセスが共存するために、異なるプロセス空間のキャッシュをアクセスしない機構が必要になる。そのために、キャッシュのタグメモリにはプロセスIDの情報を持たせ、キャッシュヒットの確認ごとにプロセスIDの一致確認を行う。

【0156】(データフロー同期)

【0157】一般的にマルチスレッドの同期は、あるスレッドからの書き込みをトリガにして直接別のスレッドを起動する方式がもっとも単純かつ有効である。この方式はデータフロー方式とよばれ、プログラムモデルから見てもっとも単純な方式である。プログラム上では、あるアドレスへのデータライトを自動的に感知してスレッドを再開するように設定するだけである。

【0158】この機構の実装のために、仮想記憶とデータキャッシュに特別な機構を設ける。仮想記憶には、あるアドレスのライトアクセスがあった場合にスレッドを生起する情報を書き込んでおく。そのアドレスを含むデータメモリをデータキャッシュに読み込む際に、データフロー参照がある情報も同時に取得する。

【0159】データキャッシュ側には共有ビットを書き込むだけとなる。形としては、TLBのデータフロー同期エントリとデータを共有するという形になる。これに

よって、各キャッシュエントリにはデータフロー同期情報を持たせる必要はない。前述のディレクトリ共有機構で十分であり、TLBから二次キャッシュに向けてデータフロー同期の開始を伝達する。

【0160】厳密なメモリ共有機構では、ある時点での共有メモリの状態は、どのプロセッサから見ても同じであることが要求される。ところが、この厳密なメモリ共有は、キャッシュの搭載や、メモリの階層分割によって現実には不可能になりつつある。そのため、近年ではプロセッサの仕様の方を変更し、同期命令前後のデータアクセスの順序だけを維持するように定義を変えた。プロセッサの種類によって細かい違いはあるが、基本的にはこれをルーズコンシステンシと呼ぶ。

【0161】本発明のプロセッサでは、同期命令は他の演算ユニットからのデータの書きこみを待ち、すべて到達した時点でスレッドを再開する。ところが、遠距離の演算ユニットには制御信号が即座に届かないため、同期命令までに実行されたストアかどうかの判定は厳密には不可能である。

【0162】そのために、同期命令における「同時」の定義を変更する。たとえ実時間では後に実行されたストア命令も、同期命令の再開までに伝達が間に合った場合には時勢的に前だとみなす。

【0163】そして、同期とは、PMTパイプラインを一周回分待ち合わせて、他のスレッドの、「同時」の時間以前に実行された全てのストアを受理するまで待つこととする。これによって、単体のスレッドの場合と同じく、全てのスレッドのデータ転送はスレッドの移動に間に合えば良い。パイプラインが一周した時点でスレッドを再開させるが、その時点では同期命令「以前」の全てのストアは実行され、再開地点以降のデータキャッシュに格納されている。

【0164】この方法によって、全てのスレッドにわたって、同期変数の前後のメモリアccessの順序を保持することができる。なおかつ、同期中に他のスレッドの動作が可能になり、性能へのペナルティーも隠蔽できる。

【0165】図25に本発明のプロセッサにおける同期の動作を示す。スレッドBからのStore Aは、スレッドAのLoad Aで読み込むことが出来る。スレッドAのSYNC命令より実時間的には後に実行されているにもかかわらず、SYNC命令の再開までにキャッシュの伝達が終了しているためである。仮想時間的に前かどうかの判断基準は、前のSYNC命令のパイプラインの到達よりも早いかどうかで決定すれば十分である。こうして、複数のSYNC命令間で、SYNC命令前後のデータ格納順序を保つことができる。

【0166】さらに、従来のプロセッサと異なり、SYNC命令で他のスレッドを止める必要はなく、SYNC命令の伝達もスレッドと同じ速度で伝達すれば十分である。

【0167】図26に、ソフトウェアモデルから見た同期の動作について示す。スレッドAのSYNC命令の前に実行されたスレッドBのStoreAは、仮想時間では前に実行されたSYNC命令のさらに前に行われているため、スレッドAから読み込むことができる。

【0168】スレッド間の同期は、同期変数へのアクセスに対して、明示的にOSのソフトウェアによるスケジューラを起動して管理することが多い。しかし、前述のデータフロー同期機構を自動的に利用すれば最も高速である。

【0169】具体的には、あるデータをロードする同期命令の実行によって、データフロー同期ユニットにそのスレッドの状態とロードアドレスを転送する。スレッドはその時点でスリープする。データのストアはデータフロー同期ユニットとディレクトリ方式キャッシュコヒーレンシによって判定されて、待ち状態のスレッドを直接起こすことができる。

【0170】(パケット制御信号)

【0171】既存のスーパースカラ、VLIW方式に代表される命令レベル方式では、信号は可能な限り速く伝達することを要求される。ところが、回路規模が大きくなるとそれは現実的には不可能になる。理由は主に3つある。まず、微細化が進むと、配線遅延の比率が大きくなる。さらに回路規模が大きくなると、回路間の配線が爆発的に増大する。さらに、周波数が高くなると、隣接する配線間のクロストークやグラウンドバウンスが問題となる。前者の対処としては、配線を短縮するか、配線間の距離を大きくとりシールドする必要が出てくる。後者の対処には、電源配線を配線に対して最適化して、電流ループの大きさを最小限にする必要がある。

【0172】それに対して、PMT方式は、隣接するユニットを除き、制御信号の伝達は多少の遅れが許される。ということは、長距離の信号伝達に使用される信号線を、複数の信号が共有することができる。こうして、長距離の配線の本数を最小限にする。

【0173】更に、長距離の配線は一気に送ってしまうのではなく、中継する回路で受け止めてシフトレジスタ的に順に送ることができる。こうして、1クロックの間で伝送するのはルーター間の距離だけで済み、制御信号が動作周波数の向上を阻害することは無くなる。中継のためのルーターやラッチの規模が大きくなるという欠点はあるが、それは半導体のプロセスの向上の恩恵をそのまま受けることが出来て、相対的な影響は少なくなる。

【0174】個々の配線を最小限の長さにして、信号伝達の多少の遅れを許容することにより、その配線のドライブを行うトランジスタの駆動電流を不必要に上げる必要がなくなり、信号の高周波成分の増加を抑制することができる。これはクロストークやグラウンドバウンスなどの抑制につながり、これらの対策に必要な回路の増加を防ぐこともできる。

【0175】遅延時間に関しては、PMT方式の隣接ユニット以外の転送レイテンシを許容する特性によって問題にならなくなる。こうして、並列度を維持し、回路規模を最小限に維持しながら周波数性能の向上を可能にする。

【0176】パケット制御信号は、データ転送などの目的ではアドレス、データとともに送られる。すなわち、アドレス、データを転送するパケットは、アドレスバス、データバスの空きをスレッドバッファで待ち合わせることになる。これによって、各バスのアービトレーションはパケットルーターが一括して処理することができる。

【0177】本発明のプロセッサは、命令キャッシュ、演算ユニット、外部インターフェースなどのユニットごとにパケットルーターを随所に配置し、遠距離の制御信号の伝達の中継を行う。パケットルーターには、複数のパケットルーターと送受信を行うためのバスを持ち、必要に応じてデータバスなどの補助的なバスを並行して設ける。

【0178】個々のパケットルーターは一意的番号を割り振られる。番号はスレッドの進行方向にあわせて昇順に割り振られ、付随するバス信号、伝達先のユニットによって一意にルーティングの方法も決定される。

【0179】このパケット制御信号によって、隣接するユニットを除く全てのユニットへの制御が行われる。

【0180】本発明のプロセッサにおけるパケットは、到達予定時間の情報をパケット情報に含む。この時間とパケットルーターの持つタイミングカウンタを照合することにより、パケットが予定通り伝達されているかどうかを判定する。

【0181】パケットが遅滞している場合は、並行して走るスレッドに対して即座にパイプラインストールを要求して、スレッドを止める。パケット遅延の例外処理を発行して、OSレベルのソフトウェアが対処を行ってスレッドを再開させる。

【0182】本発明のプロセッサは、各ユニットの内部状態を全ての演算ユニットから監視、改変することを可能にする。そのために、演算ユニットからの要求をパケットに変換し、パケットルーターを利用して順次伝達する。伝達先のユニットは、内部状態を含んだパケットを送信元の演算ユニットに伝送する。なお、ロードのためのレイテンシは無論マルチスレッドで隠蔽される。

【0183】(プロセッサ間通信)

【0184】本発明のプロセッサを複数利用する際に、本発明の内部の演算ユニットと同じように、プロセッサをリング状に連結すれば、プロセッサ間転送ルーブットを最大にすることができる。これによって、1つのスレッドは複数のプロセッサにわたって展開することができ、命令、データ共有の利点を最大限に生かすことができる。

【0185】だが、本発明のプロセッサの内部と同じく、データの転送にはパイプラインの隣接転送だけではなく遠距離の転送も考えられる。リング方式転送の欠点は遠距離に伝送するのが難しいという点である。そのため、遠距離の演算ユニット間同士でショートカットバスで伝送することは、全体の転送速度を大きく向上させる。

【0186】このような転送はレイテンシ時間が増大するものであるが、複数のプロセッサ間での通信はそれらの間のパイプライン全てを通過する時間で行われれば良いため、数十クロック以上のレイテンシが許される。このため、プロセッサ外の低速インターフェースには最適である。

【0187】本発明のプロセッサでは制御信号をパケット化しているため、同じ制御信号を複数のプロセッサに分配できる。ユニットを指定するための識別コードを拡張し、全てのプロセッサを一意に表現することで、マルチプロセッサに向けて自由に制御信号パケットを伝送できる。

【0188】本発明のプロセッサを複数利用する際には、個々のプロセッサに個別にメモリを接続する。各プロセッサがデータの実体の場所を特定するために、個々のプロセッサが持つ仮想記憶を利用する。この場合、仮想記憶のエントリはそれぞれコピーを持つことになり、キャッシュと同じ共有管理を行うことになる。そのため、仮想記憶には共有状態を示すビットを設ける。ただし、オリジナルは常にメモリに接続された仮想記憶となる。

【0189】仮想記憶の改変の際には、キャッシュのフラッシュと同時に、他の仮想記憶に改変を直接伝達する。改変を伝達された仮想記憶は、共有状態に応じてそれぞれキャッシュのフラッシュを実行する。

【0190】本発明のプロセッサ同士で、データの共有がある場合は、仮想記憶のページ単位でデータの共有情報を設定する。キャッシュラインごとのビットを持つことができないため、ページ全体が共有状態の場合はその都度内部キャッシュのタグにアクセスして確認する必要がある。

【0191】まず、プロセッサから外部にロードストア要求を行うケースについて述べる。まず、ロード命令では、キャッシュにエントリがない場合、あるいはTLBに対して共有状態が指定されている場合は、TLBを介してプロセッサ外部からデータを取得する。TLBにアクセスを行い、ローカルメモリではなく外部のメモリとデータを共有している場合は、プロセッサ外部にリード要求を出す。

【0192】ストア命令では、二次キャッシュにTLBへの共有状態が設定されていることにより、TLBへのアクセスを行う。共有状態に設定されている場合は、データのコピーの無効化(インバリッド)を伝達する。

【0193】次に、プロセッサ外部からロード要求を受理した場合について述べる。受理した仮想アドレスに対して内部のTLBへのアクセスを行う。内部キャッシュで共有状態に設定されている場合は、内部のキャッシュに仮想アドレスでアクセスして、プロセッサ外部にデータを伝達する。

【0194】次に、プロセッサ外部からインバリッド要求を受理した場合も、同様に受理した仮想アドレスに対して内部のTLBへのアクセスを行う。内部キャッシュで共有状態に設定されている場合は、内部のキャッシュに仮想アドレスでアクセスして、内部キャッシュにインバリッドを伝達する。

【0195】なお、TLBのエントリがない場合は、OSによる仮想記憶処理を行う。

【実施例】

【0196】(第一実施例)

【0197】図1に、本発明の第一実施例を示す。101は本発明のプロセッサである。

【0198】命令発行ユニット102は、スレッド発行ユニット103、命令キャッシュ104を内蔵する。スレッド発行ユニット103は、命令キャッシュ104にプログラムポインタ値を伝達して、実行ユニット105に実行すべき命令を伝達する。

【0199】実行ユニット105は、4つの共有レジスタファイル106と、4つの16ビット演算ユニット107と、複数の特殊演算ユニット108から構成される。共有レジスタファイル106と16ビット演算ユニット107、および特殊演算ユニット108は、オペランドクロスバスで相互に接続されている。スレッドのレジスタ値などの状態は全て、隣接する実行ユニット105に伝送される。ただし、従来のPMT方式と異なり、1つのスレッドの状態は4クロックで転送される。末端に到達した状態は、スレッド状態信号132によって最初の実行ユニットに伝送される。実行ユニットからのスレッド生成、分岐発行は、分岐発行制御信号109、134によってスレッド発行ユニット103に伝達される。

【0200】一次データキャッシュ111は8つ搭載され、そのうちの4つが1つの実行ユニット105に接続されている。接続にはクロスバスが使用され、同時に4つの一次データキャッシュへの任意のアクセスを可能にしている。ただし、同じデータキャッシュへの複数のアクセスがかち合った場合には、1つのアクセスだけを行い、他のアクセスを行ったスレッドをストールさせる。なお、従来のPMT方式と異なり、4つの一次キャッシュはアドレス値によって特定でき、1つのスレッドからすべてのバンクに自由にアクセスできる。

【0201】4つの一次データキャッシュ111~114は、1つのアクセスバッファ115に接続され、隣接するライトバッファと、やはり隣接する二次キャッシュ

116へのデータのやり取りを行う。

【0202】二次キャッシュ116は、2つの一次キャッシュからのアクセスバッファ115、131と、TLBなどのに接続されたアクセスバッファ117から要求を受理する。二次キャッシュユニット116は一次キャッシュと異なり、命令もデータも格納する。そして、二次キャッシュも複数の要求を受理するために複数のバンクに分けられてる。

【0203】アクセスバッファ117は、二次キャッシュ116からの要求によって外部とのアクセスを行う際に、データのバッファリングを行う。

【0204】新規スレッド発行ユニット127は、割り込み信号126の入力に応じて、内部に蓄積した待機状態のスレッドを発行する。あるいは、実行ユニット105からの直接のスレッド生成要求によってスレッドを発行する。そのために、スレッド発行ユニット127は、スレッド発行ユニット103に向けてスレッド発行制御信号133を出力する。

【0205】グローバルTLB120は、仮想アドレス信号の物理アドレスに変換し、物理アドレスをローカルメモリアンターフェース122に伝送する。外部バスは基本的には仮想アドレスであることに注意。

【0206】ローカルメモリアンターフェース122は、グローバルTLB120からの要求に応じて、ローカルメモリバス信号123を通じて外部メモリとのデータアクセスを行う。I/Oもローカルメモリアンターフェース122によってアクセスできる。

【0207】共有バスインターフェース124は、共有バス信号125を通じて他のプロセッサに対してデータを送受信する。共有バス信号125から受理されたローカルメモリアクセス要求に対して、グローバルTLB120でプロセッサ内部でデータを共有しているかどうかの判定を行う。

【0208】(第二実施例)

【0209】図5に、本発明の第二の実施例の模式図を示す。

【0210】501は本発明の第二の実施例のプロセッサである。命令発行ユニット102と、実行ユニット105と、4つの一次キャッシュ111、二次キャッシュ116は隣接して配置される。この組が全体に8つ配置されることで、この第二実施例のプロセッサは32のスレッドを同時に動作させることができる。本発明のプロセッサには、ユニットの搭載数に上限はない。

【0211】この第二実施例の個々のユニットは、本発明の第一の実施例に搭載されているユニットとほとんど共通であり、ユニットの組み合わせがだけが異なる。

【0212】前段プロセッサ接続インターフェース502は、別のプロセッサからのデータ転送を受理する。実アドレスで要求されたアクセスを、TLB120を用いて内部のキャッシュ、ローカルメモリで共有されている

かどうかを判定する。

【0213】IPユニット504はソフトウェアよりもハードウェアの方が効率が良い処理を行うためのユニットである。これらはそれぞれ演算ユニットの近傍に配置される。演算ユニットはIPユニットの出力データをソフトウェアで即座に整形するため、IPとプロセッサ間の転送が最小限になる。

【0214】2つのローカルメモリアンターフェース122は、二次キャッシュからのメモリアクセス要求を受理して同時にメモリとのアクセスを行う。アクセスの前にはグローバルTLB120を利用して物理アドレスへの変換を行う。

【0215】I/Oバスインターフェース510はプロセッサに直接接続されたローカルなI/Oへのインターフェースである。

【0216】新規スレッド発行ユニット127は、スレッド発行命令の要求に応じてスレッド発行を行うとともに、割り込み信号126、ソフトウェア例外などの要求に応じて休眠状態のスレッドを生起する。

【0217】この実施例のプロセッサは、通常のマルチスレッドプログラムを利用して、浮動小数点命令を含めて32並列動作を可能にしながら、規模的には単一プロセッサの8倍強の素子数で実現できる。個々のキャッシュは小容量だが、全てのキャッシュの内容を全てのスレッドから共有することができるので、個々のスレッドが1つの高速大容量キャッシュを持つのに等しい。

【0218】(命令発行ユニット)

【0219】図6は、命令発行ユニット102の内部構造の模式図である。

【0220】パケットルーター601は、スレッドを制御する制御パケット信号603を受理し、このスレッド発行ユニットで受理可能であるかを判定する。

【0221】制御パケット信号の内容がスレッドの受理の場合は、プライオリティー選択ユニット604に制御信号を伝達する。制御信号の内容がキャッシュの直接制御の場合は命令キャッシュ制御ユニット605に制御信号を伝達する。制御信号の内容がローカルTLB制御の場合は、命令ローカルTLBユニット607に制御信号を伝達する。さらに、スレッド移住の要求である場合は、スレッド移住ユニット620に制御信号を伝達する。

【0222】待ち状態スレッドが一杯などの理由でパケット制御を受理できない場合は、別の隣接するパケットルーターに、制御パケット信号619を通じて伝送する。

【0223】プライオリティー選択ユニット604は、待ち状態スレッドバッファ618の中から、実行可能状態でかつ最もプライオリティー値の高いスレッドを1つ選択する。ただし、キャッシュミスなどで実行できない状態のスレッドは選択されない。このプライオリティー

選択ユニット604は、待ち状態のスレッドの数に対して爆発的に規模を増大させるため、待ち状態スレッドバッファ618の数を増やしすぎないことが求められる。そのために、パケットルータ602では、待ち状態のスレッドを1つのスレッド発行ユニットに集中させない制御が行われる。

【0224】本実施例では、命令キャッシュだけは物理空間キャッシュとする。異なるプロセス空間に属する命令を共有するためである。命令キャッシュはキャッシュ制御ユニット605、キャッシュタグメモリ606、命令TLB607、キャッシュデータメモリ608で構成される。

【0225】キャッシュ制御ユニット605は、スレッドごとの命令キャッシュアクセスを実行し、パケットルータ602を介して要求される命令キャッシュへの直接アクセスを実行する。さらに、パケットルータ602からのグローバルTLBの改変によるTLB607のエントリの無効化も行うことができる。

【0226】キャッシュタグメモリ606には、全ての物理アドレスが格納され、さらに、分岐予測、データフロー予測情報が格納される。

【0227】スレッド状態制御ユニット609は、キャッシュのヒットチェックを行う。命令TLB607によって変換された物理アドレスと、命令キャッシュタグ606の結果が一致すれば、キャッシュはヒットしたことになる。その場合は、4つ分の命令を命令メモリ616から取得して命令順序アライナ614に伝達して実行可能な状態にしておく。

【0228】スレッド状態制御ユニット609は、前の命令発行ユニットの出したスレッド状態信号608を受理する。前のスレッドよりも待ち状態のプライオリティが高い場合は、無条件でスレッドを発行する。前のスレッドがない場合は、前に実行した命令と同じ命令を使うスレッドが待機状態であれば、待機状態のスレッドを優先して発行する。命令アドレスが一致しない場合は、キャッシュから取得しておいた命令を発行する。発行したスレッドの状態は、隣接する命令発行ユニットにスレッド状態信号615で伝達される。

【0229】命令順序アライナ614は、蓄積された4つのスレッドのそれぞれ4つの命令を、1クロックづつずらして出力する。命令の種類によって配置を変えるようなことはしない。

【0230】スレッド状態制御ユニット609は、内部に格納された現在のスレッドのPCと、新規に発行されるスレッドのPCを比較し、一致するようならば、命令順序アライナ614に蓄積された命令の再利用を要求する。こうして、スレッドは同一の優先順位である限り、同じ命令を使用するものが優先的に実行される。

【0231】スレッド移住制御ユニット620は、演算ユニットで発生した分岐、スレッド発行を示す分岐要求

信号613を受理する。自身の命令キャッシュに格納されていない場合は、パケットルータ602からキャッシュの要求を行う。他に命令をすでにキャッシュした命令発行ユニットがあれば、スレッドの移住を行うためにスレッド状態をパケットルータ602に伝送する。

【0232】命令バス信号617には、二次キャッシュ116からリプレースされる命令が送られる。取得した命令は、命令キャッシュのデータメモリ616に格納される。取得した命令は、スレッドが空き次第即座に発行される。

【0233】命令メモリは、命令アドレスと独立した命令を順に格納することができる。そのため、予測された分岐先を含めた命令の動作順に格納される。この機構を実現するために、命令キャッシュタグメモリ606はすべてのアドレスビットを含み、キャッシュヒット時にすべてのアドレスの比較を行う。

【0234】この機構を使用すると、同じ命令を使用し、同じ分岐方向を採択するスレッドは、命令キャッシュに常にヒットすることになり、命令リプレース時間だけでなく、分岐ペナルティ時間すら削減することができる。この機構は、同一の動作をする大量のスレッドで最大の効果を発揮する。

【0235】なお、この分岐予測が的中したかどうかを確認するために、命令TAGメモリには予想される分岐方向のビットを持たせる。レジスタ内容への分岐については命令キャッシュタグメモリ606から発行された次の命令アドレスを使用する。命令キャッシュのインデックスは、直前の命令キャッシュのインデックス値を常に使用する。インデックス値の算出は、スレッド発行時、命令キャッシュミスヒット時のみ行われる。

【0236】同一の構造のスレッドでは、スレッド内部で同じ命令間でデータの受け渡しが行われる場合が多い。ただし、すべてのスレッドで同じアドレスを利用してデータを受け渡す場合もあれば、レジスタに対する相対アドレスを使用する場合もある。スタック、ヒープを用いる一般的な場合では、むしろ後者が多い。そのような場合では、データキャッシュ間の転送が必要になる。

【0237】そのために、命令間でデータの授受があるという予測ビットを設ける。データフロー予測ビットは、その命令が書き込んだデータアドレスを、自動的に別のラインに送ることを可能にする。

【0238】データフロー予測ビットには、バリッドビットとともに、送り先の演算ユニットを示す「ライン番号」を格納しておく。データのアドレスではないことに注意する。

【0239】データキャッシュミスで、データの実体を検索する際にやってきたパケットは、一次データキャッシュのヒットを検出することで、一次データキャッシュに隣接する命令キャッシュに向かってデータフロー予測ビットを書き込んでいく。そのために、データキャッシ

ュミスパケットには、データキャッシュミスの発生した演算ユニットの識別番号が伝達される。

【0240】なお、1つのライト命令に対して、複数のリード命令が同じデータを参照する場合は、リード命令同士の転送となる。そのために、データフロー予測ビットはロード命令にも必要になる。

【0241】分岐命令とロードストア命令は同時に利用されないため、データフロー予測ビットと分岐予測ビットは共用され、命令デコード結果によって使い分けられる。

【0242】スレッド間で共有するデータが多い場合は、PMT方式が優れる。それに対して、自身のスレッド内部の転送量が大きく、スレッド間で共有するデータが少ない場合は、SMP方式が優れる。これらの双方の長所を取り入れるために、SMP実行モードを設ける。

【0243】SMP実行モードは隣接する命令発行ユニット102の負荷が高く、データキャッシュのトランザクションの負荷が高い場合に、同じスレッド発行ユニットで連続して1つのスレッドを管理するモードである。本発明の実施例では、1つのスレッド発行ユニットで4つのスレッドを動作できる。

【0244】SMP実行モードでは、スレッド状態を隣接する命令発行ユニット102に伝達せず、次のPCアドレスを自身のキャッシュ制御ユニット605で利用する。キャッシュ制御ユニット605は、キャッシュから4命令を取得して、命令順序アライナ614に送る。

【0245】他の演算ユニット、キャッシュとのキャッシュコヒーレンシや同期は、PMTモードと同じ階層キャッシュコヒーレンシ機構を用いて行われる。すなわち、本発明のプロセッサは、SMPモードでは階層キャッシュの共有メモリマルチプロセッサそのものとして機能する。

【0246】(演算ユニット)

【0247】図7は、4並列実行ユニット105の内部構造を示す模式図である。

【0248】命令デコードユニット703は、命令発行ユニットから送られた命令727をデコードし、各演算ユニットを制御する。同時に、4つのプログラムカウンタをインクリメントする。分岐命令が実行された場合は、演算ユニットで算出された分岐後のプログラムカウンタを利用する。更新されたプログラムカウンタは、隣接する命令デコードユニットに伝達される。

【0249】双方の実施例では、実行ユニット内部には、レジスタファイル704を4つ搭載している。1つのレジスタファイルは4つの演算ユニットで共有される。そして同時に1つの演算ユニットに対してのみレジスタを供給する。

【0250】レジスタファイル704は、コンテキストスイッチに対応するために4つのバンクを持つ。そして、レジスタファイル704は、隣接レジスタ転送を4

クロックで完了する。そのため、一般的なRISCプロセッサと同じ3つのリードポートと、隣接転送用の2つのレジスタリードライトの機能を持つ。現在実行中のスレッドが3つのリードポートを利用している間、さらに2つのレジスタを出力し、隣接する4並列実行ユニット105に転送する。そして、隣接する4並列実行ユニット105内部の、レジスタファイル704のうちの利用されていないバンクが、2つのレジスタの値を受け取って書きこむ。

【0251】こうして、レジスタファイル704は、現行のスーパーカラプロセッサよりも少ないポート数で実現でき、アクセスのための遅延時間を増加させないで済む。

【0252】オペランドクロスバスイッチ706は、4つのレジスタファイル704の値を、それぞれの演算ユニットに分配する。3つのオペランドを持つレジスタを4組分配する。受領する演算ユニット側には4入力のセレクタが3つ配置される。

【0253】演算ユニットで算出された演算結果は、即座にレジスタファイル704に伝達することはない。演算結果フォワーディング717を利用して結果を利用する演算ユニットに伝達する。そして、レジスタファイル704への書き戻しは、オペランドショートカット信号722によって隣接する演算ユニット105のレジスタファイルに伝達される。

【0254】整数演算ユニット708は、フラグ判定、16ビットの範囲内での算術、シフト演算、分岐アドレス生成などを行う。4並列実行ユニット105内部に4つ配置され、それぞれが独自にスレッドの命令実行を行う。

【0255】この整数演算ユニットは16ビット程度の加算器、シフタ、そして16ビットを超えた演算が行われたことを感知する回路で構成される。これは演算ラインごとに実装される。

【0256】16ビットを超える桁の変更が発生する演算は、パイプラインをストールして、共有64ビット演算ユニット710を利用して再計算を行う。64ビット演算ユニットは16ビットの4倍以上の回路が必要になるため、16ビット演算ユニットとオーバーフロー検出回路の組み合わせを利用し、それを4つ搭載して代用しても全体の演算ユニット数、回路規模あたりの性能を増やすことができる。

【0257】この方法が全体の性能をかえって向上させることができるのは、本発明の方式がマルチスレッドによって十分な並列処理を行うことができるという前提による。VLW方式などの命令レベル並列では、並列動作可能な命令が並列度より少ない場合が多く、このようなペナルティは絶対に許されない。

【0258】分岐ユニット721は分岐予測の判定と、分岐の発行、およびスレッドの発行制御を行う。ただ

し、分岐アドレスを算出するのは整数演算ユニット718による。実際分岐は4命令に1回程度の頻度で実行される傾向が強いので、4つのスレッドで共有される。

【0259】分岐ユニット721は、分岐予測情報との照合を行い、一致した場合は自身のアドレス情報だけを更新する。分岐予測非成立の場合は、スレッド発行ユニットに分岐要求を伝達すると同時に、別の待ち状態のスレッドに切り替える。コンテキストスイッチは即座に行われ、実行ユニットの待ち時間はない。

【0260】基本的に、分岐後の処理は直後の実行ユニットで実行される。分岐予測が的中する場合は、自動的に分岐後の命令が次の実行ユニットに伝送される。

【0261】ただし、キャッシュミスの場合は、キャッシュの共有状態を確認することで、すでに命令が格納されている実行ユニットを検索する。発見された場合は、その実行ユニットにスレッドを移住させる。基本的にスレッドの移住には全てのレジスタファイルの転送が必要となる。ただし、データのほうはデータキャッシュコヒーレンシ機構が自動的に働くので必要はない。

【0262】関数からのリターンの場合は、スレッドを呼び出し元の実行ユニットに移住させる。ただし、渡すレジスタは1つの返り値のみである。スタックの退避、復帰は自動的に行われるので転送は必要ない。

【0263】SMPモードは、直後の演算ユニットで待ちあわせているスレッドのプライオリティーが高く、さらに後続のスレッドの負荷が低い場合に発生する。空いた演算ユニットを有効に利用するための手段である。

【0264】レジスタ同期ユニット723は、レジスタ内容の隣接ユニットへの転送と、スレッドの移住のためのメモリへの自動読み書きを行う。

【0265】スレッドの移住は、1つのバンクのレジスタの内容をそっくり他のスレッドに入れ替える作業である。実施例1のプロセッサにおいて、スレッド移住には合計4クロックを要する。

【0266】スレッドの移住には、メモリを介してレジスタの値を伝達する。スタックポインタから利用すべきメモリアドレスを演算ユニット708で算出し、現在のレジスタをロードストアユニット713に送る。新規のスレッドに対しても、スタックポインタからアドレスを算出し、ロードストアユニット713から新規のレジスタセットを読み込む。レジスタ退避の際には、ロードストアユニット713のアドレスバスもデータ転送に利用する。同時に4つのスレッド移住を行うため、8つのレジスタを同時に転送する能力を有する。

【0267】浮動小数点加算ユニット719、浮動小数点乗算ユニット712は、整数演算ユニットと異なり、精度が常に一定であり、動作が細かく決定されているので、倍精度の演算ユニットの機能のすべてを実装する必要がある。ただし、浮動小数点命令の出現頻度を考慮して、1つの実行ユニット108ごとに、浮動小数点加算

ユニット719と、乗算と加算を同時に行う浮動小数点乗算ユニット712が1つずつ配置される。

【0268】なお、これらのレイテンシの長い演算は、複数のスレッドが同時に利用する。演算中は、これらの共有演算ユニットの内部にスレッドの情報が格納され、結果の値とともに整数演算ユニットに伝達される。

【0269】除算ユニット718は、除算、平方根などの、時間のかかり、かつ出現頻度の低い浮動小数点演算を行う。除算、平方根の演算は乗算と異なり、現実的な規模でパイプライン化して高速化する手段はない。そのため、1つの演算あたり数クロックのスループット時間が必要になる。そして、1つの除算ユニット718は、除算命令の出現頻度を考慮して、4つのスレッドで共有される。

【0270】ロードストアユニット713は、4つのロードストア命令の実行を同時に行い、8ワード分の転送能力を持つ。4つの演算ユニット705からの要求を受理してロードストアを行うとともに、待ち状態のスレッドのロードを実行する機能を持つ。

【0271】バイト単位の転送をワードに符号に応じて拡張する操作、あるいはその逆もこのユニットで行われる。

【0272】ロードストアユニット713には、4つのデータキャッシュが接続され、アクセスを行うアドレスによって使い分ける。データのアクセスは、同時に複数のユニットのアクセスを可能にする。そのために、4つのアドレス、データバスを互いにクロスバ接続する。

【0273】同じ一次キャッシュへのアクセスが重なった場合は、優先度の低いスレッドを停止して、ロードの実行を待つ。キャッシュミスの場合も同様である。

【0274】ロードの衝突、キャッシュミスによるスレッドの停止の場合には、停止したスレッドの代わりに、前に停止してロードの終了したスレッドを再開する。

【0275】なお、前にロード、あるいはストアしたデータと、同じアドレスを利用するロード命令が直後に存在する場合は、データキャッシュへのアクセスを行わずに、同じデータを渡す。通常のプロセッサのライトバッファと異なり、渡す対象は同一スレッドでなくても良い。この機構によって、同一の命令を利用するスレッドの連続動作させる際のデータキャッシュアクセスが最小限となる。

【0276】演算結果フォワーディングユニット717は、実行ユニット105内部の演算ユニット間のデータの受け渡しを行う。同時に、長時間演算ユニットを利用する必要のある命令では、隣接する実行ユニット105に途中経過のレジスタ値を渡す。この機構によって、除算などの時間のかかる命令をパイプライン動作させることができる。同一の除算などの命令を利用するスレッドが連続する場合のスループット性能を高めるためである。

【0277】(データキャッシュユニット)

【0278】本発明のプロセッサは、データキャッシュのスループット確保、遠距離の一次キャッシュ間の転送のために、階層キャッシュ構造を取る。さらに、スレッド間の仮想記憶機構の共有のために、データキャッシュは基本的に仮想アドレスとしている。

【0279】データキャッシュは大きなスループットを要求されるため、擬似的に複数の要求を受理する構造とする。そして、キャッシュ内部のデータの共有管理のために、ディレトリ方式キャッシュコヒーレンスを採用する。ディレトリ方式はデータアクセスのレイテンシに劣るが、複数のキャッシュの要求に対応しやすい方式である。ディレトリ方式の詳細については、文献1のP679からの記載を参照のこと。

【0280】文献1: Computer Architecture a Quantitative Approach Second Edition
著者: John L. Hennessy, David A. Patterson

出版社: Morgan Kaufmann Publishers, Inc.

【0281】図8に、本発明の第一の実施例における一次データキャッシュ111、二次キャッシュ116の接続関係模式図を示す。

【0282】4並列実行ユニット105には、一次データキャッシュ111が4つ接続される。4つの一次データキャッシュ111は、すべてが1つの二次キャッシュ116に接続される。なお、二次キャッシュはデータ、命令の双方を格納する。

【0283】803は一次データキャッシュのタグである。806は、二次キャッシュのタグである。

【0284】データキャッシュは仮想アドレス空間を利用し、複数のプロセスが混在するため、異なったプロセス空間のエントリが混在する。そのため、タグメモリ内部にはプロセス空間のIDが配置され、一致比較の時にアドレスとともに比較される。さらに、タグメモリ内部には共有先を特定する共有ビットを有する。

【0285】一次データキャッシュ111、二次キャッシュ116は、アドレスの下位で分割したバンクを持ち、隣接する転送は同時に、そして、連続するアドレスは複数のキャッシュバンクが同時にアクセスさせることを可能にする。二次キャッシュタグメモリ806、二次キャッシュデータメモリバンク807も、アドレスに対して分割され、複数のアクセスを同時に受理する。

【0286】データキャッシュ制御ユニット802は、キャッシュミスの場合に適切なキャッシュからデータを要求する。さらに、データ転送の要求に応じて、適切なキャッシュにデータを転送する。さらに、内部のキャッシュの共有状態を管理する。

【0287】実行ユニット105が一次データキャッシ

ュ111への読み込みを行うケースについて説明する。一次キャッシュデータメモリ804からデータを読み込むと同時に、一次キャッシュタグメモリ803に対してアクセスを行う。一般的なキャッシュと同じく、タグメモリの読み出し内容が要求されたアドレスと一致しない場合、あるいはそのエントリが無効となっている場合、データキャッシュミスとする。その場合、スレッドに対してストールを要求し、二次キャッシュ116からデータを要求する。

【0288】実行ユニット105が一次データキャッシュ111への書き込みを行うケースについては、まず一次キャッシュタグメモリ803だけに対してアクセスを行う。アドレスが一致してかつ、該当するデータが共有状態に指定されている場合は、二次キャッシュ116に対してインバリッド要求を発行する。

【0289】一次データキャッシュタグ803には、2ビットの共有情報を含む。隣接する一次キャッシュへの共有状態と、それ以外のキャッシュとの共有状態である。

【0290】アクセスバッファ115は、一次データキャッシュ111から二次キャッシュ116へのアクセスが不可能である場合に、アクセス情報およびスレッドの情報を蓄積する。あるいは、二次キャッシュ116から一次キャッシュ111へのインバリッド伝達の蓄積にも用いられる。

【0291】アクセスバッファ115は、一次キャッシュ111からの隣接転送要求を受理し、二次キャッシュ116を通さずに隣接するアクセスバッファ131にデータを送信することも行う。

【0292】同時に、アクセスバッファ117からデータを受理して、二次キャッシュ116内部の共有状態を調べる。共有状態であれば、データを格納するか、該当する一次キャッシュ111に伝送する。

【0293】二次キャッシュ116は、一次キャッシュ111からのキャッシュアクセスを受理するとともに、隣接する二次キャッシュ、さらにメモリインターフェース、あるいは実施例には存在しないが三次キャッシュからの要求を受け、適切な相手にアクセス要求等を送出する。

【0294】なお、本発明のプロセッサでは、データの転送やインバリッドの伝達は、スレッドの伝送速度に間に合えば十分である。SMP方式と異なり、階層バス間の転送レイテンシは演算ユニットの稼働率とはほとんど関係がない。そして、インバリッド伝達の方も常に一定であり、転送スループットの確保も可能になる。

【0295】図14に、本発明のキャッシュにおけるタグメモリの構造を示す。一次キャッシュ111、二次キャッシュ116はともに仮想空間であるため、タグアドレスの一致比較だけでは不十分であり、プロセスIDの一致の判定が必要である。

【0296】ディレクトリ方式キャッシュの実装のために、共有状態を示すビットを設ける。一次キャッシュは、隣接する一次キャッシュと、二次キャッシュの2つの転送先が考えられるため、2ビットの共有情報を利用する。

【0297】二次キャッシュタグ806には、6ビットの共有情報を含む。隣接する二次キャッシュへの共有状態と、4つの一次キャッシュへの共有状態4ビットと、三次キャッシュ、TLBユニットなどへの共有状態1ビットで構成される。

【0298】(仮想記憶機構)

【0299】仮想記憶機構は、内部表記のアドレス表記を実際のメモリアドレスに対応させ、内部表記のアドレス以上の実メモリ空間を扱うことを可能にする。また、複数のプロセス空間の間の保護、およびメモリに存在しないメモリ空間の判定を行う。この仮想記憶の変換を効率的に行うためのバッファが、TLBユニット120である。

【0300】本発明の方式では、この仮想記憶機構にも以下の特徴がある。

【0301】(1) TLBは演算ユニットのある一定の集団ごとにそれぞれ専属のものを置く。

【0302】(2) キャッシュは仮想アドレスとし、実際のメモリアドレスの直前まで仮想空間の変換を行わない。

【0303】(3) TLBの改変は、キャッシュにコピーがあるにもかかわらず、TLBエントリのない状態を作り出す可能性がある。

【0304】(4) スレッド間的高速同期のための、データフロー同期の機構を提供する。

【0305】複数のTLBを所持する場合は、TLB間で互いにコピーを持たせることになる。だが、オリジナルのエントリは常にメモリバンクに専属の1つとする。そのため、TLBの改変の際は、常にメモリバンクに専属のTLBに対して行う。オーナーであるTLBは、共有しているすべてのTLBに向かってページの無効化(インバリッド)を伝達する。

【0306】図9に、本発明の実施例におけるTLBユニット120の内部構造の模式図を示す。

【0307】仮想アドレス902は、TLBタグメモリ903、TLBデータメモリ909に入力される。構造的にはセットアソシアティブのキャッシュと同じである。TLBタグメモリ903は仮想アドレス902の内容と比較器904で比較され、一致した場合のみTLBデータメモリ904の内容を使用する。本実施例では、4ウェイセットアソシアティブ方式で実装することでタグメモリ、データメモリを4つ使用して、TLBのヒット率を向上させている。まったくページが一致するものがない場合は、ページフォルト例外発生ユニット905がOSプロセスを起動する。

【0308】仮想アドレスに相当するページがTLBユニット901内部に存在する場合は、TLBデータメモリ904の内容のうちの1つが、物理アドレスとして選択される。変換されたアドレスは、物理アドレス信号906から出力される。

【0309】本発明におけるTLBにはもう一つの役割がある。それは、データフロー同期と呼ばれる、指定したアドレスへのデータアクセスを自動的に検出する機能である。TLBエントリメモリ909には、アドレスの完全な一致を比較するための仮想アドレスが格納されており、ページ的一致によってデータフロー比較器908に伝達される。仮想アドレスが完全に一致した場合は、データフロー同期発生ユニット907によって、登録されたスレッドが生起される。一致比較のマスクビットによるアドレス領域の指定も可能である。

【0310】図15に、本発明のプロセッサにおけるTLBユニットのエントリを示す。通常のTLBと同じく、変換後の物理アドレス、ページごとの保護情報などを持ち、複数のプロセス空間を混在させるためのプロセスIDを持つ。

【0311】通常のTLBと異なるのは、二次キャッシュや他のプロセッサへの共有情報を6ビット格納していることと、データフロー同期のための一致比較アドレス、一致比較範囲のビットを持ち、さらに、データフローの検出で生起すべきスレッドIDを格納していることの2点である。

【0312】本発明においてTLBユニットは、キャッシュのディレクトリ共有情報を示す最上位のエントリでもある。二次キャッシュの全て、ローカルメモリ、そしてプロセッサ外部への共有を示すビットをそれぞれ持つ。

【0313】そのため、二次キャッシュ同士やメモリへのデータ転送や、二次キャッシュからプロセッサ外部へのインバリッド要求などは、まずはTLBに要求される。TLBでは、TLBエントリの持つ6ビットの共有情報に従って、4つの二次キャッシュ、プロセッサの持つローカルメモリ、及びプロセッサ外部に直接伝達される。

【0314】制御信号パケットルーター910は、TLBへの書きこみを受理するとともに、データフロー一致やページミスによる例外スレッドを発行し、スレッドパケット911に向けて伝達する。

【0315】(外部インターフェースユニット)

【0316】本発明のプロセッサは、複数のプロセッサを接続して利用するために以下の特徴を持つ。

【0317】(1) スレッドを自動的に複数のプロセッサに分配する。

【0318】(2) 各プロセッサにそれぞれローカルメモリを接続する。

【0319】(3) 各プロセッサ間のアクセスは仮想ア

ドレス空間とする

【0320】本発明のプロセッサでは複数のメモリを接続し、それらを全て1つのスレッドの仮想アドレス空間からアクセスすることを可能にする。

【0321】図10に、データキャッシュと外部を接続するTLB120、ローカルメモリアンターフェース122、プロセッサ間インターフェースユニット124の接続関係の模式図を示す。

【0322】本発明のプロセッサにおいて、基本的には物理アドレスは、TLBユニット120とローカルメモリアンターフェース122の間だけで利用される。物理アドレス専用信号1009が相互に接続される。

【0323】本発明のプロセッサにおいては、割り込みは最優先プライオリティーを持つスレッドの発行として処理される。リアルタイム性能は、スレッド制御ユニットによるプライオリティー制御によって確保できる。本発明のプロセッサは、プライオリティーの高いスレッドにいつでも動作を移すことができるためである。

【0324】本発明のプロセッサはマルチスレッドを前提としているため、複数のプロセッサ間でスレッドを発行するのにソフトウェア上の追加はほとんど必要ない。少なくともユーザーレベルのソフトウェアでは無改造で複数のプロセッサにスレッドを分配できる。

【0325】マルチプロセッサインターフェース124は、メモリアクセスバス125とともに、制御バス1007を有する。プロセッサ内部の制御バス信号1012は、そのままプロセッサ外部に出力することができる。

【0326】マルチプロセッサインターフェース124は、TLBによって該当する仮想アドレスがプロセッサ間共有状態を示す場合に、内部からの仮想アドレスを共有バス信号125に対して出力し、スレッド状態1012を制御バス1007に出力する。

【0327】本発明のプロセッサは、外部の共有バス信号125からの仮想アドレスの受信によっても、TLB120へのアクセスを行う。プロセッサ内部にデータのコピーがある場合は、TLB120のエントリが存在し、二次キャッシュへのアクセスによってデータの実体のあるキャッシュの場所も階層的に特定することができる。TLBのエントリが存在しない場合には、OSによる仮想記憶処理によって本来の物理アドレス、メモリバンクの所在を特定することになる。

【0328】(制御信号バス)制御信号をバス化して伝達する方式は、制御信号をエンコードすること、複数の経路の配線を共有することで、制御信号の配線の規模、長さを最小限にできる。さらに、複数の信号のタイミング制御を、同一の回路で行うことで単純にすることができる。その欠点は、伝達のためのレイテンシが劣ること、バスを中継するパケットルータの回路規模が大きいことである。

【0329】ところが、本発明の方式では、即座に制御信号を伝達する必要があるのは隣接するユニットにかぎられる。それ以外の制御信号は、スレッドのパイプライン進行にあわせて伝達すれば十分である。すなわち、パケット制御方式の欠点であるレイテンシは問題ではなくなる。そして、パケットルータの回路的な規模の増大も局所的なものであるため、配線短縮の効果の方が大きい。

【0330】図11に、個々のパケットルータの内部構造の模式図を示す。パケットルータは以下の3つの機能を持つ。

【0331】(1)パケットに応じてユニットの制御を行う

【0332】(2)パケットの目的地、情報量に応じて、複数のパケットルータのうちの1つを選択してパケットを送り出す。

【0333】(3)パケットのタイミングをチェックして、スレッドの進行に対して遅れていればスレッドをストールする。

【0334】1101はパケットルータである。受信した1102パケット信号を、コマンドデコーダ1103が解釈する。パケットをこのパケットルータ1101で即座に利用する場合は、制御信号デコーダ1104にパケット信号を入力する。制御信号デコーダ1104は、デコード結果と、パケットルータのあるユニットの状態信号1105に応じて、個別のステートマシン1106を動作させ、ユニットの制御をローカル制御信号1107で行う。制御信号デコーダ1104、ローカルステートマシン1106の構造はユニットごとに異なる。

【0335】パケットを中継する場合は、まず、タイミングチェック1112でパケットが時間どおりに到達しているかどうかを判定する。時間に遅れている場合はスレッドストール要求信号1111でパケットを要求したスレッドを停止する。パケットバッファ1108に蓄積する。パケットが時間以内に到達している場合は、パケット出力ユニット1110で複数のパケットバスのうちの1つを選択してパケットを出力する。

【0336】パケットの送信先は最終的な送信先に応じて静的に決定できる。トラフィックに応じた動的な経路制御などを行うわけではないため、一般的なネットワークで行うような最適な経路制御の必要はない。

【0337】図12に、本発明の第一実施例におけるパケットルータの配置を示す。

【0338】パケットルータは大まかなユニット、バスバッファごとに設置され、ユニットの制御を行う。パケット制御信号線は隣接したパケットルータの間みに配線される。

【0339】パケット制御信号は、スレッドのパイプラインの進行に従って伝送される。たとえば、演算ユニッ

トからTLBユニットへの書き込みを要求した場合は、キャッシュユニットのルーターを通過して伝達される。転送の中継に時間がかかるため、転送は数クロックを要する。ただし、転送の間に別のスレッドの動作が可能である。

【0340】この機構によって、最小限の配線で並列数に見合うだけの数の制御信号を送ることができる。

【0341】図27に、制御パケット信号の例を示す。すべての制御パケットは、32ビット程度のCP(Control Packet)信号を持つ。

【0342】Control Packetには、パケットの機能を示すPacket Command、パケットのパラメータを示すValue Fieldを持つ。Requestor Unitは要求元、Target Unitは伝達先のユニットを示す。

【0343】Remaining Timeはパケットが時間内に伝達されたかどうかの確認を行うための値である。この値をデクリメントすることで、パケットの進行が間に合っているかどうかの判定を行う。User Levelは、制御パケットの特権レベルを示す。

【0344】スレッドの情報が必要なパケットは、やはり32ビット程度のTI信号が付加される。TIにはプロセス、スレッドIDと、スレッドの優先順位、ユーザーレベルが格納されている。

【0345】この2つに加えて、アドレス、データ、PC(プログラムカウンタ)、SP(スタックポインタ)などの値が付加される。TIとPC、SPによって、スレッドのすべての情報が管理される。CPとアドレス、データが通常の内部バストランザクションに利用される。なお、制御パケット信号の仕様は、スレッド状態転送、データ転送などの目的によって変えることもでき、共用することもできる。

【発明の効果】

【0346】(回路規模)

【0347】基本的に、プロセッサに求められる性能は周波数性能と並列性能の積である。しかし、利用目的によっては、コストあたりの性能、および消費電力あたりの性能も求められる。本発明の方式は、回路の組み合わせによってそれらのいずれにも最適な構成にできることを示す。

【0348】今後のプロセッサの速度は、配線遅延にほぼ比例して決定される。半導体のプロセスの進化に従い、回路の局所的な遅延時間は縮小傾向がある。しかし、それには配線もトランジスタと同じオーダーで縮小するという前提条件が必要である。そのため、回路の大規模化によって配線が縮小されない場合は、微細化にもかかわらず周波数性能の向上は不可能になる。そのため、チップ全体の配線を行わないようにして、配線のオーダーを増加させないことが、周波数性能の向上を維持するために不可欠である。

【0349】配線の規模は、データ転送幅と転送相手の数で決まる。データ転送幅のN倍の増加に対して、配線の規模はN倍に比例して増大する。遅延の増大はわずかである。それに対して、転送相手のN倍の増加に対しては、配線の規模はNの二乗に比例して増加する。そして、遅延もN倍で増加する。そのため、転送相手を増やすことより、転送幅を増やすことの方が遥かに容易である。

【0350】本発明のプロセッサは、バスの階層化によって転送相手の組み合わせを常に4つ程度に制限している。この規模は現行のインオーダースーパースカラ方式プロセッサと同程度である。これ以上の対一接続の配線は行わないため、いくら並列度が増加しても、周波数性能を阻害する配線長の増加が発生することはない。

【0351】シフトレジスタ型転送は、自由な転送能力、比較的高いピークバンド幅、バスのアービトレーションの容易さという長所があるが、欠点としてはレイテンシ性能が最低となる。このレイテンシ性能の低下を隠蔽するためにマルチスレッドを利用する。

【0352】表1に、VLIW方式、SMP方式、本発明のPMT方式ごとの回路規模、遅延時間の比較の表を示す。

【0353】VLIW方式は、並列規模の増大に対して周波数性能を著しく低下させる。マルチプロセッサ方式は、周波数性能は維持できるが、回路規模の増大が大きい。それに対して本発明のPMT方式は、メモリ、演算ユニットの共有によって、最小限の回路規模で並列性能を増加させることができる。

【0354】(ユニット稼働率から見た性能向上)

【0355】本発明の方式は、単体のスレッドのレイテンシ性能ではほかのパイプラインプロセッサに劣るが、複数のスレッドの動作全体で性能を稼ぐことができる。そのため、全体の性能はすべてのスレッドの和である大域的な処理性能で判断されなければならない。さらに本発明の方式は、演算ユニットなどの稼働率を最大にすることで、回路規模に対する全体の性能を最大にできる。それに対して、ほかの方式の多くは回路規模を増加するほど演算ユニットなどの稼働率が下がる傾向がある。以下、演算ユニットなどの稼働率が他の方式に対して高いことを示す。

【0356】表2は、本発明の方式と、SMP方式との各状況に対する演算ユニットの停止期間の比較の表である。

【0357】本発明の方式は、自由な命令配置能力と、局所SMPモード機能によって、あらゆる演算ユニットをほぼ常に動作させることができる。従来のPMT方式が命令の配置に命令アドレスの制限があったのと対照的である。

【0358】本発明のプロセッサは、例外の発生頻度がスレッド発行ユニットの供給能力を超えない限り、ほと

んど全てのペナルティを隠蔽することができる。すなわち、スレッドが十分供給されている限り、本発明の方式はVLIW、マルチプロセッサ方式よりも演算ユニットの稼働率で勝る。しかも、それはスレッドが独立に並列動作できる限り、演算ユニットの数に比例して性能を向上できる。

【0359】マルチプロセッサ方式は、コンテキストスイッチにOSの介在が必要である。さらに、スレッドを別のプロセッサに移して再開させる「スレッドの移住」に、すべての状態をキャッシュコヒーレンシで転送する必要がある。この動作には、約100クロック以上の間プロセッサのバスを占有するため、数千クロック以上のレイテンシを隠蔽するのてなければ意味がない。さらに、スレッドを再開するには、動作しているスレッドがOSを呼び出して、各スレッドに対して再開条件が整っているかどうかを確認しなければならない。

【0360】次に、マルチプロセッサ方式にコンテキストスイッチ機能をハードウェアで実装して自動的に行うことを考える。それでも、すべてのプロセッサに大量のスレッド、そしてそれら全てのスレッドの状態と、完全なスケジューリングハードウェアを同時に搭載する必要がある。さらに、スレッドの移住には大量のプロセッサ間転送が必要になり、オーバーヘッドは削減できない。

【0361】以上の結論として、マルチプロセッサ方式とレイテンシ隠蔽機構は両立しにくい。

【0362】本発明の方式は、コンテキストスイッチはハードウェアで実装される。本発明の方式は、すべてのスレッドの空きスロットが1つのスケジューリングハードウェアを通るので、どの空き状態のノードにも即座にスレッドを供給できる。

【0363】さらに、本発明の方式では、停止していたスレッドは、基本的には停止した時と同じノードで再開することができる。この場合は状態の転送が一切必要なく、そのノードが空いた時点で即座にスレッドを再開できる。このため、スレッドの移住をほとんど行わずに、最適なスレッドの負荷分散が可能になる。

【0364】さらに、同期変数の待ち合わせに関しても、同期変数のアクセスによってバスを止めることはない。更に、データフロー同期を利用すれば、スケジューリングの必要も同期変数の確認も必要ない。この機能によって本発明のプロセッサはマルチスレッドのオーバーヘッドをなくし、マルチスレッドをあらゆるレイテンシの隠蔽に使用することを可能にしている。

【0365】本発明の方式における唯一のSMP方式に対する短所は、パイプライン間のスレッドの移住である。しかし、スレッドの移住の頻度はパイプラインを長くすることによって減少させることができる。

【0366】最小限のキャッシュ容量でスレッドの稼働率を上げるためには、同じ命令やデータを利用するスレッドを集中して実行すれば良い。それは同じ工程の仕事

を集中して行うほうが効率が良いことを意味する。本発明の方式は、命令、データキャッシュミスの管理によって、ある程度は自然にこの共有の形になる。

【0367】本発明の方式は、隣接する演算ユニットに全てのレジスタ状態を転送するかわり、共有するデータの転送量が減るPMT方式を基本とする。それに加えて、レジスタ状態を転送しない代わりに、共有するデータの転送量が最大となるSMP方式も可能にする。

【0368】PMT方式では、命令の間のデータ転送スループットは、近傍の命令間ほど多く必要とされ、命令間が遠距離になるほど減少する傾向にある。それに対して、スレッド間のデータ転送のためのスループットは、スレッド間のデータの共有が多く、並列度が增大するほど拡大する。理由は、1つのデータを大量のプロセッサがほぼ独立して参照するためである。そのために、SMP方式ではメモリバス稼働率に著しい偏りが生じる。

【0369】PMT方式は、スレッド間のデータ転送のスループットを最小限にする方式である。よって、どんなに並列度を上げて、かつ同じデータを共有しても、局所的なデータバスのデータスループットの増加を抑制することができる。すなわち、データの共有とスケラブルな並列性能向上を同時に実現することができる。

【0370】それに対して、SMP方式は、スレッド間の転送には弱い、単体の演算ユニットだけで実行ができるという長所がある。そのため、独立したスレッドの実行では、SMP方式を利用するほうがメモリバスの稼働率が最小となる。

【0371】本発明の方式は、データキャッシュ間の転送量によって自動的にPMT方式、SMP方式を使い分け、常にメモリバス稼働率を最小にすることができる。

【0372】一般的に、キャッシュの容量が増大すれば、それだけキャッシュミスの確率が減少して全体の性能を上げることができる。しかし、キャッシュの容量の増大はキャッシュアクセスの速度低下を招く。そのためには、キャッシュを分割するのが望ましいが、複数のキャッシュへの接続はやはり配線遅延による速度低下を招く。理想的なキャッシュ容量増大の方法は、キャッシュと演算ユニットを直結させて、それを組にして大量に配置することである。しかし、従来のマルチプロセッサ方式では、キャッシュを複数持たせても、複数のキャッシュのほとんどに同じ内容を格納する必要があり、キャッシュの容量増大の効果を見込むことはできない。

【0373】それに対して、本発明の方式では、PMT方式を利用する限りは、複数のキャッシュへの同じデータの複製を抑制することができ、キャッシュの容量を増大させてヒット率を向上させることができる。さらに、スレッドの中で何度も利用するデータ、あるいはスレッドの中で発生したデータについても、データを利用するキャッシュに対してのみ直接データを送るため、データの複製が最小限で済む。

【0374】(命令、データ、演算ユニットの共有)

【0375】現在のプロセッサでは、命令メモリの内容はプログラムのロード時に決定され、まず改変されることはない。それを許すと、命令の読み込み、動作順序が保証されない現在のプロセッサでは動作が保証されないためである。

【0376】そのため、命令メモリはアドレスに対して必ず同じ値が読み出され、他のスレッドからの改変のおそれもない。ということは、同じ命令メモリを利用するスレッドはすべて1つの命令を利用できれば効率的である。PMT方式の作用によって、1つの命令は連続してパイプライン状に動作する大量のスレッドから参照できる。そのため、本発明の方式はオンチップマルチプロセッサなどに比較して命令のメモリサイズ、リプレイスに要求されるメモリスループットが遥かに小さい。

【0377】本発明の方式では、パイプラインの動作を止める分岐命令、データキャッシュミスは、マルチスレッドによってある程度は隠蔽できる。しかし、スレッド発行ユニットの供給能力を超えるほど頻発する場合は、本発明の方式でもやはりパイプラインを停止することになり、性能を低下させる。そのため、命令に置かれた予測情報を用いて、そのペナルティーを極力減少するのが望ましい。

【0378】本発明の方式は、1つの命令を全てのスレッドが共有できる。そして、分岐予測情報、データフロー予測情報は、命令列の内容、すなわち命令アドレスに依存し、個別のスレッドの状態にほとんど依存しない。ということは、これらの予測情報は1つあれば全てのスレッドから共有できる。

【0379】マルチプロセッサ間データ転送は、プロセッサの数が増加するにしたがって局所的にも増大し、個々のプロセッサのバス転送性能を使用し、マルチプロセッサにおいてスケラブルな性能向上を阻害する。

【0380】プログラムで利用するデータには、細かい数値の相違はあるものの、80%の部分のプログラムで20%の部分のデータを利用するという経験則がある。たとえば、キャッシュはこの経験則を利用するものである。ということは、1つのプログラムを分割したスレッドも、その多くは同じデータを利用することになるのは当然である。この性質を利用するために、まったく違うスレッドが同じデータを利用する方法を提供する。

【0381】データは同じ命令が同じようなデータを利用するケース、あるいはまったく違うデータを利用する2つのケースが考えられる。当然データの共有の効率は命令ほどではないが、大まかなデータブロックに対しては共有できるケースが多い。そのために、データキャッシュを分散配置し、複数のスレッドから共有させる。

【0382】これによって、データキャッシュの共有と大容量化を同時に実現し、結果的に単体スレッドから見た一次キャッシュの容量を増加させることができる。無

論、一次キャッシュ間の転送量は増加するが、それはスループットのみの増大であり、比較的実装しやすい。

【0383】本発明の方式では隣接する4つ程度の演算ユニットが1つのスレッド発行ユニットを共有する。これは、分岐、例外によるスレッドの切り替えの頻度が数命令に一回という前提によるものである。

【0384】待ち状態のスレッドは、この4つの同時実行されているスレッドのうちの、どのスレッドが停止しても即座に発行できる。

【0385】さらに、演算ユニットの列の長さの増加、分岐予測などによってスレッドの移住の頻度が減れば、スレッド発行ユニットの稼働率も相対的に減少する。

【0386】そして、本発明の方式では細かいスレッドの切り替えのためのスレッドの移住も必要ない。レジスタ、データキャッシュの内容は、常にスレッドが停止した場所に待機されており、スレッドの空きスロットを待つだけで即座に実行を開始できる。

【0387】SMP方式では、キャッシュレイテンシ隠蔽のためには、すべてのプロセッサがそれぞれ実行可能な待ちスレッドを待機させておく必要がある。あるいは、隣接するいくつかのプロセッサに対してスレッド発行を行わせることになる。このことは、大量のプロセッサに対して任意のスレッドを高速に発行することが難しいことを意味する。

【0388】本発明の方式では、各スレッド発行ユニットを、すべてのスレッドがパイプラインとして通過することによって共有させる。このため、すべてのプロセッサが待ち状態のスレッドを有することなく高速コンテキストスイッチを可能にする。データキャッシュや特殊演算ユニットの結果などを取得し、再開する準備が整ったスレッドは、常に空いたあらゆるスレッドスロットに対して発行される。

【0389】(IPユニットの共有)

【0390】IPユニット間のデータの転送能力を最大にするには、IPユニット間を信号で直結するのが最も簡単である。だが、それでは全体で1つの機能しか実現できない。

【0391】次に考えられる手段は、それぞれIPユニットの間にマイクロプロセッサをそれぞれ置くことである。しかしこれでは、プログラムがIPの結合ごとに分散されることになり、処理が一様にならないという欠点がある。

【0392】さらに次に考えられるのは、IPユニットとマルチプロセッサをクロスバススイッチで結合する方法である。これならば、共有バスよりは優れた転送能力が確保できる。しかしクロスバススイッチは回路規模が(M個のプロセッサ、N個のIPユニットユニットに対して)MとNの積のオーダーで増加する方式であり、大規模並列には向かない。さらに、そのために切り替えのレイテンシ時間が遅く、自由でかつ動的な転送には向か

ない。

【0393】本発明の方式は、各ノードに対してIPユニットを接続して、IPユニット間の通信能力をノード間のデータ通信能力で確保する。IPユニット間のデータの整形は、PMTの各演算ユニットがそれぞれ独立して行い、IPユニットへの入力への負荷が低い場合はすぐに別の用途に転用できる。

【0394】IPユニットの転送能力が単体の演算ユニットの転送能力を超えるほど高い場合には、近傍の複数の演算ユニットを利用して転送し、その先の演算ユニットでデータを整形することができる。このような場合では特に、マルチプロセッサ+クロスバススイッチ方式より圧倒的にIPユニットからの転送性能を稼ぐことができる。

【0395】本発明の方式では、IPユニットはソフトウェアでは特殊命令、あるいはシステムアクセス命令として使用することができ、その配置に制限はない。実際のIPユニットの分散配置に対しては、スレッドの移住機構が自動的に対応することもできる。IPユニット間のデータ転送は、PMT方式が持つレジスタ隣接転送、キャッシュコヒーレンシ機構で行う。こうして、同じソフトウェアで自由なIPユニットの組み合わせに効率良く対応することができる。

【0396】(消費電力予測)

【0397】CMOS回路は、信号の変化のときに電力を消費する。信号が変化しなければ電力をほとんど消費しない。

【0398】ところで、本発明の方式は、同一のスレッドを連続して動作させるときは、その供給される命令、演算ユニットの状態は完全に同一である。さらに、利用するレジスタファイル、データバス、データキャッシュとのバス通信の内容もスレッド間の違いは少ない。ということは、同じスレッドをまとめて実行する時には、各スレッド間のわずかな動作の違いだけが消費電力になる。それに対して、通常のプロセッサでは、各命令ごとにすべての回路の状態が変わるため、すべての回路の半分近くの信号が変化し、消費電力となる。

【0399】結論としては、本発明の方式のプロセッサは、同一の命令、データを利用したスレッドの連続動作が可能の場合は、現行のパイプライン方式プロセッサよりも低い消費電力で同じ性能を発揮できる。アーキテクチャのレベルでこれ以上の低消費電力の手段は考えられない。

【0400】表1の記載のように、本発明のプロセッサは、マルチプロセッサ、VLIW方式に対して、性能に対する回路規模が最小である。理由は、PMT方式は命令、データ、演算ユニットの共有を行うためである。性能に対する回路規模が最小であるということは、そのまま性能に対する消費電力が最小であることを意味する。

【0401】さらに、本発明の方式は、性能に対する配線長も最小である。今後の半導体の消費電力は、配線容量の充放電が大半を占めることになると予想されるため、配線が最小であるということはそのまま消費電力の削減に繋がる。

【0402】さらに、前述した同一命令を利用するスレッドの連続動作による電力削減とあいまって、本発明の方式は、プログラム可能な回路において、最小の電力で実際の演算を行う方法であるといえる。ただし、本発明の方式は局所的にはSMP方式に近い動作モードも持つため、その部分はSMP方式と同じ消費電力になる。しかし、本発明の方式は可能な限りPMT方式で演算を行うおうとするため、演算性能に対する消費電力は常に最小になる。

【図面の簡単な説明】

【図1】本発明の構造を用いたプロセッサの構造模式図(第一実施例)

【図2】従来のVLIW方式のプロセッサの構造模式図

【図3】従来のマルチプロセッサ方式のプロセッサシステムの構造模式図

【図4】従来のPMT方式のプロセッサの構造模式図

【図5】本発明の構造を用いたプロセッサの構造模式図(第二実施例)

【図6】命令発行ユニットの内部構造模式図

【図7】最大4つのスレッドを同時に実行する、実行ユニットの内部構造模式図

【図8】一次、二次キャッシュの接続関係を示す構造模式図

【図9】TLBユニットの内部構造模式図

【図10】TLBと外部インターフェースの接続関係を示す構造模式図

【図11】パケットルーターの内部構造模式図

【図12】本発明の第一実施例における、パケットルーターの配置図。

【図13】命令キャッシュタグメモリの1ラインごとの内容

【図14】データキャッシュタグメモリの1ラインごとの内容

【図15】TLBユニットの1エントリごとの内容

【図16】従来のマルチプロセッサにおける、スレッドの動作例

【図17】本発明のプロセッサにおける、スレッドの動作例

【図18】分岐命令実行における、命令発行ユニットの選択方法を示す概念図

【図19】命令キャッシュのもつ予測情報の書き込み、利用方法を示す概念図

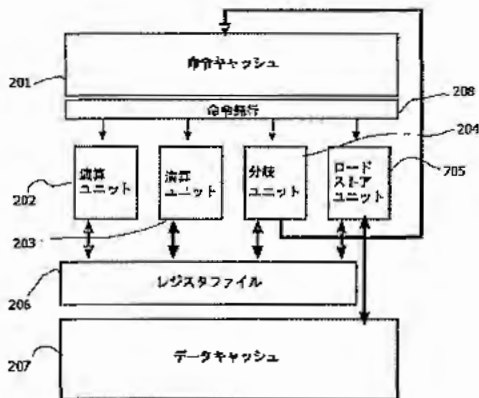
【図20】各種分岐命令の実行概念図

【図21】1つの演算ユニットにおける、パイプライン動作概念図

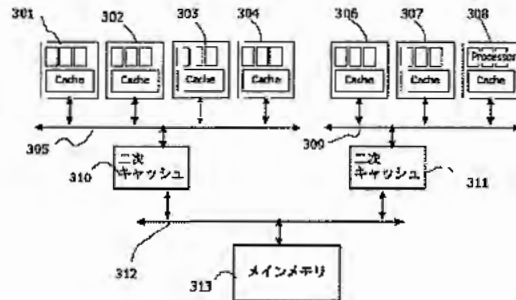
【図22】スレッド移住のレジスタ同期動作概念図	402	命令発行制御
【図23】ディレクトリ方式キャッシュのリード動作概念図	403	PCラッチ
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104 命令キャッシュメモリ	503	ショートカットバスインターフェース
105 実行ユニット	504	IPユニット
106 共有レジスタファイル	510	I/Oバスインターフェース
107 16ビット演算ユニット	511	次段外部プロセッサインターフェース
108 共有演算ユニット	602	パケットルータ
109 分岐発行制御信号	603	制御パケット信号
110 データアクセスバス信号	604	プライオリティ選択ユニット
111 一次データキャッシュ	605	命令キャッシュ制御ユニット
112 アクセスバッファ	606	命令キャッシュタグメモリ
113 一次データキャッシュ	607	命令ローカルTLB
116 二次キャッシュメモリ	608	スレッド状態信号
117 アクセスバッファ	609	スレッド状態制御ユニット
120 グローバルTLB	610	スレッド状態信号
121 データアクセスバス信号	611	分岐、データフロー予測信号
122 ローカルメモリインターフェース	612	命令信号
123 ローカルメモリバス信号	613	分岐要求信号
124 外部バスインターフェース	614	命令順序アライナ
125 外部バス	615	スレッド状態信号
126 割り込み信号	616	命令キャッシュデータメモリ
127 新規スレッド発行ユニット	617	命令リプレースバス
131 アクセスバッファ	618	待ち状態スレッド状態バッファ
132 スレッド状態信号	619	制御パケット信号
133 スレッド発行制御信号	620	スレッド移住制御ユニット
134 分岐発行制御信号	702	プログラムカウンタ信号
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202、203 演算ユニット	704	レジスタファイル
204 分岐ユニット	705	レジスタ転送バス信号
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206 レジスタファイル	707	オペランドショートカット信号
207 データキャッシュ	708	16ビット整数演算ユニット
208 命令発行ユニット	709	結果ショートカットバス信号
301、302、303、304、306、307、308 プロセッサ	710	64ビット整数演算ユニット
305、309 一次共有バス	712	浮動小数点加算+乗算ユニット
310、311 二次キャッシュ	713	ロードストアユニット
312 共有メモリバス	714	アドレスバス信号
313 メインメモリ	715	データバス信号
401 PMT方式プロセッサ	716	レジスタ待避バス信号
	717	演算結果フォワードリングタニット
	718	浮動小数点除算ユニット
	719	浮動小数点加算ユニット

- | | | | |
|------|------------------------|------------------------|-----------------|
| 720 | 結果ショートカットバス信号 | 1009 | 物理アドレス信号 |
| 721 | 分岐ユニット | 1011 | 制御パケット信号 |
| 722 | オペランドショートカット信号 | 1012 | スレッド発行パケット信号 |
| 723 | レジスタ同期ユニット | 1013 | 仮想アドレス |
| 724 | レジスタ転送バス信号 | 1101 | 制御パケットルータ |
| 725 | プログラムカウンタバス信号 | 1102 | 制御パケット信号 |
| 726 | 分岐発行パケット信号 | 1103 | 制御コマンドデコーダ |
| 802 | 一次キャッシュ制御 | 1104 | 制御信号デコーダ |
| 803 | 一次キャッシュタグメモリ | 1105 | ローカル状態信号 |
| 804 | 一次キャッシュデータメモリ | 1106 | ローカル制御ユニット |
| 805 | 二次キャッシュ制御 | 1107 | ローカル制御信号 |
| 806 | 二次キャッシュタグメモリ | 1108 | 制御パケットバッファ |
| 807 | 二次キャッシュデータメモリ | 1109 | 制御パケット信号 |
| 902 | 仮想アドレス信号 | 1110 | 制御パケット出力ユニット |
| 903 | TLBタグメモリ | 1111 | スレッドストール信号 |
| 904 | アドレス比較器 | 1112 | 制御パケットタイミングチェッカ |
| 905 | ページフォルト発生ユニット | 1201~1211 | 制御パケットルータ |
| 906 | 物理アドレス信号 | 1801 | 二次キャッシュ |
| 907 | ページトラップ・データフロー同期発生ユニット | 1802, 1804, 1807, 1809 | スレッド管理ユニット |
| 908 | TLBエントリメモリ | 1803, 1805, 1808 | 命令キャッシュ |
| 909 | 制御信号パケットルータ | 1806 | 分岐ユニット |
| 910 | ページフラッシュシーケンサ | 1901, 1905 | 命令キャッシュ |
| 911 | スレッドパケット | 1902, 1906 | 実行ユニット |
| 1001 | データバス信号 | 1903 | 分岐ユニット |
| 1004 | スレッドパケットバッファ | 1904, 1908 | データキャッシュ |
| 1007 | スレッドパケット信号 | 1907 | ロードストアユニット |

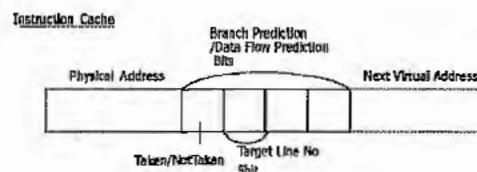
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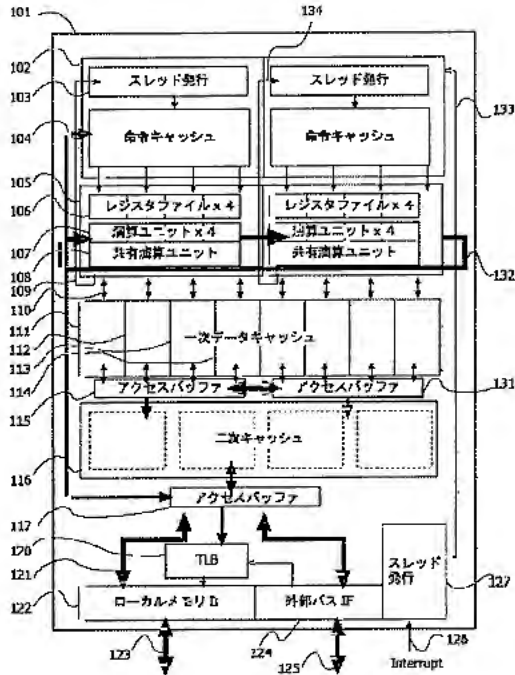
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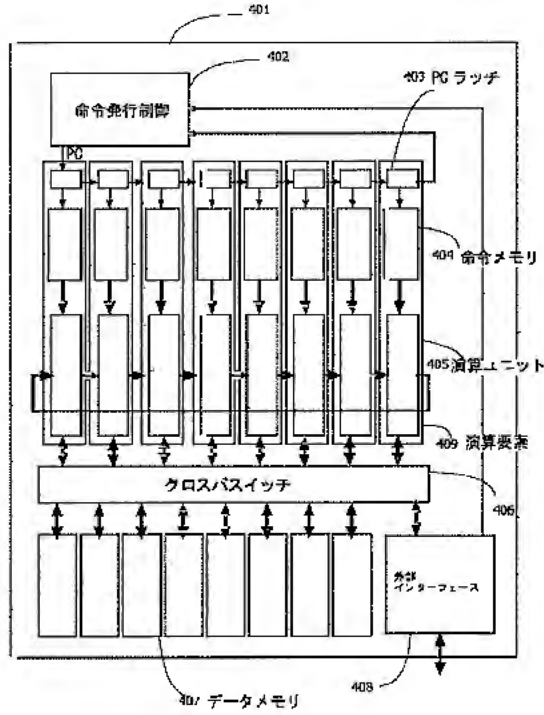
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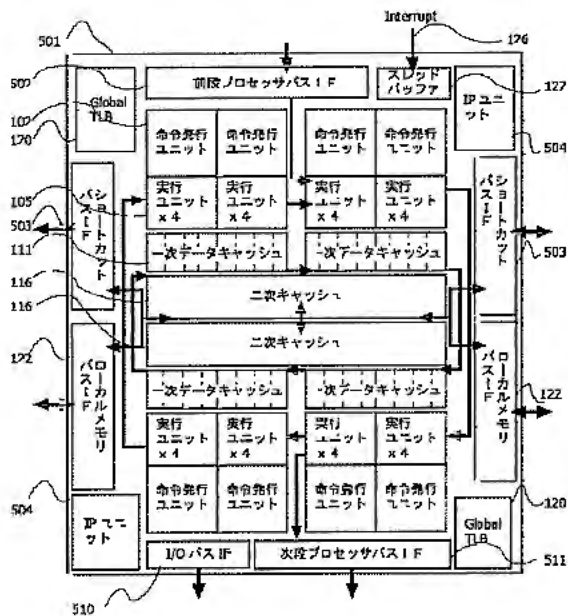
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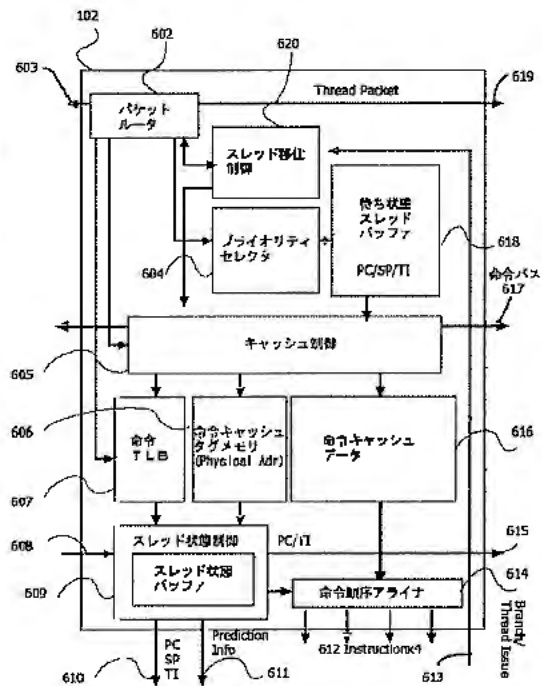
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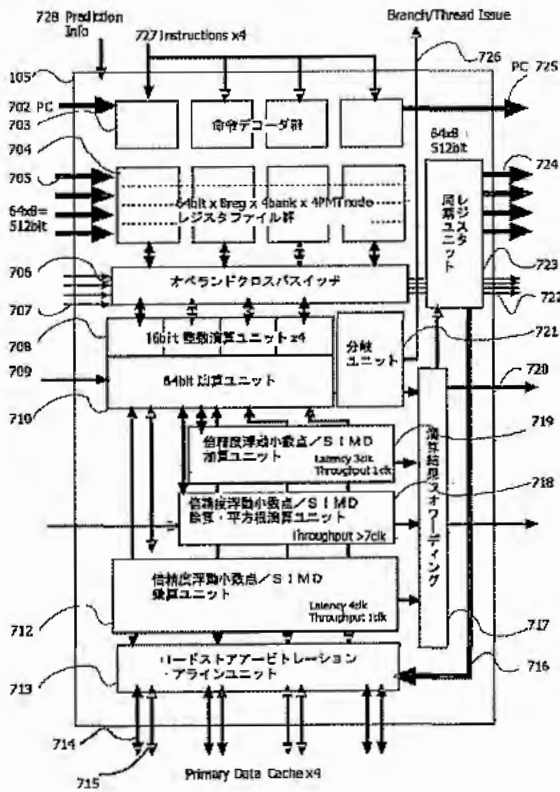
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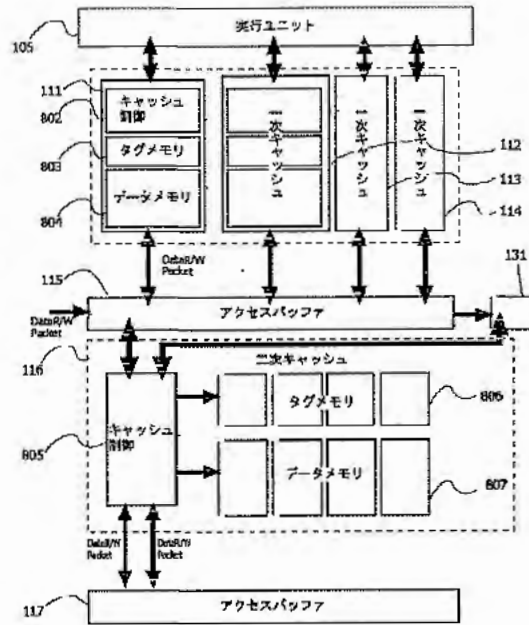
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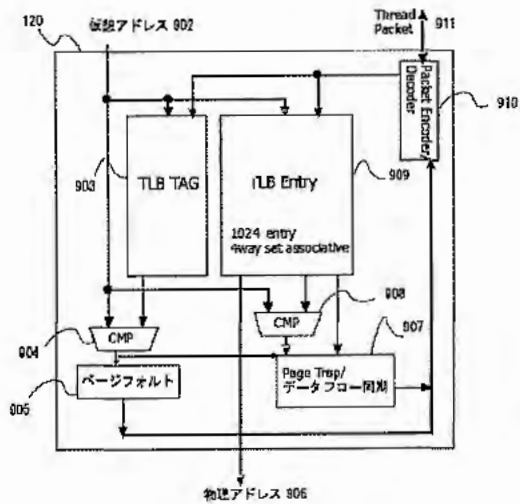
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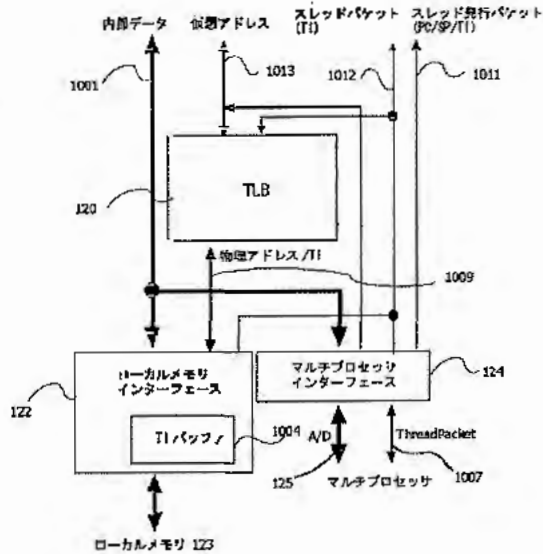
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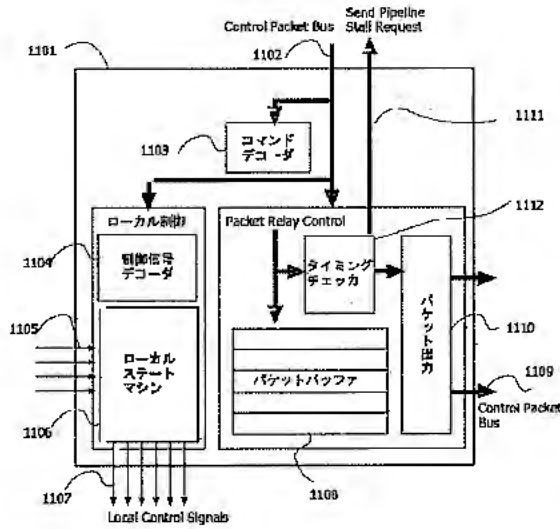
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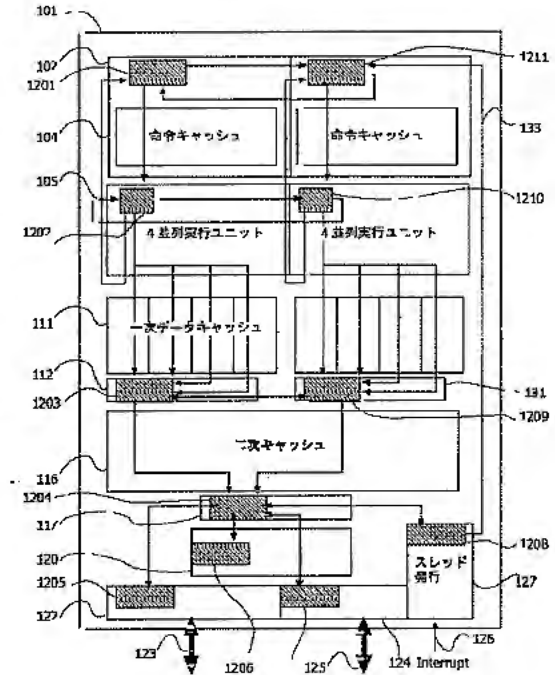
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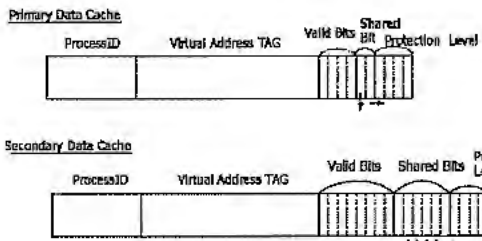
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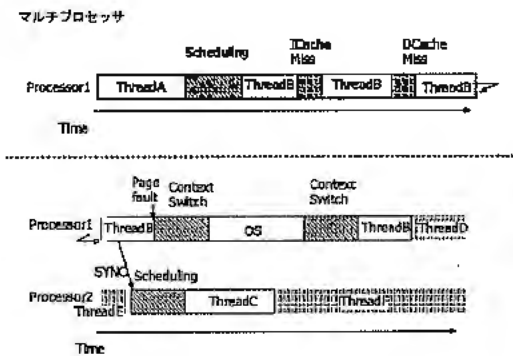
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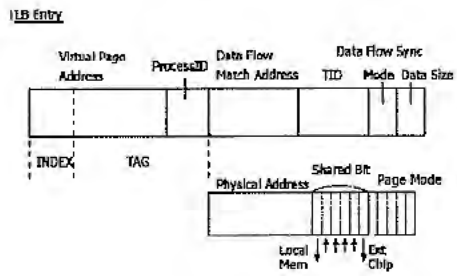
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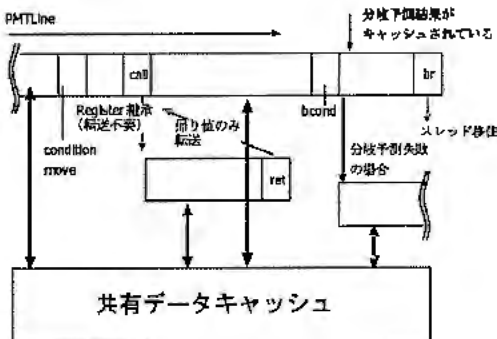
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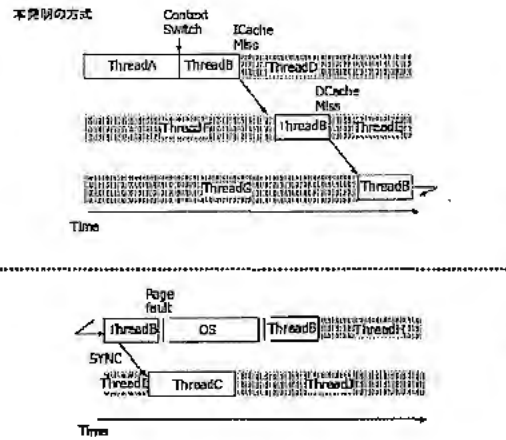
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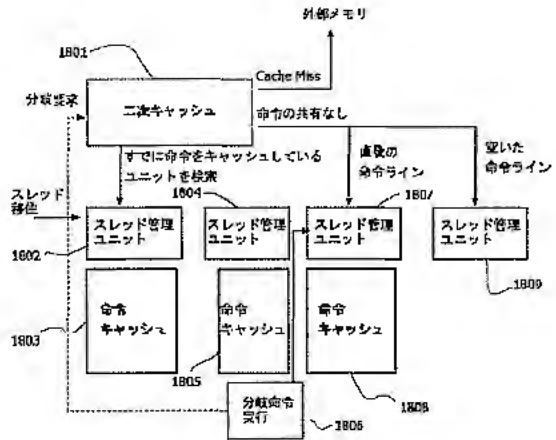
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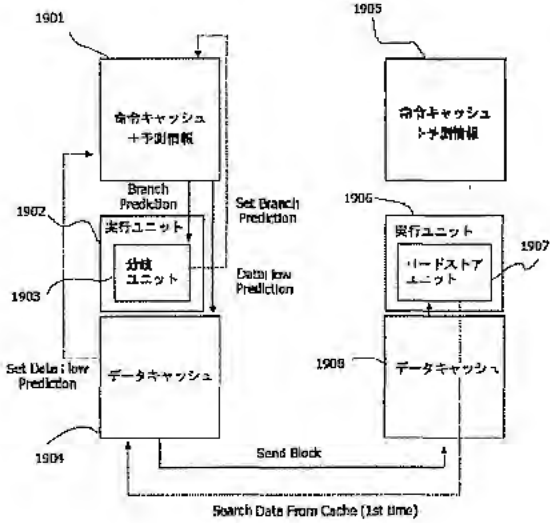
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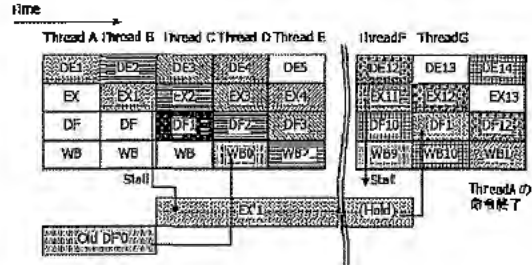
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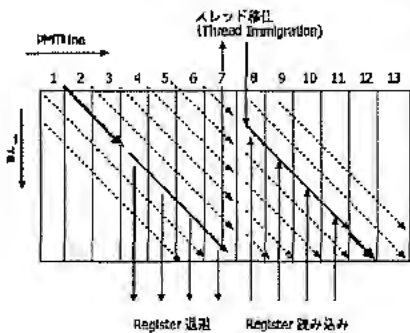
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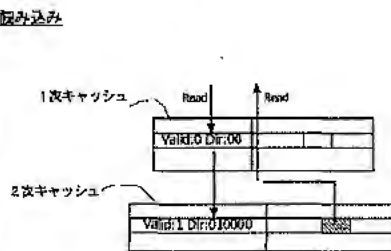
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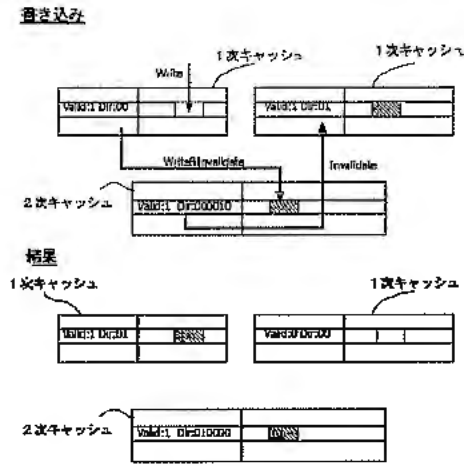
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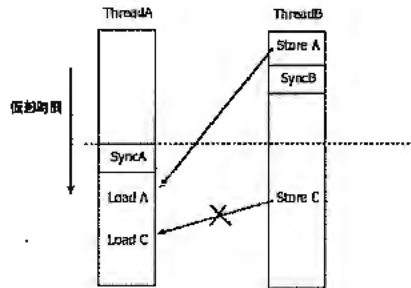
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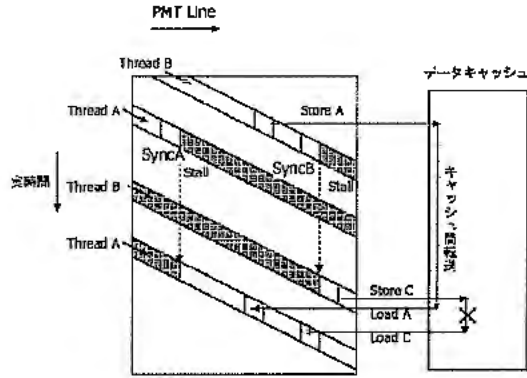
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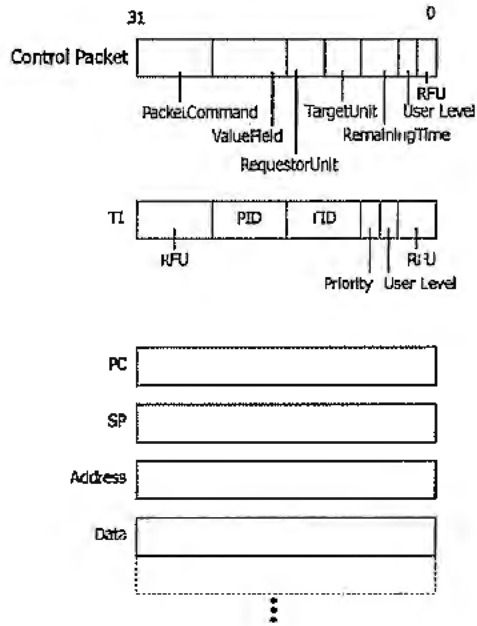
【図26】



【図25】



【図27】



フロントページの続き

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			H
			E

	310		Y
12/10		12/10	310B
12/12		12/12	A
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5B013 AA01 AA05 AA11 BB01 BB18
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5B033 AA02 AA03 AA04 AA13 AA14
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Electronic Acknowledgement Receipt

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Application Number:	12836364
International Application Number:	
Confirmation Number:	2050
Title of Invention:	RECONFIGURABLE SEQUENCER STRUCTURE
First Named Inventor/Applicant Name:	Martin Vorbach
Customer Number:	26646
Filer:	Aaron Grunberger/Eunice Chang
Filer Authorized By:	Aaron Grunberger
Attorney Docket Number:	2885/139
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Time Stamp:	15:52:59
Application Type:	Utility under 35 USC 111(a)

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U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			
RESPONSE TO NOTICE TO FILE CORRECTED APPLICATION PAPERS — FILING DATE GRANTED		Docket Number: 2885/139	Confirmation No. 2050
Application Number 12/836,364	Filing Date July 14, 2010	Examiner Unassigned	Art Unit 2827
Invention Title RECONFIGURABLE SEQUENCE STRUCTURE		Inventor(s) VORBACH	

Address to:
Mail Stop: Missing Parts
Commissioner for Patents
Alexandria, VA 22313-1450

I hereby certify that this correspondence is being electronically transmitted via ESF-Web addressed to: Mail Stop: Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on
Date: September 22, 2010
Signature: /Eunice K. Chang/
Eunice K. Chang

Sir:

1. To complete the filing requirements for the above-referenced application under 37 C.F.R. § 1.51, enclosed please find the following for submission:
 1. A copy of the Notice to File Corrected Application Papers dated August 2, 2010,
 2. A substitute specification (clean copy), and
 3. A substitute specification (mark-up copy).

No new matter has been added.

Respectfully submitted,

Dated: September 22, 2010

By: /Aaron Grunberger/
Aaron Grunberger, Reg. No. 59,210

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New York, N.Y. 10004
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CUSTOMER NO. 26646



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
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CONFIRMATION NO. 2050

26646
KENYON & KENYON LLP
ONE BROADWAY
NEW YORK, NY 10004

FORMALITIES LETTER



Date Mailed: 08/02/2010

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Filing Date Granted

An application number and filing date have been accorded to this application. The application is informal since it does not comply with the regulations for the reason(s) indicated below. Applicant is given TWO MONTHS from the date of this Notice within which to correct the informalities indicated below. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

The required item(s) identified below must be timely submitted to avoid abandonment:

- A substitute specification excluding claims in compliance with 37 CFR 1.52, 1.121(b)(3), and 1.125 is required. The substitute specification must be submitted with markings and be accompanied by a clean version (without markings) as set forth in 37 CFR 1.125(c) and a statement that the substitute specification contains no new matter (see 37 CFR 1.125(b)). Since a preliminary amendment was present on the filing date of the application and such amendment is part of the original disclosure of the application, the substitute specification must include all of the desired changes made in the preliminary amendment. See 37 CFR 1.115 and 1.215.

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RECONFIGURABLE SEQUENCER STRUCTURE

Cross-Reference to Related Applications

5 This application is a continuation of U.S. Patent Application
Serial No. 12/541,299, filed on August 14, 2009, which is a
continuation of and claims priority to U.S. Patent Application
Serial No. 12/082,073, filed on April 7, 2008, which is a
continuation of and claims priority to U.S. Patent Application
10 Serial No. 10/526,595, filed on January 9, 2006, which was the
National Stage of International Application Serial No.
PCT/EP03/38599, filed on September 8, 2003, which claims
benefit of and priority to German Patent Application Serial
No. DE 102 41 812.8, filed on September 6, 2002, the entire
15 contents of each of which are expressly incorporated herein by
reference thereto.

Description

The present invention relates to a cell element field and a
method for operating same. The present invention thus relates
20 in particular to reconfigurable data processing architectures.

The term reconfigurable architecture is understood to refer to
units (VPUs) having a plurality of elements whose function
and/or interconnection is variable during run time. These
elements may include arithmetic logic units, FPGA areas,
25 input/output cells, memory cells, analog modules, etc. Units
of this type are known by the term VPU, for example. These
typically include arithmetic and/or logic and/or analog and/or
memory and/or interconnecting modules and/or communicative
peripheral modules (IOs), typically referred to as PAEs, which
30 are arranged in one or more dimensions and are linked together
directly or by one or more bus systems. PAEs are arranged in

any configuration, mixture and hierarchy, the system being known as a PAE array or, for short, a PA. A configuring unit may be assigned to the PAE. In addition to VPU units, in principle systolic arrays, neural networks, multiprocessor systems, processors having multiple arithmetic units and/or logic cells, interconnection and network modules such as crossbar circuits, etc., as well as FPGAs, DPGAs, transputers, etc., are also known

It should be pointed out that essential aspects of VPU technology are described in the following protective rights of the same applicant as well as in the particular follow-up applications to the protective rights listed here:

P 44 16 881.0-53, DE 197 81 412.3, DE 197 81 483.2, DE 196 54 846.2-53, DE 196 54 593.5-53, DE 197 04 044.6-53, DE 198 80 129.7, DE 198 61 088.2-53, DE 199 80 312.9, PCT/DE 00/01869, DE 100 36 627.9-33, DE 100 28 397.7, DE 101 10 530.4, DE 101 11 014.6, PCT/EP 00/10516, EP 01 102 674.7, DE 102 06 856.9, 60/317,876, DE 102 02 044.2, DE 101 29 237.6-53, DE 101 39 170.6.

It should be pointed out that the documents listed above are incorporated in particular with regard to particulars and details of the interconnection, configuration, embodiment of architecture elements, trigger methods, etc., for disclosure purposes.

The architecture has considerable advantages in comparison with traditional processor architectures inasmuch as data processing is performed in a manner having a large proportion of parallel and/or vectorial data processing steps. However, the advantages of this architecture in comparison with other processor units, coprocessor units or data processing units in general are not as great when the advantages of

interconnection and of the given processor architectonic particulars are no longer achievable to the full extent.

This is the case in particular when data processing steps that are traditionally best mappable on sequencer structures are to be executed. It is desirable to design and use the reconfigurable architecture in such a way that even those data processing steps which are typically particularly suitable for being executed using sequencers are executable particularly rapidly and efficiently.

The object of the present invention is to provide a novel device and a novel method for commercial application.

The method of achieving this object is claimed independently. Preferred embodiments are characterized in the subclaims.

According to a first essential aspect of the present invention, in the case of a cell element field whose function and/or interconnection is reconfigurable in particular during run time without interfering with unreconfigured elements for data processing with coarsely granular function cell elements in particular for execution of algebraic and/or logic functions and memory cell means for receiving, storing and/or outputting information, it is proposed that function cell-memory cell combinations be formed in which a control connection to the memory means is managed by the function cell means. This control connection is for making the address and/or data input/output from the memory controllable through the particular function cell, typically an ALU-PAE. It is thus possible to indicate, for example, whether the next item of information transmitted is to be handled as an address or as data and whether read and/or write access is necessary. This transfer of data from the memory cell, i.e., the memory cell means, which may be a RAM-PAE, for example, to the function cell means, which may be an ALU-PAE, for example, then makes

it possible for new commands that are to be executed by the ALU to be loadable into the latter. It should be pointed out that function cell means and memory cell means may be combined by integration into a structural unit. In such a case it is possible to use a single bus connection to input data into the memory cell means and/or the ALU. Suitable input registers and/or output registers may then be provided and, if desired, additional data registers and/or configuration registers different from the former may also be provided as memory cell means.

It should also be pointed out that it is possible to construct a cell element field containing a plurality of different cells and/or cell groups, strips or similar regular patterns being preferably provided with the different cells because these permit a very regular arrangement while facilitating the design equally in terms of hardware design and operation. With such a strip-like arrangement or other regular layout of a small plurality of different cell elements, for example, elements having integrated function cell means-memory cell means combinations, i.e., cells in which function cell means and memory cell means are integrated according to the present invention, are provided centrally in the field, where typically only a few different program steps are to be executed within a sequencer structure because, as has been recognized, this provides very good results for traditional data stream applications, while more complex sequencer structures may be constructed at the edges of the field where, for example, an ALU-PAE which represents a separate unit possibly may be provided in addition to a separate RAM-PAE and optionally a number of I/O-PAEs using, i.e., arranging appropriate control lines or connections thereof because frequently more memory is needed there, e.g., to temporarily store results generated in the field central area of the cell

element field and/or for datastreaming, to pre-enter and/or process data needed thereby.

When cells that integrate memory cell means and function cell means are provided, e.g., in the center of the field, a small
5 memory may then be provided there for different commands to be executed by the function cell means such as the ALU. It is possible here in particular to separate the command memory and/or the configuration memory from a data memory, and it is possible to design the function memory to be so large that
10 alternatively, one of several, e.g., two different sequences may be executed. The particular sequence to be executed may occur in response to results generated in the cell and/or control signals such as carry signals, overflow signals, and/or trigger signals arriving from the outside. In this way,
15 this arrangement may also be used for wave reconfiguration methods.

In this way it is possible to construct a sequencer structure in a cell element field by providing a dedicated control connection controlled by function cells in a dedicated manner
20 between function cell and function cell means and memory cell and/or memory cell means with only two elements connected by suitable buses without requiring additional measures and/or design changes otherwise. Data, addresses, program steps, etc., may be stored in the memory cell in a manner known per
25 se from traditional processors. Since both elements, if properly configured, may also be used in another way, this yields a particularly efficient design which is particularly adaptable to sequencer structures as well as vectorial and/or parallelizable structures. Parallelization may thus be
30 supported merely via suitable PAE configurations, i.e., by providing PAEs that operate in two different spatial directions and/or via cell units equipped with data throughput registers.

It is clear here that a plurality of sequencer type structures may be constructed in the reconfigurable cell element field by using only two cells in a cell element field, namely the function cell and the information processing cell. This is
5 advantageous inasmuch as a number of different tasks that are different from one another per se must often be executed in data processing, e.g., in a multitasking-capable operating system. A plurality of such tasks must then be executed effectively and simultaneously in a single cell element field.
10 The advantages of real time applications are obvious. Furthermore it is also possible to operate the individual sequencer structures that are constructed in a cell element field, providing the control connection according to the present invention, at different clock rates, e.g., to lower
15 power consumption by executing lower priority tasks at a slower rate. It is also possible to execute sequencer type program parts in the field in parallel or vectorially in execution of algorithms that are largely parallel per se and vice versa.

20 Typically, however, it is preferable for sequencer-type structures to be clocked at a higher rate in the cell element field, whether they are sequencer-type structures having an area connected to neighboring cells or buses or whether they are combinations of spatially differentiable separate and
25 separately useable function cell elements such as ALU-PAEs and memory cell elements such as RAM-PAEs. This has the advantage that sequential program parts, which are very difficult to parallelize in any case, may be used in a general data flow processing without any negative effect on the overall data
30 processing. Examples of this include, e.g., a HUFFMANN coding which is executable much better sequentially than in parallel and which also plays an important role for applications such as MPEG4 coding, but in this case the essential other parts of

the MPEG4 coding are also easily parallelizable. Parallel data processing is then used for most parts of an algorithm and a sequential processing block is provided therein. An increase in the clock frequency in the sequencer range by a factor of 2 to 4 is typically sufficient.

It should be pointed out that instead of a strip arrangement of different cell elements, another grouping, in particular a multidimensional grouping, may also be selected.

The cell element field having the cells whose function and/or interconnection is configurable may obviously form a processor, a coprocessor and/or a microcontroller and/or a parallel plurality of combinations thereof.

The function cells are typically formed as arithmetic logic units, which may be in particular coarsely granular elements but may also be provided with a fine granular state machine, for example. In a particularly preferred exemplary embodiment, the ALUs are extended ALUs (EALUs) as described in previous patent applications of the present applicant. An extension may include in particular the control line check, command decoder unit, etc., if necessary.

The memory cells may store data and/or information in a volatile and/or nonvolatile form. When information stored in the memory cells, whether program steps, addresses for access to data or data stored in a register-type form, i.e., a heap is stored as volatile data, a complete reconfiguration may take place during run time. Alternatively it is possible to provide nonvolatile memory cells. The nonvolatile memory cells may be provided as an EEPROM area and the like, where a rudimentary BIOS program that is to be executed on boot-up of the system is stored. This permits booting up a data processing system without additional components. A nonvolatile data memory may also be provided if it is decided for reasons

of cost and/or space that the same program parts are always to be executed repeatedly, and it is also possible to alternate among such fixed program parts during operation, e.g., in the manner of a wave reconfiguration. The possibilities of providing and using such nonvolatile memories are the object of other protective rights of the present applicant. It is possible to store both volatile and nonvolatile data in the memory cells, e.g., for permanent storage of a BIOS program, and nevertheless be able to use the memory cell for other purposes.

The memory cell is preferably designed to be able to store a sufficient variety of data to be executed and/or program parts to be executed. It should be pointed out here that these program parts may be designed as program steps, each specifying what an individual PAE, in particular the assigned PAE, i.e., in particular the function cell controlling the memory cell, is to do in the next step, and they may also include entire configurations for field areas or other fields. In such a case, it is readily possible for the sequencer structure that has been created to issue a command on the basis of which cell element field areas are reconfigured. The function cell triggering this configuration then operates as a load logic at the same time. It should be pointed out that the configuration of other cells may in turn be accomplished in such a way that sequencer type data processing is performed there and it is in turn possible in these fields to configure and/or reconfigure other cells in the course of program [execution]. This results in an iterative configuration of cell element areas, and nesting of programs having sequencer structures and parallel structures is possible, these structures being nested one inside the other like babushka dolls. It should be pointed out that access to additional cell element fields outside of an individual integrated module is

possible through input/output cells in particular, which may
massively increase the total computation performance. It is
possible in particular when configurations occur in a code
part of a sequencer structure configured into a cell element
5 field to perform, if necessary, the configuration requirements
on an assigned cell element field which is managed only by the
particular sequencer structure and/or such requirements may be
issued to a configuration master unit to ensure that there is
uniform occupancy of all cell element fields. This therefore
10 results in a quasi-subprogram call by transferring the
required configurations to cells or load logics. This is
regarded as independently patentable. It should be pointed out
that the cells, if they themselves have responsibility for
configuration of other cell element field areas, may be
15 provided with FILMO structures and the like implemented in
hardware or software to ensure proper reconfiguration. The
possibility of writing to memory cells while executing
instructions, thereby altering the code, i.e., the program to
be executed, should be pointed out. In a particularly
20 preferred variant, however, this type of self-modification
(SM) is suppressed by appropriate control via the function
cell.

It is possible for the memory cell to send the information
stored in it directly or indirectly to a bus leading to the
25 function cell in response to the triggering of the function
cell controlling it. Indirect output may be accomplished in
particular when the two cells are adjacent and the information
requested by the triggering must arrive at the ALU-PAE via a
bus segment that is not directly connectable to the output of
30 the memory cell. In such a case the memory cell may output
data onto this bus system in particular via backward
registers. It is therefore preferable if at least one¹ memory

¹ TN: omitting "von" (eine von Speicherzelle...)

cell and/or function cell has such a backward register, which may be situated in the information path between the memory cell and function cell. In such a case, these registers need not necessarily be provided with additional functionalities, although this is readily conceivable, e.g., when data is requested from the memory cell for further processing, corresponding to a traditional LOAD of a typical microprocessor for altering the data even before it is loaded into the PAE, e.g., to implement a LOAD++ command. Data conduction through PAEs having ALUs and the like operating in the reverse direction should be mentioned.

The memory cell is preferably situated to receive information from the function cell controlling it, information saving via an input/output cell and/or a cell that does not control the memory cell also being possible. In particular when data is to be written into the memory cell from an input/output cell, it is preferable if this input/output cell (I/O-PAE) is also controlled by the function cell. The address at which information to be written into the memory cell or, if necessary, to also be transmitted directly to the function cell (PAE) is to be read, may also be transferred to the I/O-PAE from the ALU-PAE. In this connection it should be pointed out that this address may be determined via an address translation table, an address translation buffer or an MMU type structure in the I/O-PAE. In such a case, this yields the full functionalities of typical microprocessors. It should also be pointed out that an I/O functionality may also be integrated with a function cell means, a memory cell means and/or a function cell means-memory cell means combination.

In a preferred variant, at least one input-output means is thus assigned to the combination of function cells and memory cells, whether as an integrated function cell and a memory cell combination or as a function cell and/or memory cell

combination composed of separate units, the input/output means being used to transmit information to and/or receive information from an external unit, another function cell, function cell memory cell combination and/or memory cells.

- 5 The input-output unit is preferably likewise designed for receiving control commands from the function cell and/or the function cell means.

In a preferred variant, the control connection is designed to transmit some and preferably all of the following commands:

- 10 OPCODE FETCH,
DATA WRITE INTERNAL,
DATA WRITE EXTERNAL
DATA READ EXTERNAL,
ADDRESS POINTER WRITE INTERNAL,
15 ADDRESS POINTER WRITE EXTERNAL,
ADDRESS POINTER READ INTERNAL,
ADDRESS POINTER READ EXTERNAL,
PROGRAM POINTER WRITE INTERNAL,
PROGRAM POINTER WRITE EXTERNAL,
20 PROGRAM POINTER READ INTERNAL,
PROGRAM POINTER READ EXTERNAL,
STACK POINTER WRITE INTERNAL,
STACK POINTER WRITE EXTERNAL,
STACK POINTER READ INTERNAL,
25 STACK POINTER READ EXTERNAL,
PUSH,
POP,
PROGRAM POINTER INCREMENT.

This may be accomplished through a corresponding bit width of
30 the control line and an associated decoding at the receivers. The particular required control means and decoding means may be provided inexpensively and with no problems. As it shows, a

practically complete sequencer capability of the arrangement is obtained with these commands. It should also be pointed out that a general-purpose processor data processing unit is obtained in this way.

5 The system is typically selected so that the function cell is the only one able to access the control connection and/or a bus segment, i.e., bus system functioning as the control connection as a master. The result is thus a system in which the control line functions as a command line such as that
10 provided in traditional processors.

The function cell and the memory cell, i.e., I/O cell, are preferably adjacent to one another. The term "adjacent" may be understood preferably as the cells being situated directly side by side. "Directly" means in particular a combination of
15 such cells to form integrated units which are provided repeatedly on the cell element field, i.e., as part of same to form the field. This may mean an integral unit of memory cells and logic cells. Alternatively, they are at least close together. The system of the function cells and memory cells in
20 integrated, i.e., close, proximity to one another thus ensures that there are no latency times, or at least no significant latency times, between triggering and data input of the required information in the function cell, merely because the connections between the cells are too long. This is understood
25 to be "direct." If latency times must be taken into account, pipelining may then also be provided in the sequencer structures. This is particularly important in the case of systems with very high clock rates. It should be pointed out that it is readily possible to provide cell units clocked at a
30 suitably high frequency such as those known in the related art per se which are also able to access suitable memory cells with appropriate speed. In such a case, e.g., when architecture elements that are known per se are used for the

function cells, reconfigurability of the function cell element and the corresponding interconnections must be provided. In a particularly preferred variant, the function cells, the information providing cells such as memory cells, I/O cells
5 and the like are arranged multidimensionally, in particular in the manner of a matrix, i.e., on grid points of a multidimensional grid, etc. If there is a regular structure, as is the case there, information, i.e., operands, configurations, trigger signals, etc., is typically supplied
10 to a cell from a first row, while data, trigger signals and other information is dispensed in a row beneath that. In such a case, it is preferable if the cells are situated in one and the same row and the information transfer from the information-providing cell into the required input into the
15 function cell may then take place via a backward register. The possibility of using the registers for pipelining should also be mentioned.

Patent protection is also claimed for a method for operating a cell element field, in particular a multidimensional cell
20 element field having function cells for execution of algebraic and/or logic functions and information-providing cells, in particular memory cells and/or input/output cells for receiving and/or outputting and/or storing information, at least one of the function cells outputting control commands to
25 at least one information-providing cell, information for the function cell being provided there in response to the control commands, and the function cell being designed to perform the additional data processing in response to the information thus provided to thereby process data in the manner of a sequencer
30 at least from time to time.

Sequencer-type data processing is thus made possible in a reconfigurable field by output of the control commands to the memory cell of the sequencer structure. The commands which may

be output as control commands by the function cell permit a sequencer type operation such as that known from traditional processors. It should be pointed out that it is readily possible to implement only parts of the aforementioned
5 commands but nevertheless ensure data processing that is completely of the sequencer type.

The present invention is described in greater detail below and as an example on the basis of the drawing, in which:

- 10 Fig. 1 shows a cell element field according to the present invention,
- Fig. 2a shows a detail thereof,
- Figs. 2b, c show the detail from Figure 2a during various data processing times,
- 15 Fig. 3 shows an alternative embodiment of the detail from Figure 2,
- Fig. 4 shows a particularly preferred variant of the detail,
- 20 Fig. 5 shows an example of the function folding onto a function cell-memory cell combination according to the present invention,
- Fig. 6a shows an example of sequential parallel data processing
- 25 Fig. 6b shows a particularly preferred exemplary embodiment of the present invention
- Fig. 7 shows an alternative to a function folding unit.

According to Figure 1, a cell element field 1 for data processing includes function cell means 2 for execution of arithmetic and/or logic functions and memory cell means 3 for receiving, storing and/or outputting information, a control connection 4 connecting function cells 2 to memory cells 3.

Cell element field 1 is freely configurable in the interconnection of elements 2, 3, 4, namely without interfering with ongoing operation of cell element parts that are not to be reconfigured. The connections may be configured by switching bus systems 5 as necessary. In addition, the particular functions of function cells 2 are configurable. The function cells are arithmetic logic units extended by certain circuits that permit reconfiguration, e.g., state machines, interface circuit for communication with external load logic 6, etc. Reference is made to the corresponding previous applications of the present applicant.

Cell elements 2, 3 of cell element field 1 are arranged two-dimensionally in rows and columns, one memory cell 3 being situated directly next to a function cell 2 with three memory cell-function cell pairs per row, the function cells and memory cells being interconnected by control connections 4. Function cells and memory cells 2, 3, or the combination thereof have inputs which are connected to the bus system above the row in which the particular cell element is located to receive data therefrom. In addition, cells 2, 3 have outputs which output data to bus system 5 below the row. As explained below, each memory cell 3 is also provided with a backward register (BW) through which data from the bus below a row may be guided through to the bus above the particular row.

Memory cell means 3 preferably has at least three memory areas, namely a data area, a program memory area and a stack area, etc. However, in other variants of the present invention

it may be adequate provide only two areas, namely a data memory and a program area memory, each optionally forming part of a memory cell means. It is possible in particular to perform not simply a separation of a memory that is identical in terms of hardware and is homogeneous per se into different areas but instead to provide memory areas that are actually separated physically, i.e., in terms of hardware technology. In particular the memory width and/or depth may also be adapted to the particular requirements. When a memory is designed in such a way that it has a program area and a data area in operation, it is preferable to design this memory, i.e., memory area for simultaneous access to data and program memory areas, e.g., as a dual port memory. It may also be possible to provide closely connected memory areas, in particular within a memory cell means-function cell means combination formed into an integrated area as a pure cache memory into which data from remote memory sites is preloaded for rapid access during data processing.

Except for control connections 4 and the particular circuits within the function cells (ALU in Figure 2) and/or memory cells (RAM in Figure 2), the cell element field for data processing in Figure 1 is a traditional cell element field such as that which is known and conventional with reconfigurable data processing systems, e.g., a VPU according to XPP technology of the present applicant. In particular, the cell element field of Figure 1 may be operated in the known way, so it has the corresponding circuits for wave reconfiguration, for debugging, transferring trigger signals, etc.

The first distinguishing features of the cell element field of the present invention are derived from control connection 4 and the corresponding circuit, which are described in greater detail below with reference to Figures 2a through 2c. It

should be pointed out that whereas in Figure 1, a control connection 4 always leads from a function cell element located farther to the left to a memory cell located farther to the right, specifically only and exactly to one such memory cell, it is also plausibly possible to provide a configurable interconnection for the control lines to be able to address either memory cells situated elsewhere and/or more than one memory cell, if necessary, when there is a great memory demand for information to be received, stored and/or output by the memory cells. For reasons of comprehensibility, however, only individual control connections which are provided in a fixed manner are referred to in Figures 1 and 2, which greatly simplifies understanding of the present invention. The control connection is also substitutable if necessary by traditional lines, assuming the proper protocols are available.

Figure 2 shows function cell 2 as an ALU and function cell 3 as a RAM. Above the row in which the cells are located runs bus 5a, connecting backward register 3a mentioned above to inputs 3b of the memory cell and 2b of the ALU. The bus system running below the cell is labeled as 5c and only the relevant segments of bus system 5a, 5b are shown here. It is apparent that bus system 5b alternatively receives data from an output 2c of ALU 2, an output 3c of RAM 3 and carries data into input 3a1 of the backward register.

ALU 2 at the same time has additional inputs and outputs 2a1, 2a2 which may be connected to other bus segments and over which the ALU receives data such as operands and outputs results.

Control connection 4 is permanently under control of the extended circuits of the ALU and represents here a connection over which a plurality of bits may be transferred. The width of control connection 4 is selected so that at least the

following control commands may be transmitted to the memory cell: DATA WRITE, DATA READ, ADDRESS POINTER WRITE, ADDRESS POINTER READ, PROGRAM POINTER WRITE, PROGRAM POINTER READ, PROGRAM POINTER INCREMENT, STACK POINTER WRITE, STACK POINTER
5 READ, PUSH, POP. Memory cell 3 at the same time has at least three memory areas, namely a stack area, a heap area and a program area. Each area is assigned its own pointer via which it is determined to which area of the stack, the heap and the program area there will be read or write access in each case.

10 Bus 5a is used jointly by units 2 and 3 in time multiplex. This is indicated in Figures 2b, 2c. Figure 2b illustrates a situation in which data may be sent from output 2a2 of ALU-PAE to the input of the RAM cell via the backward register, whereas the concurrently existing but unused connection
15 between output 3c of the RAM to bus 5b and the connection between the output of backward register BW to input 2b of the ALU-PAE at the point in time of Figure 2b is of no importance, which is why this is indicated with dashed lines. In contrast, Figure 2c shows a point in time at which memory cell 3
20 supplies information via its output 3c and the backward register to input 2b of ALU-PAE 2 from the stack, heap or program memory area via control line 4, while the output of ALU-PAE 2c is inactive and no signal is received at input 3b of the RAM-PAE. For this reason, the corresponding connections
25 are indicated with dash-dot lines and are thus depicted as being inactive.

Within RAM cell 3, a circuit 3d is provided in which the information received via control line 4 and/or control line bus segment 4 is decoded.

30 The present invention is used as follows:

First, ALU 2 receives configuration information from a central load logic, as is already known in the related art. The

transfer of information may take place in a manner known per se using the RDY/ACK protocol and the like. Reference is made to the possibility of providing a FILMO memory, etc., with the load logic to permit a proper configuration of the system.

5 Simultaneously with the data for configuring ALU 2, a series of data is transmitted from the load logic, representing a program, i.e., program part to be executed in the manner of a sequencer. Reference is made in this regard only as an example to Figure 6a in which the HUFFMANN coding is depicted as a
10 central sequential part of an MPEG4 coding which is performed in the manner of data flow per se. The ALU therefore outputs a corresponding command to line 4 during its configuration, this command setting the program pointer for writing at a preselected value within the RAM. The load logic then supplies
15 data received by the ALU over output 2c and via bus 5b1 and backward register 3a, the data going from there to input 3b of RAM-PAE 3. According to the control command on control line 4, data is then written from unit 3d to the program memory location indicated. This is repeated until all the program
20 parts received by the load logic in configuration have been stored in memory cell 3. When the configuration of the ALU is then concluded, the ALU will request the next program steps to be executed by it in the manner of a sequencer by outputting the corresponding commands on control line 4 and will receive
25 the program steps via output 3c, bus 5b, the backward register of RAM-PAE 3 and bus 5a at its input. During program execution, situations may occur in which jumps are necessary within the program memory area, data must be loaded into the ALU-PAE from the RAM-PAE, data must be stored in the stack,
30 etc. The communication in this regard between the ALU-PAE and RAM-PAE is accomplished via control line 4 so that the ALU-PAE is able to execute decoding at any point in time. Moreover, as in a traditional microprocessor, data from a stack or another

RAM memory area may be received and in addition, data may also be received in the ALU-PAE from the outside as operands.

The program sequence preconfigured in the RAM-PAE by the load logic is executed here. At the same time, command decoding is performed in the ALU-PAE as is necessary per se. This is done with the same circuits per se as those used already for decoding the commands received by the load logic.

At any point in time control line 4 is controlled via the ALU so that the RAM cell always exactly follows the type of memory access specified by the ALU. This ensures that regardless of the time multiplex use of bus elements 5a, b the elements present in the sequencer structure are instructed at all times whether addresses for data or codes to be retrieved or to be written is on the buses or whether and if so where data is to be written, etc.

The system shown with respect to Figure 2 may be extended or modified in different ways. The variants depicted in Figures 3, 4 and 6 are particularly relevant.

According to Figure 3, not only a backward register is provided on the RAM-PAE for connecting upper buses and lower buses, but also a forward register is provided on the RAM-PAE and forward and backward registers are provided on the ALU-PAE. As indicated by the multiple arrows, these may receive data from other units such as external hosts, external peripherals such as hard drives, main memories and the like and/or from other sequencer structures, PAEs, RAM-PAEs, etc., and send data to them. When an appropriate request command for new program parts from the sequencer structure formed by the ALU-PAE and the RAM-PAE is sent out, it is possible to process program blocks in the sequencer structure which are much larger than those storable in the RAM-PAE. This is an enormous

advantage in particular in complex data processing tasks, jumps over wide areas, in particular in subprograms, etc.

Figure 4 shows an even more preferred variant where the ALU-PAE communicates not only with a RAM-PAE but also at the same time with an input/output PAE which is designed to provide an interface circuit for communication with external components such as hard drives, other XPP-VPUs, external processors and coprocessors, etc. The ALU-PAE is in turn the unit which operates as the master for the control connection referred to as "CMD" and the buses are in turn used in multiplex mode. Here again, data may be transferred from the bus below the row to the bus above the row through the backward register.

The system shown in Figure 4 permits particularly easy external access to information stored in the RAM-PAE memory cell and thus allows an adaptation of the sequencer structure to existing traditional CPU technologies and their operating methods to an even greater extent inasmuch as address translation means, memory management units (MMU functions) and the like may be implemented in the input-output cell. The RAM-PAE may function here as a cache, for example, but in particular as a preloaded cache.

It should be pointed out that multiple sequencer structures may be configured into one and the same field at the same time; that function cells, memory cells and, if necessary, input-output cells may optionally be configured for sequencer structures and/or [in] a traditional manner for XPP technology and that it is readily possible for one ALU to output data to another ALU, which configures it as a sequencer and/or makes it part of a cell element field with which a certain configuration is executed. In this way, the load logic may then also become dispensable, if necessary.

According to Figure 6, two embodiments of the present invention are combined in one and the same cell element field, namely at the edges of sequencers formed by two PAEs, namely by one RAM-PAE and one ALU-PAE, and in the interior sequencers
5 formed by integrated RAM-ALU-PAEs as integrated function cell-memory cell units, where it is possible to form only part of the cells inside the field as combination cells.

Figure 5 shows at the right (Figure 5c) a function cell-memory cell means combination.

10 According to Figure 5c, a function cell-memory cell means combination labeled as 50 in general includes bus connections, i.e., bus inputs 51 for the input of operand data and configuration data and, as is preferably also possible here in particular, trigger signals (not shown) and the like and a bus
15 output 52 for output of corresponding data and/or signals.

Within the function cell means-memory cell means combination, an ALU 53 is provided as well as input registers Ri0 through Ri3 for operand data and trigger signal input registers (not shown). Configuration data registers Rc0 through Rc7 for
20 configuration data, i.e., ALU code data, result data registers Rd0'-Rd3' and output registers Ro0 through Ro3 for results, i.e., trigger signals to be output. Registers Rc and Rd for the configuration data, i.e., opcode data, are triggered by ALU 53 via control command lines 4 and supply data over
25 suitable data lines to the ALU and/or receive result data from it. It is also possible to supply information directly from bus 51 and/or input registers Ri directly to the output registers, i.e., bus 52, exactly as information may be supplied from data registers Rd0-Rd3 not only to the ALU, but
30 also to the output registers. If necessary, connections may be provided between memory areas Rd and Rc, e.g., for implementation of the possibility of self-modifying codes.

Configuration data area Rc0 through Rc7 has a control unit which makes it possible to work in parts of the area, in particular in repeated cycles and/or through jumps. For example, in a first partial configuration, commands in Rc0
5 through Rc3 may be executed repeatedly, and alternatively configuration commands in Rc4 through Rc7 may be executed, e.g., on receipt of an appropriate different trigger signal over bus line 51. This ensures executability of a wave configuration. It should be pointed out that the configuration
10 commands input are typically only instructions to the ALU but do not define complete bus connections, etc.

The unit described above, illustrated in Figure 5, is designed here to be operated with a quadruple clock pulse, like a normal PAE without memory cell means and/or control signal
15 lines 4.

To process data sequencer-style in a data flow in the function folding unit designed in this way, data flow graphs and/or areas according to Figure 5a are created at first for preselected algorithms. Memory areas Rc0 are then assigned to
20 each operation to be executed in the graph; incoming data into the graph partial area is assigned to internal input registers Ri0; the interim results are assigned to memories Rd0 through Rd3 and the output results are assigned to registers Ro. With this assignment, the graph area is executable on the function
25 folding unit. This results more or less in a data flow-sequencer transformation by this hardware.

It should be mentioned in this context that it will be preferable in general to use the system of the present invention in such a way that first a data flow graph and a
30 control flow graph are created for a data processing program using a compiler and then a corresponding partitioning is performed; the pieces obtained by the partitioning may then be

executed partially or entirely on sequencer units such as those which may be formed according to the present invention, for example. This more or less achieves data processing in the manner of data flow progressing from one cell to the next, but effects a sequential execution within the cell(s). This is advantageous when the clock frequency is to be increased because of the extremely high computation power of a system to be able to reduce the area and/or number of cells. It should also be pointed out that it is possible to perform this transformation like transition from a purely data flow type of data processing to data flow processing with local sequential parts in such a way that an iterative process is carried out, e.g., in such a manner that first a first partitioning is performed, and if it is then found in the subsequent "rolling up" of the partitioned parts on sequencer units that the resources available on the sequencers or at other sites, for example, are not sufficient, another partitioning taking this into account may be performed and a new "rolling up" may be performed. If extensive use of the function folding units is desired, the number of registers may be increased, if necessary.

It should also be pointed out that the registers in this case may be interpreted as memory cell means or parts thereof. It is apparent that by increasing the memory cell areas, more complex tasks may be arranged in particular in a sequencer fashion but significant parts of important algorithms may be executed with the small sizes indicated and this may be done with high efficiency.

In the present example, the function folding units are preferably formed in such a way that data may be shifted through them without being processed in the ALU. This may be utilized to achieve path balancing in which data packets must be executed via different branches and then recombined without

having to use forward registers such as those known from the architecture of the present applicant. At the same time and/or alternatively, it is possible for the direction of data flow not to run strictly in one direction in the cell element field through an appropriate orientation of a few function cell means, memory cell means, or function folding units but instead to have the data flow run in two opposite directions. Thus, for example, in each even row the ALUs receive their input operands from the left side and in each uneven row the ALUs receive their input operands from the right.

If data must be sent repeatedly through the field, such an arrangement is advantageous, e.g., in the case of unrolled looped bodies, etc. The alternating arrangement need not be strict. For certain applications, other geometries may be selected. For example, a different direction of flow may be selected for the middle of the field than at the edges, etc. The arrangement of function cell units of the same direction of flow side by side may be advantageous with respect to the bus connections. It should be pointed out that the arrangement in opposite directions of multiple directional function cells in one field and the resulting improved data processing independently of providing a control line or the like are regarded as inventive.

Figure 7 shows an alternative to the function folding unit shown in Figure 5.

RECONFIGURABLE SEQUENCER STRUCTURE

Cross-Reference to Related Applications

5 This application is a continuation of U.S. Patent Application
Serial No. 12/541,299, filed on August 14, 2009, which is a
continuation of and claims priority to U.S. Patent Application
Serial No. 12/082,073, filed on April 7, 2008, which is a
continuation of and claims priority to U.S. Patent Application
10 Serial No. 10/526,595, filed on January 9, 2006, which was the
National Stage of International Application Serial No.
PCT/EP03/38599, filed on September 8, 2003, which claims
benefit of and priority to German Patent Application Serial
No. DE 102 41 812.8, filed on September 6, 2002, the entire
15 contents of each of which are expressly incorporated herein by
reference thereto.

Description

The present invention relates to a cell element field and a
method for operating same. The present invention thus relates
20 in particular to reconfigurable data processing architectures.

The term reconfigurable architecture is understood to refer to
units (VPUs) having a plurality of elements whose function
and/or interconnection is variable during run time. These
elements may include arithmetic logic units, FPGA areas,
25 input/output cells, memory cells, analog modules, etc. Units
of this type are known by the term VPU, for example. These
typically include arithmetic and/or logic and/or analog and/or
memory and/or interconnecting modules and/or communicative
peripheral modules (IOs), typically referred to as PAEs, which
30 are arranged in one or more dimensions and are linked together
directly or by one or more bus systems. PAEs are arranged in

any configuration, mixture and hierarchy, the system being known as a PAE array or, for short, a PA. A configuring unit may be assigned to the PAE. In addition to VPU units, in principle systolic arrays, neural networks, multiprocessor systems, processors having multiple arithmetic units and/or logic cells, interconnection and network modules such as crossbar circuits, etc., as well as FPGAs, DPGAs, transputers, etc., are also known

It should be pointed out that essential aspects of VPU technology are described in the following protective rights of the same applicant as well as in the particular follow-up applications to the protective rights listed here:

P 44 16 881.0-53, DE 197 81 412.3, DE 197 81 483.2,
DE 196 54 846.2-53, DE 196 54 593.5-53, DE 197 04 044.6-53,
DE 198 80 129.7, DE 198 61 088.2-53, DE 199 80 312.9,
PCT/DE 00/01869, DE 100 36 627.9-33, DE 100 28 397.7,
DE 101 10 530.4, DE 101 11 014.6, PCT/EP 00/10516,
EP 01 102 674.7, DE 102 06 856.9, 60/317,876, DE 102 02 044.2,
DE 101 29 237.6-53, DE 101 39 170.6.

It should be pointed out that the documents listed above are incorporated in particular with regard to particulars and details of the interconnection, configuration, embodiment of architecture elements, trigger methods, etc., for disclosure purposes.

The architecture has considerable advantages in comparison with traditional processor architectures inasmuch as data processing is performed in a manner having a large proportion of parallel and/or vectorial data processing steps. However, the advantages of this architecture in comparison with other processor units, coprocessor units or data processing units in general are not as great when the advantages of

interconnection and of the given processor architectonic particulars are no longer achievable to the full extent.

This is the case in particular when data processing steps that are traditionally best mappable on sequencer structures are to be executed. It is desirable to design and use the reconfigurable architecture in such a way that even those data processing steps which are typically particularly suitable for being executed using sequencers are executable particularly rapidly and efficiently.

10 The object of the present invention is to provide a novel device and a novel method for commercial application.

The method of achieving this object is claimed independently. Preferred embodiments are characterized in the subclaims.

According to a first essential aspect of the present invention, in the case of a cell element field whose function and/or interconnection is reconfigurable in particular during run time without interfering with unreconfigured elements for data processing with coarsely granular function cell elements in particular for execution of algebraic and/or logic functions and memory cell means for receiving, storing and/or outputting information, it is proposed that function cell-memory cell combinations be formed in which a control connection to the memory means is managed by the function cell means. This control connection is for making the address and/or data input/output from the memory controllable through the particular function cell, typically an ALU-PAE. It is thus possible to indicate, for example, whether the next item of information transmitted is to be handled as an address or as data and whether read and/or write access is necessary. This transfer of data from the memory cell, i.e., the memory cell means, which may be a RAM-PAE, for example, to the function cell means, which may be an ALU-PAE, for example, then makes

it possible for new commands that are to be executed by the ALU to be loadable into the latter. It should be pointed out that function cell means and memory cell means may be combined by integration into a structural unit. In such a case it is possible to use a single bus connection to input data into the memory cell means and/or the ALU. Suitable input registers and/or output registers may then be provided and, if desired, additional data registers and/or configuration registers different from the former may also be provided as memory cell means.

It should also be pointed out that it is possible to construct a cell element field containing a plurality of different cells and/or cell groups, strips or similar regular patterns being preferably provided with the different cells because these permit a very regular arrangement while facilitating the design equally in terms of hardware design and operation. With such a strip-like arrangement or other regular layout of a small plurality of different cell elements, for example, elements having integrated function cell means-memory cell means combinations, i.e., cells in which function cell means and memory cell means are integrated according to the present invention, are provided centrally in the field, where typically only a few different program steps are to be executed within a sequencer structure because, as has been recognized, this provides very good results for traditional data stream applications, while more complex sequencer structures may be constructed at the edges of the field where, for example, an ALU-PAE which represents a separate unit possibly may be provided in addition to a separate RAM-PAE and optionally a number of I/O-PAEs using, i.e., arranging appropriate control lines or connections thereof because frequently more memory is needed there, e.g., to temporarily store results generated in the field central area of the cell

element field and/or for datastreaming, to pre-enter and/or process data needed thereby.

When cells that integrate memory cell means and function cell means are provided, e.g., in the center of the field, a small
5 memory may then be provided there for different commands to be executed by the function cell means such as the ALU. It is possible here in particular to separate the command memory and/or the configuration memory from a data memory, and it is possible to design the function memory to be so large that
10 alternatively, one of several, e.g., two different sequences may be executed. The particular sequence to be executed may occur in response to results generated in the cell and/or control signals such as carry signals, overflow signals, and/or trigger signals arriving from the outside. In this way,
15 this arrangement may also be used for wave reconfiguration methods.

In this way it is possible to construct a sequencer structure in a cell element field by providing a dedicated control connection controlled by function cells in a dedicated manner
20 between function cell and function cell means and memory cell and/or memory cell means with only two elements connected by suitable buses without requiring additional measures and/or design changes otherwise. Data, addresses, program steps, etc., may be stored in the memory cell in a manner known per
25 se from traditional processors. Since both elements, if properly configured, may also be used in another way, this yields a particularly efficient design which is particularly adaptable to sequencer structures as well as vectorial and/or parallelizable structures. Parallelization may thus be
30 supported merely via suitable PAE configurations, i.e., by providing PAEs that operate in two different spatial directions and/or via cell units equipped with data throughput registers.

It is clear here that a plurality of sequencer type structures may be constructed in the reconfigurable cell element field by using only two cells in a cell element field, namely the function cell and the information processing cell. This is
5 advantageous inasmuch as a number of different tasks that are different from one another per se must often be executed in data processing, e.g., in a multitasking-capable operating system. A plurality of such tasks must then be executed effectively and simultaneously in a single cell element field.
10 The advantages of real time applications are obvious. Furthermore it is also possible to operate the individual sequencer structures that are constructed in a cell element field, providing the control connection according to the present invention, at different clock rates, e.g., to lower
15 power consumption by executing lower priority tasks at a slower rate. It is also possible to execute sequencer type program parts in the field in parallel or vectorially in execution of algorithms that are largely parallel per se and vice versa.

20 Typically, however, it is preferable for sequencer-type structures to be clocked at a higher rate in the cell element field, whether they are sequencer-type structures having an area connected to neighboring cells or buses or whether they are combinations of spatially differentiable separate and
25 separately useable function cell elements such as ALU-PAEs and memory cell elements such as RAM-PAEs. This has the advantage that sequential program parts, which are very difficult to parallelize in any case, may be used in a general data flow processing without any negative effect on the overall data
30 processing. Examples of this include, e.g., a HUFFMANN coding which is executable much better sequentially than in parallel and which also plays an important role for applications such as MPEG4 coding, but in this case the essential other parts of

the MPEG4 coding are also easily parallelizable. Parallel data processing is then used for most parts of an algorithm and a sequential processing block is provided therein. An increase in the clock frequency in the sequencer range by a factor of 2 to 4 is typically sufficient.

It should be pointed out that instead of a strip arrangement of different cell elements, another grouping, in particular a multidimensional grouping, may also be selected.

The cell element field having the cells whose function and/or interconnection is configurable may obviously form a processor, a coprocessor and/or a microcontroller and/or a parallel plurality of combinations thereof.

The function cells are typically formed as arithmetic logic units, which may be in particular coarsely granular elements but may also be provided with a fine granular state machine, for example. In a particularly preferred exemplary embodiment, the ALUs are extended ALUs (EALUs) as described in previous patent applications of the present applicant. An extension may include in particular the control line check, command decoder unit, etc., if necessary.

The memory cells may store data and/or information in a volatile and/or nonvolatile form. When information stored in the memory cells, whether program steps, addresses for access to data or data stored in a register-type form, i.e., a heap is stored as volatile data, a complete reconfiguration may take place during run time. Alternatively it is possible to provide nonvolatile memory cells. The nonvolatile memory cells may be provided as an EEPROM area and the like, where a rudimentary BIOS program that is to be executed on boot-up of the system is stored. This permits booting up a data processing system without additional components. A nonvolatile data memory may also be provided if it is decided for reasons

of cost and/or space that the same program parts are always to be executed repeatedly, and it is also possible to alternate among such fixed program parts during operation, e.g., in the manner of a wave reconfiguration. The possibilities of providing and using such nonvolatile memories are the object of other protective rights of the present applicant. It is possible to store both volatile and nonvolatile data in the memory cells, e.g., for permanent storage of a BIOS program, and nevertheless be able to use the memory cell for other purposes.

The memory cell is preferably designed to be able to store a sufficient variety of data to be executed and/or program parts to be executed. It should be pointed out here that these program parts may be designed as program steps, each specifying what an individual PAE, in particular the assigned PAE, i.e., in particular the function cell controlling the memory cell, is to do in the next step, and they may also include entire configurations for field areas or other fields. In such a case, it is readily possible for the sequencer structure that has been created to issue a command on the basis of which cell element field areas are reconfigured. The function cell triggering this configuration then operates as a load logic at the same time. It should be pointed out that the configuration of other cells may in turn be accomplished in such a way that sequencer type data processing is performed there and it is in turn possible in these fields to configure and/or reconfigure other cells in the course of program [execution]. This results in an iterative configuration of cell element areas, and nesting of programs having sequencer structures and parallel structures is possible, these structures being nested one inside the other like babushka dolls. It should be pointed out that access to additional cell element fields outside of an individual integrated module is

possible through input/output cells in particular, which may
massively increase the total computation performance. It is
possible in particular when configurations occur in a code
part of a sequencer structure configured into a cell element
5 field to perform, if necessary, the configuration requirements
on an assigned cell element field which is managed only by the
particular sequencer structure and/or such requirements may be
issued to a configuration master unit to ensure that there is
uniform occupancy of all cell element fields. This therefore
10 results in a quasi-subprogram call by transferring the
required configurations to cells or load logics. This is
regarded as independently patentable. It should be pointed out
that the cells, if they themselves have responsibility for
configuration of other cell element field areas, may be
15 provided with FILMO structures and the like implemented in
hardware or software to ensure proper reconfiguration. The
possibility of writing to memory cells while executing
instructions, thereby altering the code, i.e., the program to
be executed, should be pointed out. In a particularly
20 preferred variant, however, this type of self-modification
(SM) is suppressed by appropriate control via the function
cell.

It is possible for the memory cell to send the information
stored in it directly or indirectly to a bus leading to the
25 function cell in response to the triggering of the function
cell controlling it. Indirect output may be accomplished in
particular when the two cells are adjacent and the information
requested by the triggering must arrive at the ALU-PAE via a
bus segment that is not directly connectable to the output of
30 the memory cell. In such a case the memory cell may output
data onto this bus system in particular via backward
registers. It is therefore preferable if at least one¹ memory

¹ TN: omitting "von" (eine von Speicherzelle...)

cell and/or function cell has such a backward register, which may be situated in the information path between the memory cell and function cell. In such a case, these registers need not necessarily be provided with additional functionalities, although this is readily conceivable, e.g., when data is requested from the memory cell for further processing, corresponding to a traditional LOAD of a typical microprocessor for altering the data even before it is loaded into the PAE, e.g., to implement a LOAD++ command. Data conduction through PAEs having ALUs and the like operating in the reverse direction should be mentioned.

The memory cell is preferably situated to receive information from the function cell controlling it, information saving via an input/output cell and/or a cell that does not control the memory cell also being possible. In particular when data is to be written into the memory cell from an input/output cell, it is preferable if this input/output cell (I/O-PAE) is also controlled by the function cell. The address at which information to be written into the memory cell or, if necessary, to also be transmitted directly to the function cell (PAE) is to be read, may also be transferred to the I/O-PAE from the ALU-PAE. In this connection it should be pointed out that this address may be determined via an address translation table, an address translation buffer or an MMU type structure in the I/O-PAE. In such a case, this yields the full functionalities of typical microprocessors. It should also be pointed out that an I/O functionality may also be integrated with a function cell means, a memory cell means and/or a function cell means-memory cell means combination.

In a preferred variant, at least one input-output means is thus assigned to the combination of function cells and memory cells, whether as an integrated function cell and a memory cell combination or as a function cell and/or memory cell

combination composed of separate units, the input/output means being used to transmit information to and/or receive information from an external unit, another function cell, function cell memory cell combination and/or memory cells.

- 5 The input-output unit is preferably likewise designed for receiving control commands from the function cell and/or the function cell means.

In a preferred variant, the control connection is designed to transmit some and preferably all of the following commands:

- 10 OPCODE FETCH,
DATA WRITE INTERNAL,
DATA WRITE EXTERNAL
DATA READ EXTERNAL,
ADDRESS POINTER WRITE INTERNAL,
15 ADDRESS POINTER WRITE EXTERNAL,
ADDRESS POINTER READ INTERNAL,
ADDRESS POINTER READ EXTERNAL,
PROGRAM POINTER WRITE INTERNAL,
PROGRAM POINTER WRITE EXTERNAL,
20 PROGRAM POINTER READ INTERNAL,
PROGRAM POINTER READ EXTERNAL,
STACK POINTER WRITE INTERNAL,
STACK POINTER WRITE EXTERNAL,
STACK POINTER READ INTERNAL,
25 STACK POINTER READ EXTERNAL,
PUSH,
POP,
PROGRAM POINTER INCREMENT.

This may be accomplished through a corresponding bit width of
30 the control line and an associated decoding at the receivers.
The particular required control means and decoding means may be provided inexpensively and with no problems. As it shows, a

practically complete sequencer capability of the arrangement is obtained with these commands. It should also be pointed out that a general-purpose processor data processing unit is obtained in this way.

5 The system is typically selected so that the function cell is the only one able to access the control connection and/or a bus segment, i.e., bus system functioning as the control connection as a master. The result is thus a system in which the control line functions as a command line such as that
10 provided in traditional processors.

The function cell and the memory cell, i.e., I/O cell, are preferably adjacent to one another. The term "adjacent" may be understood preferably as the cells being situated directly side by side. "Directly" means in particular a combination of
15 such cells to form integrated units which are provided repeatedly on the cell element field, i.e., as part of same to form the field. This may mean an integral unit of memory cells and logic cells. Alternatively, they are at least close together. The system of the function cells and memory cells in
20 integrated, i.e., close, proximity to one another thus ensures that there are no latency times, or at least no significant latency times, between triggering and data input of the required information in the function cell, merely because the connections between the cells are too long. This is understood
25 to be "direct." If latency times must be taken into account, pipelining may then also be provided in the sequencer structures. This is particularly important in the case of systems with very high clock rates. It should be pointed out that it is readily possible to provide cell units clocked at a
30 suitably high frequency such as those known in the related art per se which are also able to access suitable memory cells with appropriate speed. In such a case, e.g., when architecture elements that are known per se are used for the

function cells, reconfigurability of the function cell element and the corresponding interconnections must be provided. In a particularly preferred variant, the function cells, the information providing cells such as memory cells, I/O cells and the like are arranged multidimensionally, in particular in the manner of a matrix, i.e., on grid points of a multidimensional grid, etc. If there is a regular structure, as is the case there, information, i.e., operands, configurations, trigger signals, etc., is typically supplied to a cell from a first row, while data, trigger signals and other information is dispensed in a row beneath that. In such a case, it is preferable if the cells are situated in one and the same row and the information transfer from the information-providing cell into the required input into the function cell may then take place via a backward register. The possibility of using the registers for pipelining should also be mentioned.

Patent protection is also claimed for a method for operating a cell element field, in particular a multidimensional cell element field having function cells for execution of algebraic and/or logic functions and information-providing cells, in particular memory cells and/or input/output cells for receiving and/or outputting and/or storing information, at least one of the function cells outputting control commands to at least one information-providing cell, information for the function cell being provided there in response to the control commands, and the function cell being designed to perform the additional data processing in response to the information thus provided to thereby process data in the manner of a sequencer at least from time to time.

Sequencer-type data processing is thus made possible in a reconfigurable field by output of the control commands to the memory cell of the sequencer structure. The commands which may

be output as control commands by the function cell permit a sequencer type operation such as that known from traditional processors. It should be pointed out that it is readily possible to implement only parts of the aforementioned
5 commands but nevertheless ensure data processing that is completely of the sequencer type.

The present invention is described in greater detail below and as an example on the basis of the drawing, in which:

- 10 Fig. 1 shows a cell element field according to the present invention,
- Fig. 2a shows a detail thereof,
- Figs. 2b, c show the detail from Figure 2a during various data processing times,
- 15 Fig. 3 shows an alternative embodiment of the detail from Figure 2,
- Fig. 4 shows a particularly preferred variant of the detail,
- 20 Fig. 5 shows an example of the function folding onto a function cell-memory cell combination according to the present invention,
- Fig. 6a shows an example of sequential parallel data processing
- 25 Fig. 6b shows a particularly preferred exemplary embodiment of the present invention
- Fig. 7 shows an alternative to a function folding unit.

According to Figure 1, a cell element field 1 for data processing includes function cell means 2 for execution of arithmetic and/or logic functions and memory cell means 3 for receiving, storing and/or outputting information, a control connection 4 connecting function cells 2 to memory cells 3.

Cell element field 1 is freely configurable in the interconnection of elements 2, 3, 4, namely without interfering with ongoing operation of cell element parts that are not to be reconfigured. The connections may be configured by switching bus systems 5 as necessary. In addition, the particular functions of function cells 2 are configurable. The function cells are arithmetic logic units extended by certain circuits that permit reconfiguration, e.g., state machines, interface circuit for communication with external load logic 6, etc. Reference is made to the corresponding previous applications of the present applicant.

Cell elements 2, 3 of cell element field 1 are arranged two-dimensionally in rows and columns, one memory cell 3 being situated directly next to a function cell 2 with three memory cell-function cell pairs per row, the function cells and memory cells being interconnected by control connections 4. Function cells and memory cells 2, 3, or the combination thereof have inputs which are connected to the bus system above the row in which the particular cell element is located to receive data therefrom. In addition, cells 2, 3 have outputs which output data to bus system 5 below the row. As explained below, each memory cell 3 is also provided with a backward register (BW) through which data from the bus below a row may be guided through to the bus above the particular row.

Memory cell means 3 preferably has at least three memory areas, namely a data area, a program memory area and a stack area, etc. However, in other variants of the present invention

it may be adequate provide only two areas, namely a data memory and a program area memory, each optionally forming part of a memory cell means. It is possible in particular to perform not simply a separation of a memory that is identical in terms of hardware and is homogeneous per se into different areas but instead to provide memory areas that are actually separated physically, i.e., in terms of hardware technology. In particular the memory width and/or depth may also be adapted to the particular requirements. When a memory is designed in such a way that it has a program area and a data area in operation, it is preferable to design this memory, i.e., memory area for simultaneous access to data and program memory areas, e.g., as a dual port memory. It may also be possible to provide closely connected memory areas, in particular within a memory cell means-function cell means combination formed into an integrated area as a pure cache memory into which data from remote memory sites is preloaded for rapid access during data processing.

Except for control connections 4 and the particular circuits within the function cells (ALU in Figure 2) and/or memory cells (RAM in Figure 2), the cell element field for data processing in Figure 1 is a traditional cell element field such as that which is known and conventional with reconfigurable data processing systems, e.g., a VPU according to XPP technology of the present applicant. In particular, the cell element field of Figure 1 may be operated in the known way, so it has the corresponding circuits for wave reconfiguration, for debugging, transferring trigger signals, etc.

The first distinguishing features of the cell element field of the present invention are derived from control connection 4 and the corresponding circuit, which are described in greater detail below with reference to Figures 2a through 2c. It

should be pointed out that whereas in Figure 1, a control connection 4 always leads from a function cell element located farther to the left to a memory cell located farther to the right, specifically only and exactly to one such memory cell, it is also plausibly possible to provide a configurable interconnection for the control lines to be able to address either memory cells situated elsewhere and/or more than one memory cell, if necessary, when there is a great memory demand for information to be received, stored and/or output by the memory cells. For reasons of comprehensibility, however, only individual control connections which are provided in a fixed manner are referred to in Figures 1 and 2, which greatly simplifies understanding of the present invention. The control connection is also substitutable if necessary by traditional lines, assuming the proper protocols are available.

Figure 2 shows function cell 2 as an ALU and function cell 3 as a RAM. Above the row in which the cells are located runs bus 5a, connecting backward register 3a mentioned above to inputs 3b of the memory cell and 2b of the ALU. The bus system running below the cell is labeled as 5c and only the relevant segments of bus system 5a, 5b are shown here. It is apparent that bus system 5b alternatively receives data from an output 2c of ALU 2, an output 3c of RAM 3 and carries data into input 3a1 of the backward register.

ALU 2 at the same time has additional inputs and outputs 2a1, 2a2 which may be connected to other bus segments and over which the ALU receives data such as operands and outputs results.

Control connection 4 is permanently under control of the extended circuits of the ALU and represents here a connection over which a plurality of bits may be transferred. The width of control connection 4 is selected so that at least the

following control commands may be transmitted to the memory cell: DATA WRITE, DATA READ, ADDRESS POINTER WRITE, ADDRESS POINTER READ, PROGRAM POINTER WRITE, PROGRAM POINTER READ, PROGRAM POINTER INCREMENT, STACK POINTER WRITE, STACK POINTER
5 READ, PUSH, POP. Memory cell 3 at the same time has at least three memory areas, namely a stack area, a heap area and a program area. Each area is assigned its own pointer via which it is determined to which area of the stack, the heap and the program area there will be read or write access in each case.

10 Bus 5a is used jointly by units 2 and 3 in time multiplex. This is indicated in Figures 2b, 2c. Figure 2b illustrates a situation in which data may be sent from output 2a2 of ALU-PAE to the input of the RAM cell via the backward register, whereas the concurrently existing but unused connection
15 between output 3c of the RAM to bus 5b and the connection between the output of backward register BW to input 2b of the ALU-PAE at the point in time of Figure 2b is of no importance, which is why this is indicated with dashed lines. In contrast, Figure 2c shows a point in time at which memory cell 3
20 supplies information via its output 3c and the backward register to input 2b of ALU-PAE 2 from the stack, heap or program memory area via control line 4, while the output of ALU-PAE 2c is inactive and no signal is received at input 3b of the RAM-PAE. For this reason, the corresponding connections
25 are indicated with dash-dot lines and are thus depicted as being inactive.

Within RAM cell 3, a circuit 3d is provided in which the information received via control line 4 and/or control line bus segment 4 is decoded.

30 The present invention is used as follows:

First, ALU 2 receives configuration information from a central load logic, as is already known in the related art. The

transfer of information may take place in a manner known per se using the RDY/ACK protocol and the like. Reference is made to the possibility of providing a FILMO memory, etc., with the load logic to permit a proper configuration of the system.

5 Simultaneously with the data for configuring ALU 2, a series of data is transmitted from the load logic, representing a program, i.e., program part to be executed in the manner of a sequencer. Reference is made in this regard only as an example to Figure 6a in which the HUFFMANN coding is depicted as a
10 central sequential part of an MPEG4 coding which is performed in the manner of data flow per se. The ALU therefore outputs a corresponding command to line 4 during its configuration, this command setting the program pointer for writing at a preselected value within the RAM. The load logic then supplies
15 data received by the ALU over output 2c and via bus 5b1 and backward register 3a, the data going from there to input 3b of RAM-PAE 3. According to the control command on control line 4, data is then written from unit 3d to the program memory location indicated. This is repeated until all the program
20 parts received by the load logic in configuration have been stored in memory cell 3. When the configuration of the ALU is then concluded, the ALU will request the next program steps to be executed by it in the manner of a sequencer by outputting the corresponding commands on control line 4 and will receive
25 the program steps via output 3c, bus 5b, the backward register of RAM-PAE 3 and bus 5a at its input. During program execution, situations may occur in which jumps are necessary within the program memory area, data must be loaded into the ALU-PAE from the RAM-PAE, data must be stored in the stack,
30 etc. The communication in this regard between the ALU-PAE and RAM-PAE is accomplished via control line 4 so that the ALU-PAE is able to execute decoding at any point in time. Moreover, as in a traditional microprocessor, data from a stack or another

RAM memory area may be received and in addition, data may also be received in the ALU-PAE from the outside as operands.

The program sequence preconfigured in the RAM-PAE by the load logic is executed here. At the same time, command decoding is performed in the ALU-PAE as is necessary per se. This is done with the same circuits per se as those used already for decoding the commands received by the load logic.

At any point in time control line 4 is controlled via the ALU so that the RAM cell always exactly follows the type of memory access specified by the ALU. This ensures that regardless of the time multiplex use of bus elements 5a, b the elements present in the sequencer structure are instructed at all times whether addresses for data or codes to be retrieved or to be written is on the buses or whether and if so where data is to be written, etc.

The system shown with respect to Figure 2 may be extended or modified in different ways. The variants depicted in Figures 3, 4 and 6 are particularly relevant.

According to Figure 3, not only a backward register is provided on the RAM-PAE for connecting upper buses and lower buses, but also a forward register is provided on the RAM-PAE and forward and backward registers are provided on the ALU-PAE. As indicated by the multiple arrows, these may receive data from other units such as external hosts, external peripherals such as hard drives, main memories and the like and/or from other sequencer structures, PAEs, RAM-PAEs, etc., and send data to them. When an appropriate request command for new program parts from the sequencer structure formed by the ALU-PAE and the RAM-PAE is sent out, it is possible to process program blocks in the sequencer structure which are much larger than those storable in the RAM-PAE. This is an enormous

advantage in particular in complex data processing tasks,
jumps over wide areas, in particular in subprograms, etc.

Figure 4 shows an even more preferred variant where the ALU-
PAE communicates not only with a RAM-PAE but also at the same
5 time with an input/output PAE which is designed to provide an
interface circuit for communication with external components
such as hard drives, other XPP-VPUs, external processors and
coprocessors, etc. The ALU-PAE is in turn the unit which
operates as the master for the control connection referred to
10 as "CMD" and the buses are in turn used in multiplex mode.
Here again, data may be transferred from the bus below the row
to the bus above the row through the backward register.

The system shown in Figure 4 permits particularly easy
external access to information stored in the RAM-PAE memory
15 cell and thus allows an adaptation of the sequencer structure
to existing traditional CPU technologies and their operating
methods to an even greater extent inasmuch as address
translation means, memory management units (MMU functions) and
the like may be implemented in the input-output cell. The RAM-
20 PAE may function here as a cache, for example, but in
particular as a preloaded cache.

It should be pointed out that multiple sequencer structures
may be configured into one and the same field at the same
time; that function cells, memory cells and, if necessary,
25 input-output cells may optionally be configured for sequencer
structures and/or [in] a traditional manner for XPP technology
and that it is readily possible for one ALU to output data to
another ALU, which configures it as a sequencer and/or makes
it part of a cell element field with which a certain
30 configuration is executed. In this way, the load logic may
then also become dispensable, if necessary.

According to Figure 6, two embodiments of the present invention are combined in one and the same cell element field, namely at the edges of sequencers formed by two PAEs, namely by one RAM-PAE and one ALU-PAE, and in the interior sequencers
5 formed by integrated RAM-ALU-PAEs as integrated function cell-memory cell units, where it is possible to form only part of the cells inside the field as combination cells.

Figure 5 shows at the right (Figure 5c) a function cell-memory cell means combination.

10 According to Figure 5c, a function cell-memory cell means combination labeled as 50 in general includes bus connections, i.e., bus inputs 51 for the input of operand data and configuration data and, as is preferably also possible here in particular, trigger signals (not shown) and the like and a bus
15 output 52 for output of corresponding data and/or signals.

Within the function cell means-memory cell means combination, an ALU 53 is provided as well as input registers Ri0 through Ri3 for operand data and trigger signal input registers (not shown). Configuration data registers Rc0 through Rc7 for
20 configuration data, i.e., ALU code data, result data registers Rd0'-Rd3' and output registers Ro0 through Ro3 for results, i.e., trigger signals to be output. Registers Rc and Rd for the configuration data, i.e., opcode data, are triggered by ALU 53 via control command lines 4 and supply data over
25 suitable data lines to the ALU and/or receive result data from it. It is also possible to supply information directly from bus 51 and/or input registers Ri directly to the output registers, i.e., bus 52, exactly as information may be supplied from data registers Rd0-Rd3 not only to the ALU, but
30 also to the output registers. If necessary, connections may be provided between memory areas Rd and Rc, e.g., for implementation of the possibility of self-modifying codes.

Configuration data area Rc0 through Rc7 has a control unit which makes it possible to work in parts of the area, in particular in repeated cycles and/or through jumps. For example, in a first partial configuration, commands in Rc0 through Rc3 may be executed repeatedly, and alternatively configuration commands in Rc4 through Rc7 may be executed, e.g., on receipt of an appropriate different trigger signal over bus line 51. This ensures executability of a wave configuration. It should be pointed out that the configuration commands input are typically only instructions to the ALU but do not define complete bus connections, etc.

The unit described above, illustrated in Figure 5, is designed here to be operated with a quadruple clock pulse, like a normal PAE without memory cell means and/or control signal lines 4.

To process data sequencer-style in a data flow in the function folding unit designed in this way, data flow graphs and/or areas according to Figure 5a are created at first for preselected algorithms. Memory areas Rc0 are then assigned to each operation to be executed in the graph; incoming data into the graph partial area is assigned to internal input registers Ri0; the interim results are assigned to memories Rd0 through Rd3 and the output results are assigned to registers Ro. With this assignment, the graph area is executable on the function folding unit. This results more or less in a data flow-sequencer transformation by this hardware.

It should be mentioned in this context that it will be preferable in general to use the system of the present invention in such a way that first a data flow graph and a control flow graph are created for a data processing program using a compiler and then a corresponding partitioning is performed; the pieces obtained by the partitioning may then be

executed partially or entirely on sequencer units such as those which may be formed according to the present invention, for example. This more or less achieves data processing in the manner of data flow progressing from one cell to the next, but effects a sequential execution within the cell(s). This is advantageous when the clock frequency is to be increased because of the extremely high computation power of a system to be able to reduce the area and/or number of cells. It should also be pointed out that it is possible to perform this transformation like transition from a purely data flow type of data processing to data flow processing with local sequential parts in such a way that an iterative process is carried out, e.g., in such a manner that first a first partitioning is performed, and if it is then found in the subsequent "rolling up" of the partitioned parts on sequencer units that the resources available on the sequencers or at other sites, for example, are not sufficient, another partitioning taking this into account may be performed and a new "rolling up" may be performed. If extensive use of the function folding units is desired, the number of registers may be increased, if necessary.

It should also be pointed out that the registers in this case may be interpreted as memory cell means or parts thereof. It is apparent that by increasing the memory cell areas, more complex tasks may be arranged in particular in a sequencer fashion but significant parts of important algorithms may be executed with the small sizes indicated and this may be done with high efficiency.

In the present example, the function folding units are preferably formed in such a way that data may be shifted through them without being processed in the ALU. This may be utilized to achieve path balancing in which data packets must be executed via different branches and then recombined without

having to use forward registers such as those known from the architecture of the present applicant. At the same time and/or alternatively, it is possible for the direction of data flow not to run strictly in one direction in the cell element field through an appropriate orientation of a few function cell means, memory cell means, or function folding units but instead to have the data flow run in two opposite directions. Thus, for example, in each even row the ALUs receive their input operands from the left side and in each uneven row the ALUs receive their input operands from the right.

If data must be sent repeatedly through the field, such an arrangement is advantageous, e.g., in the case of unrolled looped bodies, etc. The alternating arrangement need not be strict. For certain applications, other geometries may be selected. For example, a different direction of flow may be selected for the middle of the field than at the edges, etc. The arrangement of function cell units of the same direction of flow side by side may be advantageous with respect to the bus connections. It should be pointed out that the arrangement in opposite directions of multiple directional function cells in one field and the resulting improved data processing independently of providing a control line or the like are regarded as inventive.

Figure 7 shows an alternative to the function folding unit shown in Figure 5.

**U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE**

INFORMATION DISCLOSURE STATEMENT		Docket Number: 2885/139	Confirmation Number: 2050
Application Number 12/836,364	Filing Date July 14, 2010	Examiner Unassigned	Art Unit 2827
Invention Title RECONFIGURABLE SEQUENCER STRUCTURE		Inventors Martin VORBACH	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I hereby certify that this correspondence is being electronically transmitted to the United States Patent and Trademark Office via the Office electronic filing system on
Date: September 22, 2010
Signature: /Eunice K. Chang/
Eunice K. Chang

Sir:

Pursuant to 37 CFR § 1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom. The filing of this Information Disclosure Statement and the enclosed PTO Form No. 1449, shall not be construed as an admission that the information cited is prior art, or is considered to be material to patentability as defined in 37 C.F.R. § 1.56(b). The paragraphs marked below are applicable. It is believed that no fees other than those indicated below are due, but authorization is hereby given to charge any additional fees due, or to credit any overpayment, to Kenyon & Kenyon LLP, deposit account 11-0600.

1. This Information Disclosure Statement is being filed (a) within three months of the filing date of a national application other than a continued prosecution application under 37 C.F.R. §1.53(d), (b) within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, (c) before the mailing date of a first Office Action on the merits in the present application, OR (d) before the mailing of a first office action after filing of a request for continued examination. No certification or fee is required.

2. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a final action, Notice of Allowance, or any action that otherwise closes prosecution.

a. I hereby certify that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(1).

b. I hereby certify that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(2).

c. The required fee of \$180.00 under 37 CFR §1.17(p) is being paid by credit card to ensure consideration of the disclosed information. Any additional fees may be charged to Deposit Account No. 11-0600 of Kenyon & Kenyon LLP

3. English-language Abstracts of the non-English language references are attached hereto.

Respectfully submitted,

Date: September 22, 2010

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INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/139	Serial No. 12/836,364
	Applicant(s) VORBACH	
	Filing Date July 14, 2010	Group Art Unit 2827

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	90/010,450		Vorbach et al.			March 27, 2009
	6,173,419	January 9, 2001	Barnett			
	6,668,237	December 23, 2003	Guccione et al.			
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EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	1044571	February 16, 1989	Japan			Abstract	

OTHER DOCUMENTS

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Ballagh et al., "Java Debug Hardware Models Using JBits," 8 th Reconfigurable Architectures Workshop, 2001, 8 pages.
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EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

INTER-PROCESSOR COUPLING SYSTEM

Publication number: JP1044571 (A)

Publication date: 1989-02-16

Inventor(s): KAWAMURA RYOSAKU +

Applicant(s): OMRON TATEISI ELECTRONICS CO +

Classification:

- international: G06F13/38; G06F15/16; G06F15/167; G06F5/06; G06F13/38; G06F15/16; G06F5/06; (IPC1-7): G06F13/38; G06F15/16; G06F5/06

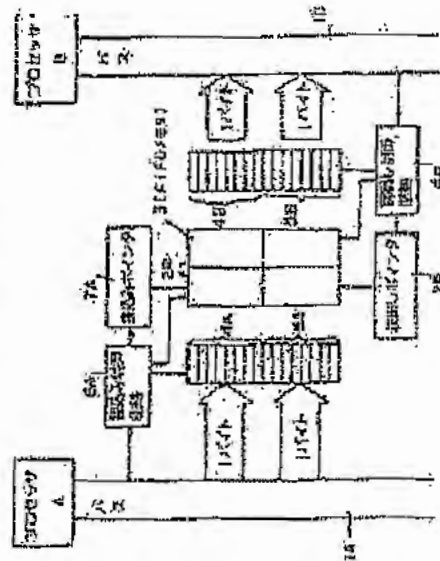
- European:

Application number: JP19870201105 19870812

Priority number(s): JP19870201105 19870812

Abstract of JP 1044571 (A)

PURPOSE: To improve coupling efficiency by coupling between the 1st and 2nd processors through a FIFO capable of shifting two or more data in a parallel state by the prescribed number of steps. **CONSTITUTION:** The FIFO memory 3 capable of shifting two 1-byte data in the parallel state by two steps is connected between the system bus 1A of the processor A and the system bus 1B of the processor B. A write control circuit 6A controls data writing from the processor A to writing side latches 4A, 5A and data writing from the latches 4A, 5A to the FIFO memory 3. A read control circuit 6B controls data reading from the FIFO memory 3 to reading side latches 4B, 5B, and when the latches 4B, 5B are emptied, two byte data are read out from an area pointed out by a reading pointer 7B and written in the latches 4B, 5B.



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⑫ 公開特許公報(A)

昭64-44571

⑬ Int. Cl. ⁴	識別記号	庁内整理番号	⑭ 公開
G 06 F 15/16	3 2 0	Y-6745-5B	昭和64年(1989)2月16日
8/06		Z-7230-5B	
13/38	3 4 0	C-8840-5B	審査請求 未請求 発明の数 1 (全8頁)

⑮ 発明の名称 プロセッサ間結合方式

⑯ 特 願 昭62-201105

⑰ 出 願 昭62(1987)8月12日

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⑳ 代 理 人 弁理士 和田 成則

明 細 書

1. 発明の名称

プロセッサ間結合方式

2. 特許請求の範囲

(1) 第1のプロセッサシステムと第2のプロセッサシステムとの間に2以上のデータを並列状態のまま所定段数だけシフト可能なFIFOメモリを設け、

該FIFOメモリの入力側各データポートには第1のプロセッサシステムのアドレス空間内のアドレスを割付ける一方、出力側各データポートには第2のプロセッサシステムのアドレス空間内のアドレスを割付け、

該FIFOメモリを適宜にシフトさせることにより、第1のプロセッサシステムから第2のプロセッサシステムへと2以上のデータを並列かつ非同期に転送すること、

を特徴とするプロセッサ間結合方式。

3. 発明の詳細な説明

(発明の分野)

この発明は、マルチプロセッサシステムに好適なプロセッサ間結合方式に関する。

【発明の概要】

この発明では、第1のプロセッサシステムと第2のプロセッサシステムとの間を、2以上のデータを並列状態のまま所定段数だけシフト可能なFIFOメモリを介して結合し、両プロセッサ間を効率良く結合したものである。

【従来技術とその問題点】

従来、マルチプロセッサシステム等に適用されるプロセッサ間結合方式としては、第5図に示されるように、同一の大きさのアドレス空間を、両プロセッサ間で共有するいわゆる共有メモリ方式が一般的である。

しかしながら、このような共有メモリ方式においては、大量のデータを共有する必要がある場合には、共有メモリ空間を広く確保せねばならず、その結果共有メモリ空間以外に使用可能な空間が十分に確保できないこと、片方のプロセッサが共有メモリをアクセス中のときには、他方のプロセッサ

サは共有メモリをアクセスできないこと、共有メモリ空間として確保できる最大範囲は、プロセッサがアドレスできる範囲によって制限されてしまうことなどの問題点があった。

また、第6図に示されるように、共有メモリ内において、待ち行列処理が必要な場合には、待ち行列処理のための複雑なソフトウェアが必要となること、一方のプロセッサが待ち行列処理中の場合、他方のプロセッサはその待ち行列にアクセスできないこと、待ち行列処理を行なったとしても、一度にシフト可能なデータ数は1個に限られるため、処理の高効率化に制約を受けることなどの問題点があった。

《発明の目的》

この発明の目的は、大量のデータを共有する必要がある場合にも、共有アドレス空間が少なくても済み、また待ち行列処理のために複雑なソフトウェアが不要であり、また共有アドレス空間に対して相方のプロセッサが同時にアクセスを行なうことができ、さらに複数のデータの授受を同一タイ

ミングで行い得るようにしたプロセッサ間結合方式を提供することにある。

《発明の構成と効果》

この発明は上記の目的を達成するために、第1のプロセッサシステムと第2のプロセッサシステムとの間に2以上のデータを並列状態のままで所定段数だけシフト可能なFIFOメモリを設け、

該FIFOメモリの入力側各データポートには第1のプロセッサシステムのアドレス空間内のアドレスを割付ける一方、出力側各データポートには第2のプロセッサシステムのアドレス空間内のアドレスを割付け、

該FIFOメモリを適宜にシフトさせることにより、第1のプロセッサシステムから第2のプロセッサシステムへと2以上のデータを並列かつ非同時に転送することを特徴とするものである。

このような構成によれば、大量のデータを共有する必要がある場合にも、共有アドレス空間が少なくても済み、また待ち行列処理のために複雑なソフトウェアが不要であり、また共有アドレス空間

- 3 -

- 4 -

に対して相方のプロセッサが同時にアクセスを行なうことができ、さらに複数のデータの授受を同一タイミングで行い得るという効果がある。

《実施例の説明》

第1図は、本発明に係るプロセッサ間結合方式の一実施例を示す回路図、第2A図～第2E図はその動作説明図である。

この例では、プロセッサAからプロセッサBに対し、2個の1バイトデータをFIFOメモリ3を介して転送するようにしている。

すなわち、第1図において、プロセッサAのシステムバス1AとプロセッサBのシステムバス1Bとの間には、2個の1バイトデータを並列状態のままで2段シフト可能なFIFOメモリ3が設けられている。

このFIFOメモリ3の入力側各データポートには1バイト構成からなるラッチ4A、5Aが接続されており、これらのラッチ4A、5AにはプロセッサAのアドレス空間内のアドレスが割り付けられている。

また、FIFOメモリ3の出力側各データポートには同様にして2個のラッチ4B、5Bが接続されており、これらのラッチ4B、5Bにも同様にして、プロセッサBのアドレス空間内のアドレスが割り付けられている。

送込制御回路6Aは、送込側ラッチ4A、5Aに対するプロセッサAからのデータ送込みおよび送込側ラッチ4A、5AからFIFOメモリ3内のデータ送込みを制御するもので、送込側ラッチ4A、5Aが満杯になるとともに、そのデータは送込ポインタ7Aで示されるFIFOメモリ3内のエリアへと自動的に送込まれ、同時にラッチ4A、5Aは空クリアされる。

送込制御回路6Bは、FIFOメモリ3から送込側ラッチ4B、5Bに対するデータ送出しを制御するもので、送込側ラッチ4B、5Bが空になると、自動的に送込ポインタ7Bで示されるFIFOメモリ3内のエリアから、2個のバイトデータを送出し、これを送込側ラッチ4B、5Bに送込むようになされている。

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次に、以上の構成よりなるシステムの動作を、第2A図～第2G図を参照しながら説明する。

第2A図はリセット直後の状態を示すもので、この状態では書込ポインタの内容と読出ポインタの内容とは同一であり、また書込側ラッチ4A、5Aおよび読出側ラッチ4B、5Bはそれぞれ零クリアされている。

この状態において、プロセッサA側から順次1個ずつ1バイトデータの書込処理を行なうと、第2B図および第2C図に示されるように、書込制御回路6Aの作用によって、2個の1バイトデータはラッチ4A、5Aと順次書込まれる。

第2C図に示されるように、ラッチ4A、5Aが相方書込まれて書込側ラッチが全て満杯となると、書込制御回路6Aの作用によって、ラッチ4A、5Aのデータは、自動的に書込ポインタ7Aで示されるFIFOメモリ3内のエリアへと、第2D図に示されるように書込まれ、その後ラッチ4A、5Aの内容は零クリアされる。

また、書込ポインタ7Aの内容は、FIFOメ

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与えられると、読出ポインタ7Bで指定されるFIFOメモリ3内のデータは、読出制御回路6Bの作用によって、読出側の2個のラッチ4B、5Bへと読出され、以後これらのデータはプロセッサB側で読取ることができる。

このように本実施例回路では、2個の1バイトデータを並列状態のまま2段にシフトさせ、プロセッサA側からプロセッサB側へと転送させることができ、この際プロセッサA側およびB側で占有するアドレス空間は2バイトであるにも拘らず、バッファ空間としてはFIFOメモリ3による4バイト分を確保することができる。

そして、このバッファリング空間の大きさは、FIFOメモリ3のシフト段数によって任意に増加することができ、従来の共有メモリ方式のように、プロセッサA側またはB側のアドレス空間によって、制限されることはなくなる。

また、2以上のデータを並列状態のままA側からB側へと転送できるため、例えば2バイト構成および4バイト構成の命令等を転送する場合に、

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メモリ3内の次に書込まれるべきエリアを示すこととなる。

このとき、B側の処理方式によっては、Bが読出すことのできるデータがFIFOメモリ内に準備できたことを示す回路（割込発生回路など）を動作させても良い。

すなわち、第2E図に示されるように、B側で2個の1バイトデータをとらせたFIFOメモリ3から取出すことが可能であるということは、読出側のラッチ4B、5Bへ既に格納されているということを実証する。

一方、第2D図の状態において、A側からさらに2個の1バイトデータを、第2F図に示されるように、ラッチ4A、5Aへと書込むと、書込制御回路6Aでは書込側ラッチが満杯になったことを検出し、第2G図に示されるように、新たな2個の1バイトデータは、書込ポインタ7Aで示されるFIFOメモリ3内のエリアへと書込まれ、同時に書込側ラッチ4A、5Aは零クリアされる。

第2G図の状態において、B側から読出指令が

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プロセッサの処理速度を向上させることができる。

第3図は他の実施例を示すもので、この例ではチップ外データバス幅8ビット、チップ内データバス幅8ビット(8/8)のマイクロプロセッサMC6809と、チップ外データバス幅8ビット、チップ内データバス幅16ビット(8/16)のマイクロプロセッサ80188を本方式により結合したものである。

両者を結合するためのFIFOメモリとしては、1バイト×512段のFIFOメモリチップ(例えば、インテグレイテッド デバイス テクノロジー社IDT7201S/L、IDT7202S/L等)を片方向について2048個設置し、それを双方向用にそれぞれ設置している。

従って、双方向について2048×512×2=2Mバイトの共有メモリを持つことになる。

しかも、この大容量共有メモリは、MC6809マイクロプロセッサのアドレス空間64Kバイトを大幅に上回るものであるにも拘らず、MC6809のアドレス空間の中では、4Kバイトしか

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使用していない。

すなわち、アドレス空間の中でわずか4Kバイトを双方向のFIFOに割当てることによって、あたかも2Mバイトの共有バイトを持つかの如き効果を得ている。

第4図は、プロセッサAからプロセッサBへ移動するFIFOメモリの側面における処理の流れを示すフローチャートである。

この例では、送信データの挿入側に512段のキューが一杯でないことを示す「挿入可フラグ」を設ける一方、受信データの取出側ではFIFOメモリ内に受信データ残りの場合に、FIFOメモリからプロセッサBへ割込みが発生する回路を設けている。

このように本実施例によれば、プロセッサAからプロセッサBへと大量のデータを、少ないアドレス空間の占有でしかも並列に転送することができる、同時に逆方向の転送も行なうことができるわけである。

4. 図面の簡単な説明

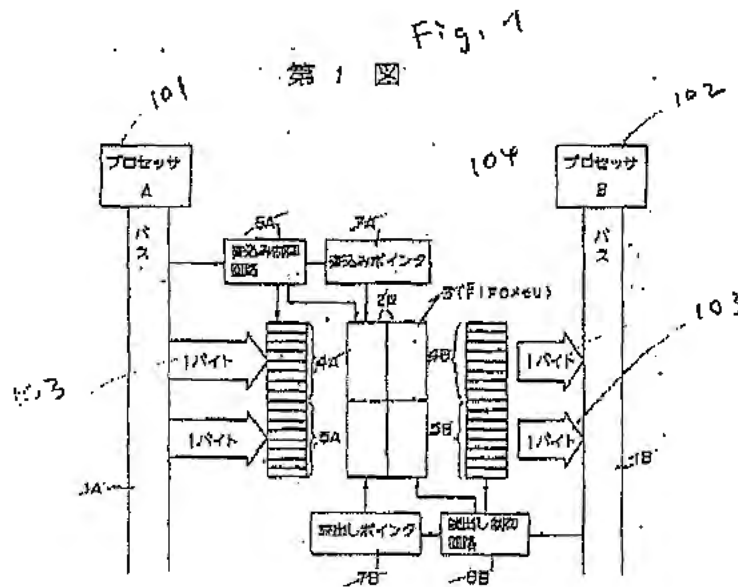
第1図は本発明に係わるプロセッサ間結合方式の一実施例を示す回路図、第2A図～第2G図は同回路の動作を示す説明図、第3図は本発明方式の他の実施例を示す回路図、第4図は同実施例の送受信制御を示すフローチャート、第5図および第6図は従来のプロセッサ間結合方式を示すメモリマップである。

- 1A, 1B…システムバス
- 3…FIFOメモリ
- 4A, 5A…書き込みラッチ
- 4B, 5B…読み出しラッチ
- 6A…書き込み制御回路
- 6B…読み出し制御回路
- 7A…書き込みポイント
- 7B…読み出しポイント
- B…割込み発生回路

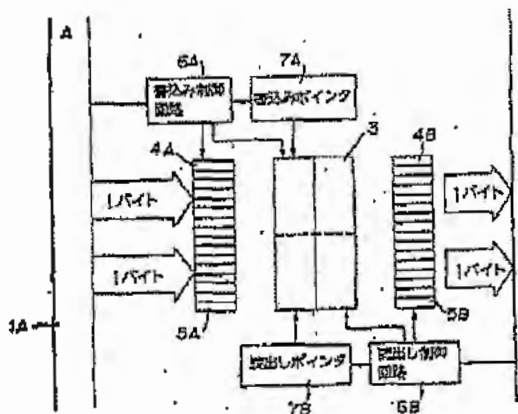
特許出願人 立石電機株式会社
代理人 弁護士 和田 成 則

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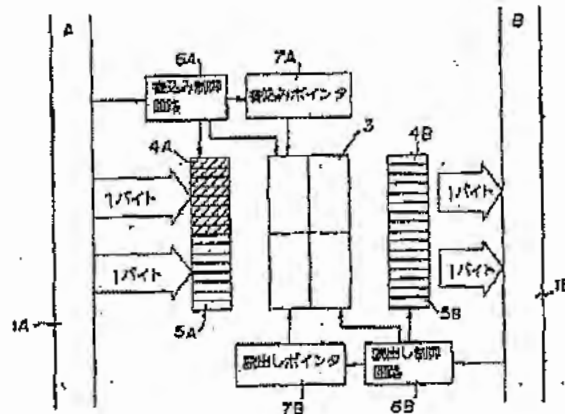
- 12 -



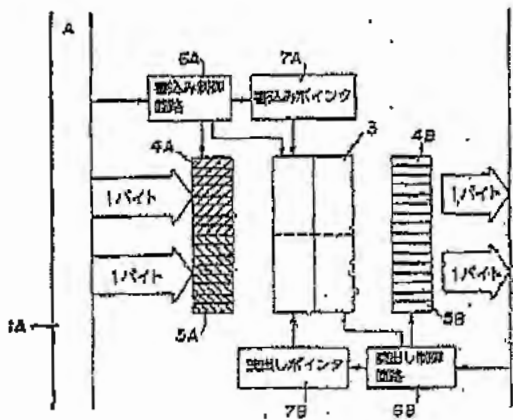
第2A図



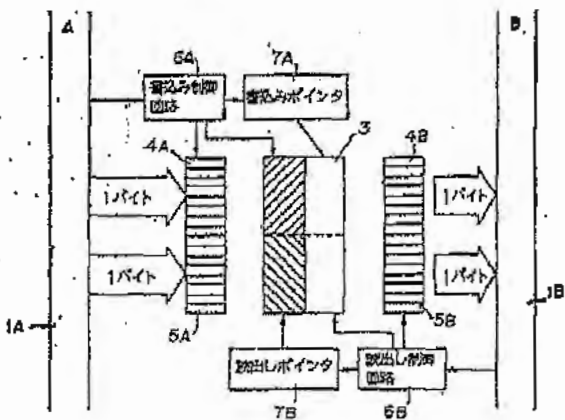
第2B図



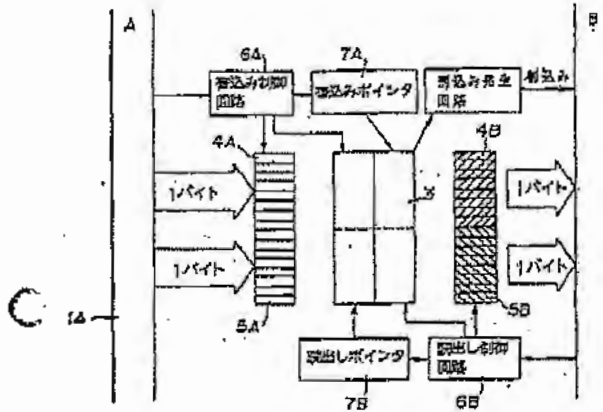
第2C図



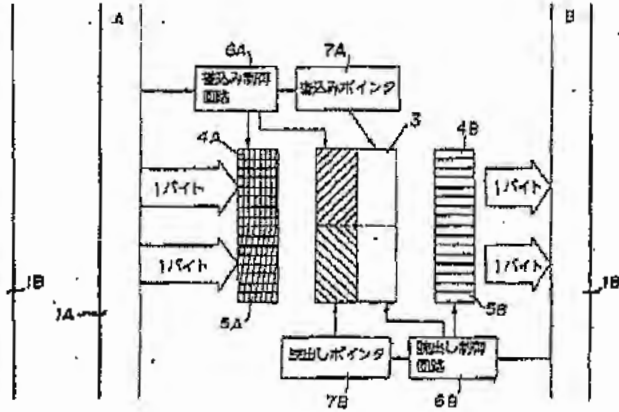
第2D図



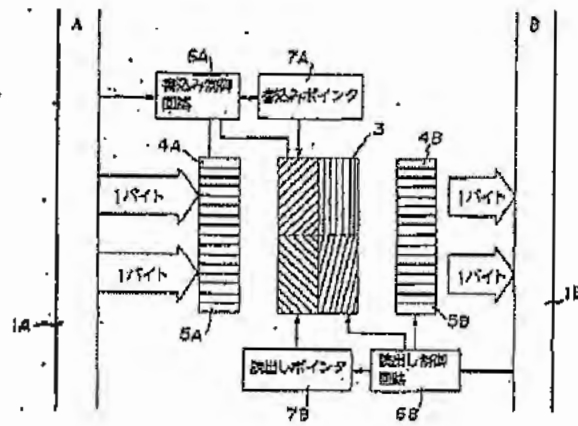
第2E図



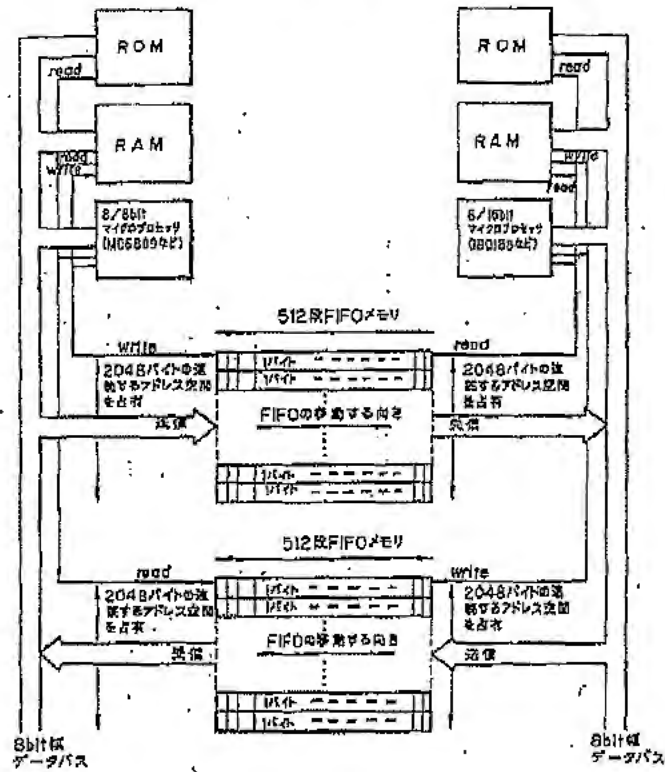
第2F図



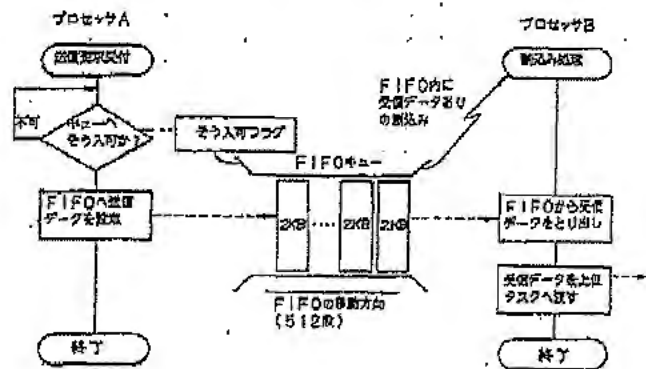
第2G図

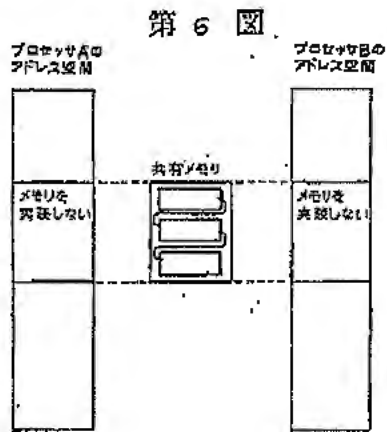
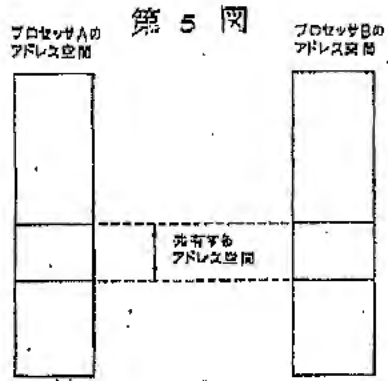


第 3 図



第 4 図





【公報種別】特許法第17条の2の規定による補正の掲載
【部門区分】第6部門第3区分
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特許庁長官殿

1. 事件の表示

特願昭62-201105号

2. 発明の名称

プロセッサ間結合装置

3. 補正をする者

事件との関係 特許出願人

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5. 補正命令の日付 (自発)

6. 補正の対象 明細書全文

7. 補正の内容 明細書全文を別紙の如く補正する。

明 細 書

1. 発明の名称

プロセッサ間結合装置

2. 特許請求の範囲

第1のプロセッサと第2のプロセッサとの間に、
2以上のデータを並列状態のままであらかじめ定
めた段数だけシフト可能なFIFOメモリを設け、

前記FIFOメモリの入力側各データポートに
は、前記第1のプロセッサのアドレス区間内のア
ドレスを割り付け、

前記FIFOメモリの出力側各データポートに
は、前記第2のプロセッサのアドレス区間内のア
ドレスを割り付け、

前記FIFOメモリ内に保持されたデータをシ
フトさせることにより、第1のプロセッサから第
2のプロセッサへと2以上のデータを並列かつ非
同期に転送することを特徴とする。

プロセッサ間結合装置。

3. 発明の詳細な説明

(発明の分野)

この発明は、マルチプロセッサシステムに好適なプロセッサ間結合装置に関する。

〔従来技術とその問題点〕

従来、マルチプロセッサシステム等においてプロセッサ間を結合するには、第5図に示されるように、共有メモリを用いて、同一の大きさのアドレス空間を複数のプロセッサで共有する方法が一般的である。

しかしながら、このような共有メモリを使用する場合にあっては、大量のデータを共有する必要がある場合には、共有メモリ空間を広く確保せねばならず、その結果共有メモリ空間以外に使用可能な空間が十分に確保できないこと、片方のプロセッサが共有メモリをアクセス中のときには、他方のプロセッサは共有メモリをアクセスできないこと、共有メモリ空間として確保できる最大範囲は、プロセッサがアドレスできる範囲によって制限されてしまうことなどの問題点があった。

また、第5図に示されるように、共有メモリ内において、待ち行列処理が必要な場合には、待ち

行列処理のための複雑なソフトウェアが必要となること、一方のプロセッサが待ち行列処理中の場合、他方のプロセッサはその待ち行列にアクセスできないこと、待ち行列処理を行なったとしても、一度にシフト可能なデータ数は1個に限られるため、処理の高速化に制約を受けることなどの問題点があった。

〔発明の目的〕

この発明の目的は、大量のデータを共有する必要がある場合にも、共有アドレス空間が少なくても済み、また待ち行列処理のために複雑なソフトウェアが不要であり、また共有アドレス空間に対して相方のプロセッサが同時にアクセスを行なうことができ、さらに複数のデータの授受を同一タイミングで行い得るようにしたプロセッサ間結合装置を提供することにある。

〔発明の構成と効果〕

この発明は上記の目的を達成するために、第1のプロセッサと第2のプロセッサとの間にFIFOメモリを設け、FIFOメモリ内に保持された

データをシフトさせることによって、第1のプロセッサから第2のプロセッサへと2以上のデータを並列かつ非同期に転送することを特徴とするものである。

このような構成によれば、大量のデータを共有する必要がある場合にも、共有アドレス空間が少なく済み、また待ち行列処理のために複雑なソフトウェアが不要であり、また共有アドレス空間に対して相方のプロセッサが同時にアクセスを行なうことができ、さらに複数のデータの授受を同一タイミングで行い得るという効果がある。

〔実施例の説明〕

第1図は、本発明に係わるプロセッサ間結合装置の一実施例を示す回路図、第2A図～第2G図はその動作説明図である。

この例では、プロセッサAからプロセッサBに対し、2個の1バイトデータをFIFOメモリ3を介して転送するようにしている。

すなわち、第1図において、プロセッサAのシステムバス1AとプロセッサBのシステムバス1

Bとの間には、2個の1バイトデータを並列状態のまま2段シフト可能なFIFOメモリ3が設けられている。

このFIFOメモリ3の入力側各データポートには1バイト構成からなるラッチ4A、5Aが接続されており、これらのラッチ4A、5AにはプロセッサAのアドレス空間内のアドレスが割り付けられている。

また、FIFOメモリ3の出力側各データポートには同様に2個のラッチ4B、5Bが接続されており、これらのラッチ4B、5Bにも同様に、プロセッサBのアドレス空間内のアドレスが割り付けられている。

寄込制御回路6Aは、寄込側ラッチ4A、5Aに対するプロセッサAからのデータ寄込みおよび寄込側ラッチ4A、5AからFIFOメモリ3内へのデータ寄込みを制御するもので、寄込側ラッチ4A、5Aが満杯になるとともに、そのデータは寄込ポイント7Aで示されるFIFOメモリ3内のエリアへと自動的に寄込まれ、同時にラッチ

4A, 5Aは零クリアされる。

読出制御回路6Bは、FIFOメモリ3から読出側ラッチ4B, 5Bに対するデータ読出しを制御するもので、読出側ラッチ4B, 5Bが空になると、自動的に読出ポイント7Bで示されるFIFOメモリ3内のエリアから、2個のバイトデータを読出し、これを読出側ラッチ4B, 5Bに書込むようになされている。

次に、以上の構成よりなるシステムの動作を、第2A図〜第2G図を参照しながら説明する。

第2A図はリセット直後の状態を示すもので、この状態では書込ポイントの内容と読出ポイントの内容とは同一であり、また書込側ラッチ4A, 5Aおよび読出側ラッチ4B, 5Bはそれぞれ零クリアされている。

この状態において、プロセッサA側から順次1個ずつ1バイトデータの書込処理を行なうと、第2B図および第2C図に示されるように、書込制御回路6Aの作用によって、2個の1バイトデータはラッチ4A, 5Aと順次書込まれる。

に2個の1バイトデータを、第2F図に示されるように、ラッチ4A, 5Aへと書込むと、書込制御回路6Aでは書込側ラッチが満杯になったことを検出し、第2G図に示されるように、新たな2個の1バイトデータは、書込ポイント7Aで示されるFIFOメモリ3内のエリアへと書込まれ、同時に書込側ラッチ4A, 5Aは零クリアされる。

第2G図の状態において、B側から読出指令が与えられると、読出ポイント7Bで指定されるFIFOメモリ3内のデータは、読出制御回路6Bの作用によって、読出側の2個のラッチ4B, 5Bへと読出され、以後これらのデータはプロセッサB側で読取ることができる。

このように本実施例回路では、2個の1バイトデータを並列状態のまま2段にシフトさせ、プロセッサA側からプロセッサB側へと転送させることができ、この際プロセッサA側およびB側で占有するアドレス空間は2バイトであるにも拘らず、バッファ空間としてはFIFOメモリ3による4バイト分を確保することができる。

第2C図に示されるように、ラッチ4A, 5Aが相方書込まれて書込側ラッチが全て満杯となると、書込制御回路6Aの作用によって、ラッチ4A, 5Aのデータは、自動的に書込ポイント7Aで示されるFIFOメモリ3内のエリアへと、第2D図に示されるように書込まれ、その後ラッチ4A, 5Aの内容は零クリアされる。

また、書込ポイント7Aの内容は、FIFOメモリ3内の次に書込まれるべきエリアを示すこととなる。

このとき、B側のデータ処理方法によっては、Bが読出すことのできるデータがFIFOメモリ内に準備できたことを示す回路(書込待ち回路など)を動作させても良い。

すなわち、第2E図に示されるように、B側で2個の1バイトデータとともにFIFOメモリ3から取出すことが可能であるということは、読出側のラッチ4B, 5Bへ既に格納されているということを示唆する。

一方、第2D図の状態において、A側からさら

そして、このバッファリング空間の大きさは、FIFOメモリ3のシフト段数によって任意に増加することができ、従来の共有メモリを使用する場合のように、プロセッサA側またはB側のアドレス空間によって、制限されることはなくなる。

また、2以上のデータを並列状態のままA側からB側へと転送できるため、例えば2バイト構成および4バイト構成の命令等を転送する場合に、プロセッサの処理速度を向上させることができる。

第3図は他の実施例を示すもので、この例ではチップ外データバス幅8ビット、チップ内データバス幅8ビット(8/8)のマイクロプロセッサMC6809と、チップ外データバス幅8ビット、チップ内データバス幅16ビット(8/16)のマイクロプロセッサ180188を本発明の実施に適用した形で結合したものである。

両者を結合するためのFIFOメモリとしては、1バイト×512段のFIFOメモリチップ(例えば、インテグレイテッド デバイス テクノロジー社IDT7201S/L, IDT7202S

／L等)を片方向について2048個設置し、それを双方向用それぞれ設置している。

従って、双方向について2048×512×2→2Mバイトの共有メモリを持つことになる。

しかも、この大容量共有メモリは、MC6809マイクロプロセッサのアドレス空間64Kバイトを大幅に上回るものであるにも拘らず、MC6809のアドレス空間の中では、4Kバイトしか使用していない。

すなわち、アドレス空間の中でわずか4Kバイトを双方向のFIFOに相当てることによって、あたかも2Mバイトの共有メモリを持つかの如き効果を得ている。

第4図は、プロセッサAからプロセッサBへ移動するFIFOメモリの制御における処理の流れを示すフローチャートである。

この例では、送信データの挿入側は512段のキューが一杯でないことを示す「挿入可フラグ」を設ける一方、受信データの取山側ではFIFOメモリ内に受信データ有りの場合に、FIFOメ

モリからプロセッサBへ到達する回路を設けている。

このように本実施例によれば、プロセッサAからプロセッサBへと大量のデータを、少ないアドレス空間の占有でしかも並列に転送することができ、同時に逆方向の転送も行なうことができるわけである。

4. 図面の簡単な説明

第1図は本発明に係わるプロセッサ間結合装置の一実施例を示す回路図、第2A図～第2G図は同回路の動作を示す説明図、第3図は本発明の他の実施例を示す回路図、第4図は同実施例の送受信制御を示すフローチャート、第5図および第6図は従来のプロセッサ結合の方法を示すメモリマップである。

- 1A, 1B…システムバス
- 3…FIFOメモリ
- 4A, 5A…挿込側ラッチ
- 4B, 5B…取山側ラッチ
- 6A…挿込制御回路

- 6B…取山制御回路
- 7A…挿込ポインタ
- 7B…取山ポインタ
- 8…到達発生回路

特許出願人 オムロン株式会社
代理人 和 田 成 則

Electronic Acknowledgement Receipt

EFS ID:	8472322
Application Number:	12836364
International Application Number:	
Confirmation Number:	2050
Title of Invention:	RECONFIGURABLE SEQUENCER STRUCTURE
First Named Inventor/Applicant Name:	Martin Vorbach
Customer Number:	26646
Filer:	Aaron Grunberger/Eunice Chang
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Attorney Docket Number:	2885/139
Receipt Date:	22-SEP-2010
Filing Date:	14-JUL-2010
Time Stamp:	13:59:53
Application Type:	Utility under 35 USC 111(a)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Response to Pre-Exam Formalities Notice	2885-139-RespNotCorrApPapers.pdf	5745435 <small>797a7ca25221a0e4266d66221f03e8ce2fe43078</small>	no	53

Warnings:

Information:

2	Information Disclosure Statement (IDS) Filed (SB/08)	2885-139-SupplIDS.pdf	345810 3789d4ba81124874b6783da4480cd67c1d 06b54d	no	3
Warnings:					
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3	Foreign Reference	JP-10-44571.pdf	1174951 129d4bf69b0e3c8253fb12adcd4ad4ace2c6 dec61	no	13
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FILED REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/836,364	07/14/2010	2827	722	2885/139	30	1

CONFIRMATION NO. 2050

UPDATED FILING RECEIPT



26646
KENYON & KENYON LLP
ONE BROADWAY
NEW YORK, NY 10004

Date Mailed: 10/04/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Martin Vorbach, Munich, GERMANY;

Power of Attorney: The patent practitioners associated with Customer Number 26646

Domestic Priority data as claimed by applicant

This application is a CON of 12/541,299 08/14/2009 PAT 7,782,087
which is a CON of 12/082,073 04/07/2008 PAT 7,602,214
which is a CON of 10/526,595 01/09/2006 PAT 7,394,284
which is a 371 of PCT/EP03/38599 09/08/2003

Foreign Applications

GERMANY 102 41 812.8 09/06/2002
GERMANY 103 15 295.4 04/04/2003
GERMANY 103 21 834.3 05/15/2003
EUROPEAN PATENT OFFICE (EPO) 03 019 428.6 08/28/2003

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If Required, Foreign Filing License Granted: 07/26/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/836,364**

Projected Publication Date: 01/13/2011

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**** SMALL ENTITY ****

Title

RECONFIGURABLE SEQUENCER STRUCTURE

Preliminary Class

365

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Patentanmeldung Nr. Patent application No. Demande de brevet n°

03019428.6

Der Präsident des Europäischen Patentamts:
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk



Anmeldung Nr:
Application no.: 03019428.6
Demande no:

Anmeldetag:
Date of filing: 28.08.03
Date de dépôt:

Anmelder/Applicant(s)/Demandeur(s):

PACT XPP Technologies AG
Muthmannstrasse 1
80939 München
ALLEMAGNE

Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Device and method for data processing

In Anspruch genommene Priorität(en) / Priority(ies) claimed / Priorité(s)
revendiquée(s)
Staat/Tag/Aktenzeichen/State/Date/File no./Pays/Date/Numéro de dépôt:

Internationale Patentklassifikation/International Patent Classification/
Classification internationale des brevets:

G06F9/00

Am Anmeldetag benannte Vertragsstaaten/Contracting states designated at date of
filing/Etats contractants désignées lors du dépôt:

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL
PT RO SE SI SK TR LI



1 Overview of changes vs. XPP V2.0

1.1 ALU-PAE Architecture

A PAE comprises 4 input ports and 4 output ports. Embedded with each PAE is the FREG path newly named DF with its dataflow capabilities, like *MERGE*, *SWAP*, *DEMUX* as well as *ELUT*.

2 input ports Ri0 and Ri1 are directly connected to the ALU. Two output ports receive the ALU results.

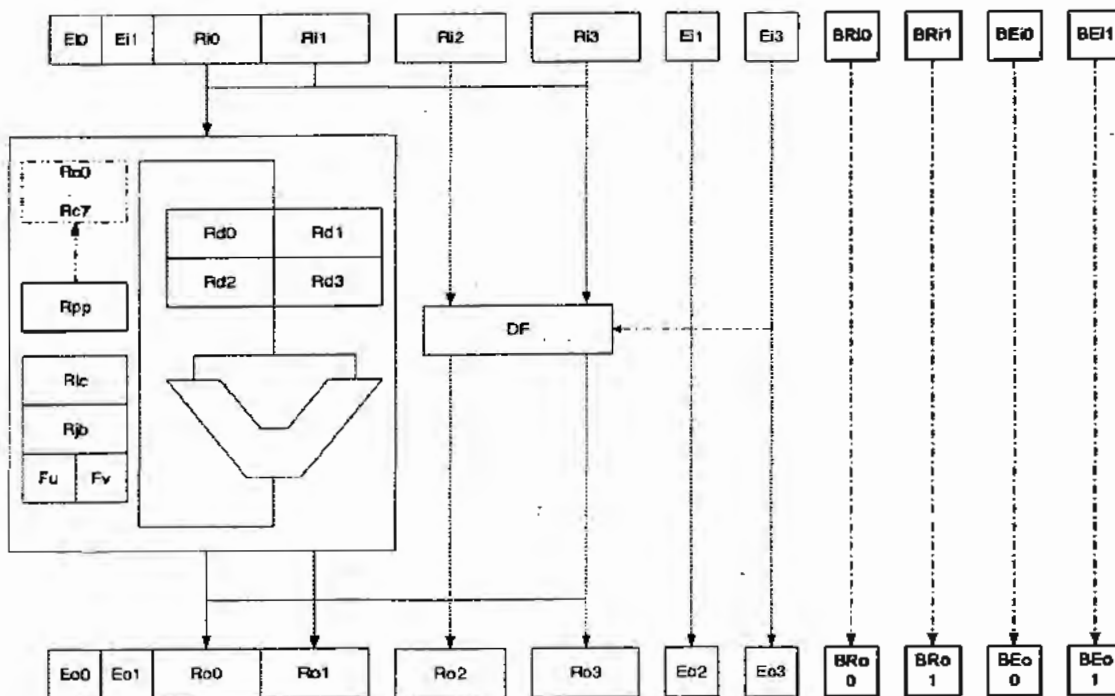
Ri2 and Ri3 are typically fed to the DF path which output is Ro2 and Ro3.

Alternatively Ri2 and Ri3 can serve as inputs for the ALU as well. This extension is needed to provide a suitable amount of ALU inputs if *Function Folding* (as described later) is used. In this mode Ro2 and Ro3 serve as additional outputs.

Associated to each data register (Ri or Ro) is an event port (Ei or Eo).



It is to decide whether an additional data and event bypass BRi0-1, BEi0-1 is implemented. The decision depends on how often Function Folding will be used and how many inputs and outputs are required in average.



1.1.1 Other extensions

SIMD operation is implemented in the ALUs to support 8 and 16 bit wide data words for i.e. graphics and imaging.

Saturation is supported for ADD/SUB/MUL instructions for i.e. voice, video and imaging algorithms.

1.2 Function Folding

1.2.1 Basics and Input/output paradigms

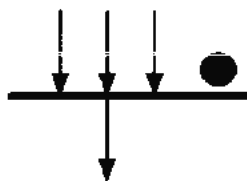
Within this chapter the basic operation paradigms of the XPP architecture are repeated for a better understanding based on Petri-Nets. In addition the Petri-Nets will be enhanced for a better understanding of the subsequently described changes of the current XPP architecture.

Each PAEs operates as a data flow node as defined by Perti-Nets. A Petri-Net supports a calculation of multiple inputs and produces one single output. Special for a Perti-Net is, that the operation is delayed until all inputs are available.

For the XPP technology this means:

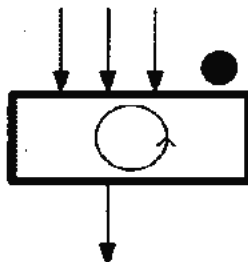
1. all necessary data is available
2. all necessary events are available

The quantity of data and events is defined by the data and control flow, the availability is displayed at runtime by the handshake protocol RDY/ACK.



The thick arbor indicates the operation, the dot on the right side indicates that the operation is delayed until all inputs are available.

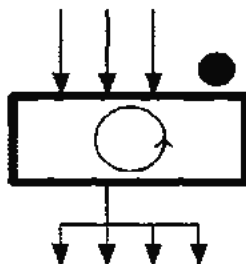
Enhancing the basic methodology function folding supports multiple operations – maybe even sequential – instead of one, defined as a *Cycle*. Important is, that the basics of Petri-Nets keep unchanged.





Typical PAE-like Petri-Nets consume one input packet per one operation. For sequential operation multiple reads of the same input packet are supported. However, the interface model again keeps unchanged.

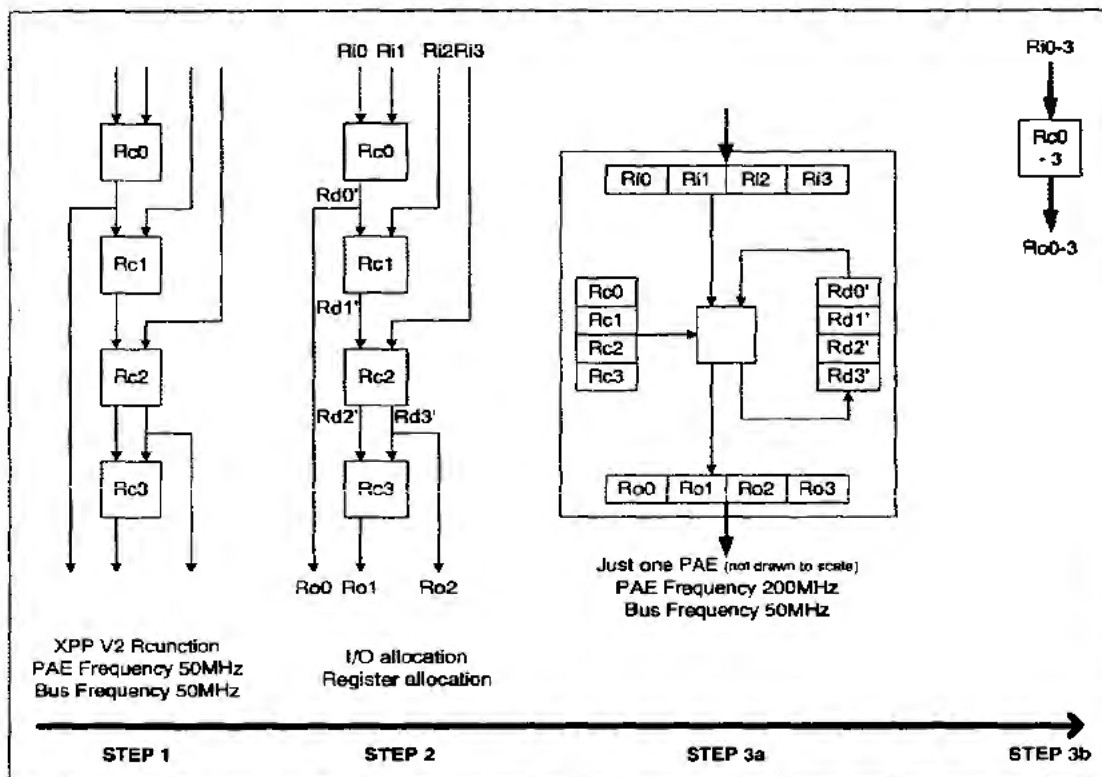
Data duplication occurs in the output path of the Petri-Net, which does not influence the operation basics again.



1.2.2 Method of Function Folding

One of the most important extensions is the capability to fold multiple PAE functions onto on PAE and execute them in a sequential manner. It is important to understand that the intention is not to support sequential processing or even microcontroller capabilities at all. The intention of Function Folding is just to take multiple dataflow operations and map them on a single PAE, using a register structure instead of a network between each function.

The goal is to save silicon area by rising to clock frequency locally in the PAEs. An additional expectation is to save power since the busses operate at a fraction of the clock frequencies of the PAEs. Data transfers over the busses, which consume much power, are reduced.



The internal registers can be implemented in two different ways:

1. dataflow model

Each register (r^i) has a valid bit which is set as soon as data has been written into the register and reset after the data has been read. Data cannot be written if valid is set, data can not be read if valid is not set. This approach implements a 100% compatible dataflow behaviour.

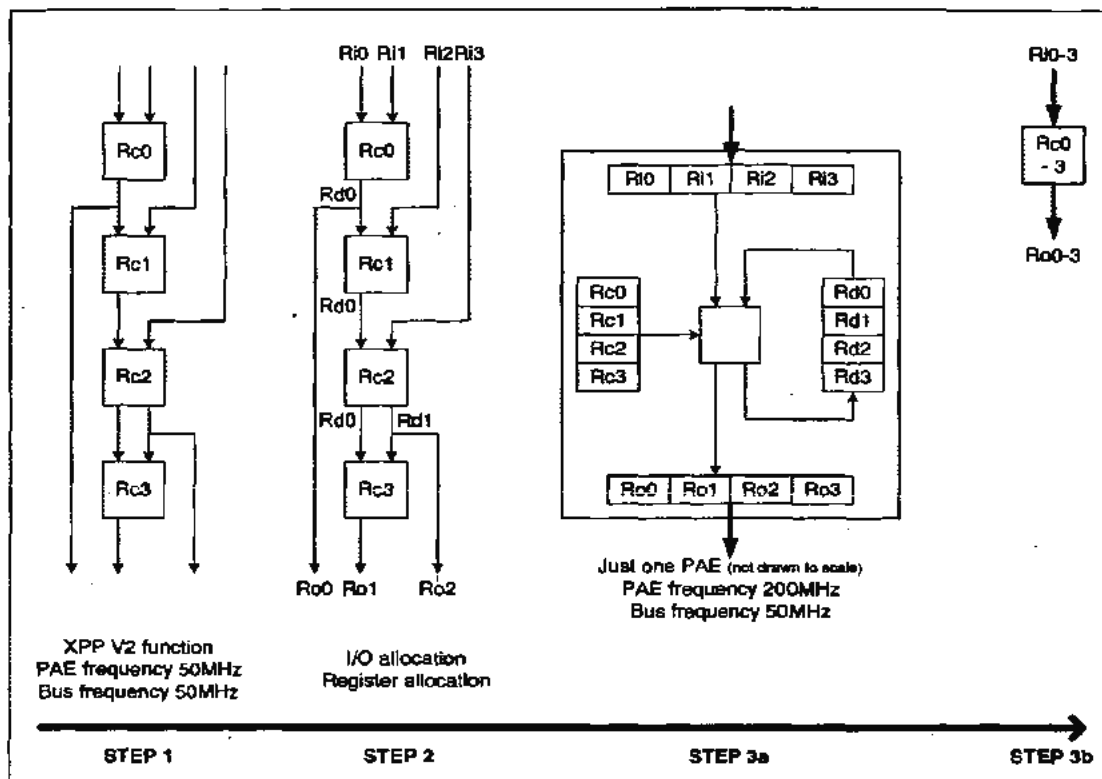
2. sequencer model

The registers have no associated valid bits. The PAE operates as a sequencer, whereas at the edges of the PAE (the bus connects) the paradigm is changed to the XPP-like dataflow behaviour.

Even if at first the dataflow model seems preferable, it has major down sides. One is that a high amount of register is needed to implement each data path and data duplication is quite complicated and not efficient. Another is that sometimes a limited sequential operation simplifies programming and hardware effort.

Therefore it is assumed consecutively that sequencer model is implemented. Since pure dataflow can be folded using automatic tools the programmer should stay within the dataflow paradigm and not be confused with the additional capabilities. Automatic tools must take care i.e. while register allocation that the paradigm is not violated.

The following figure shows that using sequencer model only 2 registers (instead of 4) are required:



For allowing complex function like i.e. address generation as well as algorithms like "IMEC"-like data stream operations the PAE has not only 4 instruction registers implemented but 8, whereas the maximum bus-clock vs. PAE-clock ration is limited to a factor of 4 for usual function folding.

It is expected that the size of the new PAE supporting Function Folding will increase by max. 25%. On the other hand 4 PAEs are reduced to 1.

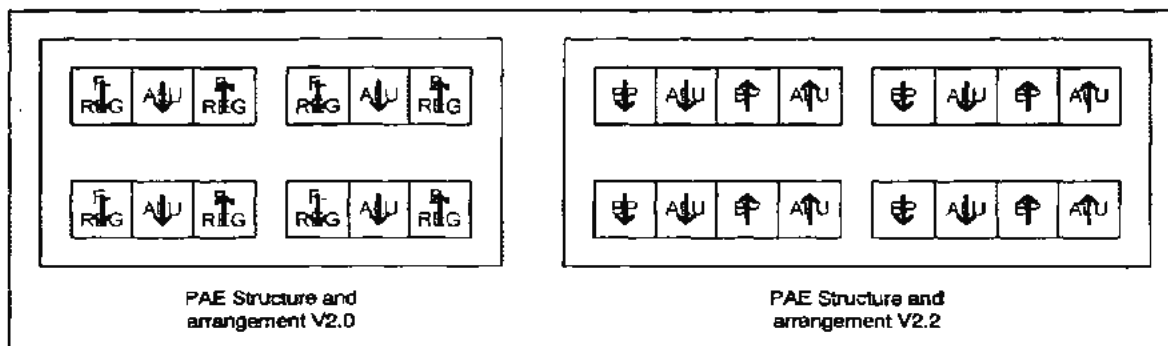
Assuming that in average not the optimum but only about 3 functions can be folded onto a single PAE a XPP64 could be replaced by a XPP21. Taking the larger PAEs into account the functionality of a XPP64 V2.0 should be executable on a XPP V2.2 with an area of less than half.

1.3 Array Structure

The V2.0 structure of the PAEs consumes much area for FREG and BREG and their associated bus interfaces. In addition feed backs through the FREGs require the insertion of registers into the feedback path, which result not only in an increased latency but also in a negative impact onto the throughput and performance of the XPP.

A new PAE structure and arrangement is proposed with the expectation to minimize latency and optimize the bus interconnect structure to achieve an optimized area.

The V2.2 PAE structure does not include BREGs any more. As a replacement the ALUs are alternating flipped horizontally which leads to improved placement and routing capabilities especially for feedback paths i.e. of loops. Each PAE contains now two ALUs and two BP paths, one from top to bottom and one flipped from bottom to top.



1.4 Bus modifications



Within this chapter are optimizations described which reduce the required area and the amount of busses. However, this modifications are only proposals yet, since the have to be evaluated based on real algorithms. It is planed to compose a questionnaire to collect the necessary input from the application programmes.

1.4.1 Next neighbour

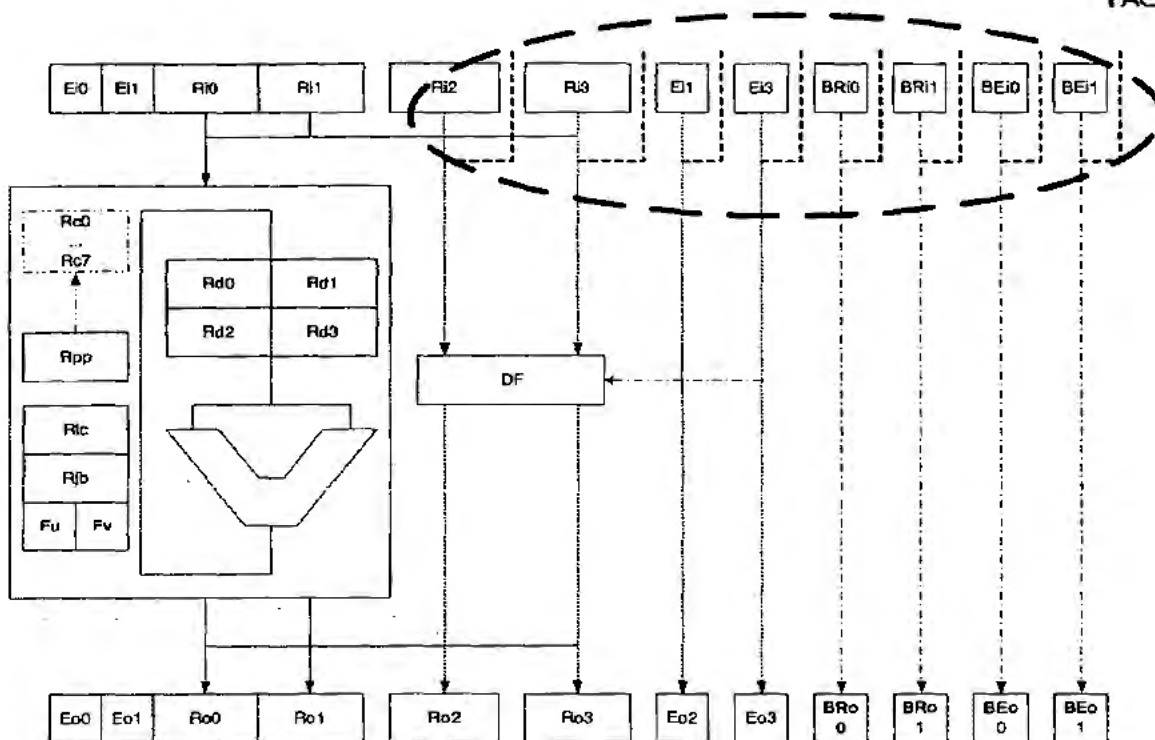
In V2.0 architecture a direct horizontal data path between two PAEs block a vertical data bus. This effect increases the required vertical busses within a XFP and drives cost unnecessarily.

Therefore in V2.2 a direct feed path between horizontal PAEs is proposed.

1.4.2 Removal of registers in busses

In V2.0 are registers implemented in the vertical busses which can be switched on by configuration for longer paths. This registers can furthermore be preloaded by configuration which requires a significant amount of silicon area.

It is proposed not to implement registers in the busses any more, but to use an enhanced DF or Bypass (PB) part within the PAEs which is able to reroute a path to the same bus using the DF or BP internal registers instead:



It is to evaluate

- a) how many resources are saved for the busses and how many are needed for the PAEs
- b) how often must registers be inserted, are 1 or max. 2 paths enough per PAE (limit is two since DF/BP offers max. 2 inputs)

1.4.3 Shifting n:1, 1:n capabilities from busses to PAEs

In V2.0 n:1 and 1:n transitions are supported by the busses which requires a significant amount of resources i.e. for the sample-and-hold stage of the handshake signals.

Depending on the size of n two different capabilities are provided with the new PAE structure:

- $n \leq 2$ The required operations are done within the DF path of the PAE
- $2 \leq n \leq 4$ The ALU path is required since 4 ports are necessary
- $n > 4$ Multiple ALUs have to be combined

This method saves a significant amount of static resources in silicon but requires dedicated PAE resources at runtime.

It is therefore to evaluate

- c) how much silicon area is saved per bus
- d) how often occurs $n=2, 2 \leq n \leq 4, n > 4$

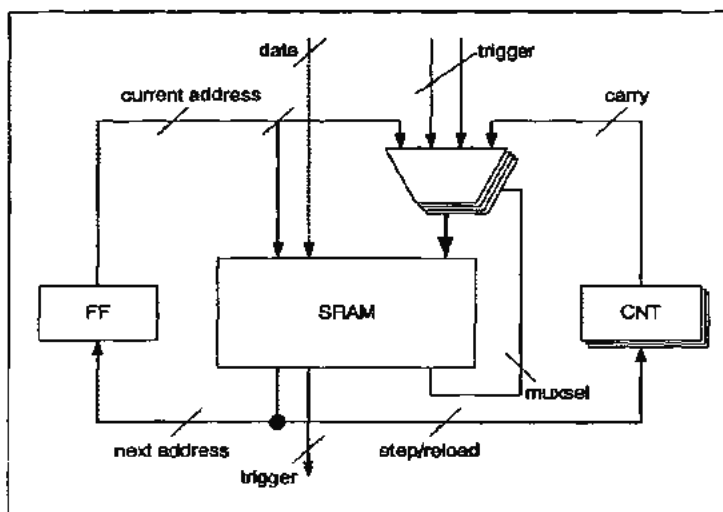
e) the ratio between saved silicon area and required PAE resources



1.5 FSM in RAM-PAEs

In the V2.0 architecture implementing control structures is very costly, a lot of resources are required and programming is quite difficult.

However memories can be used for a simple FSMs implementation. The following enhancement of the RAM-PAEs offers a cheap and easy to program solution for many of the known control issues, including HDTV.



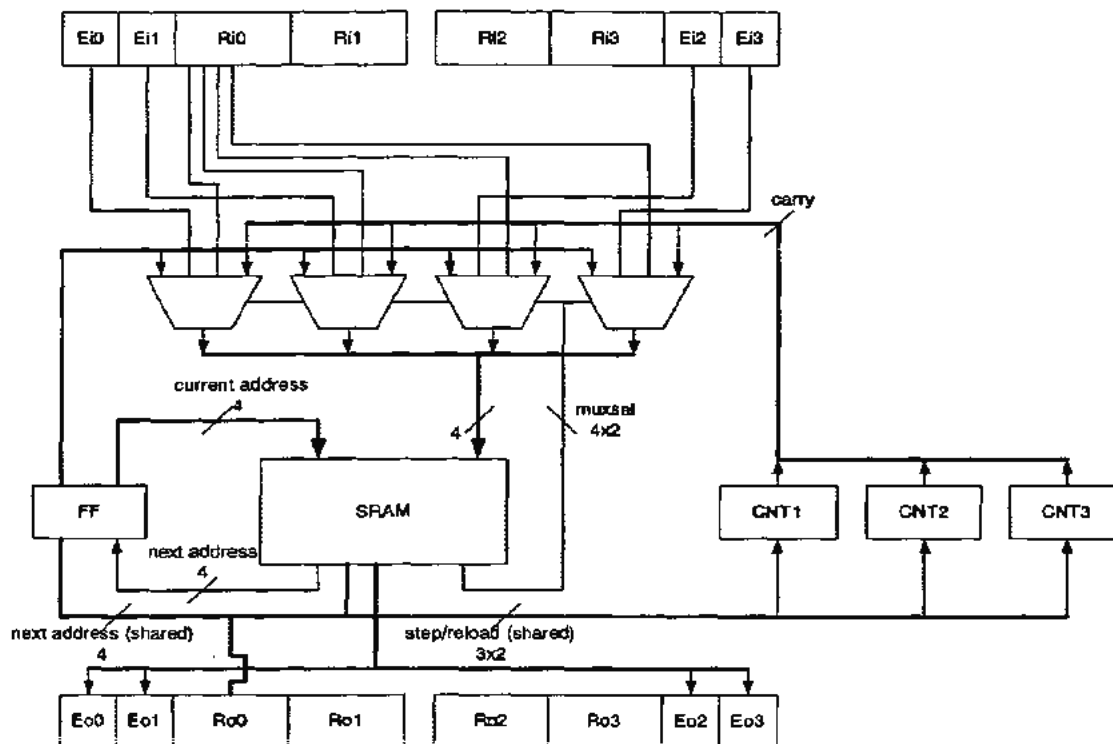
Basically the RAM-PAE is enhanced by an feedback from the data output to the address input through a register (FF) to supply subsequent address within each stage. Furthermore additional address inputs from the PAE array can cause conditional jumps, data output will generate event signals for the PAE array. Associated counters which can be reloaded and stepped by the memory output generate address input for conditional jumps (i.e. end of line, end of frame of a video picture).

At typical RAM-PAE implementation has about 16-32 data bits but only 8-12 address bits. To optimize the range of input vectors it is therefore suggestive to insert some multiplexers at the address inputs to select between multiple vectors, whereas the multiplexers are controlled by some of the output data bits.

The implementation for a XPP having 24bit wide data busses is sketched in the next figure. 4 event inputs are used as input, as well as the lower for bits of input port Ri0. 3 counters are implemented, 4 events are generated as well as the lower 10 bits of the Ro0 port.

The memory organisation is as follows:

8 address bits
 24 data bits (22 used)
 4 next address
 8 multiplexer selectors
 6 counter control (shared with 4 additional next address)
 4 output



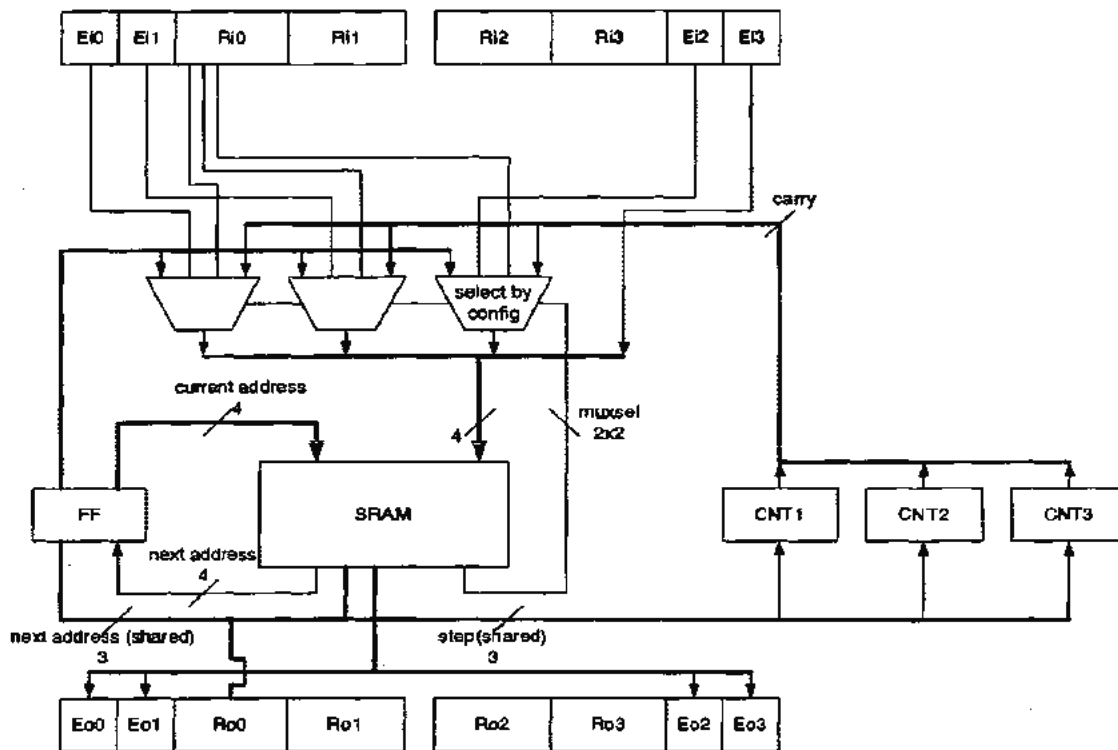
Please note that the typical memory mode of the RAM-PAE is not sketched in the block diagram above.

The width of the counters is according to the bus width of the data busses.

For a 16 bit implementation it is suggested to use the carry signal of the counters as their own reload signal (auto reload), also some of the multiplexers are not driven by the memory but "hard wired" by the configuration.

The proposed memory organisation is as follows:

8 address bits
 16 data bits (16 used)
 4 next address
 4 multiplexer selectors
 3 counter control (shared with 3 additional next address)
 4 output



Actually the RAM-PAEs are not scaleable any more since the 16-bit implementation is different from the 24-bit implementation. It is to decide whether the striped down 16-bit implementation is used for 24-bit also.

1.6 IOAG interface

1.6.1 Address Generators and bit reversal addressing

Implemented within the IO interfaces are address generators to support 1 to 3 dimensional addressing directly without any ALU-PAE resources. The address generation is done by 3 counters, each of them has configurable base address, length and step width.

The first counter (CNT1) has a step input to be controlled by the array of ALU-PAEs. Its carry is connected to the step input of CNT2, which carry again is connected to the step input of CNT3.

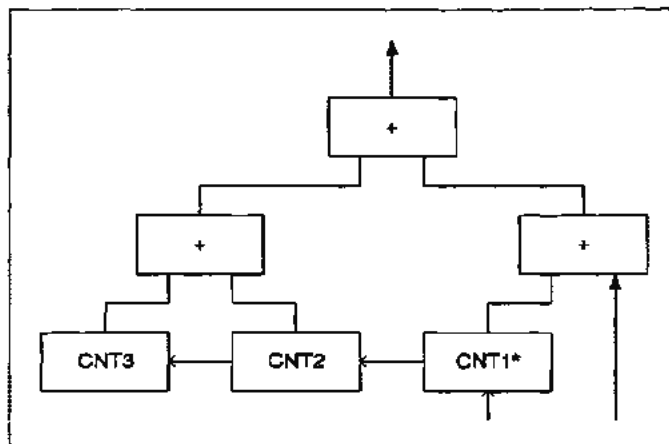
Each counter generates carry if the value is equal to the configured length. Immediately with carry the counter is reset to its configured base address.

One input is dedicated for addresses from the array of ALU-PAEs which can be added to the values of the counters. If one or more counters are not used they are configured to be zero.



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In addition CNT1 supports generation of bit reversal addressing by supplying multiple carry modes.



1.6.2 Support for different word width

In general it is necessary to support multiple word width within the PAE array. 8 and 16 bit wide data words are preferred for a lot of algorithms i.e. graphics. In addition to the already described SIMD operation, the IOAG allows the split and merge of such smaller data words.

Since the new PAE structure allows 4 input and 4 output ports, the IOAG can support word splitting and merging as follows:

I/O 0	I/O 1	I/O 2	I3
16/24/32-bit data word			address
16-bit data word	16-bit data word		address
8-bit data word	8-bit data word	8-bit data word	address

Input ports are merged within the IOAG for word writes to the IO.

For output ports the read word is split according to the configured word width.

1.7 XPP / μ P coupling

For a closed coupling of a μ P and a XPP a cache and register interface would be the preferable structure for high level tools like C-compilers. However such a close coupling is expected not to be doable in a very first step.

Two different kind of couplings are necessary for a tight coupling:

- a) memory coupling for large data streams: The most convenient method with the highest performance is a direct cache coupling, whereas an AMBA based memory coupling will be sufficient for the beginning (to be discussed with ATAIR)



PACT

- b) register coupling for small data and irregular MAC operations: Preferable is a direct coupling into the processors registers with an implicit synchronisation in the OF-stage of the processor pipeline. However coupling via load/store- or in/out-commands as external registers is acceptable with the penalty of a higher latency which causes some performance limitation (already agreed with ATAIR)



2 Specification of ALU-PAE

2.1 Overview

The ALU-PAE comprises 3 paths:

- ALU arithmetic, logic and data flow handling
- DF data flow handling and bypass
- BP bypass

Each of the paths contains 2 data busses and 1 event bus. The busses of the DF path can be rerouted to the ALU path by configuration.

2.2 ALU path Registers

The ALU path comprises 12 data registers:

- Ri0-3 Input data register 0-3 from bus
- Rv0-3 Virtual output data register 0-3 to bus
- Rd0-3 Internal general purpose register 0-3

- Ei0-3 Event input 0-3 from bus
- Ev0-3 Virtual event output register 0-3 to bus
- Fu, Fv Flag u and v according to the V2.0 PAE

Note: Ri2 and Ri3 belong typically to the DF path, but can be allocated for the ALU by configuration.

Eight instruction registers are implemented, each of them is 16 bit wide according to the opcode format.

- Rc0-7 Instruction registers

Three special purpose registers are implemented:

- Rlc Loop Counter, configured by CM, not accessible through ALU-PAE itself. Will be decremented according to JL opcode. Is reloaded after value 0 is reached.
- Rjb Jump-Back register to define the number of used entries in Rc[0..7]. It is not accessible through ALU-PAE itself.
If Rpp is equal to Rjb, Rpp is immediately reset to 0. The jump back can be bound to a condition i.e. an incoming event. If the condition is missing, the jump back will be delayed.
- Rpp Program pointer

2.3 Data duplication and multiple input reads

Since Function Folding can operate in a purely data stream mode as well as in a sequential mode (see 1.2) it is useful to support Ri reads in dataflow mode (single



read only) and sequential mode (multiple read). The according protocols are described below:

Each input register R_i can be configured to work in one of two different modes:

Dataflow Mode

This is the standard protocol of the V2.0 implementation:

A data packet is taken read from the bus if the register is empty, an ACK handshake is generated. If the register is not empty ACK the data is not latched and ACK is not generated.

If the register contains data, it can be read once. Immediately with the read access the register is marked as empty. An empty register cannot be read.

Simplified the protocol is defined as follows:

RDY & empty	→ full
	→ ACK
RDY & full	→ notACK
READ & empty	→ stall
READ & full	→ read data
	→ empty

Please note: pipeline effects are not taken into account in this description and protocol.

Sequencer Mode

The input interface is according to the bus protocol definition: A data packet is taken read from the bus if the register is empty, an ACK handshake is generated. If the register is not empty ACK the data is not latched and ACK is not generated. If the register contains data it can be read multiple times during a sequence. A sequence is defined from $R_{pp} = 0$ to $R_{pp} = R_{jb}$. During this time no new data can be written into the register. Simultaneously with the reset of R_{pp} to 0 the register content is cleared an new data is accepted from the bus.

Simplified the protocol is defined as follows:

RDY & empty	→ full
	→ ACK
RDY & full	→ notACK
READ & empty	→ stall
READ & full	→ read data
$(R_{pp} == R_{jb})$	→ empty

Please note: pipeline effects are not taken into account in this description and protocol.



2.4 Data register and event handling

Data registers are directly addressed, each data register can be individually selected. Since a two address opcode form is used, register operations follow the rule $op\ r_a \leftarrow r_a, r_b$. An virtual output register is selected by adding 'out' behind the opcode. The result will be stored in r_a and copied to the virtual output register r_v as well according to the rule $op\ out\ (r_v, r_a) \leftarrow r_a, r_b$. Please note, accessing input and (virtual) output registers follow the rules defined in chapter 2.3.

Rotating Select

Under normal conditions data and events are read one time according to the principles of Petri-Nets. Therefore for most applications a one time access per *Cycle* is sufficient. Also per definition one data or event is generated by a Petri-Net per channel and *Cycle*.

If Function Folding is done in a sequential manner synchronisation is achieved by using WAIT and SKIP commands. If multiple accesses to an event are required it can be copied by the READE instruction to the u or v flags which can be used successively for multiple commands.

The Rotating Select starts on the first access to events with the event E0, steps with the second access over E1 and E2, to E3 (at the fourth access) and restarts with the fifth access at E0 again.

Reset or Rpp == Rjb	after 1st event access	after 2nd event access	after 3rd event access	after 4th event access
E0	E1	E2	E3	continue with E0

Rotating select is supported for reading events and writing events with an explicit rotation counter for each read and write. Writing to events copies the value to the u flag at the same time, et(v) and ee(v) causes copying to the v flag.

For each opcode E0 and the internal flags u and v can be selected explicitly by the following selection modes. E0 can therefore be easily used as for multiple write event accesses per *Cycle* since there is no need to use the rotating select mode for E0 for most of the opcodes:

et (event target)
es (event source)

00	Internal u
01	Internal v
10	External Ev0
11	Rotating select: External next (Ev0/Ev1/EV2.0/EV2.2) and internal u flag

eventt (event target)
events (event source)

000	Internal u
001	Internal v
010	Ev0
011	Ev1
100	EV2.0
101	EV2.2
110	
111	Rotating select: External next



	(Ev0/Ev1/EV2.0/EV2.2) and internal u flag
--	--

Event Enable enables or disables writing a flag to an virtual event output. However the flag will be set in the internal u or v register anyhow.

ee (event enable)

0	Internal v or u
1	Internal v or u & Rotating select: External next (Ev0/Ev1/EV2.0/EV2.2) and internal v or u flag

Event sources

Instructions offering only ALU internal flags as source for the operations:

- SAT

The event addressing supports the selection between the u and v flag.

Instructions allowing directly addressed event sources using *eventt* and *events*:

- WAIT, SKIP, READE, WRITEE
- MERGE, DEMUX, SWAP

Instructions offering limited addressed event sources and rotating event select (*et*, *es*):

- SHL, SHR, DSHL, DSHR, DSHRU
- ADD, ADDC, SUB, SUBC

Event targets

Some instructions operate using rotating event select only (*et*, *es*):

- NOT, SORT, SORTU, CLZ, CLZU, AND, OR, XOR, EQ, CMP, CMPU

Some instructions support Event Enable only (*ee*):

- SHL, SHR, DSHL, DSHR, DSHRU
- ADD, ADDC, SUB, SUBC

2.4.1 n:1 Transitions

1:n transitions are not supported within the busses any more. Alternatively simple writes to multiple output registers *Ro* and event outputs *Eo* are supported. The Virtual Output registers (*Rv*) and Virtual Event (*Ev*) are translated to real Output registers (*Ro*) and real Events (*Eo*), whereas a virtual register can be mapped to multiple output registers.

To achieve this a configurable translation table is implemented for both data registers and event registers:



Rv Ev	Ro0 Eo0	Ro1 Eo1	Ro2 Eo2	Ro3 Eo3
0				
1				
2				
3				

Example:

Rv0 mapped to Ro0, Ro1

Rv1 mapped to Ro2

RV2.0 mapped to Ro3

RV2.2 unused

Rv	Ro0	Ro1	Ro2	Ro3
0	1	1	0	0
1	0	0	1	0
2	0	0	0	1
3	0	0	0	0

2.4.2 Accessing input and output registers (Ri/Rv) and events (Ei/Ev)

Independently from the opcode accessing input or output registers or events is defined as follows:

Reading an input register:

Register status	Operation
empty	wait for data
full	read data and continue operation

Writing to an output register:

Register status	Operation
empty	write data to register
full	wait until register is cleared and can accept new data

2.5 Opcode format

To achieve a small opcode size a two address code is used. The basic operation is:

$$op\ r_a \leftarrow r_a, r_b$$

Source registers can be Ri and Rd, target registers are Rv and Rd. A typical operation targets only Rd registers. If the source register for r_a is $Ri[x]$ the target register will be $Rd[x]$.

The translation is shown in the following table:



Target	Source r_a
Rd0	Rd0
Rd1	Rd1
Rd2	Rd2
Rd3	Rd3
Rd0	Ri0
Rd1	Ri1
Rd2	Ri2
Rd3	Ri3

Each operation can target a Virtual Output Register Rv by adding an *out* tag as a target identifier to the opcode:

$$\text{op out } r_a \leftarrow r_a, r_b$$

The transfer is now Ri[x] or Rd[x] to Rv[x] as shown in the table below:

Target	Source r_a
Rv0	Rd0
Rv1	Rd1
RV2.0	Rd2
RV2.2	Rd3
Rv0	Ri0
Rv1	Ri1
RV2.0	Ri2
RV2.2	Ri3

The opcode format is 16 bit wide, the standard formats are:

2.6 Clock

The PAE can operate at a configurable clock frequency of

- 1x Bus Clock
- 2x Bus Clock
- 4x Bus Clock
- [8x Bus Clock]

2.7 The DF path

The DataFlow path comprises the data registers Ri2&3 and Ro2&3 as well as the events Ei2&3 and Eo2&3. Each of the data registers Ri[n] is combined with an event E[n] whereas the according busses support different routings.

By configuration each data path and its associated event can be dedicated to the ALU path.



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The DF path supports numerous instructions, whereas the instruction is selected by configuration and only one of them can be performed during a configuration, function folding is not available.

The following instructions are implemented:

1. ADD, SUB
2. NOT, AND, OR, XOR
3. SHL, SHR, DSHL, DSHR, DSHRU
4. EQ, CMP, CMPU
5. MERGE, DEMUX, SWAP
6. SORT, SORTU
7. ELUT

2.8 The BP path

The ByPass path is a simple horizontal network between the input data registers BRi0&1 and events BEi0&1 to the output registers BRo0&1 and events BEo0&1.



3 Input Output Address Generators (IOAG)

The IOAGs are located in the RAM-PAEs and share the same registers to the busses. An IOAG comprises 3 counters with forwarded carries. The values of the counters and an immediate address input from the array are added to generate the address. One counter offers reverse carry capabilities.

3.1 Addressing modes

Several addressing modes are supported by the IOAG to support typical DSP-like addressing:

Mode	Description
Immediate	Address generated by the PAE array
xD counting	Multidimensional addressing using IOAG internal counters xD means 1D, 2D, 3D
xD circular	Multidimensional addressing using IOAG internal counters, after overflow counters reload with base address
xD plus immediate Stack	xD plus a value from the PAE array decrement after "push" operations increment after "read" operations
Reverse carry	Reverse carry for applications such as FFT

3.1.1 Immediate Addressing

The address is generated in the array and directly fed through the adder to the address output. All counters are disabled and set to 0.

3.1.2 xD counting

Counters are enabled depending on the required dimension (x-dimensions require x counters). For each counter a base address and the step width as well as the maximum address are configured. Each carry is forwarded to the next higher and enabled counter; after carry the counter is reloaded with the start address. A carry at the highest enabled counter generates an event, counting stops.

3.1.3 xD circular

The operation is exactly the same as for xD counting, with the difference that a carry at the highest enabled counter generates an event, all counters are reloaded to their base address and continue counting.

3.1.4 Stack

One counter (CNT1) is used to decrement after data writes and increment after data reads. The base value of the counter can either be configured (base address) or loaded by the PAE array.

3.1.5 Reverse carry

Typically carry is forwarded from LSB to MSB. Forwarding the carry to the opposite direction (reverse carry) allows generating address patterns which are very well suited for applications like FFT and the like. The carry is discarded at MSB.

For using reverse carry a value larger than LSB must be added to the actual value to count, wherefore the STEP register is used.

Example:
 BASE = 0h
 STEP = 1000b

Step	Counter Value
1	b0...00000
2	b0...01000
3	b0...00100
4	b0...01100
5	b0...00010
...	...
16	b0...01111
17	b0...00000

The counter is implemented to allow reverse carry at least for STEP values of -2, -1, +1, +2.



Appendix A OpCodes

Notation:

Registers

name	explanation	number of bits			
target_r	Target register and related source register	2	Rd0	00	
			Rd1	01	
			Rd2	10	
			Rd3	11	
target_o	Target output register and related source register	2	Ro0	00	
			Ro1	01	
			Ro2	10	
			Ro3	11	
target	Target register and related source register. Target will be Rd or Ro (if target identifier is set)	3	Ri0	000	
			Ri1	001	
			Ri2	010	
			Ri3	011	
			Rd0	100	
			Rd1	101	
			Rd2	110	
			Rd3	111	
target_p	Target register pair and related source register pair	2	Ro0&1	00	
			Ro2&3	01	
			Rd0&1	10	
			Rd2&3	11	
source_i	Source input register	2	Ri0	00	
			Ri1	01	
			Ri2	10	
			Ri3	11	
source	Source register	3	Ri0	000	
			Ri1	001	
			Ri2	010	
			Ri3	011	
			Rd0	100	
			Rd1	101	
			Rd2	110	
			Rd3	111	
source_p	Source register pair	2	Ri0&1	00	
			Ri2&3	01	
			Rd0&1	10	
			Rd2&3	11	
r_pair_t	Source register and target register pair	2	target	source	
			Rd0&1	Ri0	00
			Rd2&3	Ri2	01



			Rd0&1	Rd0	10
			Rd2&3	Rd2	11
tid	Target Identifier	1	0	Internal Register	
			1	Internal & External Register	
val	Value	1	one bit value		
valx	Value including don't care	2	00	0	
			01	1	
			10	X	
			11	X	
val2	2 bit value	2	00	00	
			01	01	
			10	10	
			11	11	
u/v	Select flag register Fu or Fv	1	0	Fu	
			1	Fv	
et	event target	2	00	Internal u	
			01	Internal v	
			10	External E0	
			11	External next (E1/E2/E3)	
es	event source	2	00	Internal u	
			01	Internal v	
			10	External E0	
			11	External next (E1/E2/E3)	
event	event target (or source)	3	000	Internal u	
			001	Internal v	
			010	E0	
			011	E1	
			100	E2	
			101	E3	
			110		
			111	External next (E1/E2/E3)	
ee	event enable	2	0	Internal	
			1	Internal & External next (E1/E2/E3)	



0123456	7	8	9	10	11	12	13	14	15	IF	OF	Comment
NOP 000000	0	0	0	0	0	0	0	0	0			No Operation
READ 000000	0	target_r		0	source_i		0	1	0			Read packet from input port
WRITE 000000	1	target_o		0	source		1	0				Write packet to output port
MOVE 000000	0	target_r		1	source_r		0	1	0			Move data between register
LOAD 000000	1	target_r		1	0	0	0	1	0			Load register with constant
constant												
SAT 000000	0	target_r		0	0	0	1	0	0	U		Saturate if carry '0 if previous command was SUBC '1 if previous command was ADDC
SETUV 000000	0	val	u/v	0	0	1	1	0	0		U/V	Set Flags uf and vf
SWAPUV 000000	0	0	0	1	0	1	1	0	0		U/V	Swap u and v flag
NOT 000000	tid	target		1	et		0	0			U	
JR 000000	adr7							0	1			Jump relative
JL 000000	adr7							1	1			Jump relative if Rlc is not zero
MERGE 000001	tid	target_p		source_p		event		0		U		
DEMUX 000001	tid	target_p		source_p		event		1		U		
SWAP 000010	tid	target_p		source_p		event		0		U		
WAIT 000010	0	valx		0	0	event		1		U		Wait for incoming event
SKIP 000010	0	valx		0	1	event		1		U		Wait for incoming event
EOPTR 000010	0	val2		1	0	0	0	0	1			Set event output pointer
EIPTR												Set event input pointer



000010	0	val2	1	0	0	0	1	1			
READE											Read Event to U/V
000010	0	0	u/v	1	1	event		1	U/V		
WRITEE											Write Event from U/V
000010	0	1	u/v	1	1	event		1	U/V		
SORT	tid	target_p	source_p	et(u)	et(v)				U/V		Sort two data packets
000011											
SORTU	tid	target_p	source_p	et(u)	et(v)				U/V		Sort two unsigned data packets
000100											
CLZ	tid	target	event	0	0				U		Count leading zeros
000101											
CLZU	tid	target	event	0	1				U		Count leading zeros unsigned
000101											
AND	tid	target	source	et(u)					U		
000110											
OR	tid	target	source	et(u)					U		
000111											
XOR	tid	target	source	et(u)					U		
001000											
EQ	tid	target	source	et(v)					U		Equal
001001											
CMP	tid	r_pair_t	source_p	et(u)	et(v)				U/V		
001001											
CMPU	tid	r_pair_t	source_p	et(u)	et(v)				U/V		
001010											
BSHL	tid	r_pair_t	0	source	0	0					Barrel Shift left
001011											
BSHR	tid	r_pair_t	0	source	0	1					Barrel Shift right
001011											
BSHRU	tid	r_pair_t	0	source	1	0					Barrel Shift right unsigned
001011											
MUL	tid	r_pair_t	1	source	0	0					
001011											
MULU	tid	r_pair_t	1	source	0	1					
001011											
DIV	tid	r_pair_t	1	source	1	1					
001011											



012345	6	7	8	9	10	11	12	13	14	15	IF	OF	Comment
SHL 100000	tid	r_pair_t		source			es	ee(u)	ee(v)		U	U/V	
SHR 100001	tid	r_pair_t		source			es	ee(u)	ee(v)		U	U/V	
DSHL 100010	tid	r_pair_t		source			es	ee(u)	ee(v)		U	U/V	
DSHR 100011	tid	r_pair_t		source			es	ee(u)	ee(v)		U	U/V	
DSHRU 101000	tid	r_pair_t		source			es	ee(u)	ee(v)		U	U/V	
ASI 101001 101010 101011 101100 101101 101110													Application specific instructions

01234	5	6	7	8	9	10	11	12	13	14	15	IF	OF	Comment
ADD 11000	tid	target			source			es	ee(u)	ee(v)		U	U/V	
ADDC 11001	tid	target			source			es	ee(u)	ee(v)		U	U/V	
SUB 11010	tid	target			source			es	ee(u)	ee(v)		U	U/V	
SUBC 11011	tid	target			source			es	ee(u)	ee(v)		U	U/V	

Akte: PACT48/EP ----

EPO - Munich
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28. Aug. 2003

European Patent Application

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Title: Device and method for data processing

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Claims

1. A data processing unit having a plurality of cells, in particular coarse-grained logic cells, interconnected and/or interconnectable for data processing wherein at least one cell, preferably a number of cells have instruction storage means for storing instructions to be executed so as that said coarse-grained cells form a plurality of sequencers within said array.
20
2. A method for operating data processing in an array comprising a plurality of logic cells, in particular coarse-grained logic cells interconnected and/or interconnectable for data processing, wherein data are transferred into cells from an input and/or from other cells via busses, characterised in that at least some of the busses are used for effecting a configuration of said
25
30

Akte: PACT48/EP

cells, in particular during runtime and/or without effecting cells not to be configured.

3. Method according to claim 2, wherein said busses are used
5 with a frequency different from the frequency of data processing in at least some of the cells.

**U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE**

INFORMATION DISCLOSURE STATEMENT		Docket Number: 2885/139	Confirmation Number: 2050
Application Number 12/836,364	Filing Date July 14, 2010	Examiner Don P. Le	Art Unit 2819
Invention Title RECONFIGURABLE SEQUENCER STRUCTURE		Inventors Martin VORBACH	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I hereby certify that this correspondence is being electronically transmitted to the United States Patent and Trademark Office via the Office electronic filing system on

Date: October 25, 2010

Signature: /Eunice K. Chang/
Eunice K. Chang

Sir:

Pursuant to 37 CFR § 1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom. The filing of this Information Disclosure Statement and the enclosed PTO Form No. 1449, shall not be construed as an admission that the information cited is prior art, or is considered to be material to patentability as defined in 37 C.F.R. § 1.56(b). The paragraphs marked below are applicable. It is believed that no fees other than those indicated below are due, but authorization is hereby given to charge any additional fees due, or to credit any overpayment, to Kenyon & Kenyon LLP, deposit account 11-0600.

1. This Information Disclosure Statement is being filed (a) within three months of the filing date of a national application other than a continued prosecution application under 37 C.F.R. §1.53(d), (b) within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, (c) before the mailing date of a first Office Action on the merits in the present application, OR (d) before the mailing of a first office action after filing of a request for continued examination. No certification or fee is required.

2. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a final action, Notice of Allowance, or any action that otherwise closes prosecution.

a. I hereby certify that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(1).

b. I hereby certify that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(2).

c. The required fee of \$180.00 under 37 CFR §1.17(p) is being paid by credit card to ensure consideration of the disclosed information. Any additional fees may be charged to Deposit Account No. 11-0600 of Kenyon & Kenyon LLP

3. Since this application was filed after June 30, 2003, copies of U.S. references are not included.

Respectfully submitted,

Date: October 25, 2010

/Aaron Grunberger/
Aaron Grunberger
Reg. No. 59,210

KENYON & KENYON LLP
One Broadway
New York, NY 20004
(212) 425-7200 telephone
(212) 425-5288 facsimile
CUSTOMER NUMBER 26646

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/139	Serial No. 12/836,364
	Applicant(s) VORBACH	
	Filing Date July 14, 2010	Group Art Unit 2819

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	4,151,611	April 24, 1979	Sugawara et al.			
	5,036,493	July 30, 1991	Nielsen			
	5,568,624	October 22, 1996	Sites et al.			
	5,581,734	December 3, 1996	DiBrino et al.			
	6,078,736	June 20, 2000	Guccione			
	6,212,544	April 3, 2001	Borkenhagen et al.			
	6,624,819	September 23, 2003	Lewis			
	6,725,334	April 20, 2004	Barroso et al.			
	7,759,968	July 20, 2010	Hussein et al.			
	2002/0099759	July 25, 2002	Gootherts			
	2003/0154349	August 14, 2003	Berg et al.			
	2007/0083730	April 12, 2007	Vorbach et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

OTHER DOCUMENTS

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Culler, D.E; Singh, J.P., "Parallel Computer Architecture," Page 17, 1999, Morgan Kaufmann, San Francisco, CA USA, XP002477559.
	Short, Kenneth L., <i>Microprocessors and Programmed Logic</i> , Prentice Hall, Inc., New Jersey 1981, p. 34.
	Webster's Ninth New Collegiate Dictionary, Merriam-Webster, Inc., 1990, page 332 (definition of "dedicated").

EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

Electronic Acknowledgement Receipt

EFS ID:	8692757
Application Number:	12836364
International Application Number:	
Confirmation Number:	2050
Title of Invention:	RECONFIGURABLE SEQUENCER STRUCTURE
First Named Inventor/Applicant Name:	Martin Vorbach
Customer Number:	26646
Filer:	Aaron Grunberger/Eunice Chang
Filer Authorized By:	Aaron Grunberger
Attorney Docket Number:	2885/139
Receipt Date:	25-OCT-2010
Filing Date:	14-JUL-2010
Time Stamp:	14:16:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	2885-139-SupplIDS.pdf	345793 <small>4a449959c5591e72356245152dfd6126d06e8e2a</small>	no	3

Warnings:

Information:

INTEL - 1004

This is not an USPTO supplied IDS fillable form

2	NPL Documents	Culler-et-al-Pg-17.pdf	118705	no	1
			563dfd755eb476d2957f9f424706006571d89725		

Warnings:

Information:

3	NPL Documents	Short-Kenneth-Microprocessors-Logic.pdf	640057	no	4
			0454d704c313ceaab0ba41bef38f109ad3496821		

Warnings:

Information:

4	NPL Documents	Websters-DEDICATED.pdf	366255	no	3
			68bf9bacad0bb4b5369274b48efd83d98e54b20f		

Warnings:

Information:

Total Files Size (in bytes):			1470810		
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



NOTICE OF ALLOWANCE AND FEE(S) DUE

26646 7590 11/12/2010

KENYON & KENYON LLP
ONE BROADWAY
NEW YORK, NY 10004

EXAMINER
LE, DON P
ART UNIT PAPER NUMBER
2819
DATE MAILED: 11/12/2010

Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO.

12/836,364 07/14/2010 Martin Vorbach 2885/139 2050

TITLE OF INVENTION: RECONFIGURABLE SEQUENCER STRUCTURE

Table with 7 columns: APPLN. TYPE, SMALL ENTITY, ISSUE FEE DUE, PUBLICATION FEE DUE, PREV. PAID ISSUE FEE, TOTAL FEE(S) DUE, DATE DUE

nonprovisional YES \$755 \$300 \$0 \$1055 02/14/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

- A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.
B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

- A. Pay TOTAL FEE(S) DUE shown above, or
B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26646 7590 11/12/2010

**KENYON & KENYON LLP
 ONE BROADWAY
 NEW YORK, NY 10004**

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/836,364	07/14/2010	Martin Vorbach	2885/139	2050

TITLE OF INVENTION: RECONFIGURABLE SEQUENCER STRUCTURE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$755	\$300	\$0	\$1055	02/14/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
LE, DON P	2819	326-038000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

"Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE _____ (B) RESIDENCE: (CITY AND STATE OR COUNTRY) _____

Please check the appropriate assignee category or categories (will not be printed on the patent) : Individual Corporation or other private group entity Government

4a. The following fee(s) are submitted:

Issue Fee

Publication Fee (No small entity discount permitted)

Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

A check is enclosed.

Payment by credit card. Form PTO-2038 is attached.

The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

Table with columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO., EXAMINER, ART UNIT, PAPER NUMBER. Includes application details for Martin Vorbach and examiner LE, DON P.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability

Application No.

12/836,364

Examiner

Don P. Le

Applicant(s)

VORBACH, MARTIN

Art Unit

2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

- 1. This communication is responsive to document filed 7/14/2010.
- 2. The allowed claim(s) is/are 18-47.
- 3. Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some* c) None of the:
 - 1. Certified copies of the priority documents have been received.
 - 2. Certified copies of the priority documents have been received in Application No. _____.
 - 3. Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

- 4. A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 - 5. CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) hereto or 2) to Paper No./Mail Date _____.
 - (b) including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**
- 6. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- 1. Notice of References Cited (PTO-892)
- 2. Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date See Continuation Sheet
- 4. Examiner's Comment Regarding Requirement for Deposit of Biological Material
- 5. Notice of Informal Patent Application
- 6. Interview Summary (PTO-413), Paper No./Mail Date _____.
- 7. Examiner's Amendment/Comment
- 8. Examiner's Statement of Reasons for Allowance
- 9. Other _____.

Continuation of Attachment(s) 3. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date: 7/14/2010, 7/14/2010, 8/2/2010, 9/22/2010, 10/25/2010.

Allowable Subject Matter

1. Claims 18-47 are allowed.
2. The following is an examiner's statement of reasons for allowance:

With respect to claim 18, the prior art does not teach a multi-processor chip, comprising: a plurality of data processing cells, each adapted for sequentially executing at least one of algebraic and logic functions and having: at least one arithmetic logic trait; at least one data register file; a program pointer; and at least one instruction decoder; a plurality of memory cells; at least one interface unit; at least one Memory Management Unit (MMU); and a bus system for interconnecting the plurality of data processing cells, the plurality of memory cells, and the at least one interface trait; wherein the bus system is adapted for programmably interconnecting at runtime at least one of data processing cells and memory cells with at least one of memory cells and one or more of the at least one interface unit.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don P. Le whose telephone number is 571-272-1806. The examiner can normally be reached on 7AM - 5PM.

Art Unit: 2819

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Barnie Rexford can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Don P Le/
Primary Examiner, Art Unit 2819
11/7/2010

Notice of References Cited	Application/Control No. 12/836,364	Applicant(s)/Patent Under Reexamination VORBACH, MARTIN	
	Examiner Don P. Le	Art Unit 2819	Page 1 of 1

U.S. PATENT DOCUMENTS

*	Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A US-2008/0313383	12-2008	Morita et al.	711/6
*	B US-2005/0091468	04-2005	Morita et al.	711/202
	C US-			
	D US-			
	E US-			
	F US-			
	G US-			
	H US-			
	I US-			
	J US-			
	K US-			
	L US-			
	M US-			

FOREIGN PATENT DOCUMENTS

*	Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N				
	O				
	P				
	Q				
	R				
	S				
	T				

NON-PATENT DOCUMENTS

*	Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)				
	U				
	V				
	W				
	X				

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.


EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	17	register and pointer and MMU and runtime and (memory adj cell) and arithmetic and interface and interconnect	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/11/07 07:24
L2	36	register and pointer and MMU and runtime and (memory adj cell)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/11/07 07:51
L3	3792	runtime and (programmable adj logic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/11/07 07:52
L4	461	3 and arithmetic	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/11/07 07:52
L5	201	4 and pointer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/11/07 07:52

11/ 7/ 2010 7:52:44 AM

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Search Notes 	Application/Control No. 12836364	Applicant(s)/Patent Under Reexamination VORBACH, MARTIN
	Examiner Don P Le	Art Unit 2819

SEARCHED			
Class	Subclass	Date	Examiner
326	37-41, 46	11/20105	dl

SEARCH NOTES		
Search Notes	Date	Examiner
east + interference	11/7/2010	dl

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
	see search notes	11/7/2010	dl

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INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/139	Serial No. 12/836,364
	Applicant(s) VORBACH	
	Filing Date July 14, 2010	Group Art Unit 2827

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	90/010,450		Vorbach et al.			March 27, 2009
	6,173,419	January 9, 2001	Barnett			
	6,668,237	December 23, 2003	Guccione et al.			
	6,836,842	December 28, 2004	Guccione et al.			
	2002/0010853	January 24, 2002	Trimberger et al.			
	2002/0152060	October 17, 2002	Tseng			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	1044571	February 16, 1989	Japan			Abstract	

OTHER DOCUMENTS

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Ballagh et al., "Java Debug Hardware Models Using JBits," 8 th Reconfigurable Architectures Workshop, 2001, 8 pages.
	Bellows et al., "Designing Run-Time Reconfigurable Systems with JHDL," Journal of VLSI Signal Processing 28, Kluwer Academic Publishers, The Netherlands, 2001, pp. 29-45.
	Guccione et al., "JBits: Java based interface for reconfigurable computing," Xilinx, Inc., San Jose, CA, 1999, 9 pages.
	Price et al., "Debug of Reconfigurable Systems," Xilinx, Inc., San Jose, CA, Proceedings of SPIE, 2000, pp. 181-187.
	Sundararajan et al., "Testing FPGA Devices Using JBits," Proc. MAPLD 2001, Maryland, USA, Katz (ed.), NASA, CA, 8 pages.

EXAMINER	/Don Le/	DATE CONSIDERED	11/06/2010
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/139	Serial No. 12/836,364
	Applicant(s) VORBACH	
	Filing Date July 14, 2010	Group Art Unit 2819

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
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	5,568,624	October 22, 1996	Sites et al.			
	5,581,734	December 3, 1996	DiBrino et al.			
	6,078,736	June 20, 2000	Guccione			
	6,212,544	April 3, 2001	Borkenhagen et al.			
	6,624,819	September 23, 2003	Lewis			
	6,725,334	April 20, 2004	Barroso et al.			
	7,759,968	July 20, 2010	Hussein et al.			
	2002/0099759	July 25, 2002	Gootherts			
	2003/0154349	August 14, 2003	Berg et al.			
	2007/0083730	April 12, 2007	Vorbach et al.			

FOREIGN PATENT DOCUMENTS


EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

OTHER DOCUMENTS

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Culler, D.E; Singh, J.P., "Parallel Computer Architecture," Page 17, 1999, Morgan Kaufmann, San Francisco, CA USA, XP002477559.
	Short, Kenneth L., <u>Microprocessors and Programmed Logic</u> , Prentice Hall, Inc., New Jersey 1981, p. 34.
	Webster's Ninth New Collegiate Dictionary, Merriam-Webster, Inc., 1990, page 332 (definition of "dedicated").

EXAMINER	/Don Le/	DATE CONSIDERED	11/06/2010
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Issue Classification 	Application/Control No. 12836364	Applicant(s)/Patent Under Reexamination VORBACH, MARTIN
	Examiner Don P Le	Art Unit 2819

ORIGINAL				INTERNATIONAL CLASSIFICATION													
CLASS		SUBCLASS		CLAIMED						NON-CLAIMED							
326		38		H	0	3	K	19 / 173 (2006.01.01)									
CROSS REFERENCE(S)																	
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																
326	46																

Claims renumbered in the same order as presented by applicant
 CPA
 T.D.
 R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17	16	33										
	2	1	18	17	34										
	3	2	19	18	35										
	4	3	20	19	36										
	5	4	21	20	37										
	6	5	22	21	38										
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	8	7	24	23	40										
	9	8	25	24	41										
	10	9	26	25	42										
	11	10	27	26	43										
	12	11	28	27	44										
	13	12	29	28	45										
	14	13	30	29	46										
	15	14	31	30	47										
	16	15	32												

NONE	Total Claims Allowed:	
(Assistant Examiner)	30	
/Don P Le/ Primary Examiner, Art Unit 2819	(Date) 11/07/2010	O.G. Print Claim(s) 1
(Primary Examiner)	(Date)	O.G. Print Figure 2A

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/139	Serial No. Unassigned
	Applicant(s) VORBACH	
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EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	RE34363	August 31, 1993	Freeman			
	RE34,444	November 16, 1993	Kaplinsky			
	RE37,195	May 29, 2001	Kean			
	60/109,417	November 18, 1998	Jefferson et al.			
	2,067,477	January 12, 1937	J.B. Cooper			
	3,242,998	March 29, 1966	C.H. Gubbins			
	3,681,578	August 1, 1972	Stevens			
	3,757,608	September 11, 1973	Willner			
	3,855,577	December 17, 1974	Vandierendonck			
	4,233,667	November 11, 1980	Devine et al.			
	4,414,547	November 8, 1983	Knapp et al.			
	4,489,857	February 6, 1986	Agrawal et al.			
	4,498,134	February 5, 1985	Hansen et al.			
	4,498,172	February 5, 1985	Bhavsar			
	4,566,102	January 21, 1986	Hefner			
	4,571,736	February 18, 1986	Agrawal et al.			
	4,590,583	May 20, 1986	Miller			
	4,591,979	May 27, 1986	Iwashita			
	*4,623,997	November 18, 1986	Tulpule			
	4,663,706	May 5, 1987	Allen et al.			
	4,667,190	May 19, 1987	Fant et al.			
	4,682,284	July 21, 1987	Schrofer			
	4,706,216	November 10, 1987	Carter			
	4,720,778	January 19, 1988	Hall et al.			
	4,720,780	January 19, 1988	Dolecek			
	4,739,474	April 19, 1988	Holsztynski			
	4,761,755	August 2, 1988	Ardini et al.			
	4,811,214	March 7, 1989	Nosenchuck et al.			
	4,852,043	July 25, 1989	Guest			
	4,852,048	July 25, 1989	Morton			
	4,860,201	August 22, 1989	Stolfo et al.			
	4,870,302	September 26, 1989	Freeman			
	4,882,687	November 21, 1989	Gordon			
	4,884,231	November 28, 1989	Mor et al.			
	4,891,810	January 2, 1990	de Corlieu et al.			
	4,901,268	February 13, 1990	Judd			
	4,910,665	March 20, 1990	Mattheyses et al.			
	4,918,440	April 17, 1990	Furtek et al.			

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EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	4,959,781	September 25, 1990	Rubinstein et al.			
	4,967,340	October 30, 1990	Dawes			
	4,972,314	November 20, 1990	Getzinger et al.			
	5,010,401	April 23, 1991	Murakami et al.			
	5,014,193	May 7, 1991	Garner et al.			
	5,015,884	May 14, 1991	Agrawal et al.			
	5,021,947	June 4, 1991	Campbell et al.			
	5,023,775	June 11, 1991	Poret			
	5,034,914	July 23, 1991	Osterlund			
	5,041,924	August 20, 1991	Blackborow et al.			
	5,043,978	August 27, 1991	Nagler et al.			
	5,047,924	September 10, 1991	Fujioka et al.			
	5,065,308	November 12, 1991	Evans			
	5,072,178	December 10, 1991	Matsumoto			
	5,081,375	January 14, 1992	Pickett et al.			
	5,099,447	March 24, 1992	Myszewski			
	5,109,503	April 28, 1992	Cruikshank et al.			
	5,113,498	May 12, 1992	Evan et al.			
	5,115,510	May 19, 1992	Okamoto et al.			
	5,123,109	June 16, 1992	Hillis			
	5,125,801	June 30, 1992	Nabity et al.			
	5,128,559	July 7, 1992	Steele			
	5,142,469	August 25, 1992	Weisenborn			
	5,144,166	September 1, 1992	Camarota et al.			
	5,193,202	March 9, 1993	Jackson et al.			
	5,203,005	April 13, 1993	Horst			
	5,204,935	April 20, 1993	Mihara et al.			
	5,208,491	May 4, 1993	Ebeling et al.			
	5,212,716	May 18, 1993	Ferraiolo et al.			
	*5,212,777	May 18, 1993	Gove et al.			
	5,218,302	June 8, 1993	Loewe et al.			
	5,226,122	July 6, 1993	Thayer et al.			
	5,233,539	August 3, 1993	Agrawal et al.			
	5,237,686	August 17, 1993	Asano et al.			
	5,247,689	September 21, 1993	Ewert			
	5,274,593	December 28, 1993	Proebsting			
	5,276,836	January 4, 1994	Fukumaru et al.			
	5,287,472	February 15, 1994	Horst			
	5,287,532	February 15, 1994	Hunt			

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EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,294,119	March 15, 1994	Vincent et al.			
	5,301,284	April 5, 1994	Estes et al.			
	5,301,344	April 5, 1994	Kolchinsky			
	5,303,172	April 12, 1994	Magar et al.			
	5,311,079	May 10, 1994	Ditlow et al.			
	5,327,125	July 5, 1994	Iwase et al.			
	5,336,950	August 9, 1994	Popli et al.			
	5,343,406	August 30, 1994	Freeman et al.			
	5,347,639	September 13, 1994	Rechtschaffen et al.			
	5,349,193	September 20, 1994	Mott et al.			
	5,353,432	October 4, 1994	Richek et al.			
	5,361,373	November 1, 1994	Gilson			
	5,379,444	January 3, 1995	Mumme			
	5,392,437	February 21, 1995	Matter et al.			
	5,408,643	April 18, 1995	Katayose			
	5,410,723	April 25, 1995	Schmidt et al.			
	5,412,795	May 2, 1995	Larson			
	5,418,952	May 23, 1995	Morley et al.			
	5,418,953	May 1995	Hunt et al.			
	5,421,019	May 30, 1995	Holsztynski et al.			
	5,422,823	June 6, 1995	Agrawal et al.			
	5,425,036	June 13, 1995	Liu et al.			
	5,426,378	June 20, 1995	Ong			
	5,428,526	June 27, 1995	Flood et al.			
	5,430,687	July 4, 1995	Hung et al.			
	5,440,245	August 8, 1995	Galbraith et al.			
	5,440,538	August 15, 1995	Olsen et al.			
	5,442,790	August 15, 1995	Nosenchuck			
	5,444,394	August 22, 1995	Watson et al.			
	5,448,186	September 5, 1995	Kawata			
	5,455,525	October 3, 1995	Ho et al.			
	5,457,644	October 10, 1995	McCollum			
	5,465,375	November 7, 1995	Thepaut et al.			
	5,469,003	November 21, 1995	Kean			
	5,473,266	December 5, 1995	Ahanin et al.			
	5,473,267	December 5, 1995	Stansfield			
	5,475,583	December 12, 1995	Bock et al.			
	5,475,803	December 12, 1995	Stearns et al.			
	5,475,856	December 12, 1995	Kogge			

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EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,477,525	December 19, 1995	Masanobu Okabe			
	5,483,620	January 9, 1996	Pechanek et al.			
	5,485,103	January 16, 1996	Pedersen et al.			
	5,485,104	January 16, 1996	Agrawal et al.			
	5,489,857	February 6, 1996	Agrawal et al.			
	5,491,353	February 13, 1996	Kean			
	5,493,239	February 20, 1996	Zlotnick			
	5,497,498	March 5, 1996	Taylor			
	5,506,998	April 9, 1996	Kato et al.			
	5,510,730	April 23, 1996	El Gamal et al.			
	5,511,173	April 23, 1996	Yamaura et al.			
	5,513,366	April 30, 1996	Agarwal et al.			
	5,521,837	May 28, 1996	Frankle et al.			
	5,522,083	May 28, 1996	Gove et al.			
	5,525,971	June 11, 1996	Flynn			
	5,530,873	June 25, 1996	Takano			
	5,530,946	June 25, 1996	Bouvier et al.			
	5,532,693	July 2, 1996	Winters et al.			
	5,532,957	July 2, 1996	Malhi			
	5,535,406	July 9, 1996	Kolchinsky			
	5,537,057	July 16, 1996	Leong et al.			
	5,537,580	July 16, 1996	Giomi et al.			
	5,537,601	July 16, 1996	Kimura et al.			
	5,541,530	July 30, 1996	Cliff et al.			
	5,544,336	August 6, 1996	Kato et al.			
	5,548,773	August 20, 1996	Kemeny et al.			
	5,550,782	August 27, 1996	Cliff et al.			
	5,555,434	September 10, 1996	Carlstedt			
	5,559,450	September 24, 1996	Ngai et al.			
	5,561,738	October 1, 1996	Kinerk et al.			
	5,570,040	October 29, 1996	Lytle et al.			
	*5,572,710	November 5, 1996	Asano et al.			
	5,574,930	November 12, 1996	Halverson Jr. et al.			
	5,581,731	December 3, 1996	King et al.			
	5,583,450	December 10, 1996	Trimberger et al.			
	5,586,044	December 17, 1996	Agrawal et al.			
	5,587,921	December 24, 1996	Agrawal et al.			
	5,588,152	December 24, 1996	Dapp et al.			
	5,590,345	December 31, 1996	Barker et al.			

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EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,590,348	December 31, 1996	Phillips et al.			
	5,596,742	January 21, 1997	Agarwal et al.			
	5,600,265	February 4, 1997	El Gamal Abbas et al.			
	5,600,845	February 4, 1997	Gilson			
	*5,606,698	February 25, 1997	Powell			
	5,611,049	March 11, 1997	Pitts			
	5,617,547	April 1, 1997	Feeney et al.			
	5,625,806	April 29, 1997	Kromer			
	5,625,836	April 29, 1997	Barker et al.			
	*5,627,992	May 6, 1997	Baror			
	5,634,131	May 27, 1997	Matter et al.			
	*5,646,544	July 8, 1997	Iadanza			
	5,646,545	July 8, 1997	Trimberger et al.			
	5,649,176	July 15, 1997	Selvidge et al.			
	5,649,179	July 15, 1997	Steenstra et al.			
	5,652,529	July 29, 1997	Gould et al.			
	5,652,894	July 29, 1997	Hu et al.			
	5,655,069	August 5, 1997	Ogawara et al.			
	5,655,124	August 5, 1997	Lin			
	5,657,330	August 12, 1997	Matsumoto			
	*5,659,785	August 19, 1997	Pechanek et al.			
	5,659,797	August 19, 1997	Zandveld et al.			
	5,675,743	October 7, 1997	Mavity			
	5,675,757	October 7, 1997	Davidson et al.			
	5,680,583	October 21, 1997	Kuijsten			
	5,694,602	December 2, 1997	Smith			
	*5,696,791	December 9, 1997	Yeung			
	5,706,482	January 6, 1998	Matsushima et al.			
	5,713,037	January 27, 1998	Wilkinson et al.			
	5,717,943	February 10, 1998	Barker et al.			
	5,732,209	March 24, 1998	Vigil et al.			
	5,734,921	March 31, 1998	Dapp et al.			
	5,737,516	April 7, 1998	Circello et al.			
	5,737,565	April 7, 1998	Mayfield			
	5,742,180	April 21, 1998	Detton et al.			
	5,745,734	April 28, 1998	Craft et al.			
	5,748,872	May 5, 1998	Norman			
	5,748,979	May 5, 1998	Trimberger			
	5,752,035	May 12, 1998	Trimberger			

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EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,754,459	May 19, 1998	Telikepalli			
	5,754,820	May 19, 1998	Yamagami			
	5,754,827	May 19, 1998	Barbier et al.			
	5,754,871	May 19, 1998	Wilkinson et al.			
	5,760,602	June 2, 1998	Tan			
	5,761,484	June 2, 1998	Agarwal et al.			
	5,773,994	June 30, 1998	Jones			
	5,778,439	July 7, 1998	Timberger et al.			
	5,781,756	July 14, 1998	Hung			
	5,784,636	July 21, 1998	Rupp			
	5,794,059	August 11, 1998	Barker et al.			
	5,794,062	August 11, 1998	Baxter			
	5,801,715	September 1, 1998	Norman			
	5,802,290	September 1, 1998	Casselman			
	*5,804,986	September 8, 1998	Jones			
	5,815,715	September 29, 1998	Kayhan			
	*5,815,726	September 29, 1998	Cliff			
	5,821,774	October 13, 1998	Veytsman et al.			
	5,828,229	October 27, 1998	Cliff et al.			
	5,828,858	October 27, 1998	Athanas et al.			
	5,831,448	November 3, 1998	Kean			
	5,838,165	November 17, 1998	Chatter			
	5,841,973	November 24, 1998	Cooke et al.			
	5,844,422	December 1, 1998	Trimberger et al.			
	5,844,888	December 1, 1998	Narjyka			
	5,848,238	December 8, 1998	Shimomura et al.			
	5,854,918	December 29, 1998	Baxter			
	5,857,097	January 5, 1999	Henzinger et al.			
	5,859,544	January 12, 1999	Norman			
	5,860,119	January 12, 1999	Dockser			
	5,862,403	January 19, 1999	Kanai et al.			
	5,865,239	February 2, 1999	Carr			
	5,867,691	February 2, 1999	Shiraishi			
	5,867,723	February 2, 1999	Peters et al.			
	5,870,620	February 9, 1999	Kadosumi et al.			
	5,884,075	March 16, 1999	Hester et al.			
	5,887,162	March 23, 1999	Williams et al.			
	5,887,165	March 23, 1999	Martel et al.			
	5,889,533	March 30, 1999	Lee			

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EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,889,982	March 30, 1999	Rodgers et al.			
	5,892,370	April 6, 1999	Eaton et al.			
	5,892,961	April 6, 1999	Trimberger			
	5,892,962	April 6, 1999	Cloutier			
	5,901,279	May 4, 1999	Davis III			
	5,915,123	June 22, 1999	Mirsky et al.			
	5,924,119	July 13, 1999	Sindhu et al.			
	5,926,638	July 20, 1999	Inoue, Masaharu			
	5,927,423	July 27, 1999	Wada et al.			
	5,933,023	August 3, 1999	Young			
	5,933,642	August 3, 1999	Baxter et al.			
	5,936,424	April 10, 1999	Young et al.			
	5,943,242	August 24, 1999	Vorbach et al.			
	5,956,518	September 21, 1999	DeHon et al.			
	5,960,193	September 28, 1999	Gutttag et al.			
	5,960,200	September 28, 1999	Eager et al.			
	5,966,143	October 12, 1999	Breternitz, Jr.			
	5,966,534	October 12, 1999	Cooke et al.			
	5,970,254	October 19, 1999	Cooke et al.			
	5,978,260	November 2, 1999	Trimberger et al.			
	5,978,583	November 2, 1999	Ekanadham et al.			
	5,996,083	November 30, 1999	Gupta et al.			
	5,999,990	December 7, 1999	Sharrit et al.			
	6,003,143	December 14, 1999	Kim et al.			
	6,011,407	January 4, 2000	New			
	6,014,509	January 11, 2000	Furtek et al.			
	6,020,758	February 1, 2000	Patel et al.			
	6,020,760	February 1, 2000	Sample et al.			
	6,021,490	February 1, 2000	Vorbach et al.			
	6,023,564	February 8, 2000	Trimberger			
	6,023,742	February 8, 2000	Ebeling et al.			
	6,026,481	February 15, 2000	New et al.			
	6,034,538	March 7, 2000	Abramovici			
	6,035,371	March 7, 2000	Magloire			
	6,038,650	March 14, 2000	Vorbach et al.			
	6,038,656	March 14, 2000	Cummings et al.			
	6,044,030	March 28, 2000	Zheng et al.			
	6,047,115	April 4, 2000	Mohan et al.			
	6,049,222	April 11, 2000	Lawman			

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EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	*6,049,866	April 11, 2000	Earl			
	6,052,773	April 18, 2000	DeHon et al.			
	6,054,873	April 25, 2000	Laramie			
	6,055,619	April 25, 2000	North et al.			
	6,058,469	May 2, 2000	Baxter			
	6,076,157	June 13, 2000	Borkenhagen et al.			
	6,077,315	June 20, 2000	Greenbaum et a.			
	6,081,903	June 27, 2000	Vorbach et al.			
	6,084,429	July 4, 2000	Trimberger			
	6,085,317	July 4, 2000	Smith			
	6,086,628	July 11, 2000	Dave et al.			
	6,088,795	July 11, 2000	Vorbach et al.			
	6,092,174	July 18, 2000	Roussakov			
	6,105,105	August 15, 2000	Trimberger et al.			
	6,105,106	August 15, 2000	Manning			
	6,108,760	August 22, 2000	Mirsky et al.			
	6,118,724	September 12, 2000	Higginbottom			
	6,119,181	September 12, 2000	Vorbach et al.			
	6,122,719	September 19, 2000	Mirsky et al.			
	6,125,408	September 26, 2000	McGee et al.			
	6,127,908	October 3, 2000	Bozler et al.			
	6,134,166	October 17, 2000	Lytle et al.			
	6,137,307	October 24, 2000	Iwanczuk et al.			
	*6,144,220	November 7, 2000	Young			
	6,150,837	November 21, 2000	Beal et al.			
	6,150,839	November 21, 2000	New et al.			
	6,154,048	November 28, 2000	Iwanczuk et al.			
	6,154,049	November 28, 2000	New			
	6,157,214	December 5, 2000	Marshall			
	6,170,051	January 2, 2001	Dowling, Eric M.			
	6,172,520	January 9, 2001	Lawman et al.			
	6,173,434	January 9, 2001	Wirthlin et al.			
	6,185,256	February 6, 2001	Saito et al.			
	6,185,731	February 6, 2001	Maeda et al.			
	6,188,240	February 13, 2001	Nakaya			
	6,188,650	February 13, 2001	Hamada et al.			
	6,198,304	March 6, 2001	Sasaki			
	6,201,406	March 13, 2001	Iwanczuk et al.			
	6,202,182	March 13, 2001	Abramovici et al.			

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EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	6,204,687	March 20, 2001	Schultz et al.			
	6,211,697	April 3, 2001	Lien et al.			
	6,212,650	April 3, 2001	Guccione, Steven A.			
	6,215,326	April 10, 2001	Jefferson et al.			
	6,216,223	April 10, 2001	Revilla et al.			
	6,219,833	April 17, 2001	Solomon et al.			
	6,230,307	May 8, 2001	Davis et al.			
	6,240,502	May 29, 2001	Panwar et al.			
	6,243,808	June 5, 2001	Wang			
	6,247,147	June 12, 2001	Beenstra			
	6,252,792	June 26, 2001	Marshall et al.			
	6,256,724	July 3, 2001	Hocevar et al.			
	6,260,179	July 10, 2001	Ohsawa et al.			
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	6,341,318	January 22, 2002	Dakhl			
	6,347,346	February 12, 2002	Taylor			
	6,349,346	February 19, 2002	Hanrahan et al.			
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	6,389,379	May 14, 2002	Lin et al.			
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	6,398,383	June 4, 2002	Huang, Yu-Hwei			
	6,400,601	June 4, 2002	Sudo et al.			
	6,404,224	June 11, 2002	Azegami et al.			
	6,405,299	June 11, 2002	Vorbach et al.			
	6,421,809	July 16, 2002	Wuytack et al.			
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	6,425,054	July 23, 2002	Nguyen			
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	6,430,309	August 6, 2002	Pressman et al.			
	6,434,642	August 13, 2002	Camilleri et al.			
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	6,434,695	August 13, 2002	Esfahani et al.			
	6,434,699	August 13, 2002	Jones et al.			
	6,435,054	October 10, 2000	Nguyen			
	6,437,441	August 20, 2002	Yamamoto			
	6,438,747	August 20, 2002	Schreiber et al.			
	6,457,116	September 24, 2002	Mirsky et al.			
	6,476,634	November 5, 2002	Bilski			
	6,477,643	November 5, 2002	Vorbach et al.			
	6,480,937	November 12, 2002	Vorbach et al.			
	6,480,954	November 12, 2002	Trimberger et al.			
	6,483,343	November 19, 2002	Faith et al.			
	6,487,709	November 26, 2002	Keller et al.			
	6,490,695	December 3, 2002	Zagorski et al.			
	6,496,971	December 17, 2002	Lesea et al.			
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	6,518,787	February 11, 2003	Allegrucci et al.			
	6,519,674	February 11, 2003	Lam et al.			
	6,523,107	February 18, 2003	Stansfield et al.			
	6,525,678	February 25, 2003	Veenstra et al.			
	6,526,520	February 25, 2003	Vorbach et al.			
	6,538,468	March 25, 2003	Moore			
	6,538,470	March 25, 2003	Langhammer et al.			
	6,539,415	March 25, 2003	Mercs			
	6,539,438	March 25, 2003	Ledzius et al.			
	6,539,477	March 25, 2003	Seawright			
	6,542,844	April 1, 2003	Hanna			
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	6,542,998	April 1, 2003	Vorbach			
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	6,631,487	October 7, 2003	Abramovici et al.			
	6,633,181	October 14, 2003	Rupp			
	6,657,457	December 2, 2003	Hanrahan et al.			
	6,658,564	December 2, 2003	Smith et al.			
	6,665,758	December 16, 2003	Frazier et al.			
	6,687,788	February 3, 2004	Vorbach et al.			
	6,697,979	February 24, 2004	Vorbach et al.			
	6,704,816	March 9, 2004	Burke, David			
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	6,717,436	April 6, 2004	Kress et al.			
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	6,754,805	June 22, 2004	Yujen Juan			
	6,757,847	June 29, 2004	Farkash et al.			
	6,757,892	June 29, 2004	Gokhale et al.			
	6,782,445	August 24, 2004	Olgiati et al.			
	6,785,826	August 31, 2004	Durham et al.			
	6,802,026	October 5, 2004	Patterson et al.			
	6,803,787	October 12, 2004	Wicker, Jr.			
	6,820,188	November 16, 2004	Stansfield et al.			
	6,829,697	December 7, 2004	Davis et al.			
	6,847,370	January 25, 2005	Baldwin et al.			
	6,868,476	March 22, 2005	Rosenbluth			
	6,871,341	March 22, 2005	Shyr			
	6,874,108	March 29, 2005	Abramovici et al.			
	6,886,092	April 26, 2005	Douglass et al.			
	6,901,502	May 31, 2005	Yano et al.			
	6,928,523	August 9, 2005	Yamada, Akira			
	6,961,924	November 1, 2005	Bates et al.			
	*6,975,138	December 13, 2005	Pani et al.			
	6,977,649	December 20, 2005	Baldwin et al.			
	7,000,161	February 14, 2006	Allen et al.			
	7,007,096	February 28, 2006	Lisitsa et al.			
	7,010,667	March 7, 2006	Vorbach et al.			
	7,028,107	April 11, 2006	Vorbach et al.			
	7,038,952	May 2, 2006	Zack et al.			
	7,043,416	May 9, 2006	Lin			
	7,210,129	April 24, 2007	May et al.			
	7,216,204	May 8, 2007	Rosenbluth			
	7,237,087	June 26, 2007	Vorbach et al.			
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	7,340,596	March 4, 2008	Crosland et al.			
	7,346,644	March 18, 2008	Langhammer et al.			
	7,350,178	March 25, 2008	Crosland et al.			
	*7,382,156	June 3, 2008	Pani et al.			
	7,595,659	September 29, 2009	Vorbach et al.			
	7,650,448	January 19, 2010	Vorbach et al.			
	2001/0001860	May 24, 2001	Bieu			
	2001/0010074	July 26, 2001	Nishihara et al.			
	2001/018733	October 18, 2001	Fujii et al.			
	2001/0032305	October 18, 2001	Barry			
	2001/0003834	June 14, 2001	Shimonishi			
	2002/0103839	August 1, 2002	Ozawa			
	2002/083308	June 27, 2002	Pereira et al.			
	2002/0038414	March 28, 2002	Taylor			
	2002/0045952	April 18, 2002	Blemei			
	2002/124238	September 5, 2002	Metzgen			
	2002/0138716	September 26, 2002	Paul et al.			
	2002/013861	August 30, 2001	Adiletta et al.			
	2002/0143505	October 3, 2002	Drusinsky			
	2002/0144229	October 3, 2002	Hanrahan			
	*2002/0156962	October 24, 2002	Chopra et al.			
	2002/0165886	November 7, 2002	Lam			
	2003/0001615	January 2, 2003	Sueyoshi et al.			
	2003/0014743	January 16, 2003	Cooke et al.			
	2003/0046607	March 6, 2003	Vorbach			
	2003/0056085	March 2, 2003	Vorbach			
	2003/0052711	March 20, 2003	Taylor			
	2003/0055861	March 20, 2003	Lai et al.			
	2003/0056091	March 20, 2003	Greenberg			
	2003/0056202	March 20, 2003	Vorbach			
	2003/0061542	March 27, 2003	Bates et al.			
	2003/062922	April 3, 2003	Douglass et al.			
	2003/0086300	May 8, 2003	Noyes et al.			
	2003/0093662	May 15, 2003	Vorbach et al.			
	2003/0097513	May 22, 2003	Vorbach et al.			
	2003/0123579	July 3, 2003	Safavi et al.			
	2003/0135686	July 17, 2003	Vorbach et al.			

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EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	2003/0192032	October 9, 2003	Andrade et al.			
	2004/0015899	January 22, 2004	May et al.			
	2004/0025005	February 5, 2004	Vorbach et al.			
	*2004/0039880	February 26, 2004	Pentkovski et al.			
	2004/0078548	April 22, 2004	Claydon et al.			
	2004/0168099	August 26, 2004	Vorbach et al.			
	2004/0199688	October 7, 2004	Vorbach et al.			
	2005/066213	March 24, 2005	Vorbach et al.			
	2005/0144210	June 30, 2005	Simkins et al.			
	2005/0144212	June 30, 2005	Simkins et al.			
	2005/0144215	June 30, 2005	Simkins et al.			
	2006/0130096	October 12, 2006	Thendean et al.			
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	2009/0085603	April 2, 2009	Paul et al.			

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						YES	NO
	0 208 457	January 14, 1987	EPO				
	0 221 360	May 13, 1987	EPO				
	0 398 552	November 22, 1990	EPO				
	0 428 327	May 22, 1991	EPO				
	0 463 721	January 2, 1992	EPO				
	0 477 809	April 1, 1992	EPO				
	0 485 690	May 20, 1992	EPO				
	0 497 029	August 5, 1992	EPO				
	0 539 595	May 5, 1993	EPO				
	0 628 917	December 14, 1994	EPO				
	0 678 985	October 25, 1995	EPO				
	0 686 915	December 13, 1995	EPO				
	0 696 001	December 5, 2001	EPO				
	0 707 269	April 17, 1996	EPO				
	0 726 532	August 14, 1996	EPO				
	0 735 685	October 2, 1996	EPO				
	0 746 106	December 4, 1996	EPO				
	0 748 051	December 11, 1996	EPO				
	0 926 594	June 30, 1999	EPO				
	1 061 439	December 20, 2000	EPO				

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EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	1 102 674	May 30, 2001	EPO				
	1 115 204	July 11, 2001	EPO			English	
	1 146 432	October 17, 2001	EPO				
	1 669 885	June 14, 2006	EPO			Abstract	
	2 752 466	February 20, 1998	France			English equivalent: USP 6,425,054 cited above	
	42 21 278	January 5, 1994	Germany				
	44 16 881	November 17, 1994	Germany			Abstract	
	38 55 673	November 20, 1996	Germany			Abstract Only	
	100 28 397	December 20, 2001	Germany				
	100 36 627	February 14, 2002	Germany				
	101 29 237	April 18, 2002	Germany				
	102 04 044	August 14, 2003	Germany				
	196 51 075	June 10, 1998	Germany			Abstract	
	196 54 593	July 2, 1998	Germany				
	196 54 595	July 2, 1998	Germany			Abstract	
	196 54 846	July 9, 1998	Germany				
	197 04 044	August 13, 1998	Germany				
	197 04 728	August 13, 1998	Germany			Abstract	
	197 04 742	September 24, 1998	Germany				
	198 07 872	August 26, 1999	Germany				
	198 22 776	March 25, 1999	Germany			Abstract	
	198 61 088	February 10, 2000	Germany				
	199 26 538	December 14, 2000	Germany			Abstract	
	2 304 438	March 19, 1997	United Kingdom			English	
	WO90/04835	May 3, 1990	PCT				
	WO90/11648	October 4, 1990	PCT				
	WO92/01987	February 6, 1992	PCT				
	WO93/11503	June 10, 1993	PCT				
	WO94/06077	March 17, 1994	PCT				
	WO94/08399	April 14, 1994	PCT				
	WO95/00161	January 5, 1995	PCT				
	WO95/26001	September 28, 1995	PCT				
	WO98/10517	March 12, 1998	PCT				
	WO98/26356	June 18, 1998	PCT				
	WO98/28697	July 2, 1998	PCT				
	WO98/29952	July 9, 1998	PCT				

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EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	WO98/31102	July 16, 1998	PCT				
	WO98/035294	August 13, 1998	PCT				
	WO98/35299	August 13, 1998	PCT				
	WO99/00731	January 7, 1999	PCT				
	WO99/00739	January 7, 1999	PCT				
	WO99/12111	March 11, 1999	PCT				
	WO99/32975	July 1, 1999	PCT				
	WO99/40522	August 12, 1999	PCT				
	WO99/44147	September 2, 1999	PCT				
	WO99/44120	September 2, 1999	PCT				
	WO00/17771	March 30, 2000	PCT				
	WO00/38087	June 29, 2000	PCT				
	WO00/045282	August 3, 2000	PCT				
	WO00/49496	August 24, 2000	PCT				
	WO00/77652	December 21, 2000	PCT				
	WO01/55917	August 2, 2001	PCT				
	WO02/13000	February 14, 2002	PCT				
	WO02/21010	March 14, 2002	PCT				
	WO02/29600	April 11, 2002	PCT				
	WO02/50665	June 27, 2002	PCT				
	WO02/071196	September 12, 2002	PCT				
	WO02/71248	September 12, 2002	PCT				
	WO02/071249	September 12, 2002	PCT				
	WO02/103532	December 27, 2002	PCT				
	WO03/017095	February 27, 2003	PCT				
	WO03/023616	March 20, 2003	PCT				
	WO03/025781	March 27, 2003	PCT				
	WO03/032975	April 24, 2003	PCT				
	WO03/036507	May 1, 2003	PCT				
	WO 03/091875	November 6, 2003	PCT				
	WO 04/053718	June 24, 2004	PCT				
	WO04/114128	December 29, 2004	PCT				
	WO05/045692	May 19, 2005	PCT				
	1-229378	September 13, 1989	Japan			Abstract	
	8-44581	February 16, 1996	Japan			Abstract	
	7-154242	June 16, 1995	Japan			Abstract	
	58-58672	April 7, 1983	Japan			Abstract	
	2-226423	September 10, 1990	Japan			Abstract	
	5-265705	October 15, 1993	Japan			Abstract	

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						YES	NO
	5-276007	October 22, 1993	Japan			Abstract	
	6-266605	September 22, 1994	Japan			Abstract	
	7-086921	March 31, 1995	Japan			Abstract	
	8-101761	April 16, 1996	Japan			Abstract	
	8-102492	April 16, 1996	Japan			Abstract	
	8-148989	June 7, 1995	Japan			Abstract	
	8-221164	August 30, 1996	Japan			Abstract	
	8-250685	September 27, 1996	Japan			Abstract	
	9-294069	November 11, 1997	Japan			Abstract	
	2-130023	May 18, 1990	Japan			Abstract	
	11-184718	July 9, 1999	Japan			Abstract	
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	2000-076066	March 14, 2000	Japan			Abstract	
	2000-181566	June 30, 2000	Japan			Computer Translation	
	2000-311156	November 7, 2000	Japan			Abstract	
	9-27745	January 28, 1997	Japan			Abstract	
	05-509184	December 16, 2003	Japan			English Equivalent = USP 5,193,202 cited above	
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	2001-167066	June 22, 2001	Japan			Abstract	
	2001-500682	January 16, 2001	Japan			Abstract	
	2000-201066	July 18, 2000	Japan			Abstract	
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	Filing Date Herewith	Group Art Unit Unassigned

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BIB DATA SHEET
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SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
12/836,364	07/14/2010	326	2819	2885/139		
APPLICANTS Martin Vorbach, Munich, GERMANY;						
** CONTINUING DATA ***** This application is a CON of 12/541,299 08/14/2009 PAT 7,782,087 which is a CON of 12/082,073 04/07/2008 PAT 7,602,214 which is a CON of 10/526,595 01/09/2006 PAT 7,394,284 which is a 371 of PCT/EP03/38599 09/08/2003						
** FOREIGN APPLICATIONS ***** GERMANY 102 41 812.8 09/06/2002 GERMANY 103 15 295.4 04/04/2003 GERMANY 103 21 834.3 05/15/2003 EUROPEAN PATENT OFFICE (EPO) 03 019 428.6 08/28/2003						
** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** * SMALL ENTITY ** 07/26/2010						
Foreign Priority claimed	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No	<input type="checkbox"/> Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
35 USC 119(a-d) conditions met	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No	Initials	GERMANY	6	30	1
Verified and Acknowledged	/DON P LE/ Examiner's Signature					
ADDRESS KENYON & KENYON LLP ONE BROADWAY NEW YORK, NY 10004 UNITED STATES						
TITLE RECONFIGURABLE SEQUENCER STRUCTURE						
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	Applicant(s) VORBACH	
	Filing Date July 14, 2010	Group Art Unit 2827

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	90/011,087	July 8, 2010 (filing date)	Vorbach et al.			

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Index of Claims 	Application/Control No. 12836364	Applicant(s)/Patent Under Reexamination VORBACH, MARTIN
	Examiner Don P Le	Art Unit 2819

✓	Rejected
=	Allowed


-	Cancelled
÷	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

Claims renumbered in the same order as presented by applicant
 CPA
 T.D.
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CLAIM		DATE							
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	Filing Date Herewith	Group Art Unit Unassigned

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	Yeung, L., et al., "A 2.4GOPS Data-Driven Reconfigurable Multiprocessor IC for DSP," Dept. of EECS, U. California Berkeley, 1995 IEEE International Solid State Circuits Conference, pp. 108-110.
	ZILOG Preliminary Product Specification, "Z86C95 CMOS Z8 Digital Signal Processor," 1992, pp. 1-82.
	ZILOG Preliminary Product Specification, "Z89120 Z89920 (ROMless) 16-Bit Mixed Signal Processor," 1992, pp. 1-82.
	Defendants' Invalidity Contentions in <i>PACT XPP Technologies, AG v. XILINX, Inc., et al.</i> , (E.D. Texas Dec. 28, 2007) (No. 2:07cv563), including Exhibits A through K in separate PDF files.

EXAMINER	/Don Le/	DATE CONSIDERED	11/06/2010
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s) : Martin VORBACH
Serial No. : 12/836,364
Filing Date : July 14, 2010
For : MULTI-CORE PROCESSING SYSTEM (as amended)
Group Art Unit : 2819
Examiner : Don P. Le
Confirmation No. : 2050

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I hereby certify this correspondence is being electronically transmitted to the United States Patent and Trademark Office via the Office electronic filing system on December 17, 2010.

Signature: Eunice K. Chang/
Eunice K. Chang

AMENDMENT UNDER 37 C.F.R. § 1.312

SIR:

A Notice of Allowance for the above-identified application was mailed on November 12, 2010. Please amend the application under 37 C.F.R. § 1.312 as follows:

Amendments to the Specification begin on page 2 of this paper.

Remarks begin on page 3 of this paper.

Amendments to the Specification:

Please replace the title of the specification on page 1 with the following title:

--MULTI-CORE PROCESSING SYSTEM--.

REMARKS

The title of the specification has been amended. No new subject matter has been introduced. Approval and entry are respectfully requested.

While no fee is believed to be due, the Commissioner is authorized to charge any fees or credit any overpayment to the deposit account of Kenyon & Kenyon LLP, Deposit Account No. 11-0600. The Examiner is invited to contact the undersigned to discuss any matter concerning this application.

Respectfully submitted,
KENYON & KENYON LLP

Date: December 17, 2010

By: /Aaron Grunberger/
Aaron Grunberger
Reg. No. 59,210

One Broadway
New York, New York 10004
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(212) 425-5288 (facsimile)

CUSTOMER NO.: 26646

Electronic Acknowledgement Receipt

EFS ID:	9064125
Application Number:	12836364
International Application Number:	
Confirmation Number:	2050
Title of Invention:	RECONFIGURABLE SEQUENCER STRUCTURE
First Named Inventor/Applicant Name:	Martin Vorbach
Customer Number:	26646
Filer:	Aaron Grunberger/Eunice Chang
Filer Authorized By:	Aaron Grunberger
Attorney Docket Number:	2885/139
Receipt Date:	17-DEC-2010
Filing Date:	14-JUL-2010
Time Stamp:	15:44:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment after Notice of Allowance (Rule 312)	2885-139-Rule312amd.pdf	149630 c4e91bab2fc82e5402b54d086e4edb7922c88cf3	no	3

Warnings:

Information:

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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/139	Serial No. Unassigned
	Applicant(s) VORBACH	
	Filing Date Herewith	Group Art Unit Unassigned

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	RE34363	August 31, 1993	Freeman			
	RE34,444	November 16, 1993	Kaplinsky			
	RE37,195	May 29, 2001	Kean			
	60/109,417	November 18, 1998	Jefferson et al.			
	2,067,477	January 12, 1937	J.B. Cooper			
	3,242,998	March 29, 1966	C.H. Gubbins			
	3,681,578	August 1, 1972	Stevens			
	3,757,608	September 11, 1973	Willner			
	3,855,577	December 17, 1974	Vandierendonck			
	4,233,667	November 11, 1980	Devine et al.			
	4,414,347	November 8, 1983	Knapp et al.			
	4,489,857	February 6, 1986	Agrawal et al.			
	4,498,134	February 5, 1985	Hansen et al.			
	4,498,172	February 5, 1985	Bhavsar			
	4,566,102	January 21, 1986	Hefner			
	4,571,736	February 18, 1986	Agrawal et al.			
	4,590,583	May 20, 1986	Miller			
	4,591,979	May 27, 1986	Iwashita			
	*4,623,997	November 18, 1986	Tulpule			
	4,663,706	May 5, 1987	Allen et al.			
	4,667,190	May 19, 1987	Fant et al.			
	4,682,284	July 21, 1987	Schrofer			
	4,706,216	November 10, 1987	Carter			
	4,720,778	January 19, 1988	Hall et al.			
	4,720,780	January 19, 1988	Dolecek			
	4,739,474	April 19, 1988	Holsztynski			
	4,761,755	August 2, 1988	Ardini et al.			
	4,811,214	March 7, 1989	Nosenchuck et al.			
	4,852,043	July 25, 1989	Guest			
	4,852,048	July 25, 1989	Morton			
	4,860,201	August 22, 1989	Stolfo et al.			
	4,870,302	September 26, 1989	Freeman			
	4,882,687	November 21, 1989	Gordon			
	4,884,231	November 28, 1989	Mor et al.			
	4,891,810	January 2, 1990	de Corlicu et al.			
	4,901,268	February 13, 1990	Judd			
	4,910,665	March 20, 1990	Matheyses et al.			
	4,918,440	April 17, 1990	Furtek et al.			

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.L./

Page 1

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/139	Serial No. Unassigned
	Applicant(s) VORBACH	
	Filing Date Herewith	Group Art Unit Unassigned

EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,754,459	May 19, 1998	Telikopalli			
	5,754,820	May 19, 1998	Yamagami			
	5,754,827	May 19, 1998	Barbier et al.			
	5,754,871	May 19, 1998	Wilkinson et al.			
	5,760,602	June 2, 1998	Tan			
	5,761,484	June 2, 1998	Agarwal et al.			
	5,773,994	June 30, 1998	Jones			
	5,778,430	July 7, 1998	Timberger et al.			
	5,781,756	July 14, 1998	Hung			
	5,784,636	July 21, 1998	Rupp			
	5,794,059	August 11, 1998	Barker et al.			
	5,794,062	August 11, 1998	Baxter			
	5,801,715	September 1, 1998	Norman			
	5,802,290	September 1, 1998	Casselman			
	*5,804,986	September 8, 1998	Jones			
	5,815,715	September 29, 1998	Kayhan			
	*5,815,726	September 29, 1998	Cliff			
	5,821,774	October 13, 1998	Veytsman et al.			
	5,828,229	October 27, 1998	Cliff et al.			
	5,828,858	October 27, 1998	Athanas et al.			
	5,831,448	November 3, 1998	Kean			
	5,838,165	November 17, 1998	Chatter			
	5,841,973	November 24, 1998	Cooke et al.		Kessler	
	5,844,422	December 1, 1998	Timberger et al.			
	5,844,888	December 1, 1998	Nerjyka		Markkula, Jr. et al.	
	5,848,238	December 8, 1998	Shimomura et al.			
	5,854,918	December 29, 1998	Baxter			
	5,857,097	January 5, 1999	Henzinger et al.			
	5,859,544	January 12, 1999	Norman			
	5,860,119	January 12, 1999	Dockser			
	5,862,403	January 19, 1999	Kanai et al.			
	5,865,239	February 2, 1999	Carr			
	5,867,691	February 2, 1999	Shiraishi			
	5,867,723	February 2, 1999	Peters et al.			
	5,870,620	February 9, 1999	Kadosumi et al.			
	5,884,075	March 16, 1999	Hester et al.			
	5,887,162	March 23, 1999	Williams et al.			
	5,887,165	March 23, 1999	Martel et al.			
	5,889,533	March 30, 1999	Lee			

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.L./

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/139	Serial No. Unassigned
	Applicant(s) VORBACH	
	Filing Date Herewith	Group Art Unit Unassigned

EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,889,982	March 30, 1999	Rodgers et al.			
	5,892,370	April 6, 1999	Eaton et al.			
	5,892,961	April 6, 1999	Trimberger			
	5,892,962	April 6, 1999	Cloutier			
	5,901,279	May 4, 1999	Davis III			
	5,915,123	June 22, 1999	Mirsky et al.			
	5,924,119	July 13, 1999	Sindhu et al.			
	5,926,638	July 20, 1999	Inoue, Masaharu			
	5,927,423	July 27, 1999	Wada et al.			
	5,933,023	August 3, 1999	Young			
	5,933,642	August 3, 1999	Baxter et al.			
	5,936,424	<i>Aug.</i> April 10 , 1999	Young et al.			
	5,943,242	August 24, 1999	Vorbach et al.			
	5,956,518	September 21, 1999	DeHon et al.			
	5,960,193	September 28, 1999	Guttag et al.			
	5,960,200	September 28, 1999	Eager et al.			
	5,966,143	October 12, 1999	Breternitz, Jr.			
	5,966,534	October 12, 1999	Cooke et al.			
	5,970,254	October 19, 1999	Cooke et al.			
	5,978,260	November 2, 1999	Trimberger et al.			
	5,978,583	November 2, 1999	Ekanadham et al.			
	5,996,083	November 30, 1999	Gupta et al.			
	5,999,990	December 7, 1999	Sharrif et al.			
	6,003,143	December 14, 1999	Kim et al.			
	6,011,407	January 4, 2000	New			
	6,014,509	January 11, 2000	Furtick et al.			
	6,020,758	February 1, 2000	Patel et al.			
	6,020,760	February 1, 2000	Sample et al.			
	6,021,490	February 1, 2000	Vorbach et al.			
	6,023,564	February 8, 2000	Trimberger			
	6,023,742	February 8, 2000	Ebeling et al.			
	6,026,481	February 15, 2000	New et al.			
	6,034,538	March 7, 2000	Abramovici			
	6,035,371	March 7, 2000	Magloire			
	6,038,650	March 14, 2000	Vorbach et al.			
	6,038,656	March 14, 2000	Cummings et al.			
	6,044,030	March 28, 2000	Zheng et al.			
	6,047,115	April 4, 2000	Mohan et al.			
	6,049,222	April 11, 2000	Lawman			

*RV
1/6/01*

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.L./

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/139	Serial No. Unassigned
	Applicant(s) VORBACH	
	Filing Date Herewith	Group Art Unit Unassigned

EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	6,378,068	April 23, 2002	Foster et al.			
	6,381,624	April 30, 2002	Colon-Bonet et al.			
	6,389,379	May 14, 2002	Lin et al.			
	6,389,579	May 14, 2002	Phillips et al.			
	6,392,912	May 21, 2002	Hanrahan et al.			
	6,398,383	June 4, 2002	Huang, Yu-Hwei			
	6,400,601	June 4, 2002	Sudo et al.			
	6,404,224	June 11, 2002	Azegami et al.			
	6,405,299	June 11, 2002	Vorbach et al.			
	6,421,809	July 16, 2002	Wuytack et al.			
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	6,425,054	July 23, 2002	Nguyen			
	6,425,068	July 23, 2002	Vorbach			
	*6,426,649	July 30, 2002	Fu et al.			
	*6,427,156	July 30, 2002	Chapman et al.			
	6,430,309	August 6, 2002	Pressman et al.			
	6,434,642	August 13, 2002	Camilleri et al.			
	*6,434,672	August 13, 2002	Galther			
	6,434,695	August 13, 2002	Esfahani et al.			
	6,434,699	August 13, 2002	Jones et al.			
RL 1/6/11	6425054	October 10, 2002	Nguyen			July 2002
	6,437,441	August 20, 2002	Yamamoto			
	6,438,747	August 20, 2002	Schreiber et al.			
	6,457,116	September 24, 2002	Mirsky et al.			
	6,476,634	November 5, 2002	Bilski			
	6,477,643	November 5, 2002	Vorbach et al.			
	6,480,937	November 12, 2002	Vorbach et al.			
	6,480,954	November 12, 2002	Trimberger et al.			
	6,483,343	November 19, 2002	Faith et al.			
	6,487,709	November 26, 2002	Keller et al.			
	6,490,695	December 3, 2002	Zagorski et al.			
	6,496,971	December 17, 2002	Lesea et al.			
	6513077	January 7, 2003	Vorbach et al.			
	6,504,298	January 14, 2003	Gibson et al.			
	6,507,898	January 14, 2003	Schreiber et al.			
	6,507,947	January 14, 2003	Schreiber et al.			
	*6,512,804	January 28, 2003	Johnson et al.			

Page 10
ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.L./

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/139	Serial No. Unassigned
	Applicant(s) VORBACH	
	Filing Date Herewith	Group Art Unit Unassigned

EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	7,254,649	August 7, 2007	Subramanian et al.			
	7,340,596	March 4, 2008	Crosland et al.			
	7,346,644	March 18, 2008	Langhammer et al.			
	7,350,178	March 25, 2008	Crosland et al.			
	*7,382,156	June 3, 2008	Pani et al.			
	7,595,659	September 29, 2009	Vorbach et al.			
	7,650,448	January 19, 2010	Vorbach et al.			
	2001/0001860	May 24, 2001	Bieu			
	2001/0010074	July 26, 2001	Nishihara et al.			
	2001/018733	Aug. October 18, 2001	Fujii et al.			
	2001/0032305	October 18, 2001	Bary			
	2001/0003834	June 14, 2001	Shimonishi			
	2002/0103839	August 1, 2002	Ozawa			
	2002/083308	June 27, 2002	Pereira et al.			
	2002/0038414	March 28, 2002	Taylor			
	2002/0045952	April 18, 2002	Blemel			
	2002/124238	September 5, 2002	Metzgen			
	2002/0138716	September 26, 2002	Master Paul et al.			
	2002/013861	August 30, 2001	Adiletta et al.			Jan 2002
	2002/0143505	October 3, 2002	Drusinsky			
	2002/0144229	October 3, 2002	Hanrahan			
	*2002/0156962	October 24, 2002	Chopra et al.			
	2002/0165886	November 7, 2002	Lam			
	2003/0001615	January 2, 2003	Sueyoshi et al.			
	2003/0014743	January 16, 2003	Cooke et al.			
	2003/0046607	March 6, 2003	Vorbach et al.			
	2003/0056085	March 2, 2003	Vorbach			
	2003/0052711	March 20, 2003	Taylor			
	2003/0055861	March 20, 2003	Lai et al.			
	2003/0056091	March 20, 2003	Greenberg			
	2003/0056202	March 20, 2003	Vorbach et al.			
	2003/0061542	March 27, 2003	Bates et al.			
	2003/062922	April 3, 2003	Douglass et al.			
	2003/0086300	May 8, 2003	Noyes et al.			
	2003/0093662	May 15, 2003	Vorbach et al.			
	2003/0097513	May 22, 2003	Vorbach et al.			
	2003/0123579	July 3, 2003	Safavi et al.			
	2003/0135686	July 17, 2003	Vorbach et al.			

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Page 13
ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.L./

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/139	Serial No. Unassigned
	Applicant(s) VORBACH	
	Filing Date Herewith	Group Art Unit Unassigned

EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	2003/0192032	October 9, 2003	Andrade et al.			
	2004/0015899	January 22, 2004	May et al.			
	2004/0025005	February 5, 2004	Vorbach et al.			
	*2004/0039880	February 26, 2004	Pentkovski et al.			
	2004/0078548	April 22, 2004	Claydon et al.			
	2004/0168099	August 26, 2004	Vorbach et al.			
	2004/0199688	October 7, 2004	Vorbach et al.			
	2005/066213	March 24, 2005	Vorbach et al.			
	2005/0144210	June 30, 2005	Simkins et al.			
	2005/0144212	June 30, 2005	Simkins et al.			
	2005/0144215	June 30, 2005	Simkins et al.			
RL 1/6/11	2006/0230094	October 12, 2006	Thendean et al.			
	2006/0230094	October 12, 2006	Simkins et al.			
	2009/0085603	April 2, 2009	Paul et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	0 208 457	January 14, 1987	EPO				
	0 221 360	May 13, 1987	EPO				
	0 398 552	November 22, 1990	EPO				
	0 428 327	May 22, 1991	EPO				
	0 463 721	January 2, 1992	EPO				
	0 477 809	April 1, 1992	EPO				
	0 485 690	May 20, 1992	EPO				
	0 497 029	August 5, 1992	EPO				
	0 539 595	May 5, 1993	EPO				
	0 628 917	December 14, 1994	EPO				
	0 678 985	October 25, 1995	EPO				
	0 686 915	December 13, 1995	EPO				
	0 696 001	December 5, 2001	EPO				
	0 707 269	April 17, 1996	EPO				
	0 726 532	August 14, 1996	EPO				
	0 735 685	October 2, 1996	EPO				
	0 746 106	December 4, 1996	EPO				
	0 748 051	December 11, 1996	EPO				
	0 926 594	June 30, 1999	EPO				
	1 061 439	December 20, 2000	EPO				

Page 14
ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.L./



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

12/836,364	07/14/2010	Martin Vorbach	2885/139	2050
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26646 7590 01/07/2011
KENYON & KENYON LLP
 ONE BROADWAY
 NEW YORK, NY 10004

EXAMINER

LE, DON P

ART UNIT	PAPER NUMBER
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2819

MAIL DATE	DELIVERY MODE
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01/07/2011

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Response to Rule 312 Communication	Application No.	Applicant(s)
	12/836,364	VORBACH, MARTIN
	Examiner	Art Unit
	Don P. Le	2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. The amendment filed on 17 December 2010 under 37 CFR 1.312 has been considered, and has been:
- a) entered.
 - b) entered as directed to matters of form not affecting the scope of the invention.
 - c) disapproved because the amendment was filed after the payment of the issue fee.
Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.
 - d) disapproved. See explanation below.
 - e) entered in part. See explanation below.

/Don P Le/
Primary Examiner, Art Unit 2819
1/5/2011

Receipt date: 12/17/2010

12836364 - GAU: 2819
[2885/139]

OK to enter
/Don Le/
1/4/2010

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s) : Martin VORBACH
Serial No. : 12/836,364
Filing Date : July 14, 2010
For : MULTI-CORE PROCESSING SYSTEM (as amended)
Group Art Unit : 2819
Examiner : Don P. Le
Confirmation No. : 2050

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I hereby certify this correspondence is being electronically transmitted to the United States Patent and Trademark Office via the Office electronic filing system on December 17, 2010.

Signature: Eunice K. Chang/
Eunice K. Chang

AMENDMENT UNDER 37 C.F.R. § 1.312

SIR:

A Notice of Allowance for the above-identified application was mailed on November 12, 2010. Please amend the application under 37 C.F.R. §1.312 as follows:

Amendments to the Specification begin on page 2 of this paper.

Remarks begin on page 3 of this paper.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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CONFIRMATION NO. 2050

Bib Data Sheet

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.	
12/836,364	07/14/2010 RULE	326	2819	2885/139	
APPLICANTS					
Martin Vorbach, Munich, GERMANY;					
** CONTINUING DATA *****					
This application is a CON of 12/541,299 08/14/2009 PAT 7,782,087 which is a CON of 12/082,073 04/07/2008 PAT 7,602,214 which is a CON of 10/526,595 01/09/2006 PAT 7,394,284 which is a 371 of PCT/EP03/38599 09/08/2003					
** FOREIGN APPLICATIONS *****					
GERMANY 102 41 812.8 09/06/2002 GERMANY 103 15 285.4 04/04/2003 GERMANY 103 21 834.3 05/15/2003 EUROPEAN PATENT OFFICE (EPO) 03 019 428.6 08/28/2003					
IF REQUIRED, FOREIGN FILING LICENSE GRANTED** SMALL ENTITY **					
** 07/26/2010					
Foreign Priority claimed 35 USC 119 (a-d) conditions met	<input type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance	STATE OR COUNTRY GERMANY	SHEETS DRAWING 6	TOTAL CLAIMS 30	INDEPENDENT CLAIMS 1
Verified and Acknowledged	Examiner's Signature _____ Initials _____				
ADDRESS					
26646					
TITLE					
MULTI-CORE PROCESSING SYSTEM					
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/836,364	07/14/2010	Martin Vorbach	2885/139

CONFIRMATION NO. 2050

PUBLICATION NOTICE

26646
KENYON & KENYON LLP
ONE BROADWAY
NEW YORK, NY 10004



Title: MULTI-CORE PROCESSING SYSTEM

Publication No. US-2011-0006805-A1

Publication Date: 01/13/2011

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

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**U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE**

INFORMATION DISCLOSURE STATEMENT		Docket Number: 2885/139	Confirmation Number: 2050
Application Number 12/836,364	Filing Date July 14, 2010	Examiner Don P. Le	Art Unit 2819
Invention Title MULTI-CORE PROCESSING SYSTEM		Inventors Martin VORBACH	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Date: February 9, 2011
Signature: /Eunice K. Chang/
Eunice K. Chang

Sir:

Pursuant to 37 CFR § 1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom. The filing of this Information Disclosure Statement and the enclosed PTO Form No. 1449, shall not be construed as an admission that the information cited is prior art, or is considered to be material to patentability as defined in 37 C.F.R. § 1.56(b). The paragraphs marked below are applicable. It is believed that no fees other than those indicated below are due, but authorization is hereby given to charge any additional fees due, or to credit any overpayment, to Kenyon & Kenyon LLP, deposit account 11-0600.

1. This Information Disclosure Statement is being filed (a) within three months of the filing date of a national application other than a continued prosecution application under 37 C.F.R. §1.53(d), (b) within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, (c) before the mailing date of a first Office Action on the merits in the present application, OR (d) before the mailing of a first office action after filing of a request for continued examination. No certification or fee is required.

2. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a final action, Notice of Allowance, or any action that otherwise closes prosecution.

a. I hereby certify that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(1).

b. I hereby certify that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(2).

c. The required fee of \$180.00 under 37 CFR §1.17(p) is being paid by credit card to ensure consideration of the disclosed information. Any additional fees may be charged to Deposit Account No. 11-0600 of Kenyon & Kenyon LLP

3. Since this application was filed after June 30, 2003, copies of U.S. references are not included.

Respectfully submitted,

Date: February 9, 2011

/Aaron Grunberger/
Aaron Grunberger
Reg. No. 59,210

KENYON & KENYON LLP
One Broadway
New York, NY 20004
(212) 425-7200 telephone
(212) 425-5288 facsimile
CUSTOMER NUMBER 26646

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/139	Serial No. 12/836,364
	Applicant(s) VORBACH	
	Filing Date July 14, 2010	Group Art Unit 2819

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	3,753,008	August 14, 1973	Guarnaschelli			
	4,594,682	June 10, 1986	Drimak			
	5,996,048	November 30, 1999	Cherabuddi et al.			
	6,260,114	July 10, 2001	Schug			
	6,496,902	December 17, 2002	Faanes et al.			
	2002/0073282	June 13, 2002	Chauvel et al.			
	2003/0070059	April 10, 2003	Dally et al.			
	2005/0091468	April 28, 2005	Morita et al.			
	2008/0313383	December 18, 2008	Morita et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

OTHER DOCUMENTS

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	ARM Limited, "ARM Architecture Reference Manual," December 6, 2000, pp. A10-6-A10-7.
	Li, Zhiyuan, et al., "Configuration prefetching techniques for partial reconfigurable coprocessor with relocation and defragmentation," International Symposium on Field Programmable Gate Arrays, February 1, 2002, pp. 187-195.
	Melvin, Stephen et al., "Hardware Support for Large Atomic Units in Dynamically Scheduled Machines," Computer Science Division, University of California, Berkeley, IEEE (1988), pp. 60-63.
	Roterberg, Eric, et al., "Trace Cache: a Low Latency Approach to High Bandwidth Instruction Fetching," Proceedings of the 29 th Annual International Symposium on Microarchitecture, Paris, France, IEEE (1996), 12 pages.

EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

Electronic Patent Application Fee Transmittal

Application Number:	12836364
Filing Date:	14-Jul-2010
Title of Invention:	MULTI-CORE PROCESSING SYSTEM
First Named Inventor/Applicant Name:	Martin Vorbach
Filer:	Aaron Grunberger/Eunice Chang
Attorney Docket Number:	2885/139

Filed as Small Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Claims in excess of 20	2202	30	26	780

Miscellaneous-Filing:

Petition:

Patent-Appeals-and-Interference:

Post-Allowance-and-Post-Issuance:

Extension-of-Time:

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Request for continued examination	2801	1	405	405
Total in USD (\$)				1185

Electronic Acknowledgement Receipt

EFS ID:	9410079
Application Number:	12836364
International Application Number:	
Confirmation Number:	2050
Title of Invention:	MULTI-CORE PROCESSING SYSTEM
First Named Inventor/Applicant Name:	Martin Vorbach
Customer Number:	26646
Filer:	Aaron Grunberger/Eunice Chang
Filer Authorized By:	Aaron Grunberger
Attorney Docket Number:	2885/139
Receipt Date:	09-FEB-2011
Filing Date:	14-JUL-2010
Time Stamp:	16:06:00
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$1185
RAM confirmation Number	2836
Deposit Account	110600
Authorized User	GRUNBERGER,AARON

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

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INTEL - 1004

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2885-139-RCEandIDS.pdf	1490599 ee892776bfcfc7734ff06db6356d37072043c67	yes	14
Multipart Description/PDF files in .zip description					
	Document Description		Start		End
	Request for Continued Examination (RCE)		1		1
	Transmittal Letter		2		2
	Amendment Submitted/Entered with Filing of CPA/RCE		3		11
	Information Disclosure Statement (IDS) Filed (SB/08)		12		14
Warnings:					
Information:					
2	NPL Documents	ARM.pdf	550641 b3de2357c7331caa5f47ac6a1fe4c580de4b5499	no	4
Warnings:					
Information:					
3	NPL Documents	ZhiyuanLi.pdf	1636282 7948427458f7b49d61fccb7237a4d2f97569b2b4	no	9
Warnings:					
Information:					
4	NPL Documents	Melvin-et-al.pdf	526078 3007da0601bfcd367a0237725260cb16c2f69d31	no	4
Warnings:					
Information:					
5	NPL Documents	Rotenberg-et-al.pdf	2080890 515faa4e5a005c7d90aefa220612cccc718e6564	no	12
Warnings:					
Information:					

6	Fee Worksheet (PTO-875)	fee-info.pdf	31962	no	2
			75fc6799c6d625a9ec263b273377fbd925f676e		

Warnings:

Information:

Total Files Size (in bytes):	6316452
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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**Request
for
Continued Examination (RCE)
Transmittal**

Address to:
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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	12/836,364
Filing Date	July 14, 2010
First Named Inventor	Martin VORBACH
Art Unit	2819
Examiner Name	Don P. Le
Attorney Docket Number	2885/139

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. **Submission required under 37 CFR 1.114** Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

- a. Previously submitted, if a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.
- i. Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ii. Other _____
- b. Enclosed
- i. Amendment/Reply
- ii. Affidavit(s)/ Declaration(s)
- iii. Information Disclosure Statement (IDS)
- iv. Other Amendment Transmittal

2. **Miscellaneous**

- a. Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)
- b. Other _____

3. **Fees**

- The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.
The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to Deposit Account No. N/A
- a. RCE fee required under 37 CFR 1.17(e)
- i. RCE fee required under 37 CFR 1.17(e)
- ii. Extension of time fee (37 CFR 1.136 and 1.17)
- iii. Other Claim fees as listed on Amendment Transmittal
- b. Check in the amount of \$ _____ enclosed
- c. Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature	/Aaron Grunberger/	Date	February 9, 2011
Name (Print/Type)	Aaron Grunberger	Registration No.	59,210

CERTIFICATE OF MAILING OR TRANSMISSION

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Signature	VIA EFS WEB	Date	February 9, 2011
Name (Print/Type)	Eunice K. Chang		

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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**U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE**

AMENDMENT TRANSMITTAL LETTER		Docket Number: 2885/139	
Application Number 12/836,364	Filing Date July 14, 2010	Examiner Don P. Le	Art Unit 2819
Invention Title MULTI-CORE PROCESSING SYSTEM		Inventors Martin VORBACH	

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Alexandria, VA 22313-1450

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Date: February 9, 2011
Signature: /Eunice K. Chang/
Eunice K. Chang

Sir:

- Transmitted herewith for filing is an Amendment for the above-identified patent application.
- The filing fee has been calculated after entry of the accompanying Amendment as shown below:

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT NUMBER EXTRA	RATE (\$)	FEE (\$)
TOTAL CLAIMS	60	minus	30	30	52.00	1560.00
INDEPENDENT CLAIMS	2	minus	3		220.00	.00
MULTIPLE DEPENDENT CLAIM ADDED					390.00	0.00
					TOTAL	1560.00
					SMALL ENTITY TOTAL	780.00

- The additional claim fees of \$780.00 is being paid by credit card.

Respectfully submitted,

Date: February 9, 2011

By: /Aaron Grunberger/
Aaron Grunberger
Reg. No. 59,210
One Broadway
New York, NY 10004
(212) 425-7200
CUSTOMER NUMBER 26646

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s) : Martin VORBACH
Serial No. : 12/836,364
Filed : July 14, 2010
For : MULTI-CORE PROCESSING SYSTEM
Examiner : Don P. Le
Group Art Unit : 2819
Confirmation No. : 2050
Customer No. : 26646

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Signature: /Eunice K. Chang/
Eunice K. Chang

RCE AMENDMENT

SIR:

Pursuant to the filing of a Request for Continued Examination (RCE), please amend the above-captioned application without prejudice (of which claims 18 to 47 have been allowed) as follows:

Amendments to the Claims are found in the listing of claims, which begins on page 2 of this paper.

Remarks begin on page 9 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-17. (Canceled).

18. (Previously Presented) A multi-processor chip, comprising:
a plurality of data processing cells, each adapted for sequentially executing at least one of algebraic and logic functions and having:
at least one arithmetic logic unit;
at least one data register file;
a program pointer; and
at least one instruction decoder;
a plurality of memory cells;
at least one interface unit;
at least one Memory Management Unit (MMU); and
a bus system for interconnecting the plurality of data processing cells, the plurality of memory cells, and the at least one interface unit;
wherein the bus system is adapted for programmably interconnecting at runtime at least one of data processing cells and memory cells with at least one of memory cells and one or more of the at least one interface unit.

19. (Previously Presented) The multi-processor chip according to claim 18, wherein at least some of the memory cells are cache memories.

20. (Previously Presented) The multi-processor chip according to claim 19, wherein at least some of the cache memories are preloadable.

21. (Previously Presented) The multi-processor chip according to claim 18, wherein at least some of the memory cells are adapted to operate as a data stack.

22. (Previously Presented) The multi-processor chip according to claim 18, wherein at least some of the memory cells are adapted to operate as a data heap.

23. (Previously Presented) The multi-processor chip according to claim 18, wherein at least some of the memory cells are adapted to operate as a code memory.

24. (Previously Presented) The multi-processor chip according to claim 18, wherein at least some of the memory cells are adapted to operate as at least two of a data stack, a data heap, and a code memory.

25. (Previously Presented) The multi-processor chip according to claim 18, wherein at least some of the memory cells are adapted to operate as at least two of a data stack, a data heap, a code memory, and a cache.

26. (Previously Presented) The multi-processor chip according to claim 18, wherein at least some of the memory cells are adapted to operate as a data stack, a data heap, and a code memory.

27. (Previously Presented) The multi-processor chip according to claim 18, wherein the data processing cells are adapted to connect simultaneously to a plurality of at least one of cells and units of at least one of the memory cells, the data processing cells, and the at least one interface units.

28. (Previously Presented) The multi-processor chip according to claim 18, wherein cells of the data processing cells are adapted to connect simultaneously to other cells of the data processing cells and to a plurality of at least one of cells and units of at least one of the memory cells, the data processing cells, and the at least one interface units.

29. (Previously Presented) The multi-processor chip according to claim 18, wherein the bus system is adapted to interconnect a data processing cell simultaneously to a plurality of at least one of cells and units of at least one of the memory cells, others of the data processing cells, and the at least one interface units.

30. (Previously Presented) The multi-processor chip according to claim 18, wherein the bus system is adapted to interconnect a plurality of data processing cells simultaneously to a plurality of at least one of cells and units of at least one of the memory cells and the interface units.

31. (Previously Presented) The multi-processor chip according to claim 18, wherein the data processing cells are adapted to access a plurality of the memory cells.

32. (Previously Presented) The multi-processor chip according to claim 18, wherein the data processing cells are adapted to address a plurality of the memory cells.

33. (Previously Presented) The multi-processor chip according to claim 18, wherein the data processing cells are adapted to transfer commands to the memory cells.

34. (Previously Presented) The multi-processor chip according to claim 18, wherein the data processing cells are adapted to transfer commands to the at least one interface unit.

35. (Previously Presented) The multi-processor chip according to claim 18, wherein the data processing cells are adapted to transfer commands to memory cells and interface units.

36. (Previously Presented) The multi-processor chip according to claim 18, wherein at least one of the memory cells is adapted to store data in a non-volatile manner.

37. (Previously Presented) The multi-processor chip according to claim 18, wherein the multi-processor chip is adapted for video-processing.

38. (Previously Presented) The multi-processor chip according to claim 18, wherein at least some of at least one of the data processing cells, the memory cells, and the at least one interface unit operate at different clock rates for lowering power consumption.

39. (Previously Presented) The multi-processor chip according to claim 18, wherein the at least one MMU is implemented in the at least one interface unit.

40. (Previously Presented) The multi-processor chip according to claim 18, wherein at least one of the at least one interface unit has an implemented one of the at least one MMU.

41. (Previously Presented) The multi-processor chip according to claim 18, wherein the processing cells are connected to those of the memory cells that are in close proximity to the processing cells.

42. (Previously Presented) The multi-processor chip according to claim 18, wherein the processing cells are connected to the memory cells such that there is minimal latency times for data access.

43. (Previously Presented) The multi-processor chip according to claim 18, wherein data transmission between processing cells and memory cells is optimized for low latency times.

44. (Previously Presented) The multi-processor chip according to claim 18, wherein the processing cells access the memory cells in a manner that minimizes latency times for data access.

45. (Previously Presented) The multi-processor chip according to claim 18, wherein the processing cells are arranged with the memory cells in a manner that minimizes latency times for data access.

46. (Previously Presented) The multi-processor chip according to claim 18, wherein the processing cells connect to memory cells such that latency times for data access are minimized.

47. (Previously Presented) The multi-processor chip according to claim 18, wherein data is transmitted in a pipelined manner between the processing cells and the memory cells.

48. (New) A multi-processor chip, comprising:
a plurality of data processing cells, each adapted for sequentially executing at least one of algebraic and logic functions and having:
 at least one arithmetic logic unit;
 at least one data register file;
 a program pointer; and
 at least one instruction decoder;
a plurality of memory cells;
at least one interface unit;
at least one Memory Management Unit (MMU); and
a bus system for interconnecting the plurality of data processing cells, the plurality of memory cells, and the at least one interface unit;
wherein the bus system is adapted for dynamically interconnecting at runtime at least one of data processing cells and memory cells with at least one of memory cells and one or more of the at least one interface unit.

49. (New) The multi-processor chip according to claim 48, wherein at least some of the memory cells are cache memories.

50. (New) The multi-processor chip according to claim 49, wherein at least some of the cache memories are preloadable.

51. (New) The multi-processor chip according to claim 48, wherein at least some of the memory cells are adapted to operate as a data stack.

52. (New) The multi-processor chip according to claim 48, wherein at least some of the memory cells are adapted to operate as a data heap.

53. (New) The multi-processor chip according to claim 48, wherein at least some of the memory cells are adapted to operate as a code memory.

54. (New) The multi-processor chip according to claim 48, wherein at least some of the memory cells are adapted to operate as at least two of a data stack, a data heap, and a code memory.

55. (New) The multi-processor chip according to claim 48, wherein at least some of the memory cells are adapted to operate as at least two of a data stack, a data heap, a code memory, and a cache.

56. (New) The multi-processor chip according to claim 48, wherein at least some of the memory cells are adapted to operate as a data stack, a data heap, and a code memory.

57. (New) The multi-processor chip according to claim 48, wherein the data processing cells are adapted to connect simultaneously to a plurality of at least one of cells and units of at least one of the memory cells, the data processing cells, and the at least one interface units.

58. (New) The multi-processor chip according to claim 48, wherein cells of the data processing cells are adapted to connect simultaneously to other cells of the data processing cells and to a plurality of at least one of cells and units of at least one of the memory cells, the data processing cells, and the at least one interface units.

59. (New) The multi-processor chip according to claim 48, wherein the bus system is adapted to interconnect a data processing cell simultaneously to a plurality of at least one of cells and units of at least one of the memory cells, others of the data processing cells, and the at least one interface units.

60. (New) The multi-processor chip according to claim 48, wherein the bus system is adapted to interconnect a plurality of data processing cells simultaneously to a plurality of at least one of cells and units of at least one of the memory cells and the interface units.

61. (New) The multi-processor chip according to claim 48, wherein the data processing cells are adapted to access a plurality of the memory cells.

62. (New) The multi-processor chip according to claim 48, wherein the data processing cells are adapted to address a plurality of the memory cells.

63. (New) The multi-processor chip according to claim 48, wherein the data processing cells are adapted to transfer commands to the memory cells.

64. (New) The multi-processor chip according to claim 48, wherein the data processing cells are adapted to transfer commands to the at least one interface unit.

65. (New) The multi-processor chip according to claim 48, wherein the data processing cells are adapted to transfer commands to memory cells and interface units.

66. (New) The multi-processor chip according to claim 48, wherein at least one of the memory cells is adapted to store data in a non-volatile manner.

67. (New) The multi-processor chip according to claim 48, wherein the multi-processor chip is adapted for video-processing.

68. (New) The multi-processor chip according to claim 48, wherein at least some of at least one of the data processing cells, the memory cells, and the at least one interface unit operate at different clock rates for lowering power consumption.

69. (New) The multi-processor chip according to claim 48, wherein the at least one MMU is implemented in the at least one interface unit.

70. (New) The multi-processor chip according to claim 48, wherein at least one of the at least one interface unit has an implemented one of the at least one MMU.

71. (New) The multi-processor chip according to claim 48, wherein the processing cells are connected to those of the memory cells that are in close proximity to the processing cells.

72. (New) The multi-processor chip according to claim 48, wherein the processing cells are connected to the memory cells such that there is minimal latency times for data access.

73. (New) The multi-processor chip according to claim 48, wherein data transmission between processing cells and memory cells is optimized for low latency times.

74. (New) The multi-processor chip according to claim 48, wherein the processing cells access the memory cells in a manner that minimizes latency times for data access.

75. (New) The multi-processor chip according to claim 48, wherein the processing cells are arranged with the memory cells in a manner that minimizes latency times for data access.

76. (New) The multi-processor chip according to claim 48, wherein the processing cells connect to memory cells such that latency times for data access are minimized.

77. (New) The multi-processor chip according to claim 48, wherein data is transmitted in a pipelined manner between the processing cells and the memory cells.

REMARKS

With the addition of new claims 48 to 77, claims 18 to 77 are currently pending in the present application, since claims 1 to 17 were previously canceled. No new matter has been entered. Approval and entry are respectfully requested.

Claims 18 to 47 were previously allowed. It is respectfully submitted that all of the presently pending claims are allowable. Prompt consideration and allowance of the present application are therefore earnestly solicited.

Dated: February 9, 2011

Respectfully submitted,

By: /Aaron Grunberger/

Aaron Grunberger
Reg. No. 59,210

KENYON & KENYON LLP
One Broadway
New York, New York 10004
(212) 425-7200

CUSTOMER NO 26646

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/836,364	Filing Date 07/14/2010	<input type="checkbox"/> To be Mailed
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APPLICATION AS FILED – PART I			OTHER THAN SMALL ENTITY				
	(Column 1)	(Column 2)	SMALL ENTITY <input checked="" type="checkbox"/>	OR			
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)
<input type="checkbox"/> BASIC FEE <small>(37 CFR 1.16(a), (b), or (c))</small>	N/A	N/A	N/A		OR	N/A	
<input type="checkbox"/> SEARCH FEE <small>(37 CFR 1.16(k), (j), or (m))</small>	N/A	N/A	N/A		OR	N/A	
<input type="checkbox"/> EXAMINATION FEE <small>(37 CFR 1.16(e), (p), or (q))</small>	N/A	N/A	N/A		OR	N/A	
TOTAL CLAIMS <small>(37 CFR 1.16(i))</small>	minus 20 =	*	X \$ =		OR	X \$ =	
INDEPENDENT CLAIMS <small>(37 CFR 1.16(h))</small>	minus 3 =	*	X \$ =		OR	X \$ =	
<input type="checkbox"/> APPLICATION SIZE FEE <small>(37 CFR 1.16(s))</small>	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s)				OR		
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENT <small>(37 CFR 1.16(j))</small>					OR		
			TOTAL		OR	TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II					OTHER THAN SMALL ENTITY				
	(Column 1)	(Column 2)	(Column 3)						
AMENDMENT	02/09/2011	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)
	Total <small>(37 CFR 1.16(i))</small>	* 60	Minus ** 60	= 0	X \$28 =	0	OR	X \$ =	
	Independent <small>(37 CFR 1.16(h))</small>	* 2	Minus *** 3	= 0	X \$110 =	0	OR	X \$ =	
	<input type="checkbox"/> Application Size Fee <small>(37 CFR 1.16(s))</small>						OR		
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <small>(37 CFR 1.16(j))</small>						OR		
					TOTAL ADD'L FEE	0	OR	TOTAL ADD'L FEE	

	(Column 1)	(Column 2)	(Column 3)						
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)
	Total <small>(37 CFR 1.16(i))</small>	*	Minus **	=	X \$ =		OR	X \$ =	
	Independent <small>(37 CFR 1.16(h))</small>	*	Minus ***	=	X \$ =		OR	X \$ =	
	<input type="checkbox"/> Application Size Fee <small>(37 CFR 1.16(s))</small>						OR		
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <small>(37 CFR 1.16(j))</small>						OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/MELINDA OLIVER/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



NOTICE OF ALLOWANCE AND FEE(S) DUE

26646 7590 02/28/2011
KENYON & KENYON LLP
ONE BROADWAY
NEW YORK, NY 10004

EXAMINER	
LE, DONP	
ART UNIT	PAPER NUMBER

2819

DATE MAILED: 02/28/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/836,364	07/14/2010	Martin Vorbach	2885/139	2050

TITLE OF INVENTION: MULTI-CORE PROCESSING SYSTEM

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$755	\$300	\$0	\$1055	05/31/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

26646 7590 02/28/2011
KENYON & KENYON LLP
 ONE BROADWAY
 NEW YORK, NY 10004

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/836,364	07/14/2010	Martin Vorbach	2885/139	2050

TITLE OF INVENTION: MULTI-CORE PROCESSING SYSTEM

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$755	\$300	\$0	\$1055	05/31/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
LE, DON P	2819	326-038000

<p>1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).</p> <p><input type="checkbox"/> Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.</p> <p><input type="checkbox"/> "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.</p>	<p>2. For printing on the patent front page, list</p> <p>(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____</p> <p>(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____</p> <p>3 _____</p>
---	---

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE _____ (B) RESIDENCE: (CITY and STATE OR COUNTRY) _____

Please check the appropriate assignee category or categories (will not be printed on the patent) : Individual Corporation or other private group entity Government

<p>4a. The following fee(s) are submitted:</p> <p><input type="checkbox"/> Issue Fee</p> <p><input type="checkbox"/> Publication Fee (No small entity discount permitted)</p> <p><input type="checkbox"/> Advance Order - # of Copies _____</p>	<p>4b. Payment of Fee(s); (Please first reapply any previously paid issue fee shown above)</p> <p><input type="checkbox"/> A check is enclosed.</p> <p><input type="checkbox"/> Payment by credit card. Form PTO-2038 is attached.</p> <p><input type="checkbox"/> The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).</p>
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5. Change in Entity Status (from status indicated above)

a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Alexandria, Virginia 22313-1450
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Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO.
Values: 12/836,364, 07/14/2010, Martin Vorbach, 2885/139, 2050

26646 7590 02/28/2011
KENYON & KENYON LLP
ONE BROADWAY
NEW YORK, NY 10004

EXAMINER

LE, DONP

ART UNIT PAPER NUMBER

2819

DATE MAILED: 02/28/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability

Application No.

12/836,364

Examiner

Don P. Le

Applicant(s)

VORBACH, MARTIN

Art Unit

2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

- 1. This communication is responsive to RCE filed 2/9/2011.
- 2. The allowed claim(s) is/are 18-77.
- 3. Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some* c) None of the:
 - 1. Certified copies of the priority documents have been received.
 - 2. Certified copies of the priority documents have been received in Application No. _____.
 - 3. Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

- 4. A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 - 5. CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) hereto or 2) to Paper No./Mail Date _____.
 - (b) including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**
- 6. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- 1. Notice of References Cited (PTO-892)
- 2. Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3. Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date 2/9/2011
- 4. Examiner's Comment Regarding Requirement for Deposit of Biological Material
- 5. Notice of Informal Patent Application
- 6. Interview Summary (PTO-413),
Paper No./Mail Date _____.
- 7. Examiner's Amendment/Comment
- 8. Examiner's Statement of Reasons for Allowance
- 9. Other _____.

/Don P Le/
Primary Examiner, Art Unit 2819
2/12/2011

EAST Search History


EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L11	11	((("3753008") or ("4594682") or ("5996048") or ("6260114") or ("6496902")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/02/12 18:29
L12	4	((("20020073282") or ("20030070059") or ("20050091468") or ("20080313383")).PN.	US-PGPUB	OR	OFF	2011/02/12 18:31
L13	41781	runtime and interface	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/12 18:31
L14	37275	13 and memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/12 18:31
L15	14944	14 and register	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/12 18:32
L16	6146	15 and pointer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/12 18:32
L17	3591	16 and cache	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/12 18:32

L18	676	17 and decoder	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/12 18:33
L19	210	18 and mmu	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/12 18:33

2/ 12/ 2011 6:37:52 PM

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Index of Claims 	Application/Control No. 12836364	Applicant(s)/Patent Under Reexamination VORBACH, MARTIN
	Examiner Don P Le	Art Unit 2819

✓	Rejected
=	Allowed

-	Cancelled
÷	Restricted

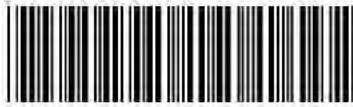
N	Non-Elected
I	Interference

A	Appeal
O	Objected

Claims renumbered in the same order as presented by applicant
 CPA
 T.D.
 R.1.47

CLAIM		DATE							
Final	Original	11/07/2010	02/12/2011						
	1	-	-						
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17	34	=	=						
18	35	=	=						
19	36	=	=						

Index of Claims




Application/Control No. 12836364	Applicant(s)/Patent Under Reexamination VORBACH, MARTIN
Examiner Don P Le	Art Unit 2819

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claims renumbered in the same order as presented by applicant CPA T.D. R.1.47


CLAIM		DATE							
Final	Original	11/07/2010	02/12/2011						
20	37	=	=						
21	38	=	=						
22	39	=	=						
23	40	=	=						
24	41	=	=						
25	42	=	=						
26	43	=	=						
27	44	=	=						
28	45	=	=						
29	46	=	=						
30	47	=	=						
31	48		=						
32	49		=						
33	50		=						
34	51		=						
35	52		=						
36	53		=						
37	54		=						
38	55		=						
39	56		=						
40	57		=						
41	58		=						
42	59		=						
43	60		=						
44	61		=						
45	62		=						
46	63		=						
47	64		=						
48	65		=						
49	66		=						
50	67		=						
51	68		=						
52	69		=						
53	70		=						
54	71		=						
55	72		=						

Index of Claims 	Application/Control No. 12836364	Applicant(s)/Patent Under Reexamination VORBACH, MARTIN
	Examiner Don P Le	Art Unit 2819

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claims renumbered in the same order as presented by applicant
 CPA
 T.D.
 R.1.47

CLAIM		DATE							
Final	Original	11/07/2010	02/12/2011						
56	73		=						
57	74		=						
58	75		=						
59	76		=						
60	77		=						

Search Notes 	Application/Control No. 12836364	Applicant(s)/Patent Under Reexamination VORBACH, MARTIN
	Examiner Don P Le	Art Unit 2819

SEARCHED			
Class	Subclass	Date	Examiner
326	37-41, 46	11/05/2010	dl
326	updated above	2/10/2011	dl

SEARCH NOTES		
Search Notes	Date	Examiner
east + interference	11/7/2010	dl
east updated + interference	2/12/2011	dl

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
	see search notes	11/7/2010	dl
	see search notes	2/12/2011	dl

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INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/139	Serial No. 12/836,364
	Applicant(s) VORBACH	
	Filing Date July 14, 2010	Group Art Unit 2819

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	3,753,008	August 14, 1973	Guarnaschelli			
	4,594,682	June 10, 1986	Drinak			
	5,996,048	November 30, 1999	Cherabuddi et al.			
	6,260,114	July 10, 2001	Schug			
	6,496,902	December 17, 2002	Faanes et al.			
	2002/0073282	June 13, 2002	Chauvel et al.			
	2003/0070059	April 10, 2003	Dally et al.			
	2005/0091468	April 28, 2005	Morita et al.			
	2008/0313383	December 18, 2008	Morita et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

OTHER DOCUMENTS

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	ARM Limited, "ARM Architecture Reference Manual," December 6, 2000, pp. A10-6-A10-7.
	Li, Zhiyuan, et al., "Configuration prefetching techniques for partial reconfigurable coprocessor with relocation and defragmentation," International Symposium on Field Programmable Gate Arrays, February 1, 2002, pp. 187-195.
	Melvin, Stephen et al., "Hardware Support for Large Atomic Units in Dynamically Scheduled Machines," Computer Science Division, University of California, Berkeley, IEEE (1988), pp. 60-63.
	Roterberg, Eric., et al., "Trace Cache: a Low Latency Approach to High Bandwidth Instruction Fetching," Proceedings of the 29 th Annual International Symposium on Microarchitecture, Paris, France, IEEE (1996), 12 pages.

EXAMINER	/Don Le/	DATE CONSIDERED	02/12/2011
----------	----------	-----------------	------------

EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
 or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26646 7590 02/28/2011
KENYON & KENYON LLP
ONE BROADWAY
NEW YORK, NY 10004

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/836,364	07/14/2010	Martin Vorbach	2885/139	2050

TITLE OF INVENTION: MULTI-CORE PROCESSING SYSTEM

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$755	\$300	\$0	\$1055	05/31/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
LE, DON P	2819	326-038000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
 Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
 "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a **Customer Number is required.**

2. For printing on the patent front page, list
 (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 Kenyon & Kenyon LLP
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
 PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.
 (A) NAME OF ASSIGNEE _____ (B) RESIDENCE: (CITY and STATE OR COUNTRY) _____

Please check the appropriate assignee category or categories (will not be printed on the patent): Individual Corporation or other private group entity Government

4a. The following fee(s) are submitted:
 Issue Fee
 Publication Fee (No small entity discount permitted)
 Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)
 A check is enclosed.
 Payment by credit card. Form PTO-2038 is attached.
 The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)
 a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Aaron Grunberger/ Date March 9, 2011
 Typed or printed name Aaron Grunberger Registration No. 59,210

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal

Application Number:	12836364
Filing Date:	14-Jul-2010
Title of Invention:	MULTI-CORE PROCESSING SYSTEM
First Named Inventor/Applicant Name:	Martin Vorbach
Filer:	Aaron Grunberger/Eunice Chang
Attorney Docket Number:	2885/139

Filed as Small Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	2501	1	755	755
Publ. Fee- early, voluntary, or normal	1504	1	300	300

INTEL - 1004

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1055

Electronic Acknowledgement Receipt

EFS ID:	9622713
Application Number:	12836364
International Application Number:	
Confirmation Number:	2050
Title of Invention:	MULTI-CORE PROCESSING SYSTEM
First Named Inventor/Applicant Name:	Martin Vorbach
Customer Number:	26646
Filer:	Aaron Grunberger/Eunice Chang
Filer Authorized By:	Aaron Grunberger
Attorney Docket Number:	2885/139
Receipt Date:	09-MAR-2011
Filing Date:	14-JUL-2010
Time Stamp:	16:13:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$1055
RAM confirmation Number	2689
Deposit Account	110600
Authorized User	GRUNBERGER,AARON

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

INTEL - 1004

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	2885-139-IFfiled.pdf	179923 24bbf395e578b1f8415deb8baedd3804c1cd4c23	no	1

Warnings:

Information:

2	Fee Worksheet (PTO-875)	fee-info.pdf	31789 6c60aefa7593fbd49a42b32d32e7c030f8b2aafc	no	2
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Warnings:

Information:

Total Files Size (in bytes): 211712

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/836,364	04/19/2011	7928763	2885/139	2050

26646 7590 03/30/2011
KENYON & KENYON LLP
ONE BROADWAY
NEW YORK, NY 10004

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Martin Vorbach, Munich, GERMANY;

**U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE**

REQUEST FOR CERTIFICATE OF CORRECTION PURSUANT TO 37 C.F.R. § 1.322, 1.323		Docket Number: 2885/139	Conf. No.: 2050
Application Number 12/836,364	Filing Date July 14, 2010	Examiner Don P. LE	Art Unit 2819
Patent Number 7,928,763	Issue Date April 19, 2011		
Invention Title MULTI-CORE PROCESSING SYSTEM		Inventor(s) Martin VORBACH	

Address to:
Commissioner For Patents
P. O. Box 1450
Alexandria, VA 22313-1450

I hereby certify that this correspondence is being electronically transmitted via ESF-Web on
Date: September 24, 2012
Signature: /Eunice Kim/
Eunice Kim

Patentee requests that the enclosed Certificate of Correction be issued for the above Patent under authority of 35 U.S.C. §§ 254, 255. The exact column and line number where the errors occur in the patent are listed on the enclosed certificate.

The payment of the 37 C.F.R. § 1.20(a) certificate of correction fee of \$100.00 is being paid by credit card. The Commissioner is also authorized to charge any additional fees or credit any overpayment in connection with this paper to Deposit Account No. 11-0600.

Dated: September 24, 2012

By: /Aaron Grunberger/
Aaron Grunberger, Reg. No. 59,210

KENYON & KENYON LLP
One Broadway
New York, New York 10004
(212) 425-7200 (telephone)
(212) 425-5288 (facsimile)

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

Page 1 of 1

PATENT NO. : 7,928,763
 APPLICATION NO.: 12/836,364
 ISSUE DATE : April 19, 2011
 INVENTOR(S) : Martin VORBACH

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the face of the patent:

Related U.S. Application Data
(63)

change

"Continuation of application No. 12/541,299, filed on Aug. 14, 2009, now Pat. No. 7,782,087, which is a continuation of application No. 12/082,073, filed on Apr. 7, 2008, now Pat. No. 7,602,214, which is a continuation of application No. 10/526,595, filed as application No. PCT/EP03/38599 on Sep. 8, 2003, now Pat. No. 7,394,284"

to --Continuation of application No. 12/541,299, filed on Aug. 14, 2009, now Pat. No. 7,782,087, which is a continuation of application No. 12/082,073, filed on Apr. 7, 2008, now Pat. No. 7,602,214, which is a continuation of application No. 10/526,595, filed as application No. PCT/EP03/09957 on Sep. 8, 2003, now Pat. No. 7,394,284--

Column 1, line 14:

change "PCT/EP03/38599" to --PCT/EP03/09957--

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Kenyon & Kenyon LLP
 One Broadway
 New York, NY 10004

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Patent Application Fee Transmittal

Application Number:	12836364
Filing Date:	14-Jul-2010
Title of Invention:	MULTI-CORE PROCESSING SYSTEM
First Named Inventor/Applicant Name:	Martin Vorbach
Filer:	Aaron Grunberger/Eunice Kim
Attorney Docket Number:	2885/139

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Certificate of correction	1811	1	100	100

Extension-of-Time:

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				100

Electronic Acknowledgement Receipt

EFS ID:	13821550
Application Number:	12836364
International Application Number:	
Confirmation Number:	2050
Title of Invention:	MULTI-CORE PROCESSING SYSTEM
First Named Inventor/Applicant Name:	Martin Vorbach
Customer Number:	26646
Filer:	Aaron Grunberger/Eunice Kim
Filer Authorized By:	Aaron Grunberger
Attorney Docket Number:	2885/139
Receipt Date:	24-SEP-2012
Filing Date:	14-JUL-2010
Time Stamp:	16:01:16
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$100
RAM confirmation Number	3088
Deposit Account	110600
Authorized User	GRUNBERGER, AARON

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

INTEL - 1004

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Certificate of Correction	2885-139-RequestforCOC.pdf	210627 97e0e4fdd44486b4a55aa9e37d404946ed3a279b	no	2

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30132 a76cb13d186efa21807cb274388c8d92d1e49ff4	no	2
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Warnings:

Information:

Total Files Size (in bytes):

240759

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

SPE RESPONSE FOR CERTIFICATE OF CORRECTION

Paper No.: _____

DATE : 10/4/2012

TO SPE OF : ART UNIT 2819

SUBJECT : Request for Certificate of Correction for Appl. No.: 12/836,364 Patent No.: 7,928,763

CofC mailroom date: 9/24/2012

Please respond to this request for a certificate of correction within 7 days.

FOR IFW FILES:

Please review the requested changes/corrections as shown in the **COCIN** document(s) in the IFW application image. No new matter should be introduced nor should the scope or meaning of the claims be changed.

Please complete the response (see below) and forward the completed response to scanning using document code **COCX**.

FOR PAPER FILES:

Please review the requested changes/corrections as shown in the attached certificate of correction. Please complete this form (see below) and forward it with the file to:

**Certificates of Correction Branch (CofC)
Randolph Square – 9D10-A
Palm Location 7580**

In particular note: Continuing data

Ernest G. White 571 272-3385
**Certificates of Correction Branch
703-756-1814**

Thank You For Your Assistance

The request for issuing the above-identified correction(s) is hereby:

Note your decision on the appropriate box.

- Approved** All changes apply.
- Approved in Part** Specify below which changes **do not** apply.
- Denied** State the reasons for denial below.

Comments: _____

SPE

INTel Unit 004

SPE RESPONSE FOR CERTIFICATE OF CORRECTION

Paper No.:20121005

DATE : October 05, 2012

TO SPE OF : ART UNIT 2819

SUBJECT : Request for Certificate of Correction on Patent No.: 7,928,763

A response is requested with respect to the accompanying request for a certificate of correction.

Please complete this form and return with file, within **7** days to:

Certificates of Correction Branch - ST (South Tower) 9A22

Palm location **7590** - Tel. No. (703) 305-8309

With respect to the change(s) requested, correcting Office and/or Applicant's errors, should the patent read as shown in the certificate of correction? No new matter should be introduced, nor should the scope or meaning of the claims be changed.

Thank You For Your Assistance

Certificates of Correction Branch

The request for issuing the above-identified correction(s) is hereby:

Note your decision on the appropriated box.

Approved

All changes apply.

Approved in Part

Specify below which changes **do not** apply.

Denied

State the reasons for denial below.

Comments:

/SHAWKI ISMAIL/
Supervisory Patent Examiner.Art Unit 2819

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,928,763 B2
APPLICATION NO. : 12/836364
DATED : April 19, 2011
INVENTOR(S) : Martin Vorbach

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title Page, Item (63):

Related U.S. Application Data

change

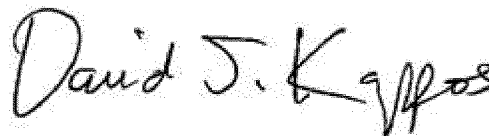
“Continuation of application No. 12/541,299, filed on Aug. 14, 2009, now Pat. No. 7,782,087, which is a continuation of application No. 12/082,073, filed on Apr. 7, 2008, now Pat. No. 7,602,214, which is a continuation of application No. 10/526,595, filed as application No. PCT/EP03/38599 on Sep. 8, 2003, now Pat. No. 7,394,284”

to --Continuation of application No. 12/541,299, filed on Aug. 14, 2009, now Pat. No. 7,782,087, which is a continuation of application No. 12/082,073, filed on Apr. 7, 2008, now Pat. No. 7,602,214, which is a continuation of application No. 10/526,595, filed as application No. PCT/EP03/09957 on Sep. 8, 2003, now Pat. No. 7,394,284--

Column 1, line 14:

change “PCT/EP03/38599” to --PCT/EP03/09957--

Signed and Sealed this
Sixth Day of November, 2012



David J. Kappos
Director of the United States Patent and Trademark Office

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:



Practitioners associated with Customer Number:

73481

OR



Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number

Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:



The address associated with Customer Number:

OR

Firm or Individual Name			
Address			
City	State	Zip	
Country			
Telephone	Email		

Assignee Name and Address: PACT XPP TECHNOLOGIES AG
Walter-Gropius-Str. 15
80807 Munich Germany

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of the practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	02/10/2014
Name	Martin Vorbach	Telephone	
Title	CTO		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)Applicant/Patent Owner: Martin VorbachApplication No./Patent No.: 7928763Filed/Issue Date: 04/19/2011Titled: MULTI-CORE PROCESSING SYSTEM

PACT XPP TECHNOLOGIES AG, a corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose one of options 1, 2, 3 or 4 below):1. The assignee of the entire right, title, and interest.2. An assignee of less than the entire right, title, and interest (check applicable box): The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest. There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.3. The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.4. The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose one of options A or B below):A. An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.B. A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:1. From: VORBACH, MARTIN To: PACT XPP TECHNOLOGIES AGThe document was recorded in the United States Patent and Trademark Office at
Reel 017171, Frame 0319, or for which a copy thereof is attached.2. From: PACT XPP TECHNOLOGIES AG To: RICHTER, THOMAS.; KRASS, MARENThe document was recorded in the United States Patent and Trademark Office at
Reel 023882, Frame 0403, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). This information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: RICHTER, THOMAS.; KRASS, MAREN To: PACT XPP TECHNOLOGIES AG

The document was recorded in the United States Patent and Trademark Office at
Reel 03225, Frame 0089, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

8. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

Additional documents in the chain of title are listed on a supplemental sheet(s).

As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.



Signature

Martin Vorbach

Printed or Typed Name

08/14/2014

Date

CTO for PACT XPP TECHNOLOGIES AG

Title or Registration Number

Electronic Acknowledgement Receipt

EFS ID:	19867922
Application Number:	12836364
International Application Number:	
Confirmation Number:	2050
Title of Invention:	MULTI-CORE PROCESSING SYSTEM
First Named Inventor/Applicant Name:	Martin Vorbach
Customer Number:	26646
Filer:	Edward Peter Heller/Emi Rhodes
Filer Authorized By:	Edward Peter Heller
Attorney Docket Number:	2885/139
Receipt Date:	14-AUG-2014
Filing Date:	14-JUL-2010
Time Stamp:	15:06:56
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	PACT_POA_140210.pdf	128954 <small>d1b7e26a7b4fb5fe0f9e1d59794fe20983524999</small>	no	2

Warnings:

The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing

Information:

2	Assignee showing of ownership per 37 CFR 3.73.	PACT-034-DE-PCT-US-3C1_CFR373c_Signed.pdf	358357 004c94b392e16394f69b0292d5b8686b6affec7a	no	2
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Warnings:

Information:

Total Files Size (in bytes):	487311
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/836,364	07/14/2010	Martin Vorbach	2885/139

CONFIRMATION NO. 2050

POA ACCEPTANCE LETTER



73481
Alliacense Limited LLC
4880 Stevens Creek Boulevard
Suite 103
San Jose, CA 95129

Date Mailed: 09/04/2014

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 08/14/2014.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/mbeyenc/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/836,364	07/14/2010	Martin Vorbach	2885/139

CONFIRMATION NO. 2050

POWER OF ATTORNEY NOTICE

26646
KENYON & KENYON LLP
ONE BROADWAY
NEW YORK, NY 10004



Date Mailed: 09/04/2014

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 08/14/2014.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/mbeyene/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Large Entity Declaration

Schedule A - Patents assigned to *Assignee*

Patent number	Issue Date	Application number	Filing Date
8686549	01- Apr 14	12/571173	30- Sep 09
7840842	23- Nov 10	11/890094	03- Aug 07
7650448	19- Jan 10	12/008543	10- Jan 08
7782087	24- Aug 10	12/541299	14- Aug 09
7928763	19- Apr 11	12/836364	14- Jul 10
7210129	24- Apr 07	09/967847	28- Sep 01
7266725	09- Apr 07	09/967497	28- Sep 01
7003660	21- Feb 06	10/297959	19- Jun 03
7010667	07- Mrz 06	10/116986	05- Apr 02
6968452	22- Nov 05	10/373595	24- Feb 03
7657877	02- Feb 10	10/480003	18- Jun 04
6990555	24- Jan 06	10/764159	24- Jan 04
7996827	09- Aug 11	10/486771	20- Sep 04
7243175	10- Jul 07	10/792168	02- Mrz 04
7657861	02- Feb 10	10/523763	22- Nov 05