DECLARATION OF GERARD P. GRENIER

I, Gerard P. Grenier, am over twenty-one (21) years of age. I have never been convicted of a felony, and I am fully competent to make this declaration. I declare the following to be true to the best of my knowledge, information and belief:

1. I am Senior Director of Content Management of The Institute of Electrical and Electronics Engineers, Incorporated ("IEEE").

2. IEEE is a neutral third party in this dispute.

3. Neither I nor IEEE itself is being compensated for this declaration.

4. Among my responsibilities as Senior Director of Content Management, I act as a custodian of certain records for IEEE.

5. I make this declaration based on my personal knowledge and information contained in the business records of IEEE.

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8. The article below has been attached as Exhibit A to this declaration:

A.	T. Miyamori; U. Olukotun, A quantitative analysis of reconfigurable coprocessors for multimedia applications, published in Proceedings. IEEE Symposium on FPGAs for Custom Computing Machines, date of conference April 17, 1998.

9. I obtained a copy of Exhibit A through IEEE Xplore, where it is maintained in the ordinary course of IEEE's business. Exhibit A is a true and correct copy of the Exhibit, as it existed on or about December 18, 2019.

10. The article and abstract from IEEE Xplore shows the date of publication. IEEE Xplore populates this information using the metadata associated with the publication.

11. T. Miyamori; U. Olukotun, A quantitative analysis of reconfigurable coprocessors for multimedia applications was published in Proceedings. IEEE Symposium on FPGAs for Custom Computing Machines, date of conference April 17, 1998. Copies of the conference proceedings were made available no later than the last day of the conference. The article is currently available for public download from the IEEE digital library, IEEE Xplore.

12. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001.

I declare under penalty of perjury that the foregoing statements are true and correct.
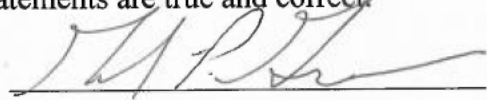
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EXHIBIT A

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A quantitative analysis of reconfigurable coprocessors for multimedia applications

Publisher: IEEE

2 Author(s)   T. Miyamori ; U. Olukotun   View All Authors

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Abstract:
Recently, computer architectures that combine a reconfigurable (or retargetable) coprocessor with a general-purpose microprocessor have been proposed. These architectures are designed to exploit large amounts of fine grain parallelism in applications. In this paper, we study the performance of the reconfigurable coprocessors on multimedia applications. We compare a Field Programmable Gate Array (FPGA) based reconfigurable coprocessor with the array processor called REMARC (Reconfigurable Multimedia Array Coprocessor). REMARC uses a 16-bit simple processor that is much larger than a Configurable Logic Block (CLB) of an FPGA. We have developed a simulator, a programming environment, and multimedia application programs to evaluate the performance of the two coprocessor architectures. The simulation results show that REMARC achieves speedups ranging from a factor of 2.3 to 7.3 on these applications. The FPGA coprocessor achieves similar performance improvements. However, the FPGA coprocessor needs more hardware area to achieve the same performance improvement as REMARC.

Published in: Proceedings. IEEE Symposium on FPGAs for Custom Computing Machines (Cat. No.98TB100251)

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