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[54] **PARALLEL PROCESSING SYSTEM HAVING ASYNCHRONOUS SIMD PROCESSING AND DATA PARALLEL CODING**

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[21] Appl. No.: **487,363**

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Related U.S. Application Data

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[51] **Int. Cl.**[6] **G06F 15/80**

[52] **U.S. Cl.** **395/800.2**; 395/379

[58] **Field of Search** 395/375, 800, 395/379, 800.2, 800.1, 800.11, 800.12, 800.13, 800.14, 800.15, 800.16, 800.21, 800.22

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[57] **ABSTRACT**

A parallel array processor for massively parallel applications is formed with low power CMOS with DRAM processing while incorporating processing elements on a single chip. Eight processors on a single chip have their own associated processing element, significant memory, and I/O and are interconnected with a hypercube based, but modified, topology. These nodes are then interconnected, either by a hypercube, modified hypercube, or ring, or ring within ring network topology. Conventional microprocessor MMPs consume pins and time going to memory. The new architecture merges processor and memory with multiple PMEs (eight 16 bit processors with 32K and I/O) in DRAM and has no memory access delays and uses all the pins for networking. Each chip will have eight 16 bit processors, each processor providing 5 MIPs performance. I/O has three internal ports and one external port shared by the plural processors on the chip. The scalable chip PME has internal and external connections for broadcast and asynchronous SIMD, MIMD and SIMIMD (SIMD/MIMD) with dynamic switching of modes. The chip can be used in systems which employ 32, 64 or 128,000 processors, and can be used for lower, intermediate and higher ranges. Local and global memory functions can all be provided by the chips themselves, and the system can connect to and support other global memories and DASD. The chip can be used as a microprocessor accelerator, in personal computer applications, as a vision or avionics computer system, or as workstation or supercomputer.

4 Claims, 24 Drawing Sheets

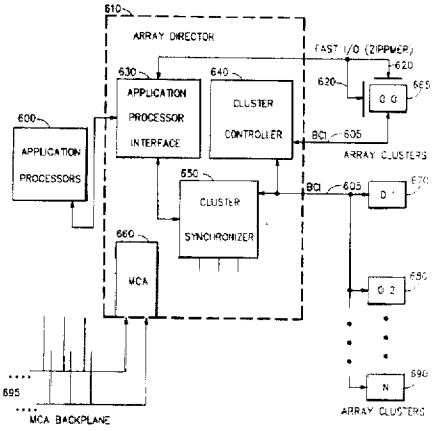

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FIG.1A
Prior Art

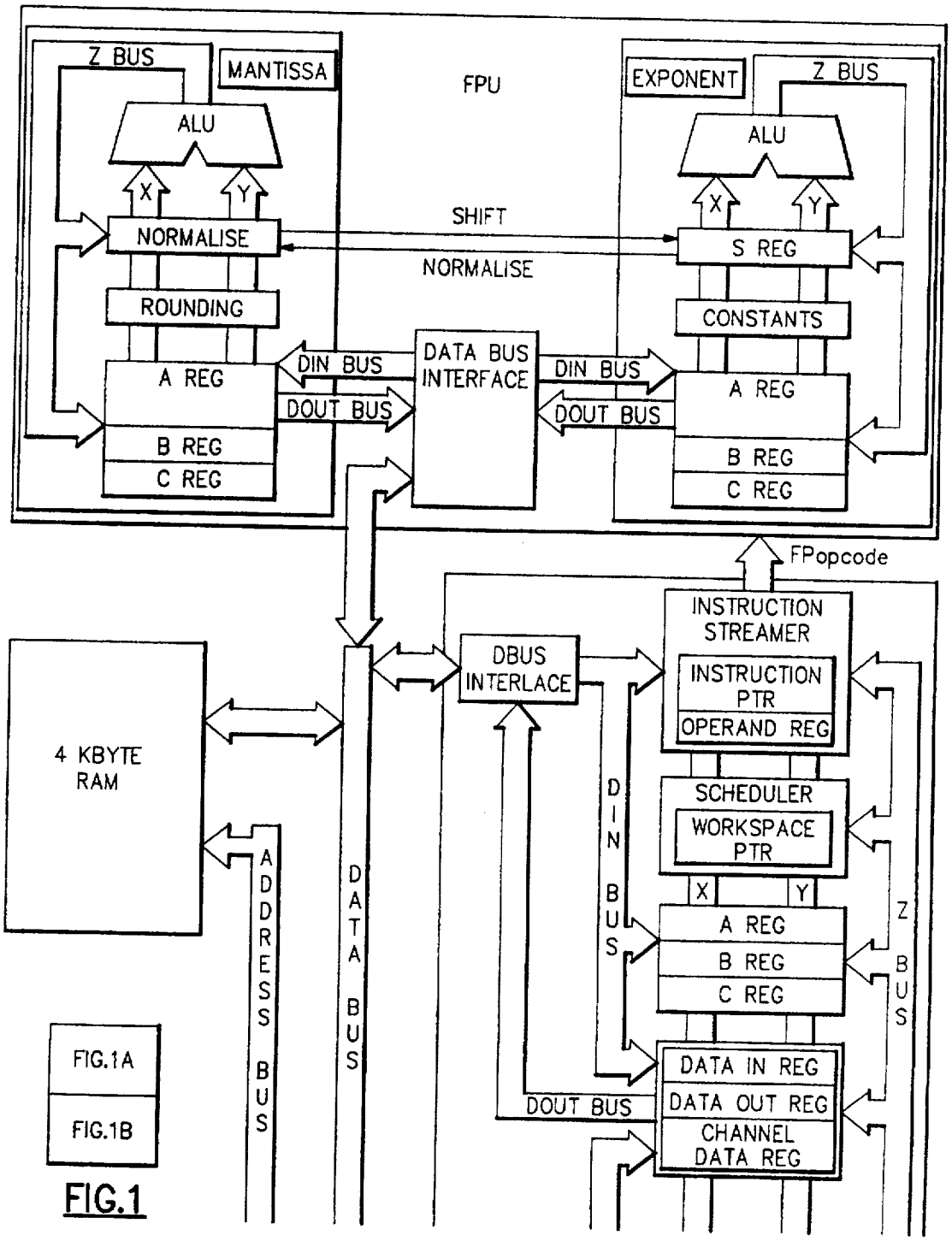

FIG.1

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