Multiprocessors and Parallel Processing

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All modules are connected in parallel to the bus which may be a full word wide or only one byte wide, or may be able to handle only a single bit at a time. As the bus becomes narrower, the control functions become more complex.

The processor and peripheral units may be connected to a single bidirectional bus as shown in Figure 2–1 or unidirectional buses may be used as shown in Figure 2–2. In the latter case the transfer path is completed through the unit on the far left, the bus modifier. The trade-offs here are primarily in the implementation of a single bidirectional interface as opposed to two unidirectional ones. The control logic of the latter is simpler; however, the former has the advantage of utilizing a single buffer register in the interface and less cabling.

It is also possible to have more than one time-shared bus as shown in Figure 2–3. This is approaching the topology of the next system configuration to be discussed, the crossbar system. The distinguishing feature of the time-shared bus is that even if there were an equal number of processors and memories, they could not all be active at the same time because of the time-sharing property of the transfer path(s).

Each packet that is placed on a bus must contain the data that are to be transferred and the address of the unit to which they are directed. There is no problem with conflicts between multiple packets arriving at a unit simultaneously, since only one packet is on the bus at a time and a transmitter has to wait until the bus is free to place its packet on the line. Even though conflict resolution is automatic and not a severe problem, the conflicts still exist and slow the operation of the ensemble considerably. Each unit on the bus must contain the circuitry necessary to recognize its address in a packet and respond accordingly.

As a "simple" example of a single bus system, consider the Digital Equipment Corporation PDP-11 which exploits fully the flexibility of its

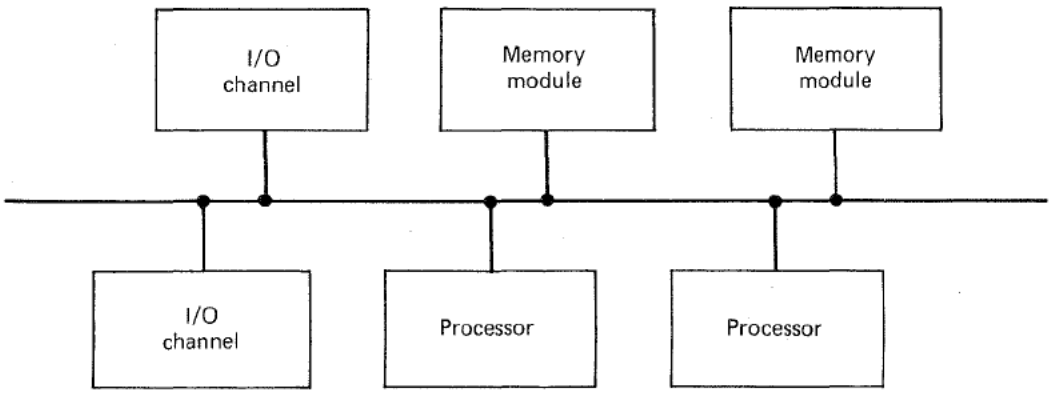

Figure 2-1 Time-shared/common-bus system organization—single bus.

established between the two units for the complete duration of the transfer. In contrast to the time-division switching done on the common-bus system, the technique used here is often referred to as space-division switching. It is very similar to the technique utilized by most telephone central offices.

Although not quite as flexible as the single bus system, it is still relatively easy to add modules to a crossbar system if the switch matrix is large enough. The size of the system is not limited by the access capabilities of the individual functional units, since they all are connected by a single port.

Conflicts in requests for the same memory module are resolved within the switch matrix utilizing one of several techniques possible. Since a full-time connection does exist, the effective transfer rates can be higher that on a single time-shared bus. Also several paths can be established simultaneously.

The crossbar matrix is totally seperate from the functional units and can also be designed in a modular manner to facilitate expansion. However, because of the complexity of the functions that the switch may have to perform, it can become quite large and complex. The switch matrix and its control circuitry for the maximum configuration of the Hughes H4400 (eight CPU's or IOC's and 16 memory modules) contains as many components as

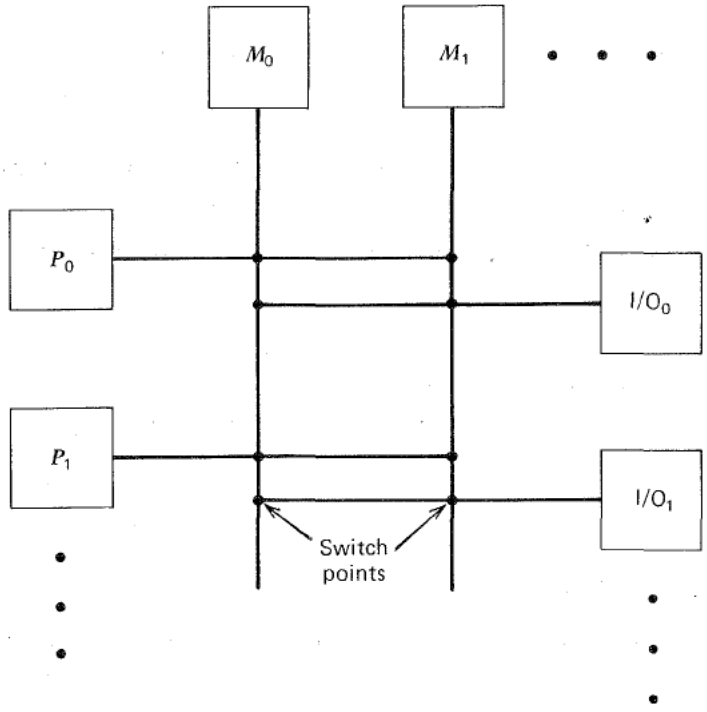

Figure 2-5 Crossbar switch system organization.

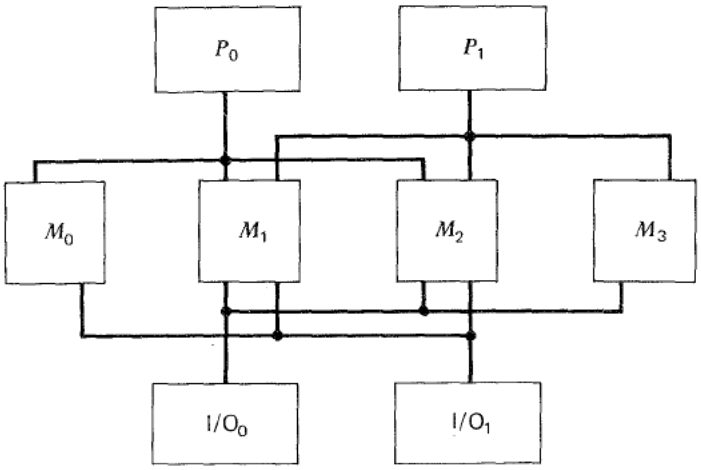

Figure 2-11 Multiport system with private memory.

associated with the connecting point. These priorities can be utilized as the basis for settling conflicts for simultaneous access with each I/O unit and processor being given preference in the access to its "primary" memory module as shown in Figure 2–10.

Just as in the previous organizations, the width of the data transfer path can be any convenient and economical size. If the basic storage unit is a word and the data transfer path is less than one word wide, then special assemble and disassembly registers will have to be included in the interface points as well as special control circuitry so that the transfer path is not preempted and broken when the transfer of a word is only partially complete.

It is not necessary that every memory module be connected to every processor. In fact in some systems it is essential that each processor have some "private memory" in which to store private tables for control functions, recovery, allocation of private resources, and so on (see Figure 2–11). There are reliability and recovery drawbacks, however, to the use of private memory. If a processor fails and the interrupted task must be completed on another processor, it may not be possible for the new processor to access the control information that it requires in order to do so.

Considerable generality is lost if every processor cannot access any memory. Flexibility in relocatability of object programs, as well as in the operating, is lost. The advantages of a single copy of the operating system are obvious. Failure of a memory module as well as of a processor (discussed above) represents a drawback to this organization if it has restrictions on processor to memory access.

In all systems of this configuration, the memory module must recognize and handle requests for access to the specific memory locations that it