IN THE UNITED STATES DISTRICT COURT FOR THE DISTRICT OF DELAWARE

| PACT XPP SCHWEIZ AG |) |
|---------------------|---------------------------|
| Plaintiff, |) C.A. No. 19-1006-JDW |
| v. |) |
| INTEL CORPORATION, |) |
| Defendant. |) |

JOINT CLAIM CONSTRUCTION CHART

Pursuant to Paragraph 9 of the Scheduling Order (D.I. No. 20), Plaintiff PACT XPP Schweiz AG ("PACT") and Intel Corporation ("Intel") hereby submit this Joint Claim Construction Chart, identifying for the Court the terms and phrases of the claims in issue, including each party's proposed construction of the disputed claim language with citations only to the intrinsic evidence in support of their respective proposed constructions.

TABLE OF EXHIBITS

| Exhibit No. | Document | | | |
|-------------|--|--|--|--|
| 1 | U.S. Patent No. 7,928,763 | | | |
| 2 | U.S. Patent No. 8,301,872 | | | |
| 3 | U.S. Patent No. 8,312,301 | | | |
| 4 | U.S. Patent No. 8,471,593 | | | |
| 5 | U.S. Patent No. 8,686,549 | | | |
| 6 | U.S. Patent No. 8,819,505 | | | |
| 7 | U.S. Patent No. 9,037,807 | | | |
| 8 | U.S. Patent No. 9,075,605 | | | |
| 9 | U.S. Patent No. 9,170,812 | | | |
| 10 | U.S. Patent No. 9,250,908 | | | |
| 11 | U.S. Patent No. 9,436,631 | | | |
| 12 | U.S. Patent No. 9,552,047 | | | |
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| 20 | Intentionally Left Blank | | | |
| 21 | Excerpts of File History of U.S. Patent No. 9,170,812 relied on by | | | |
| | Plaintiff | | | |
| 22 | Intentionally Left Blank | | | |
| 23 | Intentionally Left Blank | | | |
| 24 | Excerpts of File History of U.S. Patent No. 9,552,047 relied on by | | | |
| | Plaintiff | | | |
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| Exhibit No. | Document | | | |
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| 28 | Intentionally Left Blank | | | |
| 29 | Intentionally Left Blank | | | |
| 30 | Excerpts of File History of U.S. Patent No. 8,819,505 relied on by | | | |
| | Defendant | | | |
| 31 | Intentionally Left Blank | | | |
| 32 | Excerpts of File History of U.S. Patent No. 9,075,605 relied on by Defendant | | | |
| 33 | Excerpts of File History of U.S. Patent No. 9,170,812 relied on by Defendant | | | |
| 34 | Intentionally Left Blank | | | |
| 35 | Excerpts of File History of U.S. Patent No. 9,436,631 relied on by Defendant | | | |
| 36 | Excerpts of File History of U.S. Patent No. 9,552,047 relied on by Defendant | | | |
| 37 | DE 196 54 846 A1 | | | |

STIPULATED CLAIM TERMS

| Patent | Claim Terms and Phrases | Stipulated Claim Construction | |
|--------|-----------------------------------|-------------------------------|--|
| '605 | Preamble (claim 1) | Preamble is limiting. | |
| '908 | "train mission" (claim 4) | transmission | |
| '631 | "may executed" (claim 1) | may be executed | |
| '872 | Preambles (claims 2, 10, 14, 15) | Preambles are not limiting. | |
| '807 | Preambles (claims 1-6, 24, 26-27, | Preambles are not limiting. | |
| 807 | 29, 32, 44, and 73-74) | | |

TERMS PROPOSED BY PLAINTIFF

| Patent | Claim Terms and Phrases | Plaintiff's Proposed Construction | Defendant's Proposed Construction | Plaintiff's Intrinsic Evidence | Defendant's Intrinsic Evidence |
|--------|---|--|---|--|---|
| '763 | "interconnecting at runtime at least one of data processing cells and memory cells with at least one of memory cells and one or more of the at least one interface unit" (claims 1, 31) | connect at least one data processing cell, at least one memory cell, and at least one interface unit with each other at runtime. | See Intel's construction for "programmably interconnecting at runtime" / "dynamically interconnecting at runtime" | Ex. 1, Figs. 1, 2(a)-2(c), 3, 4, 5 7:47-11:12; 11:21-45. | See e.g., Ex. 1 ('763 patent) at 2:16-23; 12:5-17; 4:4-10; 12:38-83; 9:3-9:6; 6:56-7:6; 1:26-28; 8:45-55. |

| Patent | Claim Terms | Plaintiff's Proposed | Defendant's Proposed | Plaintiff's Intrinsic Evidence | Defendant's Intrinsic Evidence |
|--------|---|---|---|--|---|
| Тиси | and Phrases | Construction | Construction | 211101100 | |
| '763 | "the data processing cells are adapted to connect simultaneously to a plurality of at least one of cells and units of at least one of the memory cells, the data processing cells, and the at least one interface units" (claim 10) | each of the data processing cells is adapted to simultaneously connect to a plurality of elements; each of the elements is either one of the memory cells, another one of the data processing cells, or the interface unit. | See Intel's construction for "programmably interconnecting at runtime" / "dynamically interconnecting at runtime" | Ex. 1, Figs. 1, 2(a)-2(c), 3, 4, 5 7:47-11:12; 11:21-45. | See e.g., Ex. 1 ('763 patent) at 2:16-23; 12:5-17; 4:4-10; 12:38-83; 9:3-9:6; 6:56-7:6; 1:26-28; 8:45-55. |

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