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TUTORIAL:

# INTERCONNECTION NETWORKS

## for parallel and distributed processing

Chuan-lin Wu and Tse-yun Feng



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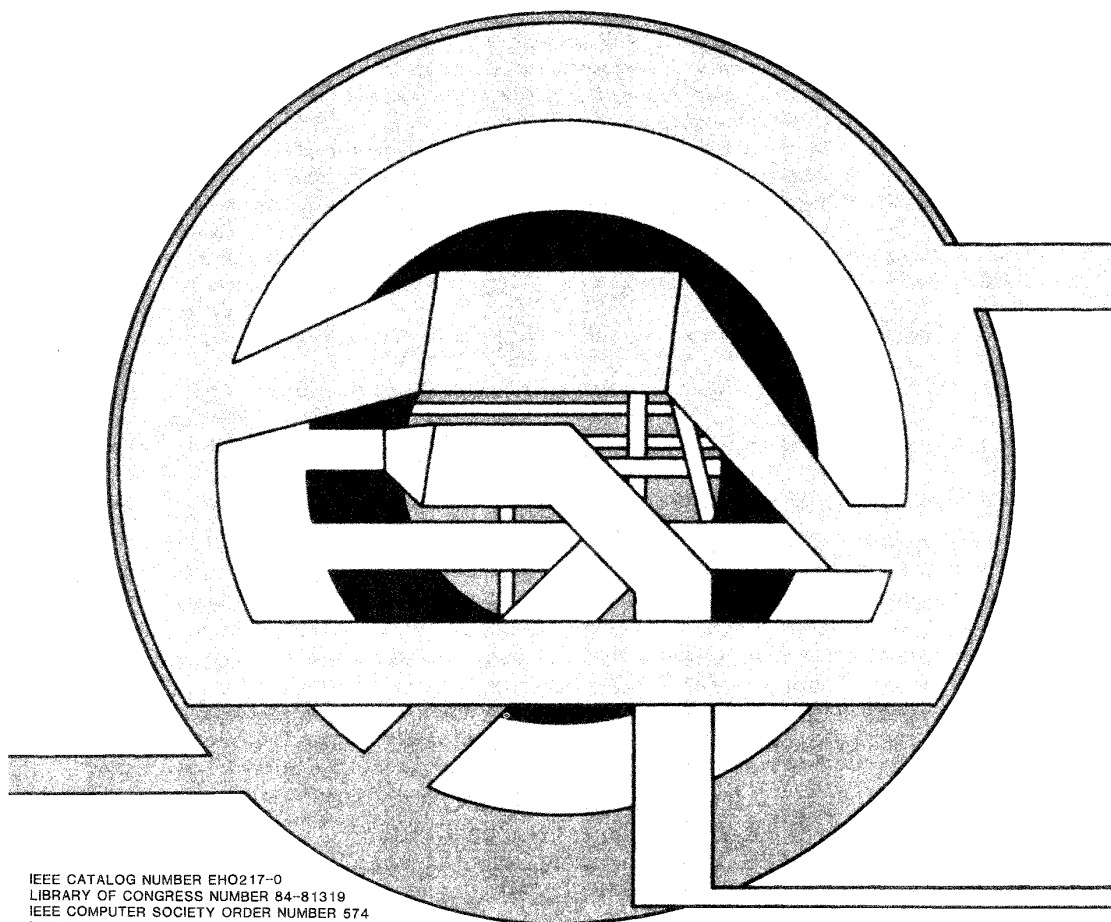
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## Preface

This tutorial presents fundamentals in interconnection networks, a crucial topic in the field of parallel/distributed processing. The interconnection network consists of software and hardware entities that are designed to facilitate efficient interprocess and interprocessor communication in a parallel processing system. Although conventional computer systems using the von Neumann model do not have many system units to be connected and the processes are sequentially executed, an interconnection network such as the time-shared bus is still a critical system component. Today, system units such as processors and memory modules have increased rapidly in new computer systems, and processes are executed in parallel to meet real-time requirements. The design of interconnection networks is emerging as the most basic issue in exploiting parallelism. The interconnection network not only has a profound impact on algorithm design, but also greatly affects system level control.

In spite of the importance of the interconnection network in future computer system design, the issues of designing interconnection networks have never been fairly and completely explored in a single publication. Even worse, researchers often ignore its impact and stubbornly think that the interconnection network is nothing but a communication idiot. It is a fallacy for people to think that there is enough work in interconnection networks. In view of this, the authors believe that a tutorial is urgently needed to promote more fruitful research efforts in the field of parallel/distributed processing.

The text of this tutorial is designed for system designers, programmers, educators, and those who are involved in the research, development, and application of various special-purpose and general-purpose computer systems. It is tutorial in nature and provides a state-of-the-art survey. It is expected that the tutorial will serve as a guide for beginners and as a major reference for all computer professionals. It is hoped that, after going through the text, readers will be able to design interconnection networks that fit their computer architecture needs, design better algorithms by taking advantage of what the interconnection network can offer, write better programs by knowing the limitations of the interconnection network, and trigger a revolution on the system control concept.

The text is organized into 12 chapters. A tutorial guide, provided at the beginning of each chapter, explains the idea and concept and also annotates an up-to-date reference list. Each chapter includes some reprint articles which explain underlying theory and developments.

Chapter 1 provides a comprehensive overview of interconnection networks, with a discussion of design trends and design issues.

Chapter 2 surveys underlying network topologies used in parallel/distributed system architecture. The topologies are divided into two categories: static and dynamic.

Chapter 3 focuses on control strategies for routing data through interconnection networks. Various routing algorithms are covered.

Chapter 4 discusses how to realize data permutations in an array processing mode, with an exploration of permutation capability of various kinds of interconnection networks.

Chapter 5 explores the performance evaluation of interconnection networks. Evaluation parameters considered include bandwidth, message delay, diameter, and effectiveness in simulating other networks.

Chapter 6 is concerned with fault diagnosis for detecting and locating faults in interconnection networks. Fault models and test procedures are considered.

Chapter 7 investigates fault-tolerance characteristics of interconnection networks, as well as ways to achieve fault tolerance.

Chapter 8 discusses issues in using very-large-scale-integrated (VLSI) circuits to design interconnection networks. Area and delay models of layouts are also formulated.

Chapter 9 covers reconfiguration techniques that are concerned with allocating network resources to achieve variable topology capability. Different approaches are discussed.

Chapter 10, on mapping, is concerned with how to partition and assign program modules to resources such as processors and memories, subject to minimizing the total number of routing steps. The mapping is done under the assumption that either (or both) the algorithm or interconnection network is fixed.

Chapter 11 explores network synthesis, which derives the optimum network topology for a transformed algorithm. Both algorithms and networks are treated as variables in the procedure.

Finally, Chapter 12 provides some examples on the construction of multistage networks. It should be noted that every system needs an interconnection network. The examples provided are used to point out the trends.

We would like to take this opportunity to thank all the authors who have contributed to this tutorial text. We apologize to those authors whose valuable papers could not be included due to page limitations. We tried to be as complete as possible in compiling the reference lists, which were based on contribution and accessibility of the work. We deeply regret any omissions and hope that they will be made known to us so that they can be included in later updates. Finally, we would like to thank the reviewers for their helpful criticisms and suggestions, and Margaret Brown and her staff of the IEEE Computer Society Press for editing the text.

Chuan-lin Wu, *University of Texas at Austin*  
Tse-yun Feng, *Pennsylvania State University*

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