



(12) **United States Patent**
Gilbertson

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(54) **SYSTEM AND METHOD FOR PROGRAMMABLY CONTROLLING DATA TRANSFER REQUEST RATES BETWEEN DATA SOURCES AND DESTINATIONS IN A DATA PROCESSING SYSTEM**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(57) **ABSTRACT**

A system and method for selectively controlling the interface throughput of data transfer requests from request sources to request destinations. The system and method provide a manner in which the flow of data transfer requests from request sources to request destinations are controlled. The data transfer requests from each of the request sources are temporarily stored for future delivery to its addressed request destination. Delivery of the stored data transfer requests to the addressed request destination is enabled according to a predetermined delivery priority scheme. Certain stored data transfer requests are identified to be selectively suspended from being prioritized and delivered to the addressed request destination. The identified data transfer requests are suspended from delivery for a definable period of time. Upon expiration of the definable period of time, the suspended data transfer requests, as well as all other stored data transfer requests, are enabled for prioritization and delivery in accordance with the predetermined delivery priority scheme.

(21) Appl. No.: **09/218,211**

(22) Filed: **Dec. 22, 1998**

(51) **Int. Cl.**⁷ **G06F 15/16**

(52) **U.S. Cl.** **709/232; 709/233; 709/234; 709/235; 710/39; 710/60**

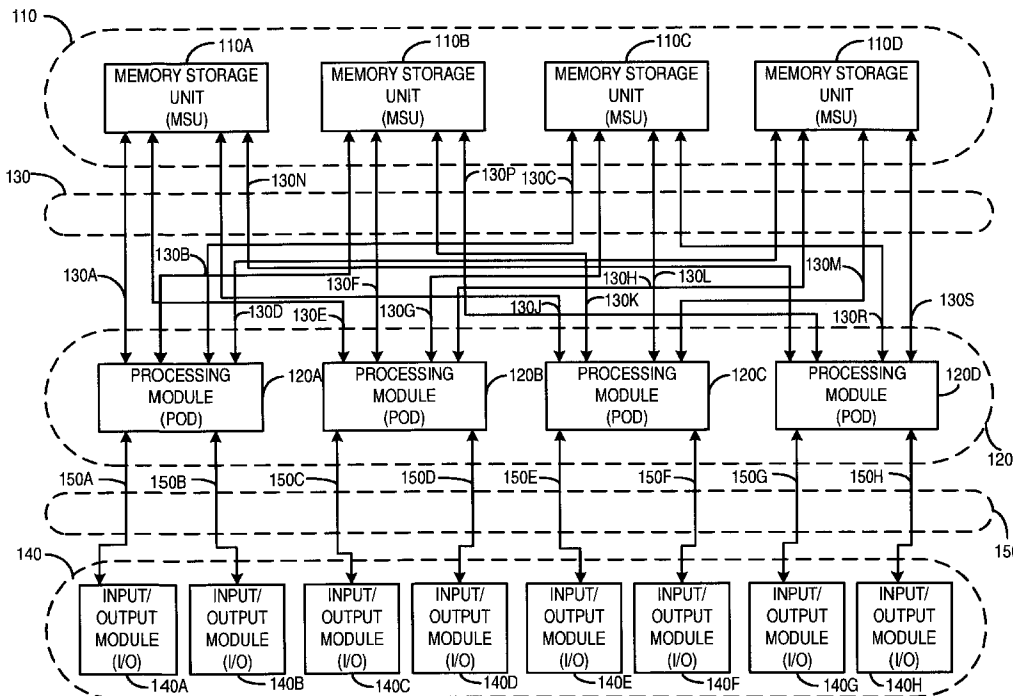
(58) **Field of Search** 709/234, 200, 709/222, 252, 243, 207, 238, 235, 232, 233, 240; 710/263, 264, 244, 112, 116, 39, 40, 52, 58-60; 711/150, 151; 370/395, 414

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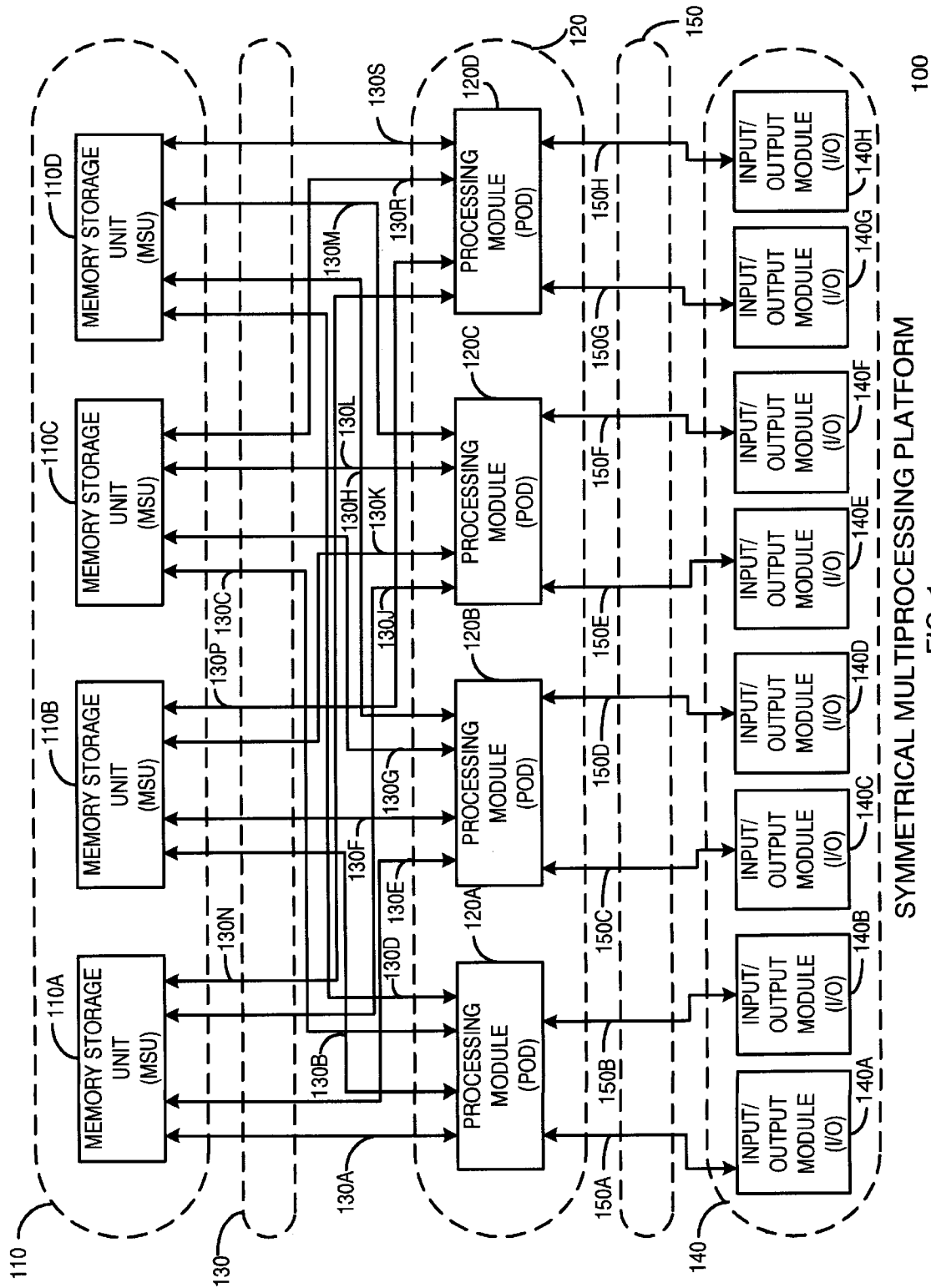
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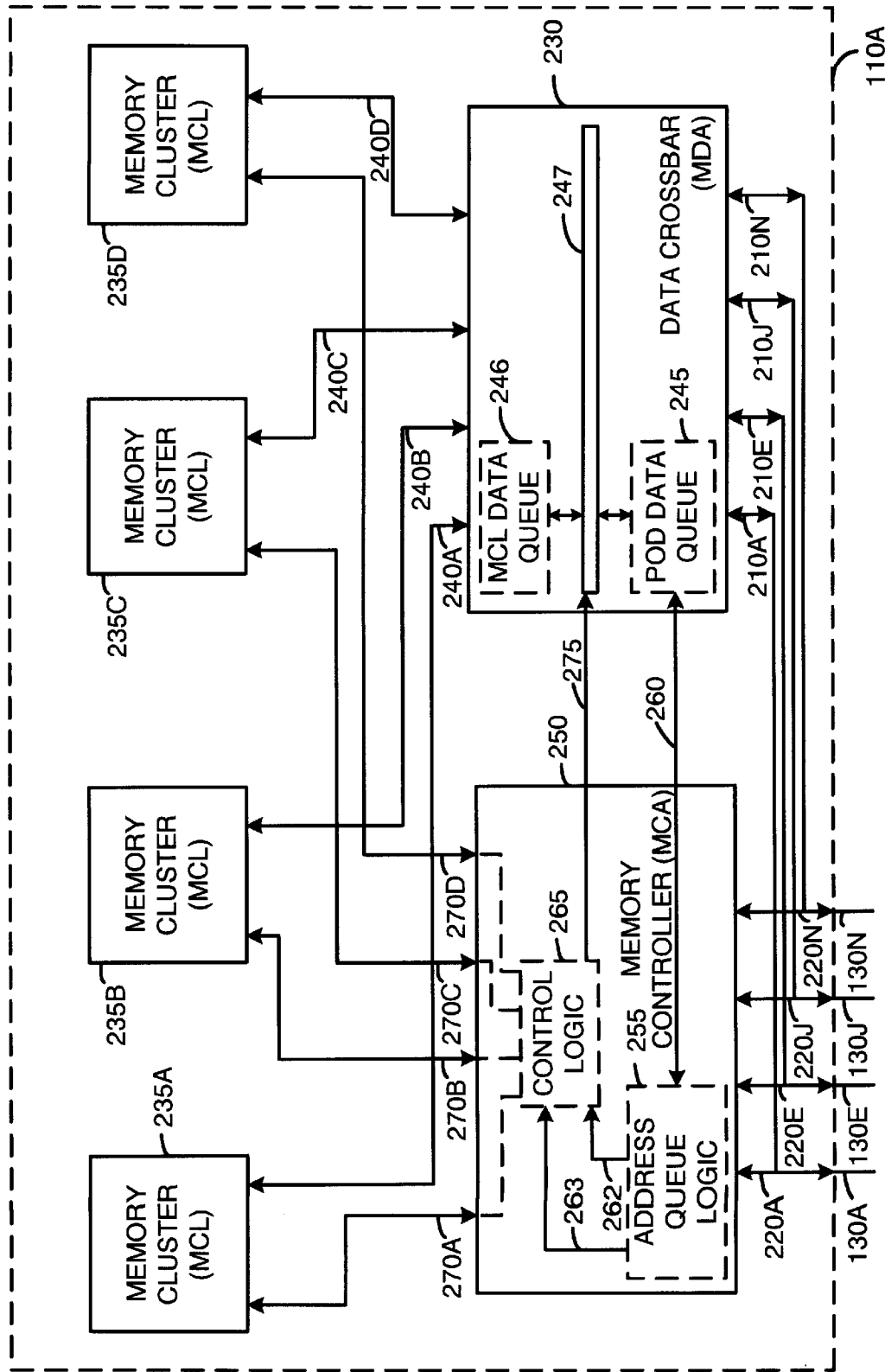
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33 Claims, 14 Drawing Sheets

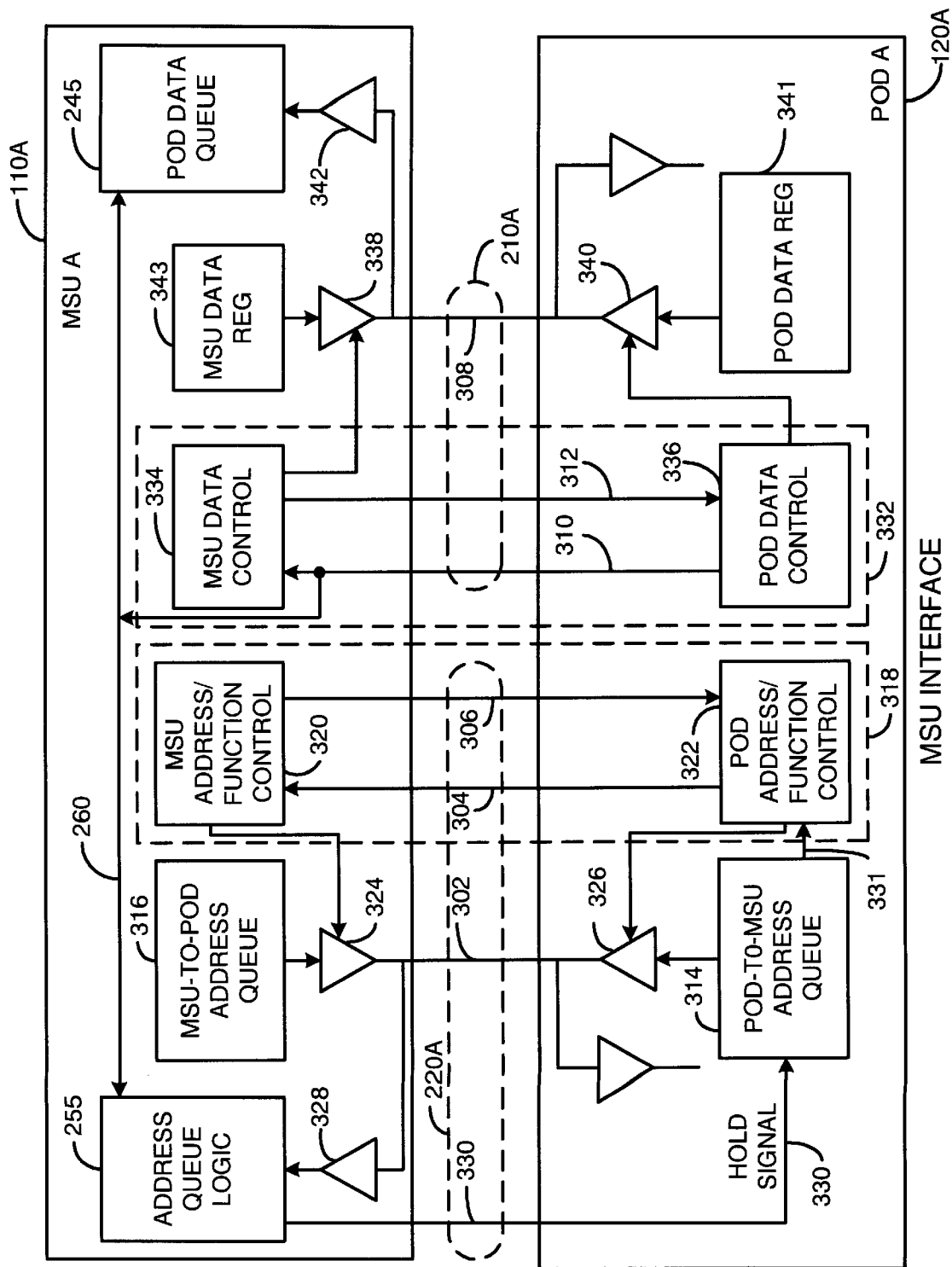


SYMMETRICAL MULTIPROCESSING PLATFORM

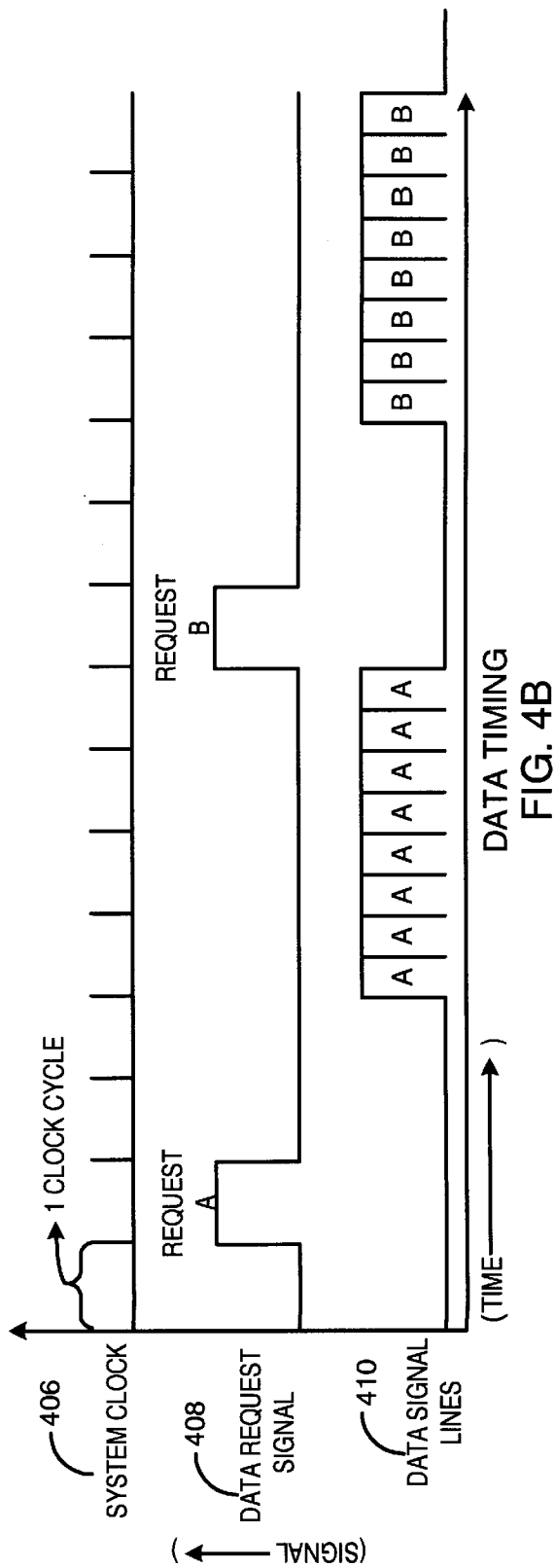
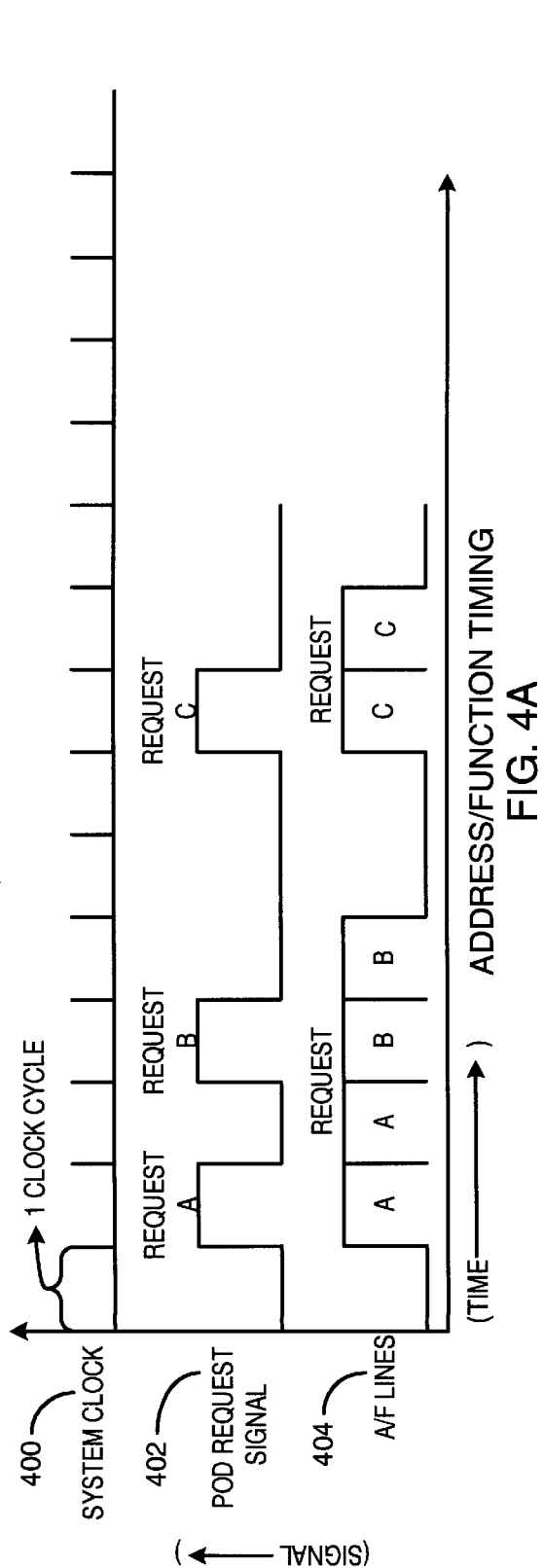




MEMORY STORAGE UNIT (MSU)
FIG. 2



MSU INTERFACE
FIG. 3



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