Low Complexity GSM Modulator for Integrated Circuit Implementations

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Abstract --- Reduced complexity Integrated Circuit (IC) design architecture for constant envelope modulation is presented. This method is demonstrated on the globally standardized Gaussian Minimum Shift Keying (GMSK) for the "Global System for Mobile Communications" (GSM). The in-phase and quadrature signals are generated directly from the input binary data, bypassing the separate steps of integrating, and then calculating the sine and cosine values. The implementation takes advantage of waveform symmetry properties thereby leading to reduction in memory requirements by 800% with respect to full storage of required waveforms. Performance comparison with a commercially available GSM IC is also carried out.

I. INTRODUCTION

The Gaussian Minimum Shift Keying (GMSK) modulation[1,2] scheme is very suitable for mobile radio applications due to the following features,
(i) Compact output spectrum which results in increase in number of available channels and at the same, maintain low adjacent channel interference.
(ii) Constant Envelope which allows RF amplifiers to operate in non linear mode with greatly improved power efficiency. This is very important in today's wireless cellular PCS systems for battery powered units.

In the following sections, conventional GMSK technique is briefly introduced and an alternative method for generating GMSK signals is described. The results of the measurements are then discussed.

A. Gaussian Minimum Shift Keying Modulation

Figure 1 shows the textbook architecture for the quadrature baseband processor. Input NRZ data is filtered using a Gaussian low pass filter (GLPF). This filter may be implemented using an actual filter that approximates the Gaussian characteristics or using the ROM look up table method. This signal after integration (b(t)) is split and fed into cosine and sine look up tables such that the input signal drives are related by the equations,

$$x(t) = \cos[\, b(t)\,] \quad (1)$$
$$y(t) = \sin[\, b(t)\,] \quad (2)$$

Evidently the I and Q signals are mathematically related or "cross correlated" [3,4] to each other. Thus in this case the predictability or cross correlation of y(t) from x(t) is defined by,

$$y(t) = \sin\{\cos^{-1}[\, x(t)]\} \quad (3)$$

This is also evident from figure 2 which shows the waveforms for the I and Q channels. It can be observed that when the quadrature (or in-phase) signal reaches its maximum magnitude, the in-phase (or quadrature) signal is crossing zero. The amplitude of the quadrature (or in-phase) signal is reduced when the in-phase (or quadrature) signal is non zero. This cross correlation property maintains the constant envelope.

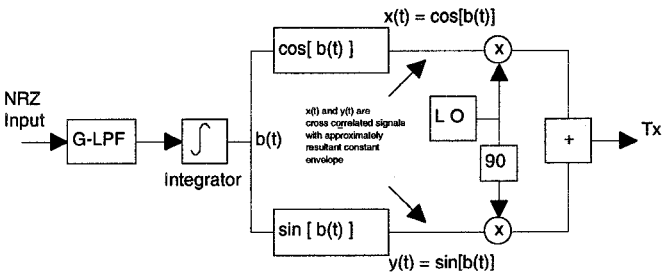

Figure 1. Textbook Implementation of GMSK Baseband Processor

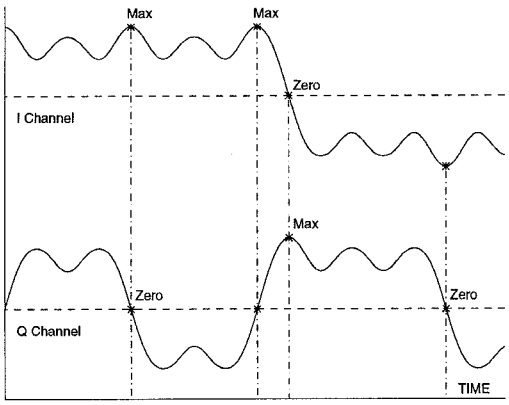

Figure 2. Cross correlated I and Q channel signals.

II. MODULATOR IMPLEMENTATION

Due to the cross correlation properties of the I and Q signals, it is possible to pre-calculate the output waveform in response to the input data. Four serial data inputs D3 through D0 (D3 is the incoming bit while D0 is the input data 4 bit duration's prior) and one Flag bit 'F' are used for the waveform selection procedure. The Flag bit alternates between a 1 or 0 per bit period and provides information as to which half of the symbol waveform to select. When F = 0, the first half of the symbol waveform is selected for the I channel while for the Q channel the second half is selected. In addition when F = 0, D0 and D2 provide data transition information for the I channel while D1 and D3 provide data transition information for the Q channel. For the I channel, when F = 0, D2 is the current bit and D0 is the past bit. For the Q channel, D1 is the current bit and D3 is the next incoming bit. If the current bit is 1, then the respective waveform is of positive amplitude else of negative amplitude. If the I channel (D0 to D2) and Q channel (D1 to D3) show no data transition then the respective waveforms begin and end at intermediate values else they will begin or end at ± 1 or 0.

With F = 1, the relationship of D0 through D3 with the I and Q channels is reversed. Now D1 and D3 provide information for the I channel while D0 and D2 provide information for the Q channel. The 32 different wavelet pairs in response to 4 serial data inputs and Flag are shown in Table I [5]. For each set in Table I, the top wavelet is for the I channel and the one below it is for Q channel.

Thus using Table I, the output waveforms for the I and Q channel are selected in response to 4 data input bits and one Flag bit. Thus the GMSK modulator can be implemented as a ROM Look Up table system as discussed further. The block diagram of our implementation is shown in Figure 3 followed by the baseband processor description.

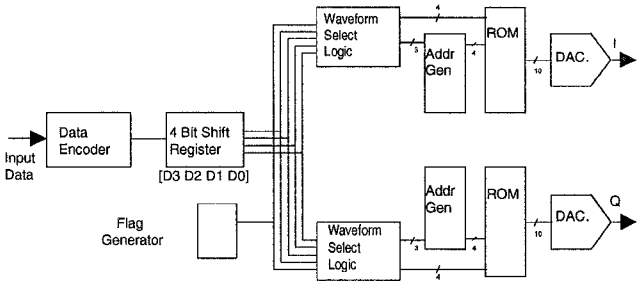

Figure 3. Block diagram of the GMSK modulator

A) ROM Look Up table and Waveform Select Logic

Advantage of the symmetry of the waveform is taken. Thus only 4 waveforms as shown in Figure 4 need to be stored in the ROM Look Up Table [6]. Each waveform contains 8 samples per bit duration. By inverting the stored waveform, memory reduction by a factor of 2 is achieved. Time reflecting the waveform reduces the memory requirement by another factor of 2. Also since 16 samples are used per symbol, and we use 8 samples per bit duration, a further reduction by a factor of 2 is achieved. The stored waveforms are 10 bits wide and 8 times oversampled (per bit duration)

TABLE I

Wavelets to be selected for I and Q channels based on F D3 D2 D1 D0 (Read in this order under each set). The incoming bit is D3 while D0 is the input data 4 bit times prior. In each set the top wavelet is for I channel while the wavelet below for Q channel [5].

Set 1 00000	Set 2 00001	Set 3 00010	Set 4 00011	Set 5 00100	Set 6 00101	Set 7 00110	Set 8 00111
Set 9 01000	Set 10 01001	Set 11 01010	Set 12 01011	Set 13 01100	Set 14 01101	Set 15 01110	Set 16 01111
Set 17 10000	Set 18 10001	Set 19 10010	Set 20 10011	Set 21 10100	Set 22 10101	Set 23 10110	Set 24 10111
Set 25 11000	Set 26 11001	Set 27 11010	Set 28 11011	Set 29 11100	Set 30 11101	Set 31 11110	Set 32 11111

which requires a ROM of 4 waveforms x 10 bits/ sample x 8 samples = 320 bits per channel. With no waveform reduction, 16 symbol duration waveforms will be required. Hence a memory reduction of 8 times (800%) with respect to the full symbol storage is gained.

In response to the 4 input data bits and 1 Flag, the I and Q waveform select logic selects one of the 4 waveforms and generates control signals to invert and or time reflect the selected waveform. Time reflection is achieved by the count DOWN mode of the address generator.

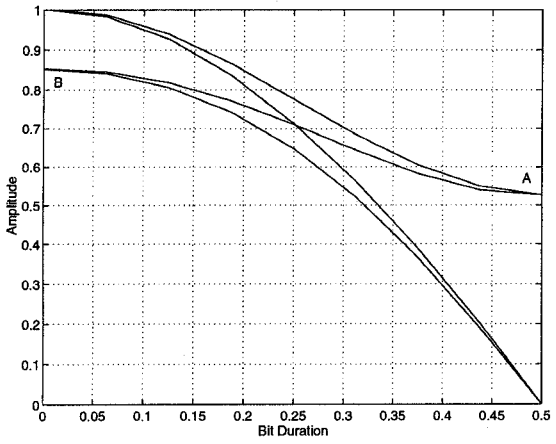

Figure 4. Waveforms stored in the ROM for $BT_b = 0.3$ with A = 0.52 and B = 0.85. 8 samples are used per bit duration waveform.

B) Data Encoder

To ensure that the output data pattern is identical to that generated by a differentially encoded GSM modulator, a data encoder is designed. Depending on present state (S_{n-1}) and incoming bit (D_n), the next state (S_n) will be determined as per the state diagram shown in Figure 5. The 1 or 0 on the X or Y axis denotes the output of the state. If the present state is initially on the X axis (Figure 5a) then during the next bit time, the present state will be on the Y axis (Figure 5b). The Flag bit which alternates per bit time is used to control the output of the data encoder as shown in Figure 6.

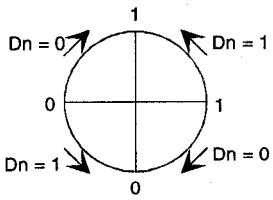

Figure 5a. State Diagram beginning on X axis .

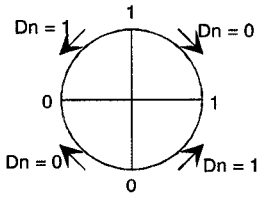

Figure 5b. State Diagram beginning on Y axis.

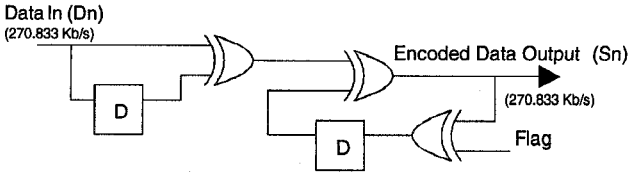

Figure 6. Data Encoder Logic Circuit.

III. DISCUSSION OF RESULTS

For measurement purposes, a baseband processing system is designed and implemented with a Field Programmable Gate Array (FPGA). The design utilizes about 99 out of a maximum 196 Configurable Logic Blocks (CLB) which is about 50% device utilization. The GSM data rate of 270.833 Kb/s generated by a pseudorandom data generator is used. Results are compared to those generated with a commercially available GSM IC.

Figure 7 shows the output waveforms generated by the designed system (Figure 7a) and the GSM IC (Figure 7b) for the same input data pattern.

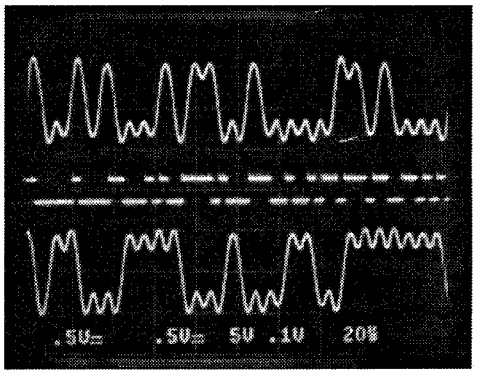

Figure 7a

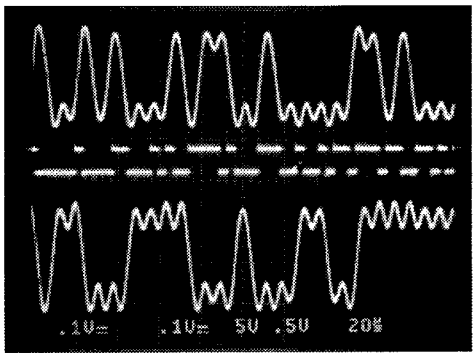

Figure 7b

Figure 7. Output I and Q baseband waveforms of the designed baseband processor (a) and of a commercially available GSM IC (b). The same input data pattern (shown in the middle) is used.

Figure 8 shows the constellation of the I and Q signals. The output signals have the same amplitudes such that the vector sum of the I and Q signals are approximately the same at virtually all phases of each bit period.

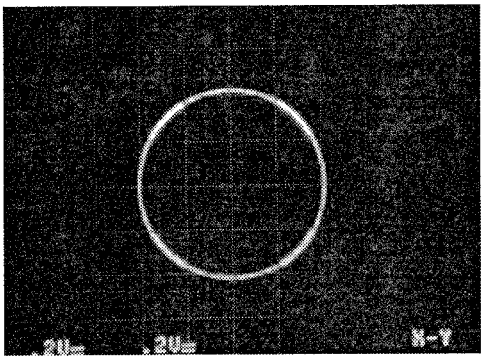

Figure 8. Constellation Diagram of the designed system

Figure 9 shows the superimposed power spectral density (PSD) results for the designed GMSK baseband processor and the commercial GSM IC. The input bit rate is 270.833 Kb/s. The GSM spectrum mask [7] is also shown. The measured spectrum does not go over the GMSK mask. Thus the baseband processor meets the GSM spectrum mask.

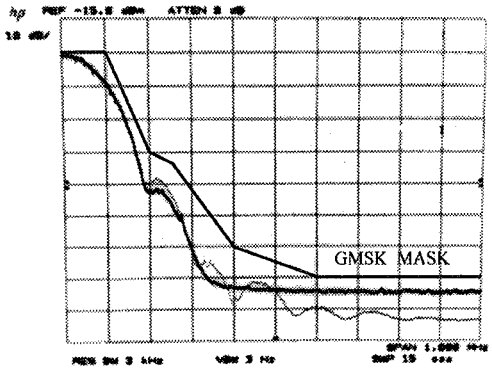

Figure 9. Measured Power Spectral Density. The bright line is the commercial GSM IC while the light trace is the designed GMSK baseband processor. GMSK mask is also shown.

Figure 10 presents the measured probability of error (P_e) versus the S/N relationship, where S/N is the average signal power to average noise power at the decision threshold input. Measurement for single channel is done where the B_iT of the post-detection filter is 0.6. The difference between the BER performance of the designed baseband processor (Curve 2) and the commercial GSM IC (Curve 1) at $P_e = 10^{-4}$ is measured to be under 0.5 dB.

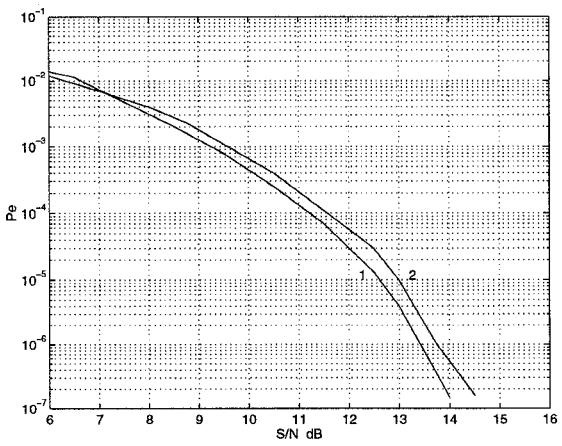

Figure 10. Pe versus S/N for the GMSK baseband processor (Curve 2) and GSM IC (Curve 1). The post-detection filter used is a 4th order Butterworth filter with $B_iT = 0.6$.

IV. CONCLUSIONS

In this paper, a design and implementation of a hardware efficient quadrature GMSK structure based on the cross-correlation concepts is discussed. Waveform symmetry leads to reduction in memory requirements. The encoder allows the data polarity to match exactly with the output polarity of the commercial GSM IC. Performance results are compared with a commercially available GSM IC. The modulator design presented here is suitable for IC implementation at various levels.

V. REFERENCES

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