

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG DISPLAY CO., LTD.,
Petitioner,

v.

SOLAS OLED LTD.,
Patent Owner.

IPR2020-00320
Patent 7,446,338 B2

Before SALLY C. MEDLEY, JESSICA C. KAISER, and JULIA HEANEY,
Administrative Patent Judges.

KAISER, *Administrative Patent Judge.*

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314; 37 C.F.R. § 42.4

On December 18, 2019, LG Display Co. Ltd. (“Petitioner”) filed a Petition requesting an *inter partes* review of claims 1–3 and 5–13 of U.S. Patent No. 7,446,338 B2, issued on November 4, 2008 (Ex. 1001, “the ’338 patent”). Paper 1 (“Pet.”). Solas OLED Ltd. (“Patent Owner”) filed a Preliminary Response. Paper 6 (“Prelim. Resp.”). On April 27, 2020, we authorized additional briefing addressing a district court claim construction order. On May 4, 2020, Petitioner filed a Supplemental Pre-Institution Brief addressing the district court claim construction. Paper 7 (“Supplemental Brief” or “Supp. Br.”). On May 11, 2020, Patent Owner filed a Response to Petitioner’s Supplemental Pre-Institution Brief. Paper 8 (“Supplemental Response Brief” or “Supp. Resp. Br.”).¹ Applying the standard set forth in 35 U.S.C. § 314(a), which requires demonstration of a reasonable likelihood that Petitioner would prevail with respect to at least one challenged claim, we grant Petitioner’s request and institute an *inter partes* review of claims 1–3 and 5–13.

I. BACKGROUND

A. The ’338 Patent (Ex. 1001)

The ’338 patent describes a display panel comprised of pixels, the pixels having a particular arrangement of transistors driving the pixels’ light-emitting elements. Ex. 1001, 2:34–41, code (57). Figure 1 of the ’338 patent is reproduced below.

¹ Additionally, on May 14, 2020, we denied Patent Owner’s May 12, 2020 request for supplemental briefing to address *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB March 20, 2020) (precedential). Ex. 3001. Specifically, we denied Patent Owner’s request because Patent Owner’s Preliminary Response did not request that the Board exercise its discretion under 35 U.S.C. § 314(a) or address *NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 (Sept. 12, 2018) (precedential).

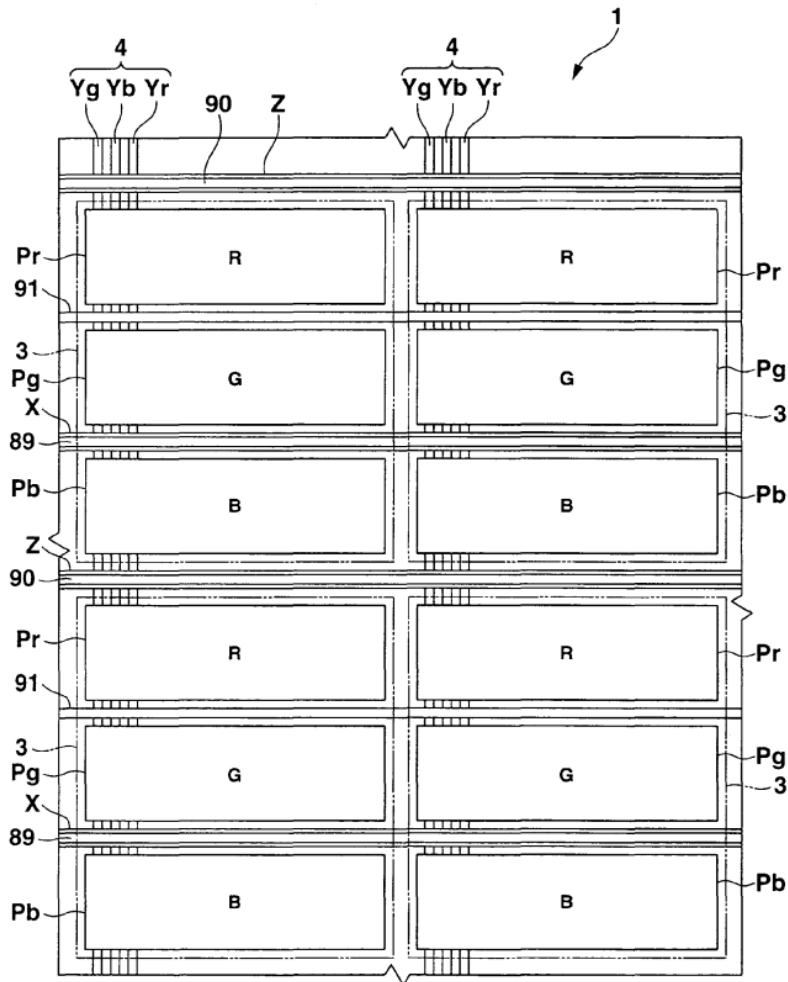


FIG.1

Figure 1 shows four adjacent pixels in display panel 1. Display panel 1 is comprised of pixels 3; in particular, the figure shows four adjacent pixels arranged in a 2-by-2 configuration, i.e., the pixels are arranged in an array. *Id.* at 4:53–55, 4:65–66. Each pixel 3 is comprised of red sub-pixel Pr, green sub-pixel Pg, and blue sub-pixel Pb. *Id.* at 4:63–65. Each sub-pixel Pr, Pg, Pb is connected to corresponding signal line Yr, Yb, Yg, respectively. *Id.* at 5:12–15. Further, each sub-pixel is connected to select interconnection 89, feed interconnection 90, and common interconnection

interconnection 90 and driving transistor 23. *Id.* at 6:61–62, 6:65–67, 7:3–6, 7:11–13, 14:47–50.

The '338 patent describes two operating periods for the pixel circuit: a “selection period” and a subsequent “light emission period.” *Id.* at 15:28, 15:58–61. During the selection period, a “feed driver applies a write feed voltage VL to supply a write current to the driving transistors 23 connected to” supply line Zi. *Id.* at 14:46–50; *see id.* at Fig. 7. The “write current (pull-out current) . . . flows from the feed interconnection 90 and supply line Zi through the drain-to-source path of the driving transistor 23 and the drain-to-source path of the switch transistor 21” and to signal line Yj. *Id.* at 15:34–41. Notably, “the switch transistor 21 functions to turn on (selection period) and off (light emission period) of the current between the signal line Yj and the source 23s of the driving transistor 23.” *Id.* at 17:26–29. That is, switch transistor 21 controls whether the write current flows through driving transistor 23, depending on whether the switch transistor is respectively turned on or off. *See id.*; *see also id.* at 15:58–61. In the “subsequent light emission period,” switch transistor 21 is “turned off.” *Id.* at 15:58–61.

Furthermore, the '338 patent describes that such pixel circuit arrangements for a display are formed “by stacking various kinds of layers on [an] insulating substrate.” *Id.* at 8:21–22. Figure 6, reproduced below, is a cross-sectional view of a pixel showing such stacked layers.

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