US005847577A

United States Patent [19]

Trimberger

[11] Patent Number: 5,847,577

[45] Date of Patent: *Dec. 8, 1998

[54] **DRAM MEMORY CELL FOR PROGRAMMABLE LOGIC DEVICES**

[75] Inventor: **Stephen M. Trimberger**, San Jose, Calif.

[73] Assignee: **Xilinx, Inc.**, San Jose, Calif.

[*] Notice: The term of this patent shall not extend beyond the expiration date of Pat. No. 5,581,198.

[21] Appl. No.: **758,286**

[22] Filed: **Nov. 1, 1996**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 394,092, Feb. 24, 1995, Pat. No. 5,581,198.

[51] **Int. Cl.**[6] **H03K 19/177**; G11C 7/00

[52] **U.S. Cl.** **326/38**; 326/41; 365/228; 711/106

[58] **Field of Search** 326/38–40; 365/222, 365/228, 230.03, 230.05, 149; 711/100, 106, 161–162

[56] **References Cited**

U.S. PATENT DOCUMENTS

Re. 34,363	8/1993	Freeman .	
3,866,182	2/1975	Yamada et al.	340/172.5
4,366,560	12/1982	McDermott et al.	365/228
4,638,425	1/1987	Hartung	364/200
4,642,487	2/1987	Carter .	
4,682,306	7/1987	Sakurai et al.	365/222
4,706,216	11/1987	Carter	365/94
4,750,155	6/1988	Hsieh	365/203
4,935,896	6/1990	Matsumura et al.	365/187
5,051,887	9/1991	Berger et al.	364/200
5,187,393	2/1993	El Gamal et al. .	
5,270,967	12/1993	Moazzami et al.	365/230.06
5,283,885	2/1994	Hollerbauer	395/425
5,375,086	12/1994	Wahlstrom	326/38
5,450,608	9/1995	Steele	395/800
5,581,198	12/1996	Trimberger	326/39
5,594,698	1/1997	Freeman	365/222

OTHER PUBLICATIONS

R. Sedgewick, "Algorithms", pp. 283–284, Addison–Wesley, 1983.

R. Sedgewick, "Algorithms", pp. 295–303, Addison–Wesley, 1983.

J.F. Wakerly, "Digital Design Principles and Practices" pp. 34–44, Prentice Hall, 1990.

Bradley Felton and Neil Hastie, "2.6 Configuration Data Verification and the Integrity Checking of SRAM–based FPGAs" GEC Plessey Semiconductors, *FPGAs,* W.R. Moore & W. Luk (eds.), 1991, Abingdon EE&C Books, 15 Harcourt Way, Abingdon, OX14 INV, UK, pp. 54–60.

J.F. Wakerly, "Digital Design, Principles and Practices", pp. 255–257, Prentice Hall, 1989.

"Semiconductor Memories", B. Prince, 2nd Edition, pp. 31–39 and pp. 654–655, 1991.

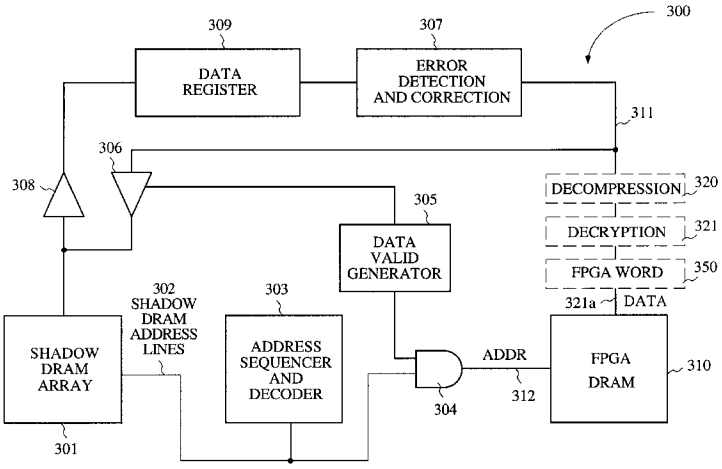
Primary Examiner—Jon Santamauro

Attorney, Agent, or Firm—Anthony C. Murabito; Wagner Murabito & Hao; Jeanette S. Harms

[57] **ABSTRACT**

A plurality of DRAM cells are used to store the state of the programmable points in a programmable logical device (e.g., a field programmable gate array or FPGA). An individual DRAM cell is used in conjunction with each programmable interconnect point (PIP) within the FPGA to hold a logical state indicating the connectivity state of the PIP. During a refresh cycle, each DRAM memory cell is loaded with its current logical state in order to maintain this state within the PIP. An information store contains duplicate data for each DRAM cell and this duplicate data is supplied and read during the refresh cycle in order to provide each DRAM cell with its proper logical state. In this manner, the refresh cycle does not alter the logic configuration of its associated FPGA DRAM cell. The information store can be a plurality of DRAM cells or the information store can be of non-volatile memory, for instance, read only memory (ROM), programmable ROM (PROM), erasable PROM (EPROM), electrically erasable PROM (EEPROM), or of non-volatile magnetic storage.

23 Claims, 5 Drawing Sheets



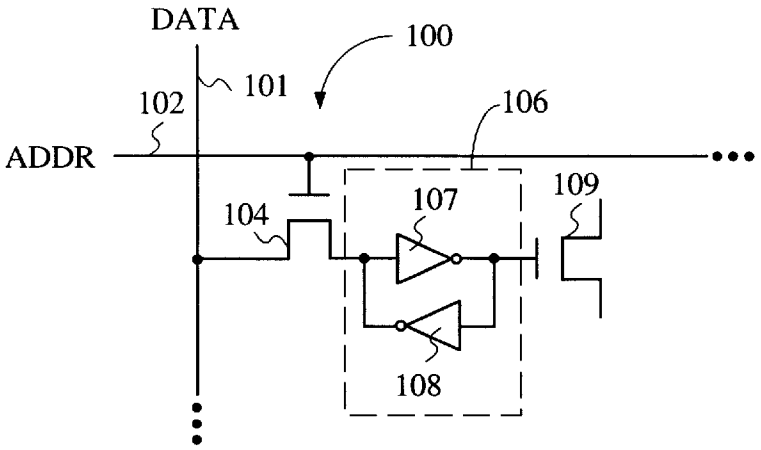


FIG. 1
PRIOR ART

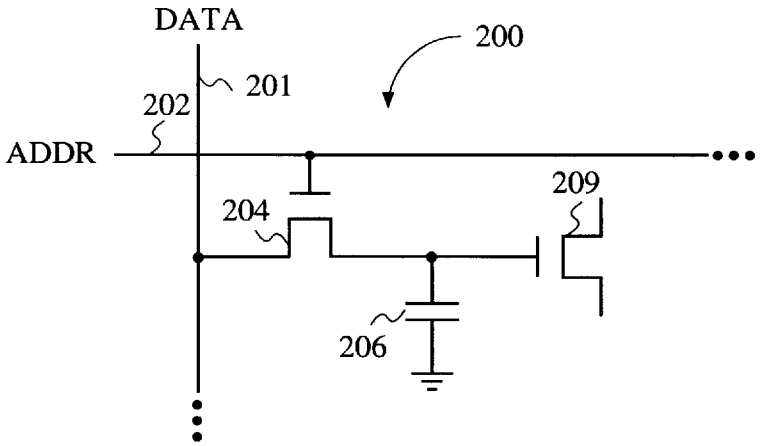


FIG. 2

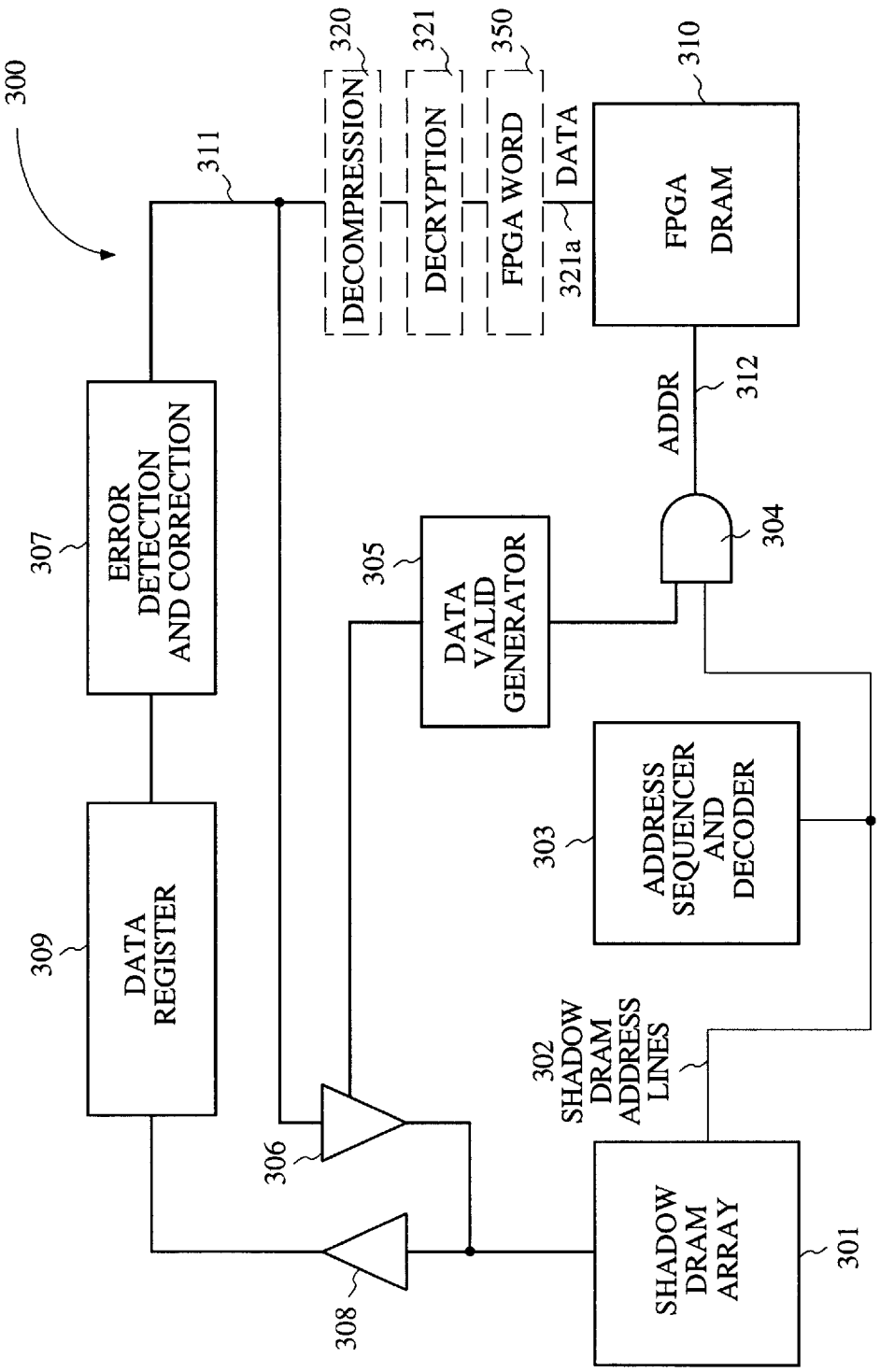


FIG. 3

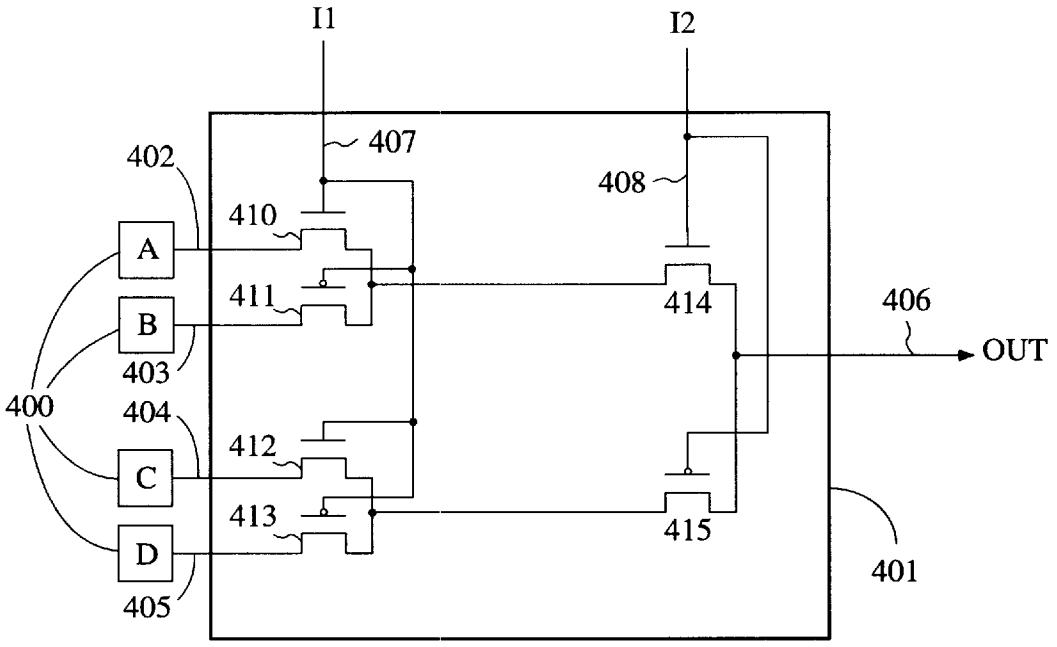


FIG. 4

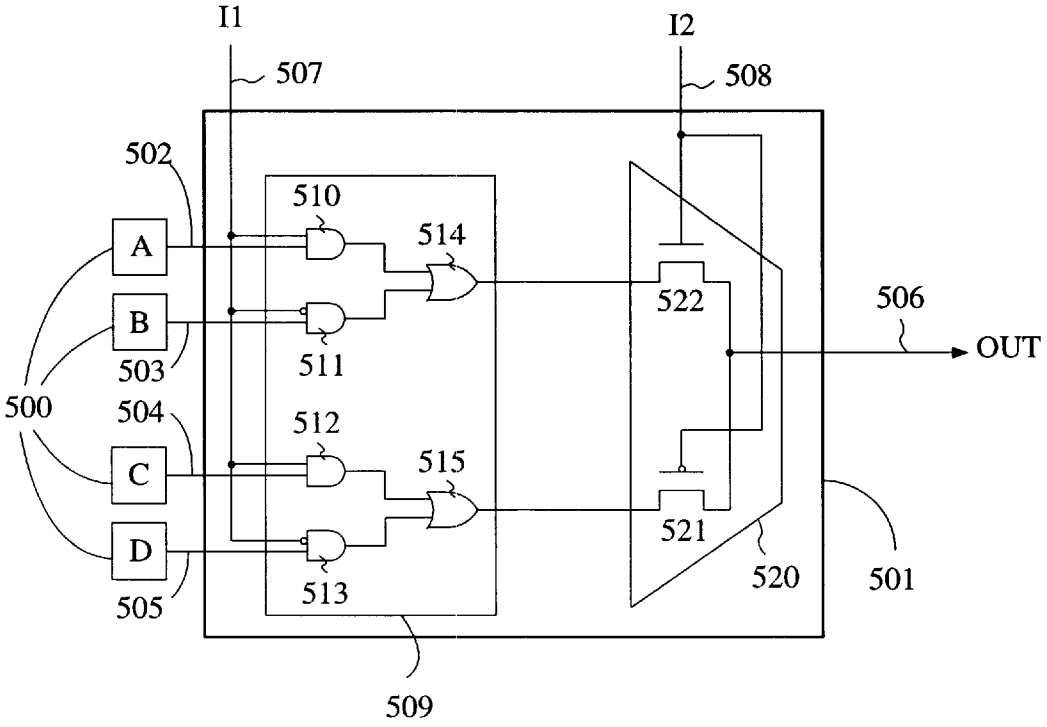


FIG. 5

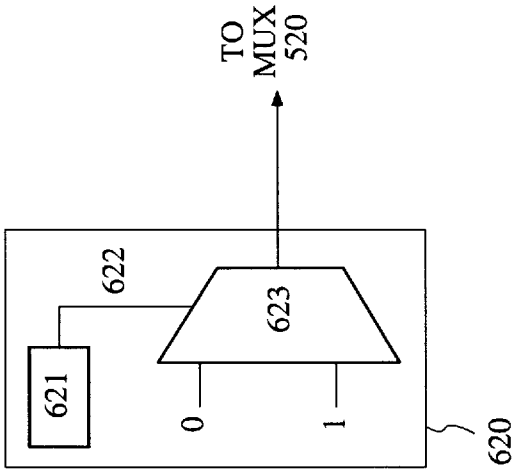


FIG. 6b

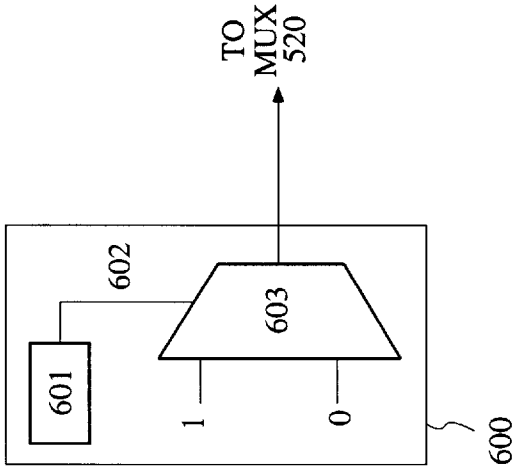


FIG. 6a

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.