Trials@uspto.gov
571-272-7822

Paper 20
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

FLEX LOGIX TECHNOLOGIES, INC.,
Petitioner,

v.

VENKAT KONDA,
Patent Owner.

IPR2020-00262
Patent 8,269,523 B2

Before SALLY C. MEDLEY, THOMAS L. GIANNETTI, and JO-ANNE M. KOKOSKI, *Administrative Patent Judges.*

GIANNETTI, *Administrative Patent Judge.*

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background

Flex Logic Technologies, Inc. ("Petitioner") filed a Petition requesting *inter partes* review of claims 1, 15–18, 20–22, 32, and 47 (the "challenged claims") of U.S. Patent No. 8,269,523 B2 (Ex. 1001, the "'523 patent"). Paper 1 ("Pet."). Patent Owner Venkat Konda filed a Preliminary Response. Paper 6 ("Prelim. Resp."). With our authorization, Petitioner filed a reply addressing certain issues raised in the Preliminary Response. Paper 10 ("Reply"). Also with our authorization, Patent Owner filed a Sur-reply. Paper 14 ("Sur-reply").

The standard for institution is set forth in 35 U.S.C. § 314, which provides that an *inter partes* review may not be instituted unless the information presented in the Petition and the Preliminary Response shows that "there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314; *see also* 37 C.F.R § 42.4(a) ("The Board institutes the trial on behalf of the Director.").

For the reasons that follow, we exercise our discretion under 35 U.S.C. § 325(d) and *deny* the Petition to institute *inter partes* review of the challenged claims of the '523 patent.

A. Related Proceedings

Petitioner identifies the following district court proceeding involving the '523 patent: *Konda Technologies Inc. v. Flex Logix Technologies, Inc.*, No. 5:18-cv-07581 (N.D. Cal.). Pet. 2.

In addition, the '523 patent is challenged by the Petitioner in two other *inter partes* reviews: IPR2020-00260 and IPR2020-00261. Pet. 3–4. Also, two post grant review proceedings brought by the Petitioner challenging a related patent (U.S. Patent No. 10,003,553) are pending: PGR2019-00037, and PGR2019-00042. *Id.* at 3. A third petition for post grant review of that related patent (PGR2019-00040) was denied. *Id.*

Patent Owner identifies also a pending application to reissue the '523 patent: U.S. Patent Application No. 16/202,067, filed November 27, 2018. Paper 4, 2.

B. Real Parties-in-Interest

Petitioner identifies Flex Logix Technologies, Inc. as the real party-in-interest. Pet. 2. Patent Owner identifies himself, Venkat Konda, as the real party-in-interest. Paper 4, 2.

C. The '523 Patent

The '523 patent is titled "VLSI Layouts of Fully Connected Generalized Networks." Ex. 1001, (54). According to the patent, multi-stage interconnection networks are widely useful in telecommunications, parallel and distributed computing. *Id.* at 2:25–27. However VLSI (Very Large Scale Integration) layouts, known in the prior art, of these interconnection networks in an integrated circuit are inefficient and complicated. *Id.* at 2:28–30.

The most commonly-used VLSI layout in an integrated circuit is based on a two-dimensional grid model comprising only horizontal and vertical tracks. *Id.* at 2:40–42. The '523 patent describes VLSI layouts of generalized multi-stage networks for broadcast, unicast, and multicast

connections using only horizontal and vertical links. *Id.* at 3:21–24. The VLSI layouts employ shuffle exchange links, where outlet links of cross links from switches in a stage in one sub-integrated circuit block are connected to inlet links of switches in the succeeding stage in another sub-integrated circuit block. *Id.* at 3:24–28. The cross links are either vertical links or horizontal, and vice versa. *Id.* at 3:28–29.

In one embodiment the sub-integrated circuit blocks are arranged in a hypercube arrangement in a two-dimensional plane. *Id.* at 3:29–31. The VLSI layouts exploit the benefits of significantly lower cross points, lower signal latency, lower power, and full connectivity with significantly fast compilation. *Id.* at 3:31–34.

D. Illustrative Claims

Claims 1, 15–18, 20–22, 32, and 47 are challenged in the Petition. *See supra*. Claim 1 is the only independent claim. Claim 1 recites:

> 1. An integrated circuit device comprising a plurality of sub-integrated circuit blocks and a routing network, and
>
> Said each plurality of sub-integrated circuit blocks comprising a plurality of inlet links and a plurality of outlet links; and
>
> Said routing network comprising of a plurality of stages y, in each said sub-integrated circuit block, starting from the lowest stage of 1 to the highest stage of y, where y≧1; and
>
> Said routing network comprising a plurality of switches of size d×d, where d≧2, in each said stage and each said switch of size d×d having d inlet links and d outlet links; and
>
> Said plurality of outlet links of said each sub-integrated circuit block are directly connected to said inlet links of said

switches of its corresponding said lowest stage of 1, and said plurality of inlet links of said each sub-integrated circuit block are directly connected from said outlet links of said switches of its corresponding said lowest stage of 1; and

Said each sub-integrated circuit block comprising a plurality of forward connecting links connecting from switches in a lower stage to switches in its immediate succeeding higher stage, and also comprising a plurality of backward connecting links connecting from switches in a higher stage to switches in its immediate preceding lower stage; and

Said each sub-integrated circuit block comprising a plurality straight links in said forward connecting links from switches in said each lower stage to switches in its immediate succeeding higher stage and a plurality cross links in said forward connecting links from switches in said each lower stage to switches in its immediate succeeding higher stage, and further comprising a plurality of straight links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage and a plurality of cross links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage,

said plurality of sub-integrated circuit blocks arranged in a two-dimensional grid of rows and columns, and

said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks which are either placed vertically above or below, or placed horizontally to the left or to the right,

each said plurality of sub-integrated circuit blocks comprising same number of said stages and said switches in each

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