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(12) **United States Patent**  
**Wong**

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(54) **INTERCONNECTION NETWORK FOR A FIELD PROGRAMMABLE GATE ARRAY**

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(73) Assignee: **Leopard Logic Inc.**, Cupertino, CA (US)

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **10/764,216**

(22) Filed: **Jan. 23, 2004**

(65) **Prior Publication Data**

US 2004/0150422 A1 Aug. 5, 2004

**Related U.S. Application Data**

(63) Continuation of application No. 09/923,294, filed on Aug. 3, 2001, now Pat. No. 6,693,456.

(60) Provisional application No. 60/223,047, filed on Aug. 4, 2000.

(51) **Int. Cl.**<sup>7</sup> ..... **H03K 19/173**; G06F 7/38

(52) **U.S. Cl.** ..... **326/41**; 326/38; 710/317

(58) **Field of Search** ..... 326/38, 39, 40, 326/41, 47; 710/317

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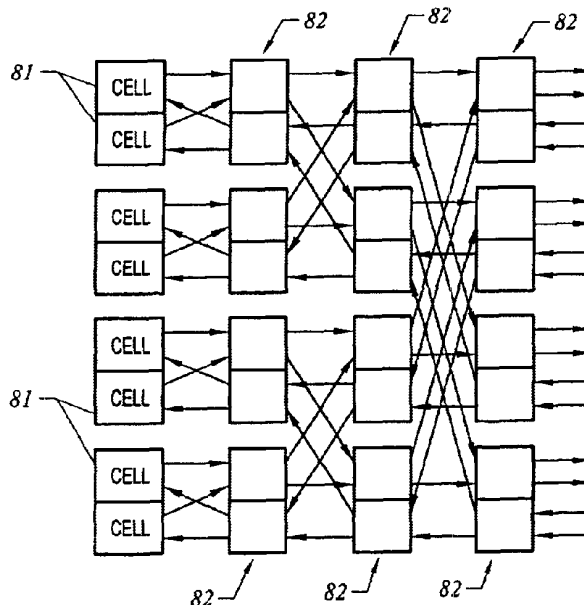
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(57) **ABSTRACT**

An interconnection network architecture which provides an interconnection network which is especially useful for FPGAs is described. Based upon Benes networks, the resulting network interconnect is rearrangeable so that routing between logic cell terminals is guaranteed. Upper limits on time delays for the network interconnect are defined and pipelining for high speed operation is easily implemented. The described network interconnect offers flexibility so that many design options are presented to best suit the desired application.

**5 Claims, 13 Drawing Sheets**



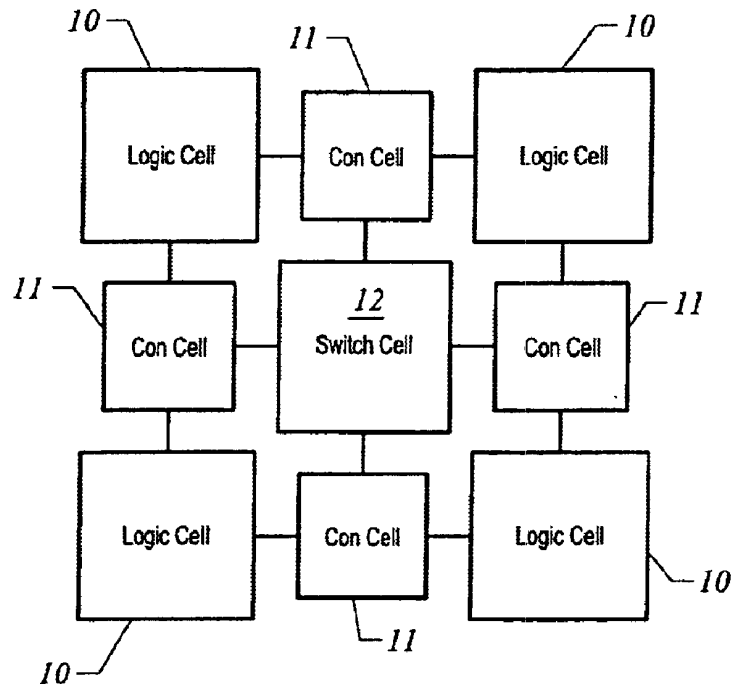


FIG. 1  
(Prior Art)

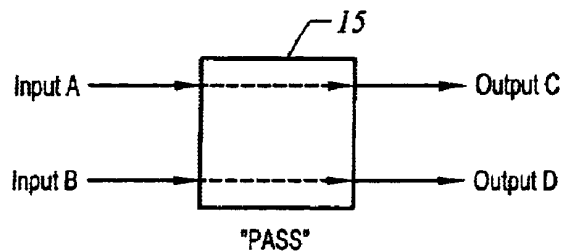


FIG. 2A

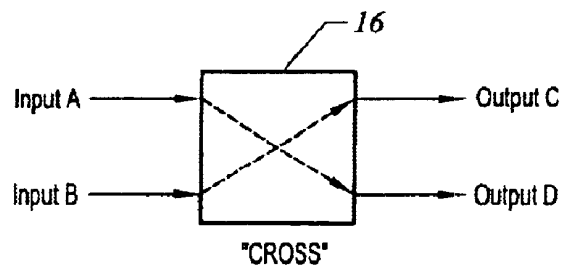


FIG. 2B

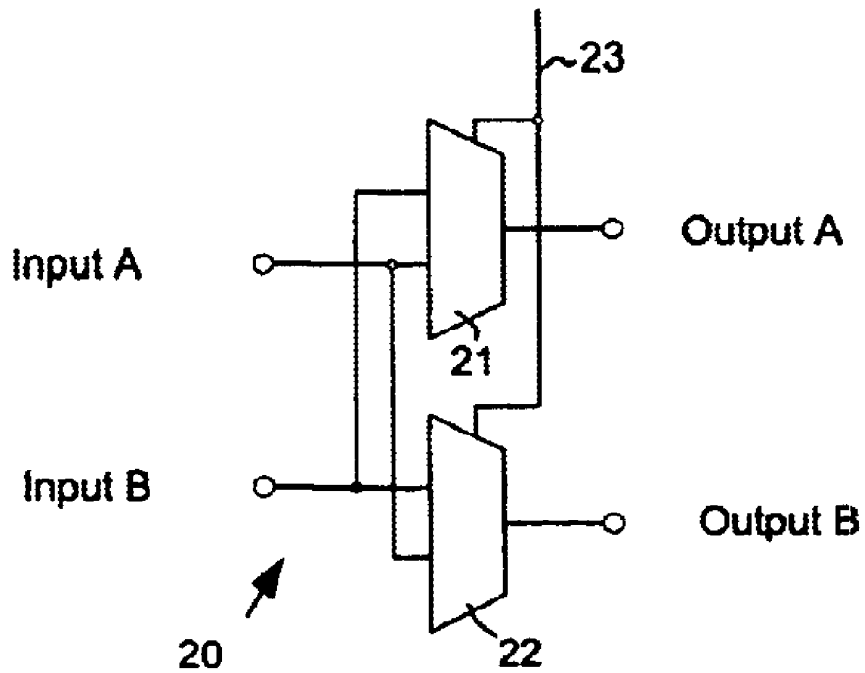


FIG. 2C

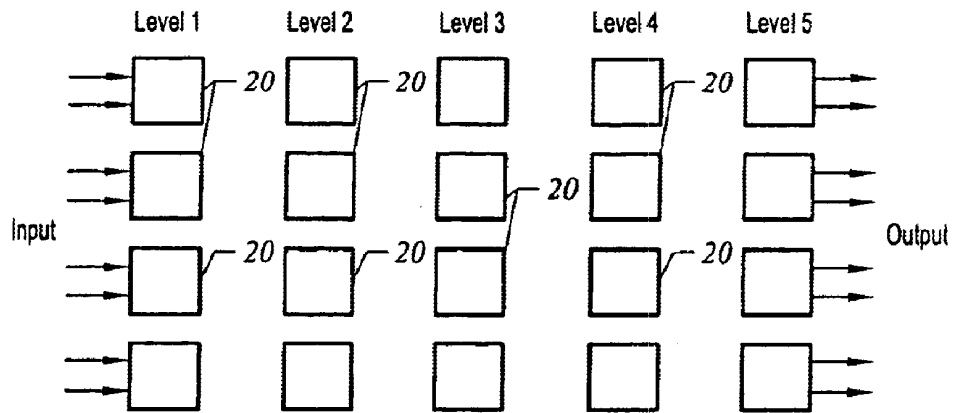


FIG. 3A

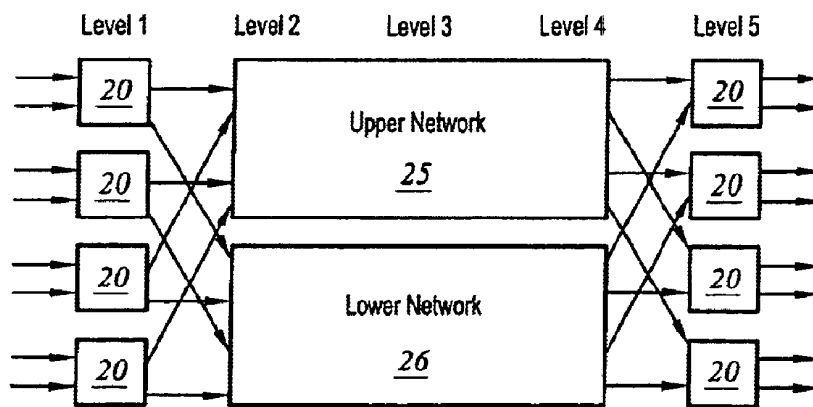


FIG. 3B

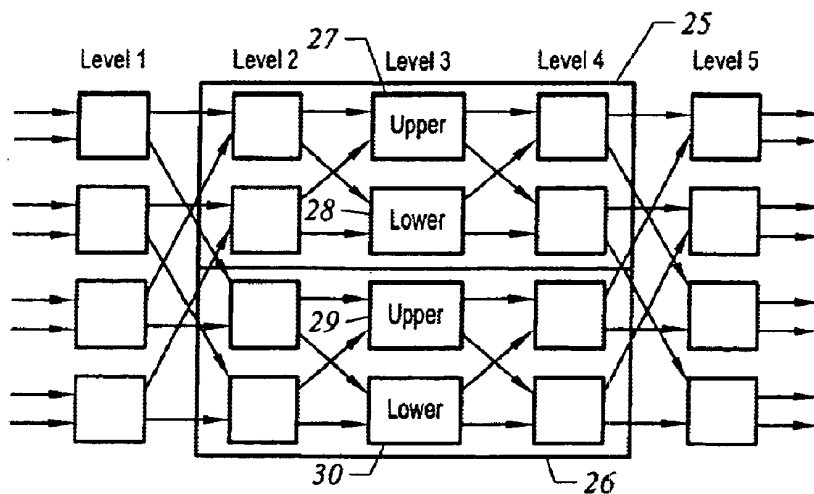


FIG. 3C

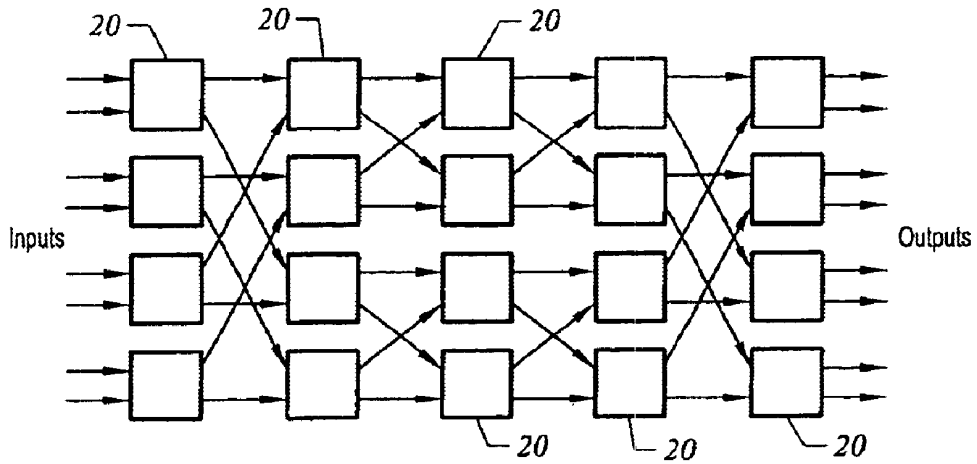


FIG. 3D

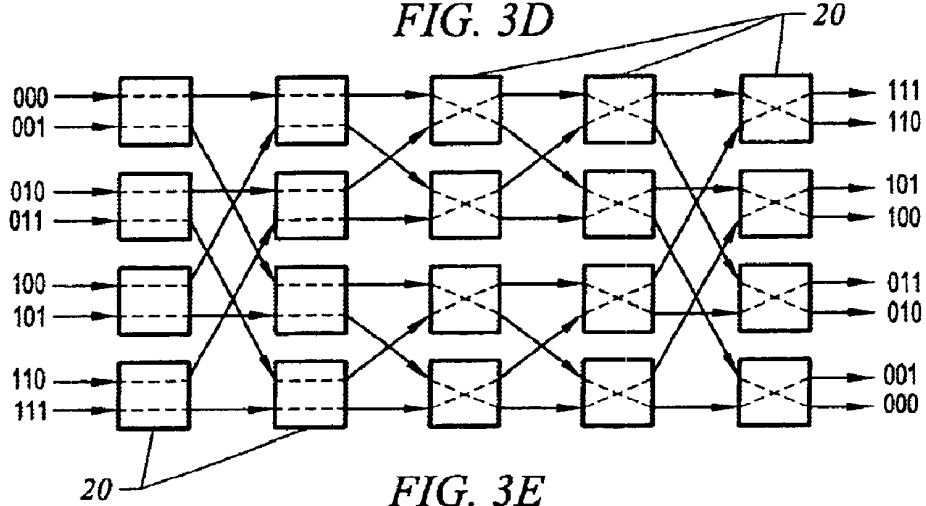


FIG. 3E

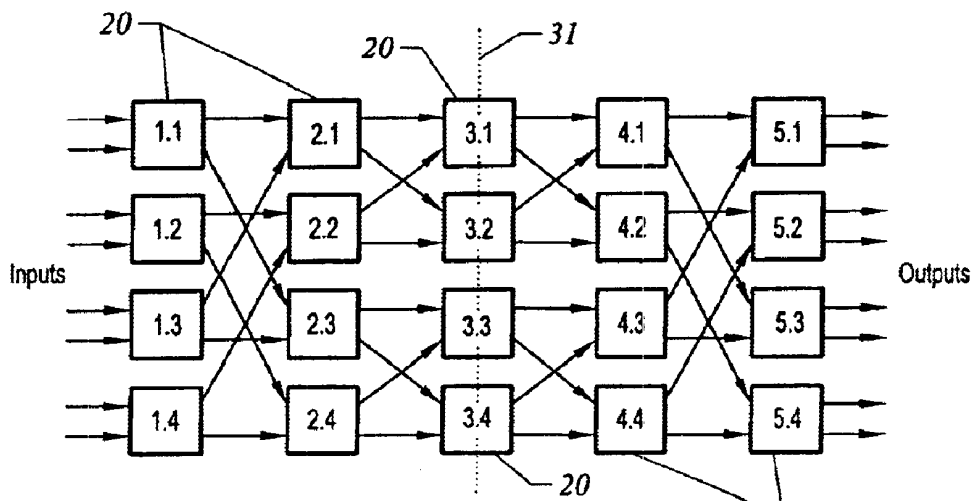


FIG. 4A

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