UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE CA 95135

MAILED

AUG 19 2019

INTERNATIONAL PATENT LEGAL ADM.

In re Application of :
KONDA, Venkat :
Application No.: 12/601,275 :
PCT No.: PCT/US08/64605 :
Int. Filing Date: 22 May 2008 : DECISION
Priority Date: 25 May 2007 :
Att. Doc. No.: V-0045US :
For: VLSI LAYOUTS OF FULLY :
CONNECTED GENERALIZED :
NETWORKS :

Applicant's Petition To Accept Late Payment of the Basic National Fee Under 37 CFR 1.137(a), filed in the above-captioned application on 08 August 2019 is **GRANTED**.

Applicant states that the entire delay in filing the required reply from the due date for the required reply until the filing of a grantable petition was unintentional. The proper response was previously filed on 22 December 2009. The petition fee has been furnished. A terminal disclaimer is not required as the application was filed on or after 08 June 1995. Accordingly, all requirements under 37 CFR 1.137(a) have been satisfied.

/Erin P. Thomson/
Erin P. Thomson
Attorney Advisor
International Patent Legal Administration
571-272-3292

In The United States Patent And Trademark Office

Application Number: 12/601,275 Application Filed: 11/22/2009

Applicant(s): Venkat Konda Patent No. 8,269,523

Title: VLSI Layouts of Fully Connected Generalized Networks Confirmation No: 6372

Examiner/Art Unit: Vibol Tan / 2819 Priority Date: 5/25/2007

San Jose, 2019 August 8

PETITION TO ACCPET LATE PAYMENT OF THE BASIC NATIONAL FEE UNDER 37 CFR 1.137

Attn: Richard Cole
Office of PCT Legal
Mail Stop PCT
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia, 22313-1450

Dear Sir/Madam:

For the above referenced application, please accept the payment of the basic national fee as being unintentionally delayed. The entire delay in filing the basic national fee from the due date for the fee until the filing of a grantable petition under 37 CFR 1.137 was unintentional. A check of $1000, the small entity fee, for this petition is enclosed.

Very respectfully,
/Venkat Konda/
Venkat Konda
6278 Grand Oak Way
San Jose, CA 95135
Phone: 408-472-3273

Electronic Patent Application Fee Transmittal

Application Number:	12601275
Filing Date:	31-May-2010
Title of Invention:	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Filer:	Venkat Konda
Attorney Docket Number:	V-0045US

Filed as Small Entity

Filing Fees for U.S. National Stage under 35 USC 371

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
PET. REVIVE ABANDON APP, DELAY PYMT-RESP	2453	1	1000	1000
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1000**

Electronic Acknowledgement Receipt

EFS ID:	36825423
Application Number:	12601275
International Application Number:	
Confirmation Number:	6372
Title of Invention:	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Customer Number:	38139
Filer:	Venkat Konda
Filer Authorized By:	
Attorney Docket Number:	V-0045US
Receipt Date:	08-AUG-2019
Filing Date:	31-MAY-2010
Time Stamp:	16:32:33
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1000
RAM confirmation Number	E201988G34075103
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Petition for review by the PCT legal office	PetUnintDelay-V0045US.pdf	75026 dc16c6a0f247024d21c0f54128af4f7c5e1ee3a0	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30076 f6cb27709e04fa0fb586944ee8732dc11110b06f	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	105102		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

In The United States Patent And Trademark Office

Application Number: 12/601,275 Application Filed: 11/22/2009

Applicant(s): Venkat Konda Patent No. 8,269,523

Title: VLSI Layouts of Fully Connected Generalized Networks Confirmation No: 6372

Examiner/Art Unit: Vibol Tan / 2819 Priority Date: 5/25/2007

San Jose, 2019 August 8

PETITION TO ACCPET LATE PAYMENT OF THE BASIC NATIONAL FEE UNDER 37 CFR 1.137

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Very respectfully,
/Venkat Konda/
Venkat Konda
6278 Grand Oak Way
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Phone: 408-472-3273

Electronic Patent Application Fee Transmittal

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First Named Inventor/Applicant Name:	Venkat Konda
Filer:	Venkat Konda
Attorney Docket Number:	V-0045US

Filed as Small Entity

Filing Fees for U.S. National Stage under 35 USC 371

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
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Claims:				
Miscellaneous-Filing:				
Petition:				
PET. REVIVE ABANDON APP, DELAY PYMT-RESP	2453	1	1000	1000
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1000**

Electronic Acknowledgement Receipt

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Application Number:	12601275
International Application Number:	
Confirmation Number:	6372
Title of Invention:	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Customer Number:	38139
Filer:	Venkat Konda
Filer Authorized By:	
Attorney Docket Number:	V-0045US
Receipt Date:	08-AUG-2019
Filing Date:	31-MAY-2010
Time Stamp:	15:45:01
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Petition for review by the PCT legal office	PetUnintDelay-V0045US.pdf	75026 dc16c6a0f247024d21c0f54128af4f7c5e1ee3a0	no	1

Warnings:

Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30076 b3624d1e735fe33fb3715c72a18b578c53b67b5d	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	105102	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

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PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT5474857

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
KONDA TECHNOLOGIES INC.	04/15/2019

RECEIVING PARTY DATA

Name:	VENKAT KONDA
Street Address:	6278 GRAND OAK WAY
City:	SAN JOSE
State/Country:	CALIFORNIA
Postal Code:	95135

PROPERTY NUMBERS Total: 2

Property Type	Number
Patent Number:	8269523
Application Number:	16202067

CORRESPONDENCE DATA

Fax Number: (408)238-2478

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 4084723273
Email: venkat@kondatech.com
Correspondent Name: KONDA TECHNOLOGIES INC.
Address Line 1: 6278 GRAND OAK WAY
Address Line 4: SAN JOSE, CALIFORNIA 95135

NAME OF SUBMITTER:	VENKAT KONDA
SIGNATURE:	/venkat Konda/
DATE SIGNED:	04/15/2019
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 2
source=Konda-pat-exe#page1.tif
source=Konda-pat-exe#page2.tif

ASSIGNMENT OF PATENTS

WHEREAS, Konda Technologies, Inc., a California corporation, located at 6278 Grand Oak Way, San Jose, CA 95135, hereinafter referred to as "Assignor," is the record owner of the patents described as

1) Title: VLSI Layouts of Fully Connected Generalized Networks
US Patent No.: 8,269,523
Patent Issue Date: September 18, 2012;

2) Title: VLSI Layouts of Fully Connected Generalized Networks
US Patent Application No.: 16/202,067
Patent Filing Date: November 27, 2018;

WHEREAS, Konda, Venkat of San Jose, California, having a residence at 6278 Grand Oak Way, San Jose, CA, hereinafter referred to as "ASSIGNEE," wishes to acquire all right, title and interest to and under the patents described above owned by Assignor and in and to any and all improvements to said applications and in any Letters Patent and Registrations which may be granted on the same in the United States or any country throughout the world;

For good and valuable consideration, receipt of which is hereby acknowledged by Assignor, effective 15th day of April, 2019, has assigned, and by these presents does assign to Assignee all right, title and interest for the United States and all foreign countries, in and to any and all improvements for the applications described above and in and to said applications and to all utility divisional continuing, substitute, renewal, reissue, and all other patent applications which have been or shall be filed in the United States and all foreign counterparts (including patent, utility model and industrial designs), and in and to any Letters Patent and Registrations which may hereafter be granted on the same in the United States and all countries throughout the world, and to claim the priority from the application as provided by the Paris Convention. The right, title and interest is to be held and enjoyed by Assignee and Assignee's successors and assigns as fully and exclusively as it would have been held and enjoyed by Assignor had this Assignment not been made, for the full term of any Letters Patent and Registrations which may be granted thereon, or of any division, renewal, continuation in whole or in part, substitution, conversion, reissue, prolongation or extension thereof.

Assignor further agrees that they will, without charge to Assignee, but at Assignee's expense, (a) cooperate with Assignee in the prosecution of U.S. Patent applications and foreign counterparts on the applications and any improvements, (b) execute, verify, acknowledge and deliver all such further papers, including patent applications and instruments of transfer, and (c) perform such other acts as Assignee lawfully may request to obtain or maintain Letters Patent and Registrations for the applications and improvements in any and all countries, and to vest title thereto in Assignee, or Assignee's successors and assigns.

IN TESTIMONY WHEREOF, Assignor has signed on the date indicated.

Date: 4/15/2019 By: Venkat Konda

Venkat Konda (Founder/CEO)
Konda Technologies Inc.
6278 Grand Oak Way
San Jose, CA 95135

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/601,275	09/18/2012	8269523	V-0045US	6372

38139 7590 08/29/2012

Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 183 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Venkat Konda, San Jose, CA;

Change(s) applied to document, /D.H.P./ 6/29/2012

This application is related to and incorporates by reference in its entirety the US Patent Application 12/601273 ~~Docket No. V-0038US~~ entitled "FULLY CONNECTED GENERALIZED BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application filed concurrently, the PCT Application Serial No. PCT/US08/64603 entitled "FULLY CONNECTED GENERALIZED BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 22, 2008, the U.S. Provisional Patent Application Serial No. 60/940, 387 entitled "FULLY CONNECTED GENERALIZED BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007, and the U.S. Provisional Patent Application Serial No. 60/940, 390 entitled "FULLY CONNECTED GENERALIZED MULTI-LINK BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

This application is related to and incorporates by reference in its entirety the US Patent Application 12/601274 ~~Docket No. V-0039US~~ entitled "FULLY CONNECTED GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application filed concurrently, the PCT Application Serial No. PCT/US08/64604 entitled "FULLY CONNECTED GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 22, 2008, the U.S. Provisional Patent Application Serial No. 60/940, 389 entitled "FULLY CONNECTED GENERALIZED REARRANGEABLY NONBLOCKING MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007, the U.S. Provisional Patent Application Serial No. 60/940, 391 entitled "FULLY CONNECTED GENERALIZED FOLDED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007 and the U.S. Provisional Patent Application Serial No. 60/940, 392 entitled "FULLY CONNECTED GENERALIZED STRICTLY NONBLOCKING MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/601,275	5/31/2010	Venkat Konda	V-0045US	6372

TITLE OF INVENTION:

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$870	$300	$1170	8/17/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1_

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2_ 3_

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE	(B) RESIDENCE: (CITY and STATE OR COUNTRY)
Konda Technologies Inc.	San Jose, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

☑ Issue Fee

☑ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _

4b. Payment of Fee(s):

☐ A check in the amount of the fee(s) is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized to charge the required fee(s), or credit any overpayment, to Deposit Account Number .

5. **Change in Entity Status** (from status indicated above)

☑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Venkat Konda/ Date 8/15/2012

Typed or printed name Venkat Konda Registration No.

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	12601275
Filing Date:	31-May-2010
Title of Invention:	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Filer:	Venkar Konda
Attorney Docket Number:	V-0045US

Filed as Small Entity

U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Publ. Fee- early, voluntary, or normal	1504	1	300	300
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	2501	1	870	870

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1170**

Electronic Acknowledgement Receipt

EFS ID:	13505897
Application Number:	12601275
International Application Number:	
Confirmation Number:	6372
Title of Invention:	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Customer Number:	38139
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Filer Authorized By:	
Attorney Docket Number:	V-0045US
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Time Stamp:	16:44:45
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1170
RAM confirmation Number	3603
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Issue Fee Payment (PTO-85B)	ptol85b-V0045US.pdf	223614 d28167872396a8b938daef41e9e9f2f113d9568	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	31848 0d3037333ad300df6fcb48c6df4c5fc1941faee5	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	255462	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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NOTICE OF ALLOWANCE AND FEE(S) DUE

38139 7590 05/17/2012

Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

EXAMINER
TAN, VIBOL

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 05/17/2012

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/601,275	05/31/2010	Venkat Konda	V-0045US	6372

TITLE OF INVENTION: VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$870	$300	$0	$1170	08/17/2012

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

38139 7590 05/17/2012

Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/601,275	05/31/2010	Venkat Konda	V-0045US	6372

TITLE OF INVENTION: VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$870	$300	$0	$1170	08/17/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
TAN, VIBOL	2819	326-041000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/601,275	05/31/2010	Venkat Konda	V-0045US	6372

38139 7590 05/17/2012

Konda Technologies, Inc
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EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 05/17/2012

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 183 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 183 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/601,275	KONDA, VENKAT	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed 5/8/12*.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1 and 3-49*.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Allowable Subject Matter

1. The following is an examiner's statement of reasons for allowance: in combination with other limitations of the claims, the cited prior arts fail to teach said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks which are either placed vertically above or below, or placed horizontally to the left or to the right, each said plurality of sub-integrated circuit blocks comprising same number of said stares and said switches in each said stage, regardless of the size of said two-dimensional grid so that each said plurality of sub-integrated circuit block with its corresponding said stages and said switches in each stage is replicable in both vertical direction or horizontal direction of said two-dimensional grid, as required by amended claim 1.

2. Claims 1 and 3-49 are now in condition for allowance.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571)272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shawki Ismail can be reached on (571) 272-3985. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Vibol Tan/
Primary Examiner, Art Unit 2819

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BIB DATA SHEET

CONFIRMATION NO. 6372

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/601,275	05/31/2010	326	2819	V-0045US

APPLICANTS
Venkat Konda, San Jose, CA;

**** CONTINUING DATA ***************************
This application is a 371 of PCT/US08/64605 05/22/2008
which claims benefit of 60/940,394 05/25/2007

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **** ** SMALL ENTITY **
04/08/2010

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /VIBOL TAN/ Examiner's Signature	☐ Met after Allowance VTan Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	39	49	1

ADDRESS
Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135
UNITED STATES

TITLE
VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS

FILING FEE RECEIVED		
1279	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S25	35	(US-20080267182-$ or US-20040114586-$ or US-20030021267-$ or US-20030112797-$ or US-20030053456-$ or US-20020051447-$ or US-20020031118-$ or US-20020031117-$).did. or (US-8098081-$ or US-7924052-$ or US-7468974-$ or US-7424011-$ or US-7424010-$ or US-7397796-$ or US-7349387-$ or US-7346049-$ or US-7130920-$ or US-6567858-$ or US-7136380-$ or US-6456838-$ or US-6157643-$ or US-6049542-$ or US-5856977-$ or US-5406556-$ or US-4813038-$ or US-7139266-$ or US-7103059-$ or US-7099314-$ or US-7065074-$ or US-7050429-$ or US-7042873-$ or US-7031303-$ or US-7016345-$ or US-6952418-$).did. or (US-6201808-$).did.	US-PGPUB; USPAT	OR	OFF	2012/05/08 15:44
S26	42	konda-venkat.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/05/08 15:44
S27	84	(routing adj network) and (multicast adj connections)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/05/08 15:58
S28	1365	(routing adj network) and (inputs) and (outputs)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/05/08 15:59
S29	229142	(("326") or ("370")).CLAS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/05/08 15:59
S30	693	S28 and S29	US-PGPUB; USPAT; USOCR; FPRS;	OR	OFF	2012/05/08 15:59

			EPO; JPO; DERWENT; IBM_TDB			
S31	380	S30 and links	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/05/08 16:00
S32	1	S30 and (straight adj links) and (vertical adj links) and (horizontal adj links)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/05/08 16:01
S33	1	((straight adj links) and (vertical adj links) and (horizontal adj links)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/05/08 16:02

EAST Search History (Interference)

<This search history is empty>

5/ 10/ 2012 7:09:30 AM
C:\ Users\ vtan\ Documents\ EAST\ Workspaces\ 12601275.wsp

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12601275	KONDA, VENKAT
	Examiner	Art Unit
	VIBOL TAN	2819

SEARCHED			
Class	Subclass	Date	Examiner
326	38-41	2/2/12	VTan
370	390, 312, 360, 388, 412	2/2/12	VTan

SEARCH NOTES		
Search Notes	Date	Examiner
Inventor search	2/2/12	VTan
search report pct/us2008/064605	2/1/12	VTan
EAST text search	2/2/12	VTan
EAST text update	5/8/12	VTan

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
uspgpub, uspat & upad	text search	5/8/12	VTan

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12601275	KONDA, VENKAT
	Examiner	**Art Unit**
	VIBOL TAN	2819

ORIGINAL		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
326	41	H 0 3 K 19 / 177 (2006.01)	

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
326	38				

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	16	17	32	33	48	49								
	2	17	18	33	34										
2	3	18	19	34	35										
3	4	19	20	35	36										
4	5	20	21	36	37										
5	6	21	22	37	38										
6	7	22	23	38	39										
7	8	23	24	39	40										
8	9	24	25	40	41										
9	10	25	26	41	42										
10	11	26	27	42	43										
11	12	27	28	43	44										
12	13	28	29	44	45										
13	14	29	30	45	46										
14	15	30	31	46	47										
15	16	31	32	47	48										

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	48	
/VIBOL TAN/ Primary Examiner.Art Unit 2819	05/10/2012	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1c

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12601275	KONDA, VENKAT
	Examiner	Art Unit
	VIBOL TAN	2819

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/08/2012								
	1	=								
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CLAIM		DATE								
Final	Original	05/08/2012								
	37	=								
	38	=								
	39	=								
	40	=								
	41	=								
	42	=								
	43	=								
	44	=								
	45	=								
	46	=								
	47	=								
	48	=								

In The United States Patent And Trademark Office

Application Number: 12/601,275

Application Filed: 11/22/2009

Applicant(s): Venkat Konda

Title: VLSI Layouts of Fully Connected Generalized Networks

Examiner/Art Unit: Vibol Tan / 2819

International Application Number: PCT/US08/64605

International Application Filed: 5/22/2008

Priority Date: 5/25/2007

San Jose, 2012 May 8, Tue

SUPPLEMENTAL AMENDMENT

(and the response to office letter dated 2/7/2012)

Mail Stop Amendment

Commissioner for Patents

P.O. Box 1450

Alexandria, Virginia, 22313-1450

Dear Sir/Madam:

In response to the office action mailed 2012 February 7, Applicant has submitted Amendment A on April 30, 2012. In the Amendment A filed on April 30, 2012,

Applicant has made mistakes with the format of the claims and not identifying the cancelled claim. To correct those mistakes, please consider the following Supplemental Amendment.

5 AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

CLAIMS

What is claimed is:

1. (currently amended): An integrated circuit device comprising a plurality of sub-integrated circuit blocks and a routing network, and

Said each plurality of sub-integrated circuit blocks comprising a plurality of inlet links and a plurality of outlet links; and

~~Said routing network interconnects any one of said outlet link of one of said sub-integrated circuit block to one or more said inlet links of one or more of said sub-integrated circuit blocks; and~~

Said routing network comprising of a plurality of stages y, in each said sub-integrated circuit block, starting from the lowest stage of 1 to the highest stage of y, where $y \geq 1$; and

Said routing network comprising a plurality of switches of size $d \times d$, where $d \geq 2$, in each said stage and each said switch of size $d \times d$ having d inlet links and d outlet links; and

~~Said each sub-integrated circuit block comprising a plurality of said switches corresponding to each said stage; and~~

Said plurality of outlet links of said each sub-integrated circuit block are directly connected to said inlet links of said switches of its corresponding said lowest stage of 1, and said plurality of inlet links of said each sub-integrated circuit block are directly connected from said outlet links of said switches of its corresponding said lowest stage of 1; and

Said each sub-integrated circuit block comprising a plurality of forward connecting links connecting from switches in a lower stage to switches in ~~the~~ its immediate succeeding higher stage, and also comprising a plurality of backward connecting links connecting from switches in a higher stage to switches in ~~the~~ its immediate preceding lower stage; and

Said each sub-integrated circuit block comprising a plurality straight links in said forward connecting links from switches in said each lower stage to switches in ~~the~~ its immediate succeeding higher stage and a plurality cross links in said forward connecting links from switches in said each lower stage to switches in ~~the~~ its immediate succeeding higher stage, and further comprising a plurality of straight links in said backward connecting links from switches in said each higher stage to switches in ~~the~~ its immediate preceding lower stage and a plurality of cross links in said backward connecting links from switches in said each higher stage to switches in ~~the~~ its immediate preceding lower stage,

said plurality of sub-integrated circuit blocks arranged in a two-dimensional grid of rows and columns, and

said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks which are either placed vertically above or below, or placed horizontally to the left or to the right,

each said plurality of sub-integrated circuit blocks comprising same number of said stages and said switches in each said stage, regardless of the size of said two-dimensional grid so that each said plurality of sub-integrated circuit block with its corresponding said stages and said switches in each stage is replicable in both vertical direction or horizontal direction of said two-dimensional grid.

2. (cancelled): ~~The integrated circuit device of claim 1, wherein said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and~~

~~said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks.~~

3. (currently amended): The integrated circuit device of claim 1, ~~wherein said plurality of sub-integrated circuit blocks arranged in a two-dimensional grid~~

said two-dimensional grid of said sub-integrated circuit blocks with their corresponding said stages and said switches in each stage is scalable by any power of 2, and,

for each multiplication of 2 of the size of total said sub-integrated circuit blocks, by adding one more stage of switches and the layout is placed in hypercube format and also the cross links between said one more stage of switches are connected in hypercube format.

4. (Original): The integrated circuit device of claim 3, wherein said cross links in succeeding stages are connecting as alternative vertical and horizontal links between switches in said sub-integrated circuit blocks.

5. (Original): The integrated circuit device of claim 4, wherein said cross links from switches in a stage in one of said sub-integrated circuit blocks are connecting to switches in the succeeding stage in another of said sub-integrated circuit blocks so that said cross links are either vertical links or horizontal and vice versa, and hereinafter such cross links are "shuffle exchange links").

6. (Original): The integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are substantially of equal length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are substantially of equal length in the entire said integrated circuit device.

7. (Original): The integrated circuit device of claim 6, wherein the shortest horizontal shuffle exchange links are connecting at the lowest stage and between switches in two nearest neighboring said sub-integrated circuit blocks, and length of the horizontal shuffle exchange links is doubled in each succeeding stage; and the shortest vertical shuffle exchange links are connecting at the lowest stage and between switches in two nearest neighboring said sub-integrated circuit blocks, and length of the vertical shuffle exchange links is doubled in each succeeding stage.

8. (currently amended): The integrated circuit device of claim 7, wherein $y \geq (\log_2 N)$, where $N > 1$, so that the length of the horizontal shuffle exchange links in the highest stage is equal to half the size of the horizontal size of said two dimensional grid of sub-integrated circuit blocks and the length of the vertical shuffle exchange links in the highest stage is equal to half the size of the vertical size of said two dimensional grid of sub-integrated circuit blocks.

9. (Original): The integrated circuit device of claim 8, wherein $d = 2$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast Benes network with full bandwidth.

10. (Original): The integrated circuit device of claim 8, wherein $d = 2$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast Benes network and rearrangeably nonblocking for arbitrary fan-out multicast Benes network with full bandwidth.

11. (Original): The integrated circuit device of claim 8, wherein $d = 2$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast Benes network with full bandwidth.

12. (currently amended): The integrated circuit device of claim 7, wherein $y \geq (\log_2 N)$, where $N > 1$, so that the length of the horizontal shuffle exchange links in the highest stage is equal to half the size of the horizontal size of said two dimensional grid of sub-integrated circuit blocks and the length of the vertical shuffle exchange links

in the highest stage is equal to half the size of the vertical size of said two dimensional grid of sub-integrated circuit blocks, and

said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks.

13. (Original): The integrated circuit device of claim 12, wherein $d = 2$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast butterfly fat tree network with full bandwidth.

14. (Original): The integrated circuit device of claim 12, wherein $d = 2$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast butterfly fat tree network and rearrangeably nonblocking for arbitrary fan-out multicast butterfly fat tree network with full bandwidth.

15. (Original): The integrated circuit device of claim 12, wherein $d = 2$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast butterfly fat tree network with full bandwidth.

16. (Original): The integrated circuit device of claim 1, wherein said horizontal and vertical links are implemented on two or more metal layers.

17. (Original): The integrated circuit device of claim 1, wherein said switches comprising active and reprogrammable cross points and said each cross point is programmable by an SRAM cell or a Flash Cell.

18. (Original): The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks are of equal die size.

19. (Original): The integrated circuit device of claim 16, wherein said sub-integrated circuit blocks are Lookup Tables (hereinafter "LUTs") and said integrated circuit device is a field programmable gate array (FPGA) device or field programmable gate array (FPGA) block embedded in another integrated circuit device.

20. (Original): The integrated circuit device of claim 16, wherein said sub-integrated circuit blocks are AND or OR gates and said integrated circuit device is a programmable logic device (PLD).

21. (Original): The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks comprising any arbitrary hardware logic or memory circuits.

22. (Original): The integrated circuit device of claim 1, wherein said switches comprising active one-time programmable cross points and said integrated circuit device is a mask programmable gate array (MPGA) device or a structured ASIC device.

23. (Original): The integrated circuit device of claim 1, wherein said switches comprising passive cross points or just connection of two links or not and said integrated circuit device is a Application Specific Integrated Circuit (ASIC) device.

24. (Original): The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks further recursively comprise one or more super-sub-integrated circuit blocks and a sub-routing network.

25. (currently amended): The integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said

succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and $y \geq (\log_2 N)$, where $N > 1$.

26. (Original): The integrated circuit device of claim 25, wherein $d = 2$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized multi-stage network with full bandwidth.

27. (Original): The integrated circuit device of claim 25, wherein $d = 2$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized multi-stage network and rearrangeably nonblocking for arbitrary fan-out multicast generalized multi-stage network with full bandwidth.

28. (Original): The integrated circuit device of claim 25, wherein $d = 2$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized multi-stage network with full bandwidth.

29. (currently amended): The integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and $y \geq (\log_2 N)$, where $N > 1$, and

said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks.

30. (Original): The integrated circuit device of claim 29, wherein $d = 2$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized butterfly fat tree network with full bandwidth.

31. (Original): The integrated circuit device of claim 29, wherein $d = 2$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized butterfly fat tree Network and rearrangeably nonblocking for arbitrary fan-out multicast generalized butterfly fat tree network with full bandwidth.

32. (Original): The integrated circuit device of claim 29, wherein $d = 2$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized butterfly fat tree network with full bandwidth.

33. (Original): The integrated circuit device of claim 1, wherein said straight links connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and

said cross links are connecting as vertical or horizontal or diagonal links between two different said sub-integrated circuit blocks.

34. (Original): The integrated circuit device of claim 8, wherein $d = 4$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and

said routing network is rearrangeably nonblocking for unicast multi-link Benes network with full bandwidth.

35. (Original): The integrated circuit device of claim 8, wherein $d = 4$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast multi-link Benes network and rearrangeably nonblocking for arbitrary fan-out multicast multi-link Benes network with full bandwidth.

36. (Original): The integrated circuit device of claim 8, wherein $d = 4$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast multi-link Benes network with full bandwidth.

37. (Original): The integrated circuit device of claim 12, wherein $d = 4$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast multi-link butterfly fat tree network with full bandwidth.

38. (Original): The integrated circuit device of claim 12, wherein $d = 4$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast multi-link butterfly fat tree network and rearrangeably nonblocking for arbitrary fan-out multicast multi-link butterfly fat tree network with full bandwidth.

39. (Original): The integrated circuit device of claim 12, wherein $d = 4$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast multi-link butterfly fat tree network with full bandwidth.

40. (currently amended): The integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and $y \geq (\log_2 N)$, where $N > 1$.

41. (Original): The integrated circuit device of claim 40, wherein $d = 4$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized multi-link multi-stage network with full bandwidth.

42. (Original): The integrated circuit device of claim 40, wherein $d = 4$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized multi-link multi-stage network and rearrangeably nonblocking for arbitrary fan-out multicast generalized multi-link multi-stage network with full bandwidth.

43. (Original): The integrated circuit device of claim 40, wherein $d = 4$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links

and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized multi-link multi-stage network with full bandwidth.

44. (currently amended): The integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and $y \geq (\log_2 N)$, where $N > 1$, and

said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks.

45. (Original): The integrated circuit device of claim 44, wherein $d = 4$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized multi-link butterfly fat tree network with full bandwidth.

46. (Original): The integrated circuit device of claim 44, wherein $d = 4$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized multi-link butterfly fat tree Network and rearrangeably nonblocking for arbitrary fan-out multicast generalized multi-link butterfly fat tree network with full bandwidth.

47. (Original): The integrated circuit device of claim 44, wherein $d = 4$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized multi-link butterfly fat tree network with full bandwidth.

48. (currently amended): The integrated circuit device of claim 1, wherein said plurality of forward connecting links use a plurality of buffers to amplify signals driven through them and said plurality of backward connecting links use a plurality of buffers to amplify signals driven through them; and said buffers can be inverting or non-inverting buffers.

49. (currently amended): The integrated circuit device of claim 1, wherein said ~~wherein said~~ all switches of size $d \times d$ are either fully populated or partially populated.

CONCLUSION

For all of the above reasons, applicant submits that the Claims are now in proper form, and that the Claims all define patentably over the prior art. Therefore applicant submits that this application is now in condition for allowance, which action he respectfully solicits.

Conditional request for Constructive Assistance

Applicant has amended the claims of this application so that they are proper, definite, and define novel structure which is also unobvious. If, for any reason this application is not believed to be in full condition for allowance, applicant respectfully request the constructive assistance and suggestions of the Examiner pursuant to M.P.E.P § 2173.02 and § 707.07(j) in order that the undersigned can place this application in allowable condition as soon as possible and without the need for further proceedings.

Very respectfully,

/Venkat Konda/

Venkat Konda

Konda Technologies, Inc (USPTO Customer Number: 38139)

6278 Grand Oak Way

San Jose, CA 95135

Phone: 408-472-3273

Fax: 408-238-2478

Electronic Acknowledgement Receipt

EFS ID:	12733551
Application Number:	12601275
International Application Number:	
Confirmation Number:	6372
Title of Invention:	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Customer Number:	38139
Filer:	Venkar Konda
Filer Authorized By:	
Attorney Docket Number:	V-0045US
Receipt Date:	08-MAY-2012
Filing Date:	31-MAY-2010
Time Stamp:	22:22:15
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Supplemental Response or Supplemental Amendment	SuppleAmend-V0045US.pdf	144109 3e7bd4b5740546aeb12e5e0cfd93e5979edc5277	no	15

Warnings:	
Information:	

Total Files Size (in bytes):	144109

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/601,275	05/31/2010	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☒ RATE ($)	SMALL ENTITY ☒ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 05/08/2012	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 48	Minus	** 49	= 0	X $30 =	0	OR	X $ =	
Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $125 =	0	OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE	0	OR	TOTAL ADD'L FEE	

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/STELLA LITTLE/

PTO/SB/06 (07-06)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/601,275	Filing Date 05/31/2010	☐ To be Mailed

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☒		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	05/08/2012	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 48	Minus	** 49	= 0	X $30 =	0	OR	X $ =	
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $125 =	0	OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE	0	OR	TOTAL ADD'L FEE	

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/TINA M. BELL/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/601,275	05/31/2010	Venkat Konda	V-0045US	6372

38139 7590 05/01/2012

Konda Technologies, Inc
6278 GRAND OAK WAY
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EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

MAIL DATE	DELIVERY MODE
05/01/2012	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Applicant-Initiated Interview Summary	Application No.	Applicant(s)	
	12/601,275	KONDA, VENKAT	
	Examiner	Art Unit	
	Vibol Tan	2819	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Vibol Tan*. (3)_____.

(2) *Venkat Konda*. (4)_____.

Date of Interview: *30 April 2012*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☐ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☒102 ☐103 ☐Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *1*.

Identification of prior art discussed: *6,940,308 (Wong)*.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Agreement was reached for the proposed amendment of claim 1 to read as an integrated circuit device comprising a plurality of sub-integrated circuit blocks and a routing network, and Said each plurality of sub-integrated circuit blocks comprising a plurality of inlet links and a plurality of outlet links; andSaid routing network comprising of a plurality of stages , in each said sub-integrated circuit block, starting from the lowest stage of 1 to the highest stage of, where; and Said routing network comprising a plurality of switches of size, where, in each said stage and each said switch of size having inlet links and outlet links; andSaid plurality of outlet links of said each sub-integrated circuit block are directly connected to said inlet links of said switches of its corresponding said lowest stage of 1, and said plurality of inlet links of said each sub-integrated circuit block are directly connected from said outlet links of said switches of its corresponding said lowest stage of 1; and Said each sub-integrated circuit block comprising a plurality of forward connecting links connecting from switches in a lower stage to switches in the its immediate succeeding higher stage, and also comprising a plurality of backward connecting links connecting from switches in a higher stage to switches in the its immediate preceding lower stage; and Said each sub-integrated circuit block comprising a plurality straight links in said forward connecting links from switches in said each lower stage to switches in the its immediate succeeding higher stage and a plurality cross links in said forward connecting links from switches in said each lower stage to switches in the its immediate succeeding higher stage, and further comprising a plurality of straight links in said backward connecting links from switches in said each higher stage to switches in the its immediate preceding lower stage and a plurality of cross links in said backward connecting links from switches in said each higher stage to switches in the its immediate preceding lower stage,said plurality of sub-integrated circuit blocks arranged in a two-dimensional grid of rows and columns, and said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks which are either placed vertically above or below, or placed horizontally to the left or to the right; and each said plurality of sub-integrated circuit blocks comprising same number of said stages and said switches in each said stage, regardless of the size of said two-dimensional grid so that each said plurality of sub-integrated circuit block with its corresponding said stages and said switches in each stage is replicable in both vertical direction or horizontal direction of said two-dimensional grid.

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/Vibol Tan/ Primary Examiner, Art Unit 2819	

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

In The United States Patent And Trademark Office

Application Number: 12/601,275

Application Filed: 11/22/2009

Applicant(s): Venkat Konda

Title: VLSI Layouts of Fully Connected Generalized Networks

Examiner/Art Unit: Vibol Tan / 2819

International Application Number: PCT/US08/64605

International Application Filed: 5/22/2008

Priority Date: 5/25/2007

San Jose, 2012 Apr 30, Mon

AMENDMENT A

(and the response to office letter dated 2/7/2012)

Mail Stop Amendment

Commissioner for Patents

P.O. Box 1450

Alexandria, Virginia, 22313-1450

Dear Sir/Madam:

In response to the office action mailed 2012 February 7, please consider the following Amendment A.

First Applicant addresses the novelty and unobviousness of the current invention over the prior art, including the U.S. Patent 6,940,308 by Wong and the U.S Patent 7,154,887 by Wu et. al. Applicant also submits that he has reviewed all the other cited references and they do not show the current invention or render it obvious.

I. IN RESPONSE TO CLAIM REJECTIONS – USC 102(b):

First Applicant submits that the current patent application discloses the VLSI layouts or floor plans of the Benes Network, Butterfly Fat Tree Networks including more generalizations of these networks. The layout is critical to implement these networks in a semiconductor chip which is typically a 2D-plane. As such topologies of the Benes Network and Butterfly Fat Tree networks are known in the prior art and the topologies of the Benes Network and Butterfly Fat Tree networks disclosed in the current invention are the same as in the prior art. However the layouts of these networks are novel.

In addition the layouts disclosed in the current invention include generalized multi-stage networks $V(N_1, N_2, d, s)$, generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$, generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$, generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$, and generalized hypercube networks $V_{hcube}(N_1, N_2, d, s)$ for s = 1,2,3 or any number in general.

The following table addresses the list of items where the current invention is different/superior over column-based layout (or floor plan) disclosed in U.S. Patent 6,940,308 by Wong:

Item addressed	**Solutions in US patent 6,940,308 by Wong**	**Solutions in Current Application**
Layout format	Column-based layout	2D-grid in row-column layout (Key insight in the disclosure is to arrange the sub-integrated circuits in a hypercube topology)
Fundamental sub-integrated circuit	As disclosed in Fig. 13A, the basic building block of the column-based layout is based on (as mentioned in Col. 13, lines 22-24) "There are two logic cells 81 per switch cell 82, connected in the so called "butterfly pattern", consistent with the Benes Network topology: …". It is clear that column-based layout has the following properties: 1) Basic building block (or sub-integrated circuit) has cross links connected between switches of two	As disclosed in Figs. 1C – 1G, the 2D-grid in row-column layout disclosed in the current patent application has no butterfly pattern in the layout. In other words the cross links between switches of two succeeding stages are always connected between two sub-integrated circuits which are placed either horizontally in the same column or vertically in the same row. Also the cross

	succeeding stages with in the same sub-integrated circuit. Otherwise there will not be a butterfly pattern.	links between two succeeding stages are either vertical links (as shown in Figs. 1D & 1F) or horizontal links (as shown in Figs. 1E & 1G).
To scale the layout for bigger size of network (or sub-integrated circuits)	As disclosed in Fig. 13B, columns are doubled by adding one more stage of switches in both the columns (for example Fig. 13A is replicated to get Fig. 13B and a new stage of switches 83 are added and the cross links between the new stage of switches in the two columns become horizontal links). 1) It is clear as the network is scaled up, only columns are increasing. 2) And the basic building block is the same as that shown in Fig. 13A.	As disclosed in Fig. 1H, the layout doubles in both columns and rows alternatively, as the size of the network is doubled repeatedly as needed, in hypercube layout format.
Industry Applicability or practical use of the layout (FPGA vendors typically take the same basic block (consisting of a	The applicant believes column-based layout is impractical for an FPGA vendor to manufacture FPGA devices with different size of basic blocks, as the number of basic blocks in each device determine the size of each	Same basic block can be easily used to manufacture FPGAs of different sizes. (The layout disclosed in the current invention is already adopted by an

certain set of LUTs and registers) and manufacture devices of different sizes of basic blocks (typically called slice, CLB or PLC etc.)	column (as that shown in FIG. 13A) and each device will require a different size of each column to manufacture the devices close to square in size. And hence it is impractical for an FPGA vendor to employ column-based layout.	FPGA vendor namely Quicklogic corporation, located in Sunnyvale, CA).
Locality between two neighboring basic blocks either horizontally or vertically	From Fig. 13A, it can be seen that for a signal from a logic cell to be routed horizontally to the nearest neighboring column, the signal needs to go through all the stages 82 (whose cross links are connected with in the same column) before connecting out to the logic cell in the basic block of the nearest neighboring column.	For most of the logic cells in this layout, a signal from a logic cell can be routed vertically or horizontally to the nearest neighboring logic cell by passing through one or two stages of switches.

2. IMPRACTCIAL TREE-BASED LAYOUT DISCLOSED IN PATENT 6,940,308 BY WONG:

1) The tree-based layout disclosed in patent 6,940,308 by Wong is also not practical to implement by an FPGA vendor because:

a) From Fig. 14C it is evident that the switches corresponding to the higher stages get pulled into the middle of the layout. For example in Fig. 14C, the switches A4 – P4 are placed in the center or middle of the layout. As the size of the logic cells increase from 16 to bigger sizes, this problem will get even worse as the highest stage switches get pulled into the middle of the layout. The next highest stage switches get pulled into close to the middle of the layout. Similarly the higher the stage of switches they are placed close to the middle of the layout and the lower the stage of switches they are placed close to the logic cells.

b) Evidently the logic cells and the switches corresponding to the all the stages for that logic cell cannot be designed as a repeatable basic block and hence this tree-based layout is not practical to implement by an FPGA vendor.

II. IN RESPONSE TO CLAIM REJECTIONS – USC 103(a):

1. LAYOUT FOR REARRANGEBALY AND STRICLTY NON-BOCKING NETWORKS FOR ARBITRARY FAN-OUT MULTICAST CONNECTIONS:

1) US patent 7,154,887 by Wu et. al. disclosed a grooming switch based on a rearrangeably non-blocking clos network for arbitrary fan-out multicast traffic. To make 3-stage clos network which is rearrangeably non-blocking for unicast connections, US patent 7,154,887 by Wu et. al. disclosed a rearrangeably non-blocking clos network with 5 stages for arbitrary fan-out multicast traffic by adding 2 more stages.

2) As disclosed in the "CROSS REFERENCE TO RELATED APPLICATIONS" of the current patent application, by the same applicant, the current patent application also discloses VLSI layouts for:

a) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-stage networks disclosed in the US Application Serial No. 12/530,207 entitled "FULLY CONNECTED GENERALIZED MULTI-STAGE NETWORKS" by the same applicant.

b) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-stage networks disclosed in the US Application Serial No. 12/601,273 entitled "FULLY CONNECTED GENERALIZED BUTTERFLY FAT TREE NETWORKS" by the same applicant.

c) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-stage networks disclosed in the US Application Serial No. 12/601,274 entitled "FULLY CONNECTED GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS" by the same applicant.

Claims: Claims 1-3, 8, 12, 25, 29, 40, 44, 48-49 of record are amended and substitute new claims as follows.

CLAIMS

What is claimed is:

1. (currently amended): An integrated circuit device comprising a plurality of sub-integrated circuit blocks and a routing network, and

Said each plurality of sub-integrated circuit blocks comprising a plurality of inlet links and a plurality of outlet links; and

~~Said routing network interconnects any one of said outlet link of one of said sub-integrated circuit block to one or more said inlet links of one or more of said sub-integrated circuit blocks; and~~

Said routing network comprising of a plurality of stages y, in each said sub-integrated circuit block, starting from the lowest stage of 1 to the highest stage of y, where $y \geq 1$; and

Said routing network comprising a plurality of switches of size $d \times d$, where $d \geq 2$, in each said stage and each said switch of size $d \times d$ having d inlet links and d outlet links; and

~~Said each sub-integrated circuit block comprising a plurality of said switches corresponding to each said stage; and~~

Said plurality of outlet links of said each sub-integrated circuit block are directly connected to said inlet links of said switches of its corresponding said lowest stage of 1, and said plurality of inlet links of said each sub-integrated circuit block are directly connected from said outlet links of said switches of its corresponding said lowest stage of 1; and

Said each sub-integrated circuit block comprising a plurality of forward connecting links connecting from switches in a lower stage to switches in ~~the~~ its immediate succeeding higher stage, and also comprising a plurality of backward connecting links connecting from switches in a higher stage to switches in ~~the~~ its immediate preceding lower stage; and

Said each sub-integrated circuit block comprising a plurality straight links in said forward connecting links from switches in said each lower stage to switches in ~~the~~ its immediate succeeding higher stage and a plurality cross links in said forward connecting links from switches in said each lower stage to switches in ~~the~~ its immediate succeeding higher stage, and further comprising a plurality of straight links in said backward connecting links from switches in said each higher stage to switches in ~~the~~ its immediate preceding lower stage and a plurality of cross links in said backward connecting links from switches in said each higher stage to switches in ~~the~~ its immediate preceding lower stage,

said plurality of sub-integrated circuit blocks arranged in a two-dimensional grid of rows and columns, and

said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks which are either placed vertically above or below, or placed horizontally to the left or to the right,

each said plurality of sub-integrated circuit blocks comprising same number of said stages and said switches in each said stage, regardless of the size of said two-dimensional grid so that each said plurality of sub-integrated circuit block with its corresponding said stages and said switches in each stage is replicable in both vertical direction or horizontal direction of said two-dimensional grid.

2. (currently amended): The integrated circuit device of claim 1, ~~wherein said plurality of sub-integrated circuit blocks arranged in a two-dimensional grid~~ said two-dimensional grid of said sub-integrated circuit blocks with their corresponding said stages and said switches in each stage is scalable by any power of 2, and,

for each multiplication of 2 of the size of total said sub-integrated circuit blocks, by adding one more stage of switches and the layout is placed in hypercube format and

also the cross links between said one more stage of switches are connected in hypercube format.

3. (Original): The integrated circuit device of claim 2, wherein said cross links in succeeding stages are connecting as alternative vertical and horizontal links between switches in said sub-integrated circuit blocks.

4. (Original): The integrated circuit device of claim 3, wherein said cross links from switches in a stage in one of said sub-integrated circuit blocks are connecting to switches in the succeeding stage in another of said sub-integrated circuit blocks so that said cross links are either vertical links or horizontal and vice versa, and hereinafter such cross links are "shuffle exchange links").

5. (Original): The integrated circuit device of claim 4, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are substantially of equal length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are substantially of equal length in the entire said integrated circuit device.

6. (Original): The integrated circuit device of claim 5, wherein the shortest horizontal shuffle exchange links are connecting at the lowest stage and between switches in two nearest neighboring said sub-integrated circuit blocks, and length of the horizontal shuffle exchange links is doubled in each succeeding stage; and the shortest vertical shuffle exchange links are connecting at the lowest stage and between switches in two nearest neighboring said sub-integrated circuit blocks, and length of the vertical shuffle exchange links is doubled in each succeeding stage.

7. (currently amended): The integrated circuit device of claim 6, wherein $y \geq (\log_2 N)$, where $N > 1$, so that the length of the horizontal shuffle exchange links in the highest stage is equal to half the size of the horizontal size of said two dimensional grid of sub-integrated circuit blocks and the length of the vertical shuffle exchange links

in the highest stage is equal to half the size of the vertical size of said two dimensional grid of sub-integrated circuit blocks.

8. (Original): The integrated circuit device of claim 7, wherein $d = 2$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast Benes network with full bandwidth.

9. (Original): The integrated circuit device of claim 7, wherein $d = 2$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast Benes network and rearrangeably nonblocking for arbitrary fan-out multicast Benes network with full bandwidth.

10. (Original): The integrated circuit device of claim 7, wherein $d = 2$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast Benes network with full bandwidth.

11. (currently amended): The integrated circuit device of claim 6, wherein $y \geq (\log_2 N)$, where $N > 1$, so that the length of the horizontal shuffle exchange links in the highest stage is equal to half the size of the horizontal size of said two dimensional grid of sub-integrated circuit blocks and the length of the vertical shuffle exchange links in the highest stage is equal to half the size of the vertical size of said two dimensional grid of sub-integrated circuit blocks, and

said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks.

12. (Original): The integrated circuit device of claim 11, wherein $d = 2$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast butterfly fat tree network with full bandwidth.

13. (Original): The integrated circuit device of claim 11, wherein $d = 2$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast butterfly fat tree network and rearrangeably nonblocking for arbitrary fan-out multicast butterfly fat tree network with full bandwidth.

14. (Original): The integrated circuit device of claim 11, wherein $d = 2$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast butterfly fat tree network with full bandwidth.

15. (Original): The integrated circuit device of claim 1, wherein said horizontal and vertical links are implemented on two or more metal layers.

16. (Original): The integrated circuit device of claim 1, wherein said switches comprising active and reprogrammable cross points and said each cross point is programmable by an SRAM cell or a Flash Cell.

17. (Original): The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks are of equal die size.

18. (Original): The integrated circuit device of claim 15, wherein said sub-integrated circuit blocks are Lookup Tables (hereinafter "LUTs") and said integrated circuit device is a field programmable gate array (FPGA) device or field programmable gate array (FPGA) block embedded in another integrated circuit device.

19. (Original): The integrated circuit device of claim 15, wherein said sub-integrated circuit blocks are AND or OR gates and said integrated circuit device is a programmable logic device (PLD).

20. (Original): The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks comprising any arbitrary hardware logic or memory circuits.

21. (Original): The integrated circuit device of claim 1, wherein said switches comprising active one-time programmable cross points and said integrated circuit device is a mask programmable gate array (MPGA) device or a structured ASIC device.

22. (Original): The integrated circuit device of claim 1, wherein said switches comprising passive cross points or just connection of two links or not and said integrated circuit device is a Application Specific Integrated Circuit (ASIC) device.

23. (Original): The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks further recursively comprise one or more super-sub-integrated circuit blocks and a sub-routing network.

24. (currently amended): The integrated circuit device of claim 4, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and $y \geq (\log_2 N)$, where $N > 1$.

25. (Original): The integrated circuit device of claim 24, wherein $d = 2$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage

in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized multi-stage network with full bandwidth.

26. (Original): The integrated circuit device of claim 24, wherein $d = 2$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized multi-stage network and rearrangeably nonblocking for arbitrary fan-out multicast generalized multi-stage network with full bandwidth.

27. (Original): The integrated circuit device of claim 24, wherein $d = 2$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized multi-stage network with full bandwidth.

28. (currently amended): The integrated circuit device of claim 4, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and $y \geq (\log_2 N)$, where $N > 1$, and

said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks.

29. (Original): The integrated circuit device of claim 28, wherein $d = 2$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and

said routing network is rearrangeably nonblocking for unicast generalized butterfly fat tree network with full bandwidth.

30. (Original): The integrated circuit device of claim 28, wherein $d = 2$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized butterfly fat tree Network and rearrangeably nonblocking for arbitrary fan-out multicast generalized butterfly fat tree network with full bandwidth.

31. (Original): The integrated circuit device of claim 28, wherein $d = 2$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized butterfly fat tree network with full bandwidth.

32. (Original): The integrated circuit device of claim 1, wherein said straight links connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and

said cross links are connecting as vertical or horizontal or diagonal links between two different said sub-integrated circuit blocks.

33. (Original): The integrated circuit device of claim 7, wherein $d = 4$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast multi-link Benes network with full bandwidth.

34. (Original): The integrated circuit device of claim 7, wherein $d = 4$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast multi-link Benes network and rearrangeably nonblocking for arbitrary fan-out multicast multi-link Benes network with full bandwidth.

35. (Original): The integrated circuit device of claim 7, wherein $d = 4$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast multi-link Benes network with full bandwidth.

36. (Original): The integrated circuit device of claim 11, wherein $d = 4$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast multi-link butterfly fat tree network with full bandwidth.

37. (Original): The integrated circuit device of claim 11, wherein $d = 4$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast multi-link butterfly fat tree network and rearrangeably nonblocking for arbitrary fan-out multicast multi-link butterfly fat tree network with full bandwidth.

38. (Original): The integrated circuit device of claim 11, wherein $d = 4$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said

stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast multi-link butterfly fat tree network with full bandwidth.

39. (currently amended): The integrated circuit device of claim 4, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and $y \geq (\log_2 N)$, where $N > 1$.

40. (Original): The integrated circuit device of claim 39, wherein $d = 4$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized multi-link multi-stage network with full bandwidth.

41. (Original): The integrated circuit device of claim 39, wherein $d = 4$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized multi-link multi-stage network and rearrangeably nonblocking for arbitrary fan-out multicast generalized multi-link multi-stage network with full bandwidth.

42. (Original): The integrated circuit device of claim 39, wherein $d = 4$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized multi-link multi-stage network with full bandwidth.

43. (currently amended): The integrated circuit device of claim 4, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and $y \geq (\log_2 N)$, where $N > 1$, and

said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks.

44. (Original): The integrated circuit device of claim 43, wherein $d = 4$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized multi-link butterfly fat tree network with full bandwidth.

45. (Original): The integrated circuit device of claim 43, wherein $d = 4$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized multi-link butterfly fat tree Network and rearrangeably nonblocking for arbitrary fan-out multicast generalized multi-link butterfly fat tree network with full bandwidth.

46. (Original): The integrated circuit device of claim 43, wherein $d = 4$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized multi-link butterfly fat tree network with full bandwidth.

47. (currently amended): The integrated circuit device of claim 1, wherein said plurality of forward connecting links use a plurality of buffers to amplify signals

driven through them and said plurality of backward connecting links use a plurality of buffers to amplify signals driven through them; and said buffers can be inverting or non-inverting buffers.

48. (currently amended): The integrated circuit device of claim 1, wherein said ~~wherein said~~ all switches of size $d \times d$ are either fully populated or partially populated.

1) **The rejection of Claims 1-8, 12, 16-25, 29, 33, 40, 44, and 48-49 under 35 USC 102(b)**

Accordingly applicant submit that the claims do comply with § 102(b) and therefore request withdrawal of this rejection.

2) **The rejection of Claims 9-11, 13-15, 26-28, 30-32, 34-39, 41-43, and 45-47 under 35 USC 103(a)**

Accordingly applicant submit that the claims do comply with § 103(a) and therefore request withdrawal of this rejection.

CONCLUSION

For all of the above reasons, applicant submits that the Claims are now in proper form, and that the Claims all define patentably over the prior art. Therefore applicant submits that this application is now in condition for allowance, which action he respectfully solicits.

Conditional request for Constructive Assistance

Applicant has amended the claims of this application so that they are proper, definite, and define novel structure which is also unobvious. If, for any reason this application is not believed to be in full condition for allowance, applicant respectfully request the constructive assistance and suggestions of the Examiner pursuant to M.P.E.P § 2173.02 and § 707.07(j) in order that the undersigned can place this application in allowable condition as soon as possible and without the need for further proceedings.

Very respectfully,

/Venkat Konda/

Venkat Konda

Konda Technologies, Inc (USPTO Customer Number: 38139)

6278 Grand Oak Way

San Jose, CA 95135

Phone: 408-472-3273

Fax: 408-238-2478

Electronic Acknowledgement Receipt

EFS ID:	12667779
Application Number:	12601275
International Application Number:	
Confirmation Number:	6372
Title of Invention:	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Customer Number:	38139
Filer:	Venkar Konda
Filer Authorized By:	
Attorney Docket Number:	V-0045US
Receipt Date:	30-APR-2012
Filing Date:	31-MAY-2010
Time Stamp:	18:15:10
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	AmendmentA-V0045US.pdf	188498 1ef528eeaf46ce4d077d8e28f40c4a871729bff2	no	21

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Total Files Size (in bytes):	188498

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PTO/SB/06 (07-06)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/601,275	05/31/2010	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☒ RATE ($)	SMALL ENTITY ☒ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 04/30/2012	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 48	Minus	** 49	= 0	X $30 =	0	OR	X $ =	
Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $125 =	0	OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE	0	OR	TOTAL ADD'L FEE	

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/ROLITA WIMBUSH/

PTO/SB/14 (11-08)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	V-0045US
	Application Number	
Title of Invention	VLSI Layouts of Fully Connected Generalized Networks	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1 Remove

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Venkat		Konda	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	San Jose	State/Province	CA	Country of Residence [i]	US

Citizenship under 37 CFR 1.41(b) [i] US

Mailing Address of Applicant:

Address 1	6278 Grand Oak Way		
Address 2			
City	San Jose	State/Province	CA
Postal Code	95135	Country [i]	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	38139		
Email Address	venkat@kondatech.com	Add Email	Remove Email

Application Information:

Title of the Invention	VLSI Layouts of Fully Connected Generalized Networks		
Attorney Docket Number	V-0045US	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	39	Suggested Figure for Publication (if any)	1G

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	V-0045US
	Application Number	
Title of Invention	VLSI Layouts of Fully Connected Generalized Networks	

Publication Information:

☒	Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐	**Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S. C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	38139		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country [i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
PCT/US08/64605	US	2008-05-22	◉ Yes ○ No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1 Remove

PTO/SB/14 (11-08)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	V-0045US
	Application Number	
Title of Invention	VLSI Layouts of Fully Connected Generalized Networks	

If the Assignee is an Organization check here. ☒			
Organization Name	Konda Technologies Inc.		
Mailing Address Information:			
Address 1	6278 Grand Oak Way		
Address 2			
City	San Jose	**State/Province**	CA
Country [i]	US	Postal Code	95135
Phone Number	408-472-3273	Fax Number	408-238-2478
Email Address	venkat@kondatech.com		
Additional Assignee Data may be generated within this form by selecting the **Add** button.		Add	

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

Signature	/Venkat Konda/			Date (YYYY-MM-DD)	2012-04-18
First Name	Venkat	Last Name	Konda	Registration Number	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	12576502
Application Number:	12601275
International Application Number:	
Confirmation Number:	6372
Title of Invention:	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Customer Number:	38139
Filer:	Venkar Konda
Filer Authorized By:	
Attorney Docket Number:	V-0045US
Receipt Date:	19-APR-2012
Filing Date:	31-MAY-2010
Time Stamp:	04:53:51
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	sb0014-V0045US.pdf	1420688 1b1fcb4236336b2fb79c4394e98f66b92e839166	no	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/601,275	KONDA, VENKAT	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-49* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-49* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-8, 12, 16-25, 29, 33, 40, 44, and 48-49 are rejected under 35 U.S.C. 102(b) as being anticipated by Wong (U. S. PAT. 6,940,308).

In claim 1, Wong teaches an integrated circuit device comprising a plurality of sub-integrated circuit blocks and a routing network (ASIC; col. 13, lines 4-5), and

Said each plurality of sub-integrated circuit blocks comprising a plurality of inlet links and a plurality of outlet links (input-output pin-pair; Col. 13, Line 25); and

Said routing network interconnects any one of said outlet link of one of said sub-integrated circuit block to one or more said inlet links of one or more of said sub-integrated circuit blocks (peripheral blocks of an integrated circuit; col. 14, line 48); and

Said routing network comprising of a plurality of stages y, starting from the lowest stage to the highest stage (hierarchical levels; col. 2, lines 7-12); and

Said routing network comprising a plurality of switches of size d x d, where $d \geq 2$, in each said stage and each said switch of size d x d having d inlet links and d outlet links (2x2 switch; col. 2, line 27); and

Said each sub-integrated circuit block comprising a plurality of said switches corresponding to each said stage (switches at first rank of hierarchy; col. 2, lines 34-35; Fig. 3C); and

Said each sub-integrated circuit block comprising a plurality of forward connecting links connecting from switches in lower stage to switches in the immediate succeeding higher stage (col. 2; lines 16-22; see input and output links in Fig. 2B; Fig. 3A), and also comprising a plurality of backward connecting links connecting from switches in higher stage to switches in the immediate preceding lower stage (see upper network and lower network in Fig 3B; see upper and lower in Fig. 3C; inputs and outputs, Fig. 4B); and

Said each sub-integrated circuit block comprising a plurality straight links in said forward connecting links from switches in lower stage to switches in the immediate succeeding higher stage and a plurality cross links in said forward connecting links from switches in lower stage to switches in the immediate succeeding higher stage (pass (straight) mode or cross mode; col. 5, lines 4-13; cross, Fig. 2B; see upper network and lower network in Fig. 3B; see upper and lower in Fig. 3C; inputs and outputs Fig. 4B), and further comprising a plurality of straight links in said backward connecting links from switches in higher stage to switches in the immediate preceding lower stage and a plurality of cross links in said backward connecting links from switches in higher stage to switches in the immediate preceding lower stage (pass (straight) mode or cross mode; col. 5, lines 4-13; cross, Fig. 2B; see upper network and lower network in Fig 3B; see upper and lower in Fig. 3C; inputs and outputs, Fig. 4B).

In claim 2, Wong further teaches the integrated circuit device of claim 1, wherein said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block (Fig. 13A); and

said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks (Fig. 13A).

In claim 3, Wong further teaches the integrated circuit device of claim 2, wherein said plurality of sub-integrated circuit blocks arranged in a two-dimensional grid (width and height dimensions; col. 12, lines 42-51).

In claim 4, Wong further teaches the integrated circuit device of claim 3, wherein said cross links in succeeding stages are connecting as alternative vertical and horizontal links between switches in said sub-integrated circuit blocks (col. 2, lines 7-12; Fig. 10, Fig. 14B).

In claim 5, Wong further teaches the integrated circuit device of claim 4, wherein said cross links from switches in a stage in one of said sub-integrated circuit blocks are connecting to switches in the succeeding stage in another of said sub-integrated circuit blocks so that said cross links are either vertical links or horizontal and vice versa, and hereinafter such cross links are "shuffle exchange links" (rearrangeable interconnection network; col. 1, line 61 - col. 2, Line 6; rearrangeable; col. 4, lines 12-17).

In claim 6, Wong further teaches the integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are substantially of equal length and said vertical shuffle

exchange links between switches in any two corresponding said succeeding stages are substantially of equal length in the entire said integrated circuit device (original Benes network and every route must travel through all levels, col. 7, lines 26-27; col. 11, lines 23-25).

In claim 7, Wong further teaches the integrated circuit device of claim 6, wherein the shortest horizontal shuffle exchange links are connecting at the lowest stage and between switches in two nearest neighboring said sub-integrated circuit blocks, and length of the horizontal shuffle exchange links is doubled in each succeeding stage (shorter routes; col. 7, lines 26-27; col. 11, lines 23-25); and

the shortest vertical shuffle exchange links are connecting at the lowest stage and between switches in two nearest neighboring said sub-integrated circuit blocks, and length of the vertical shuffle exchange links is doubled in each succeeding stage (length = 2*(log2 N); col. 11, lines 23-25).

In claim 8, Wong further teaches the integrated circuit device of claim 7, wherein $y \geq (\log_2 N)$ so that the length of the horizontal shuffle exchange links in the highest stage is equal to half the size of the horizontal size of said two dimensional grid of sub-integrated circuit blocks and the length of the vertical shuffle exchange links in the highest stage is equal to half the size of the vertical size of said two dimensional grid of sub-integrated circuit blocks (length = 2*(log2 N); col. 11, lines 23-25).

In claim 12, Wong further teaches the integrated circuit device of claim 7, wherein $y \geq (\log_2 N)$ so that the length of the horizontal shuffle exchange links in the highest stage is equal to half the size of the horizontal size of said two dimensional grid

of sub-integrated circuit blocks and the length of the vertical shuffle exchange links in the highest stage is equal to half the size of the vertical size of said two dimensional grid of sub-integrated circuit blocks (length = 2*(log2 N); col. 11, lines 23-25), and said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks (see u-turn links; Figs. 5 and 6B).

In claim 16, Wong further teaches the integrated circuit device of claim 1, wherein said horizontal and vertical links are implemented on two or more metal layers (CMOS integrated circuit; col. 5, lines 22-25).

In claim 17, Wong further the integrated circuit device of claim 1, wherein said switches comprising active and reprogrammable cross points and said each cross point is programmable by an SRAM cell or a Flash Cell (SRAM based FPGA; col. 2, lines 25-26; FPGA, col. 1, lines 14-17).

In claim 18, Wong further teaches the integrated circuit device of claim 1, wherein said sub-integrated circuit blocks are of equal die size (sub-network of equal size; col. 6, lines 10-11).

In claim 19, Wong further teaches the integrated circuit device of claim 16, wherein said sub-integrated circuit blocks are Lookup Tables (hereinafter "LUTs") and said integrated circuit device is a field programmable gate array (FPGA) device or field programmable gate array (FPGA) block embedded in another integrated circuit device (look-up tables; col. 8, line 51; FPGA (Field Programmable Gate Array); col. 1, lines 14-17).

In claim 20, Wong further teaches the integrated circuit device of claim 16, wherein said sub-integrated circuit blocks are AND or OR gates and said integrated circuit device is a programmable logic device (PLD) ('logic gates'; col. 7, line 36; 'programmable gate arrays'; col. 14, lines 29-31).

In claim 21, Wong further teaches the integrated circuit device of claim 1, wherein said sub-integrated circuit blocks comprising any arbitrary hardware logic or memory circuits (col. 14, lines 44-51).

In claim 22, Wong further teaches the integrated circuit device of claim 1, wherein said switches comprising active one-time programmable cross points and said integrated circuit device is a mask programmable gate array (MPGA) device or a structured ASIC device (MPGA, col. 14, lines 29-31; ASIC, col. 13, lines 4-5).

In claim 23, Wong further teaches the integrated circuit device of claim 1, wherein said switches comprising passive cross points or just connection of two links or not and said integrated circuit device is a Application Specific Integrated Circuit (ASIC) device (logic cells, col. 1, lines 29-31; ASIC, col. 13, lines 4-5).

In claim 24, Wong the integrated circuit device of claim 1, wherein said sub-integrated circuit blocks further recursively comprise one or more super-sub-integrated circuit blocks and a sub-routing network (one or more sub-networks; Col. 6, lines 7-9).

In claim 25, Wong further teaches the integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle

exchange links between switches in any two corresponding said succeeding stages are of different length and y ≥ (log2 N) (length = 2*(log2 N); col. 11, lines 23-25).

In claim 29, Wong further teaches the integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and y ≥ (log2 N) (length = 2*(log2 N); col. 11, lines 23-25), and said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks (see u-turn links; Figs. 5 and 6B).

In claim 33, Wong further teaches the integrated circuit device of claim 1, wherein said straight links connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and said cross links are connecting as vertical or horizontal or diagonal links between two different said sub-integrated circuit blocks (see link arrangement in Fig. 3B).

In claim 40, Wong teaches the integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and y ≥ (log2 N) (length = 2*(log2 N); col. 11, lines 23-25).

In claim 44, Wong further teaches the integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two

corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and y ≥ (log2 N) (length = 2*(log2 N); col. 11, lines 23-25), and said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks (see u-turn links; Figs. 5 and 6B).

In claim 48, Wong further teaches the integrated circuit device of claim 1, wherein said plurality of forward connecting links use a plurality of buffers to amplify signals driven through them and said plurality of backward connecting links use a plurality of buffers to amplify signals driven through them; and said buffers can be inverting or non-inverting buffers (buffers; col. 10, lines 59-64).

In claim 49, Wong further teaches the integrated circuit device of claim 1, wherein said wherein said all switches of size d x d are either fully populated or partially populated (populated and depopulated cells; col. 3, lines 34-41).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 9-11, 13-15, 26-28, 30-32, 34-39, 41-43, and 45-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong in view of Wu et al. (U. S. PAT. 7,154,887), hereinafter Wu.

In claim 9, Wong discloses a Benes network wherein d =2 and there is only one switch in each said stags in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links (col. 2, lines 27-30; 2x2 Benes network; col. 5, lines 26-31); but does not disclose said routing network is rearrangeably nonblocking for unicast Benes network with full bandwidth. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being rearrangeably nonblocking for unicast Benes network with full bandwidth (rearrangeably nonblocking for unicast traffic; col. 2, lines 52-54).

Therefore, it would have been obvious to one ordinarily skilled in the art at the time the invention was made to supplement the teachings of Wong and have routing network being rearrangeably nonblocking for unicast Benes network with full bandwidth, in order to satisfy specific routing requirements.

In claim 10, Wong discloses d = 2 and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links (8x8 Benes network (each switch has two logic cells that are 2x2, hence 8x8 is 4 switches); col. 2, lines 31-33), but does not disclose said routing network is strictly nonblocking for unicast Benes network and rearrangeably nonblocking for arbitrary fan-out multicast Benes network with full bandwidth. However, in the same field of endeavor, Wu discloses a rearrangeable non-

blocking switch (Abstract) and a routing network being strictly nonblocking for unicast Benes network (col. 2, lines 9-11; see Fig. 9) and rearrangeably nonblocking for arbitrary fan-out multicast Benes network with full bandwidth (col. 4, lines 6-7; see fanouts, Fig. 7B).

Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be strictly nonblocking for unicast Benes and rearrangeably nonblocking for arbitrary fan-out multicast Benes network with full bandwidth, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 11, Wong discloses d = 2 and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links ('8x8 Benes network'; col. 2, lines 31-33), but does not disclose said routing network is strictly nonblocking for arbitrary fan-out multicast Benes network with full bandwidth. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network strictly nonblocking for arbitrary fan-out multicast Benes network with full bandwidth (col. 2, lines 8-11; see fanouts, Fig. 7B).

Therefore it would have been obvious to one ordinarily skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be strictly nonblocking for arbitrary fan-out multicast Benes network with full bandwidth, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 13, Wong discloses d = 2 and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub integrated circuit block connecting said backward connecting links ('8x8 Benes network'; col. 2, lines 31-33) and a muting network being a butterfly fat tree network 7, but does not disclose said routing network is rearrangeably nonblocking for unicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being rearrangeably nonblocking for unicast traffic ('rearrangeably nonblocking for unicast traffic'; col. 2, lines 52-54).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a muting network be rearrangeably nonblocking for unicast traffic, as disclosed by Wu, in order to satisfy specific muting requirements.

In claim 14, Wong discloses wherein d = 2 and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links ('8x8 Benes network'; col. 2, lines 31-33) and a routing network being a butterfly fat tree network (col. 13, lines 23-24), but does not disclose said routing network is strictly nonblocking for unicast traffic and rearrangeably nonblocking for arbitrary fan-out multicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being strictly nonblocking for unicast traffic (col. 2, lines

9-11, see Fig. 9) and rearrangeably nonblocking for arbitrary fan-out multicast Benes network with full bandwidth (col. 4, lines 6-7; see 'fanouts', Fig. 7B).

Therefore it would have been obvious to one ordinarily skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be strictly nonblocking for unicast Benes and rearrangeably nonblocking for arbitrary fan-out multicast Benes network with full bandwidth, as disclosed by Wu, in order to satisfy specific muting requirements.

In claim 15, Wong discloses wherein d = 2 and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links ('8x8 Benes network'; col. 2, Lines 31-33) and a routing network being a butterfly fat tree network with full-bandwidth (col. 13, lines 23-24), but does not disclose said routing network is strictly nonblocking for arbitrary fan-out multicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) wherein a routing network is strictly nonblocking for arbitrary fan-out (col. 2, lines 8-11; see "fanouts', Fig. 7B).

Therefore it would have been obvious to one ordinarily skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be strictly nonblocking for arbitrary fan-out multicast Benes network with full bandwidth, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 26, Wong discloses d = 2 and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub integrated circuit block connecting said backward connecting links and said routing network is generalized with full bandwidth (col. 2, lines 27-30; '2x2 Benes network'; col. 5, lines 26-31; "networks can be generalized'; col. 6, lines 7-9), but does net disclose said routing network is rearrangeably nonblocking for unicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being rearrangeably nonblocking for unicast traffic ('rearrangeably nonblocking for unicast traffic'; col. 2, lines 52-54).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be rearrangeably nonblocking for unicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 27, Wong discloses d = 2 and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links ('8x8 Benes network' (each switch has two logic cells that are 2x2, hence 8x8 is 4 switches); col. 2, lines 31-33), and said routing network being a generalized network ('networks can be generalized'; col. 6, lines 7-9), but does not disclose said routing network is strictly nonblocking for unicast generalized multi-stage network and rearrangeably nonblocking for arbitrary fan-

out multicast generalized multi-stage network with full bandwidth. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being rearrangeably nonblocking for arbitrary fan-out multicast multi-stage network with full bandwidth (col. 4, lines 6-7; see 'fanouts', Fig. 7B).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be rearrangeably nonblocking for arbitrary fan-out multicast generalized multi-stage network with full bandwidth, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 28, Wong discloses d = 2 and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is a generalized routing network ('8x8 Benes network' (each switch has two logic cells that are 2x2, hence 8x8 is 4 switches); col. 2, lines 31-33; 'networks can be generalized'; col. 6, lines 7-9), but does not disclose said routing network is strictly nonblocking for arbitrary fan-out multicast multistage. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network strictly nonblocking for arbitrary fan-out multicast multistage (col. 2, lines 8-11; see 'fanouts', Fig. 7B).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing

network be strictly nonblocking for arbitrary fan-out multicast multistage network with full bandwidth, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 30, Wong discloses d = 2 and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub integrated circuit block connecting said backward connecting links and said routing network is a generalized butterfly fat tree network with full bandwidth (col. 2, lines 27-30; '2x2 Benes network'; col. 5, lines 26-31; 'networks can be generalized'; col. 6, lines 7-9; 'butterfly pattern'; col. 13, lines 23-24), but does not disclose said routing network is rearrangeably nonblocking for unicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being rearrangeably nonblocking for unicast traffic ('rearrangeably nonblocking for unicast traffic'; col. 2, lines 52-54).

Therefore it would have been obvious to one ordinarily skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be rearrangeably nonblocking for unicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 31, Wong discloses d = 2 and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network being a generalized butterfly fat tree network with full-bandwidth ('8x8 Benes network' (each

switch has two logic cells that are 2x2, hence 8x8 is 4 switches); col. 2, lines 31-33; 'networks can be generalized'; col. 6, lines 7-9; 'butterfly pattern'; col. 13, lines 23-24), but does not disclose said routing network is strictly nonblocking for unicast traffic and rearrangeably nonblocking for arbitrary fan-out multicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being strictly nonblocking for unicast traffic (col. 2, lines 9-11, see Fig. 9) and rearrangeably nonblocking for arbitrary fan-out multicast traffic (col. 4, lines 6-7; see 'fanouts', Fig. 7B).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a muting network be strictly nonblocking for unicast traffic and rearrangeably nonblocking for arbitrary fan-out multicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 32, Wong discloses wherein d = 2 and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network generalized butterfly fat tree network with full bandwidth ('8x8 Benes network' (each switch has two logic calls that are 2x2, hence 8x8 is 4 switches); col. 2, lines 31-33; 'networks can be generalized'; col. 6, Lines 7-9), but does not disclose said routing network is strictly nonblocking for arbitrary fan-out multicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract)

and a routing network strictly nonblocking for arbitrary fan-out multicast traffic (col. 2, lines 8-11; see 'fanouts', Fig. 7B).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be strictly nonblocking for arbitrary fan-out multicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 34, Wong discloses d = 4 ('plurality of input terminals and a number of output terminals', claim 1) and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network multi-link Benes network with full bandwidth (col. 2, lines 27-30; '2x2 Benes network'; col. 5, lines 26-31), but does not disclose said routing network is rearrangeably nonblocking for unicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being rearrangeably nonblocking for unicast traffic ('rearrangeably nonblocking for unicast traffic'; col. 2, lines 52-54).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be rearrangeably nonblocking for unicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 35, Wong discloses d = 4 ('plurality of input terminals and a number of output terminals', claim 1) and there are at least two switches in each said stage in each

said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is a multi-link Benes network ('8x8 Benes network' (each switch has two logic cells that are 2x2, hence 8x8 is 4 switches); col. 2, lines 31-33; col. 6, lines 7-9), but does not disclose said routing network is strictly nonblocking for unicast traffic and rearrangeably nonblocking for arbitrary fan-out multicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being strictly nonblocking for unicast traffic (col. 2, lines 9-11, see Fig. 9) and rearrangeably nonblocking for arbitrary fan-out multicast traffic (col. 4, lines 6-7; see 'fanouts', Fig. 7B).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be strictly nonblocking for unicast traffic and rearrangeably nonblocking for arbitrary fan-out multicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 36, Wong discloses d = 4 ('plurality of input terminals and a number of output terminals', claim 1) and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network multi-link Benes network with full bandwidth ('6x8 Benes network' (each switch has two logic cells that are 2x2, hence 8x8 is 4 switches); col. 2, lines 31-33; col. 6, lines 7-9), but does not

disclose said routing network is strictly nonblocking for arbitrary fan-out multicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being rearrangeably nonblocking for arbitrary fan-out multicast traffic (col. 4, lines 6-7; see 'fanouts', Fig. 7B).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be rearrangeably nonblocking for arbitrary fan-out multicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 37, Wong discloses d = 4 ('plurality of input terminals and a number of output terminals', claim 1) and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is a butterfly fat tree network with full bandwidth (col. 2, lines 27-30; col. 2. lines 31-33; 'butterfly pattern'; col. 13, lines 23-24); but does not disclose said routing network is rearrangeably nonblocking for unicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being rearrangeably nonblocking for unicast traffic ('rearrangeably nonblocking for unicast traffic'; col. 2, lines 52-54).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be rearrangeably nonblocking for unicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 38, Wong discloses wherein d = 4 ('plurality of input terminals and a number of output terminals', claim 1) and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links ('8x8 Benes network' (each switch has two logic cells that are 2x2. hence 8x8 is 4 switches); col. 2, lines 31-33; col. 6, lines 7-9) and said routing network is a multi-link butterfly fat tree network (col. 2, lines 27-30; col. 2, lines 31-33; 'butterfly pattern'; col. 13, lines 23-24), but does not disclose said routing network is strictly nonblocking for unicast and rearrangeably nonblocking for arbitrary fan-out multicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being strictly nonblocking for unicast traffic (col. 2, lines 9-11, see Fig. 9) and rearrangeably nonblocking for arbitrary fan-out multicast traffic (col. 4, lines 6-7; see 'fanouts', Fig. 7B).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be strictly nonblocking for unicast traffic and rearrangeably nonblocking for arbitrary fan-out multicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 39, Wong discloses d = 4 ('plurality of input terminals and a number of output terminals', claim 1) and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit

block connecting said backward connecting links and said routing network is a multi-link butterfly fat tree network with full bandwidth ('8x8 Benes network' (each switch has two logic cells that are 2x2. hence 8x8 is 4 switches; 'butterfly pattern'; col. 13, lines 23-24); col 2, lines 31-33; col. 6, lines 7-9), but does not discloses said routing network is strictly nonblocking for arbitrary fan-out multicast. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network strictly nonblocking for arbitrary fan-out multicast traffic (col. 2, lines 8-11; see 'fanouts', Fig. 7B).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be strictly nonblocking for arbitrary fan-out multicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 41, Wong discloses d = 4 ('plurality of input terminals and a number of output terminals', claim 1) and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links (col. 2, lines 27-30; col. 2, lines 31-33) and said routing network is a generalized multi-link multi-stage network with full bandwidth ('networks can be generalized'; col. 6, lines 7-9), but does not disclose said routing network is rearrangeably nonblocking for unicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network

being rearrangeably nonblocking for unicast traffic ('rearrangeably nonblocking for unicast traffic'; col. 2, lines 52-54).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be rearrangeably nonblocking for unicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 42, Wong discloses d = 4 ('plurality of input terminals and a number of output terminals', claim 1) and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links ('8x8 Benes network' (each switch has two logic cells that are 2x2, hence 8x8 is 4 switches); col. 2, lines 31-33; col. 6, lines 7-9) and said routing network is a generalized multi-link multi-stage network ('networks can be generalized'; col. 6, lines 7-9), but does not disclose said routing network is strictly nonblocking for unicast and rearrangeably nonblocking for arbitrary fan-out multicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being strictly nonblocking for unicast traffic (col. 2, lines 9-11, see Fig. 9) and rearrangeably nonblocking for arbitrary fan-out multicast traffic (col. 4, lines 6-7; see "fanouts', Fig. 7B).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be strictly nonblocking for unicast traffic and rearrangeably nonblocking for

arbitrary fan-out multicast traffic, as disclosed by Wu, In order to satisfy specific routing requirements.

In claim 43, Wong discloses d = 4 ('plurality of input terminals and a number of output terminals', claim 1) and there are at least three switches in each said stage in each said sub-integrated circuit connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is a generalized multi-link multistage network with full bandwidth ('8x8 Benes network' (each switch has two logic cells that are 2x2, hence 8x8 is 4 switches); col. 2, lines 31-33; col. 6, lines 7-9; 'networks can be generalized'; col. 6, lines 7-9), but does not disclose said routing network is strictly nonblocking for arbitrary fan-out multicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network strictly nonblocking for arbitrary fan-out multicast traffic (col. 2, lines 8-11; see 'fanouts', Fig. 7B).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be strictly nonblocking for arbitrary fan-out multicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 45, Wong discloses d = 4 ('plurality of input terminals and a number of output terminals', claim 1} and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said

backward connecting links and said routing network is a generalized multi-link butterfly fat tree network with full bandwidth (col. 2, lines 27-30; col. 2, lines 31-33; 'networks can be generalized'; col. 6, lines 7-9; 'butterfly pattern'; col. 13, lines 23-24), but does not disclose said routing network is rearrangeably nonblocking for unicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeeble non-blocking switch (Abstract) and a routing network being rearrangeably nonblocking for unicast traffic ('rearrangeably nonblocking for unicast traffic'; col. 2, lines 52-54).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be rearrangeably nonblocking for unicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 46, Wong discloses d = 4 ('plurality of input terminals and a number of output terminals', claim 1) and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network generalized multi-link butterfly fat tree network with full bandwidth ('8x8 Benes network' (each switch has two logic cells that are 2x2, hence 8x8 is 4 switches); col. 2, lines 31-33; col. 6, lines 7-9; networks can be generalized'; col. 6, lines 7-9; 'butterfly pattern'; col. 13, lines 23-24), but does not disclose said routing network is strictly nonblocking for unicast traffic and rearrangeably nonblocking for arbitrary fan-out multicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a

routing network being strictly nonblocking for unicast traffic (col. 2, lines 9-11, see Fig. 9) and rearrangeably nonblocking for arbitrary fan-out multicast traffic (col. 4, lines 6-7; see 'fanouts', Fig. 7B).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be strictly nonblocking for unicast traffic and rearrangeably nonblocking for arbitrary fan-out multicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 47, Wong discloses d = 4 ('plurality of input terminals and a number of output terminals', claim 1) and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is a generalized multilink butterfly fat tree network with full bandwidth ('8x8 Benes network' (each switch has two logic cells that are 2x2, hence 8x8 is 4 switches); col. 2, lines 31-33; col. 6, lines 7-9; networks can be generalized'; col. 6, lines 7-9; 'butterfly pattern'; Col. 13, Lines 23-24), but does not disclose said routing network is strictly nonblocking for arbitrary fan-out multicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network strictly nonblocking for arbitrary fan-out multicast traffic (col. 2, lines 8-11; see 'fanouts', Fig. 7B).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be strictly nonblocking for arbitrary fan-out multicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571)272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shawki Ismail can be reached on (571) 272-3985. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Vibol Tan/
Primary Examiner, Art Unit 2819

Notice of References Cited	Application/Control No. 12/601,275	Applicant(s)/Patent Under Reexamination KONDA, VENKAT	
	Examiner Vibol Tan	Art Unit 2819	Page 1 of 2

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*	B	US-7,154,887	12-2006	Wu et al.	370/388
*	C	US-8,098,081	01-2012	Trimberger, Stephen M.	326/41
*	D	US-7,924,052	04-2011	Feng et al.	326/41
*	E	US-7,468,974	12-2008	Carr et al.	370/388
*	F	US-7,424,011	09-2008	Konda, Venkat	370/388
*	G	US-7,424,010	09-2008	Konda, Venkat	370/388
*	H	US-7,136,380	11-2006	Li, Shuo-Yen Robert	370/388
*	I	US-7,397,796	07-2008	Smiljani , Aleksandra	370/390
*	J	US-7,349,387	03-2008	Wu, Ephrem C.	370/360
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*	L	US-7,130,920	10-2006	Sailor, Kenneth Evert	709/238
*	M	US-6,567,858	05-2003	Yang et al.	709/238

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	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

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Notice of References Cited	Application/Control No. 12/601,275	Applicant(s)/Patent Under Reexamination KONDA, VENKAT	
	Examiner Vibol Tan	Art Unit 2819	Page 2 of 2

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	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	V	
	W	
	X	

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Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	35	(US-20080267182-$ or US-20040114586-$ or US-20030021267-$ or US-20030112797-$ or US-20030053456-$ or US-20020051447-$ or US-20020031118-$ or US-20020031117-$).did. or (US-8098081-$ or US-7924052-$ or US-7468974-$ or US-7424011-$ or US-7424010-$ or US-7397796-$ or US-7349387-$ or US-7346049-$ or US-7130920-$ or US-6567858-$ or US-7136380-$ or US-6456838-$ or US-6157643-$ or US-6049542-$ or US-5856977-$ or US-5406556-$ or US-4813038-$ or US-7139266-$ or US-7103059-$ or US-7099314-$ or US-7065074-$ or US-7050429-$ or US-7042873-$ or US-7031303-$ or US-7016345-$ or US-6952418-$).did. or (US-6201808-$).did.	US-PGPUB; USPAT	OR	OFF	2012/02/02 10:27
S1	2	(("6940308") or ("7154887")).PN.	USPAT; USOCR	OR	OFF	2012/02/01 07:26
S2	3	(("6940308") or ("7154887") or ("20110037498")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/02/01 07:30
S3	81	nonblocking adj multicast	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 08:51
S4	46	non-blocking adj multicast	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 08:51
S5	8	non-blocking adj multi-cast	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 08:52
S6	111	S3 S4 S5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2012/02/02 08:52

			IBM_TDB			
S7	35	S6 and rearrangeably	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 08:53
S8	21	S6 and rearrangeable	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 08:53
S9	39	S7 S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 08:53
S10	2	(routing adj network) same (inlet adj links) same (outlet adj links)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 09:18
S11	173	(routing adj network) same (inputs) same (outputs)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 09:19
S12	223328	(("326") or ("370")).CLAS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 09:22
S13	108	S11 and S12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 09:22
S14	0	(routing adj network) same (inputs) same (outputs) same (higher adj stage) same (lower adj stage)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 09:31
S15	1	(routing adj network) and (inputs) and (outputs) and (higher adj stage) and (lower adj stage)	US-PGPUB; USPAT; USOCR; FPRS;	OR	OFF	2012/02/02 09:31

			EPO; JPO; DERWENT; IBM_TDB			
S16	2	(routing adj network) and (higher adj stage) and (lower adj stage)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 09:31
S17	24	(routing adj network) and (cross adj links)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 09:32
S18	5	(routing adj network) and (cross adj switches)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 09:32
S19	26	S17 S18	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 09:33
S20	882	(routing adj network) and stages	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 09:37
S21	20	(US-20080267182-$ or US-20040114586-$ or US-20030021267-$).did. or (US-8098081-$ or US-7924052-$ or US-7468974-$ or US-7424011-$ or US-7424010-$ or US-7397796-$ or US-7349387-$ or US-7346049-$ or US-7130920-$ or US-6567858-$ or US-7136380-$ or US-6456838-$ or US-6157643-$ or US-6049542-$ or US-5856977-$ or US-5406556-$ or US-4813038-$).did.	US-PGPUB; USPAT	OR	OFF	2012/02/02 09:39
S22	41	konda-venkat.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 09:40
S23	84	(routing adj network) and (multicast adj connections)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	OFF	2012/02/02 09:45

			DERWENT; IBM_TDB			

EAST Search History (Interference)

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12601275	KONDA, VENKAT
	Examiner	Art Unit
	VIBOL TAN	2819

SEARCHED			
Class	Subclass	Date	Examiner
326	38-41	2/2/12	VTan
370	390, 312, 360, 388, 412	2/2/12	VTan

SEARCH NOTES		
Search Notes	Date	Examiner
Inventor search	2/2/12	VTan
search report pct/us2008/064605	2/1/12	VTan
EAST text search	2/2/12	VTan

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/601,275	05/31/2010	Venkat Konda	V-0045US

CONFIRMATION NO. 6372

38139
Konda Technologies, Inc
6278 GRAND OAK WAY
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PUBLICATION NOTICE

OC000000046063228

Title:VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS

Publication No.US-2011-0037498-A1
Publication Date:02/17/2011

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

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U.S. APPLICATION NUMBER NO.	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
12/601,275	Venkat Konda	V-0045US

38139
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6278 GRAND OAK WAY
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INTERNATIONAL APPLICATION NO.	
PCT/US08/64605	
I.A. FILING DATE	PRIORITY DATE
05/22/2008	05/25/2007

CONFIRMATION NO. 6372
371 ACCEPTANCE LETTER

OC000000043058811

Date Mailed: 11/09/2010

NOTICE OF ACCEPTANCE OF APPLICATION UNDER 35 U.S.C 371 AND 37 CFR 1.495

The applicant is hereby advised that the United States Patent and Trademark Office in its capacity as a Designated / Elected Office (37 CFR 1.495), has determined that the above identified international application has met the requirements of 35 U.S.C. 371, and is ACCEPTED for national patentability examination in the United States Patent and Trademark Office.

The United States Application Number assigned to the application is shown above and the relevant dates are:

05/31/2010	05/31/2010
DATE OF RECEIPT OF 35 U.S.C. 371(c)(1), (c)(2) and (c)(4) REQUIREMENTS	DATE OF COMPLETION OF ALL 35 U.S.C. 371 REQUIREMENTS

A Filing Receipt (PTO-103X) will be issued for the present application in due course. **THE DATE APPEARING ON THE FILING RECEIPT AS THE " FILING DATE" IS THE DATE ON WHICH THE LAST OF THE 35 U.S.C. 371 (c)(1), (c)(2) and (c)(4) REQUIREMENTS HAS BEEN RECEIVED IN THE OFFICE. THIS DATE IS SHOWN ABOVE.** *The filing date of the above identified application is the international filing date of the international application (Article 11(3) and 35 U.S.C. 363).* Once the Filing Receipt has been received, send all correspondence to the Group Art Unit designated thereon.

The following items have been received:

- Indication of Small Entity Status
- Copy of the International Application filed on 11/22/2009
- Copy of the International Search Report filed on 11/22/2009
- Oath or Declaration filed on 05/31/2010
- U.S. Basic National Fees filed on 11/22/2009
- Specification filed on 11/22/2009
- Claims filed on 11/22/2009
- Abstracts filed on 11/22/2009
- Drawings filed on 11/22/2009

FORM PCT/DO/EO/903 (371 Acceptance Notice)

Applicant is reminded that any communications to the United States Patent and Trademark Office must be mailed to the address given in the heading and include the U.S. application no. shown above (37 CFR 1.5)

NISA F GILCHRIST

Telephone: (703) 756-1418

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/601,275	05/31/2010	2819	1279	V-0045US	49	1

CONFIRMATION NO. 6372

38139
Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

FILING RECEIPT

OC000000043058810

Date Mailed: 11/09/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Venkat Konda, San Jose, CA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/US08/64605 05/22/2008
which claims benefit of 60/940,394 05/25/2007

Foreign Applications

If Required, Foreign Filing License Granted: 04/08/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/601,275**

Projected Publication Date: 02/17/2011

Non-Publication Request: No

Early Publication Request: No
**** SMALL ENTITY ****

Title

VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS

Preliminary Class

326

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as

set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/601,275	05/31/2010		1279	V-0045US	49	1

CONFIRMATION NO. 6372

38139
Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

FILING RECEIPT

Date Mailed: 08/18/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Venkat Konda, San Jose, CA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/US08/64605 05/22/2008
which claims benefit of 60/940,394 05/25/2007

Foreign Applications

If Required, Foreign Filing License Granted: 04/08/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/601,275**

Projected Publication Date: 371 Perfected

Non-Publication Request: No

Early Publication Request: No
**** SMALL ENTITY ****

Title

VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS

Preliminary Class

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

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NOT GRANTED

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UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

U.S. APPLICATION NUMBER NO.	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
12/601,275	Venkat Konda	V-0045US

38139
Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

INTERNATIONAL APPLICATION NO.	
PCT/US08/64605	
I.A. FILING DATE	PRIORITY DATE
05/22/2008	05/25/2007

CONFIRMATION NO. 6372
371 ACCEPTANCE LETTER

OC000000043058811

Date Mailed: 08/18/2010

NOTICE OF ACCEPTANCE OF APPLICATION UNDER 35 U.S.C 371 AND 37 CFR 1.495

The applicant is hereby advised that the United States Patent and Trademark Office in its capacity as a Designated / Elected Office (37 CFR 1.495), has determined that the above identified international application has met the requirements of 35 U.S.C. 371, and is ACCEPTED for national patentability examination in the United States Patent and Trademark Office.

The United States Application Number assigned to the application is shown above and the relevant dates are:

05/31/2010	05/31/2010
DATE OF RECEIPT OF 35 U.S.C. 371(c)(1), (c)(2) and (c)(4) REQUIREMENTS	DATE OF COMPLETION OF ALL 35 U.S.C. 371 REQUIREMENTS

A Filing Receipt (PTO-103X) will be issued for the present application in due course. **THE DATE APPEARING ON THE FILING RECEIPT AS THE " FILING DATE" IS THE DATE ON WHICH THE LAST OF THE 35 U.S.C. 371 (c)(1), (c)(2) and (c)(4) REQUIREMENTS HAS BEEN RECEIVED IN THE OFFICE. THIS DATE IS SHOWN ABOVE.** *The filing date of the above identified application is the international filing date of the international application (Article 11(3) and 35 U.S.C. 363).* Once the Filing Receipt has been received, send all correspondence to the Group Art Unit designated thereon.

The following items have been received:

- Indication of Small Entity Status
- Copy of the International Application filed on 11/22/2009
- Copy of the International Search Report filed on 11/22/2009
- Oath or Declaration filed on 05/31/2010
- U.S. Basic National Fees filed on 11/22/2009
- Specification filed on 11/22/2009
- Claims filed on 11/22/2009
- Abstracts filed on 11/22/2009
- Drawings filed on 11/22/2009

FORM PCT/DO/EO/903 (371 Acceptance Notice)

Applicant is reminded that any communications to the United States Patent and Trademark Office must be mailed to the address given in the heading and include the U.S. application no. shown above (37 CFR 1.5)

NISA F GILCHRIST

Telephone: (703) 756-1418

PTO/SB/01 (04-09)
Approved for use through 06/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

☐ Declaration Submitted With Initial Filing OR ☒ Declaration Submitted After Initial Filing (surcharge (37 CFR 1.16(f)) required)

Attorney Docket Number	
First Named Inventor	Venkat Konda
COMPLETE IF KNOWN	
Application Number	12/601,275
Filing Date	11/22/2009
Art Unit	
Examiner Name	

I hereby declare that: (1) Each inventor's residence, mailing address, and citizenship are as stated below next to their name; and (2) I believe the inventor(s) named below to be the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention titled:

VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS

(Title of the Invention)

the application of which

☐ is attached hereto

OR

☒ was filed on (MM/DD/YYYY) 11/22/2009 as United States Application Number or PCT International Application Number 12/601,275 and was amended on (MM/DD/YYYY) _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified application, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

Authorization To Permit Access To Application by Participating Offices

☒ If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the above-identified patent application is filed access to the above-identified patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the above-identified patent application is filed to have access to the above-identified patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the above-identified patent application with respect to: 1) the above-identified patent application-as-filed; 2) any foreign application to which the above-identified patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the above-identified patent application; and 3) any U.S. application-as-filed from which benefit is sought in the above-identified patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing the Authorization to Permit Access to Application by Participating Offices.

DECLARATION — Utility or Design Patent Application

Claim of Foreign Priority Benefits

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
PCT/US08/64605	USA	5/22/2008	☐	☐	☒
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application number(s) are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

PTO/SB/01 (04-09)
Approved for use through 06/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

DECLARATION — Utility or Design Patent Application

Direct all correspondence to:	☒	The address associated with Customer Number:	38139	**OR** ☐	Correspondence address below

Name		
Address		
City	State	Zip
Country	Telephone	Email

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available. Petitioner/applicant is advised that documents which form the record of a patent application (such as the PTO/SB/01) are placed into the Privacy Act system of records DEPARTMENT OF COMMERCE, COMMERCE-PAT-7, System name: *Patent Application Files*. Documents not retained in an application file (such as the PTO-2038) are placed into the Privacy Act system of COMMERCE/PAT-TM-10, System name: *Deposit Accounts and Electronic Funds Transfer Profiles*.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

NAME OF SOLE OR FIRST INVENTOR:	☐ A petition has been filed for this unsigned inventor
Given Name (first and middle [if any])	Family Name or Surname
Venkat	Konda
Inventor's Signature	Date
/Venkat Konda/	5/30/2010

Residence: City	State	Country	Citizenship
San Jose	CA	USA	USA

Mailing Address			
6278 Grand Oak Way			
City	State	Zip	Country
San Jose	CA	95135	USA

☐ Additional inventors or a legal representative are being named on the _____ supplemental sheet(s) PTO/SB/02A or 02LR attached hereto

Electronic Patent Application Fee Transmittal

Application Number:	12601275
Filing Date:	
Title of Invention:	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Filer:	Venkar Konda
Attorney Docket Number:	V-0045US

Filed as Small Entity

U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Natl Stage Search Fee - U.S. was the ISA	2641	1	50	50
Natl Stage Exam Fee - all other cases	2633	1	110	110
Pages:				
Claims:				
Miscellaneous-Filing:				
Oath/decl > 30 mo. from priority date	2617	1	65	65
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**225**

Electronic Acknowledgement Receipt

EFS ID:	7714705
Application Number:	12601275
International Application Number:	
Confirmation Number:	6372
Title of Invention:	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Customer Number:	38139
Filer:	Venkar Konda
Filer Authorized By:	
Attorney Docket Number:	V-0045US
Receipt Date:	31-MAY-2010
Filing Date:	
Time Stamp:	02:44:41
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$225
RAM confirmation Number	6077
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Application Data Sheet	sb0001.pdf	813566 367e6d42d0fb354656cf1c0bddd5d1c98b7ef69f	no	3
Warnings:					
Information:					
This is not an USPTO supplied ADS fillable form					
2	Fee Worksheet (PTO-875)	fee-info.pdf	33177 4bb705ab794b5cc83faa09fbadf2ba145c30903a	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	846743	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

MULTIPLE DEPENDENT CLAIM FEE CALCULATION SHEET

(FOR USE WITH FORM PTO-875)

SERIAL NO. 12-601,275

FILING DATE

APPLICANT(S)

CLAIMS

	AS FILED		AFTER 1ST AMENDMENT		AFTER 2ND AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
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TOTAL IND.	1	⬇		⬇		⬇
TOTAL DEP.	48	⬅		⬅		⬅
TOTAL CLAIMS	49					

	AS FILED		AFTER 1ST AMENDMENT		AFTER 2ND AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
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TOTAL IND.		⬇		⬇		⬇
TOTAL DEP.		⬅		⬅		⬅
TOTAL CLAIMS						

PTO - 1360 (REV. 11/04)

U.S. DEPARTMENT of COMMERCE
Patent and Trademark Office

PATENT APPLICATION FEE DETERMINATION RECORD

Effective September 30,2007

Application or Docket Number: 12-601,275

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
U.S. NATIONAL STAGE FEES		
BASIC FEE	SMALL ENT. = $155	LARGE ENT. = $ 310
EXAMINATION FEE	Satisfies PCT Article 33(1)-(4) = $ 50 / $ 100	All other situations = $ 100 / $ 200
SEARCH FEE	U.S. is ISA = $ 50 / $ 100 ALL other countries = $ 205 / $ 410	ALL other situations = $ 255 / $ 510
FEE FOR EXTRA SPEC. PGS.	107 minus 100 =	7 / 50 = 1
TOTAL CHARGEABLE CLAIMS	49 minus 20 =	* 29
INDEPENDENT CLAIMS	1 minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐	RATE	FEE	OR	OTHER THAN SMALL ENTITY	RATE	FEE
	BASIC FEE	165	OR		BASIC FEE	
	EXAM. FEE	110			EXAM. FEE	
	SEARCH FEE	50			SEARCH FEE	
	X$130 ~~130~~	135			X$260	
	X $ ~~25~~ =	754	OR		X $ 50 =	
	X $ 105 =		OR		X $ 210=	
	$185		OR		$370	
	TOTAL	1214	OR		TOTAL	

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY RATE	ADDI-TIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDI-TIONAL FEE
X $ 25 =		OR	X $ 50 =	
X$105		OR	X$210	
$185		OR	$370	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDI-TIONAL FEE	OR	RATE	ADDI-TIONAL FEE
X $ 25 =		OR	X $ 50 =	
X$105		OR	X$210	
$185		OR	$370	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than '20', enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than '3', enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

U.S. APPLICATION NUMBER NO.	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
12/601,275	Venkat Konda	V-0045US

38139
Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

INTERNATIONAL APPLICATION NO.	
PCT/US08/64605	
I.A. FILING DATE	PRIORITY DATE
05/22/2008	05/25/2007

CONFIRMATION NO. 6372
371 FORMALITIES LETTER

OC000000041041187

Date Mailed: 04/08/2010

NOTIFICATION OF MISSING REQUIREMENTS UNDER 35 U.S.C. 371 IN THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US)

The following items have been submitted by the applicant or the IB to the United States Patent and Trademark Office as a Designated Office (37 CFR 1.494):

- Indication of Small Entity Status
- Priority Document
- Copy of the International Application filed on 11/22/2009
- Copy of the International Search Report filed on 11/22/2009
- Oath or Declaration filed on 11/22/2009
- U.S. Basic National Fees filed on 11/22/2009
- Specification filed on 11/22/2009
- Claims filed on 11/22/2009
- Abstracts filed on 11/22/2009
- Drawings filed on 11/22/2009

The applicant needs to satisfy supplemental fees problems indicated below.

The following items **MUST** be furnished within the period set forth below in order to complete the requirements for acceptance under 35 U.S.C. 371:

- Oath or declaration of the inventors, in compliance with 37 CFR 1.497(a) and (b), identifying the application by the International application number and international filing date.
- Oath or declaration of the inventors, in compliance with 37 CFR 1.497(a) and (b), identifying the application by the International application number and international filing date. The current oath or declaration does not comply with 37 CFR 1.497(a) and (b) in that it:
  - THE PTO/SB/01A OATH REQUIRES AN APPLICATION DATA SHEET.(37 CFR 1.76)
- To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.492(h) of $65 for a small entity in compliance with 37 CFR 1.27, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fees required for this application is $**225** for a Small Entity:

- $**65** Surcharge.
- The application search fee has not been paid. Applicant must submit $**50** to complete the search fee. Note a surcharge will be required if submitted later than commencement of the national stage (37 CFR 1.492(h)) and the basic national fee was not paid before July 1, 2005.

FORM PCT/DO/EO/905 (371 Formalities Notice)

- The application examination fee has not been paid. Applicant must submit $**110** to complete the examination fee for a small entity in compliance with 37 CFR 1.27. Note a surcharge will be required if submitted later than commencement of the national stage (37 CFR 1.492(h)) and the basic national fee was not paid before July 1, 2005.

ALL OF THE ITEMS SET FORTH ABOVE MUST BE SUBMITTED WITHIN TWO (2) MONTHS FROM THE DATE OF THIS NOTICE OR BY 32 MONTHS FROM THE PRIORITY DATE FOR THE APPLICATION, WHICHEVER IS LATER. FAILURE TO PROPERLY RESPOND WILL RESULT IN ABANDONMENT.

The time period set above may be extended by filing a petition and fee for extension of time under the provisions of 37 CFR 1.136(a).

Applicant is reminded that any communications to the United States Patent and Trademark Office must be mailed to the address given in the heading and include the U.S. application no. shown above (37 CFR 1.5)

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

ANITA D JOHNSON

Telephone: (571) 272-0386

Electronic Patent Application Fee Transmittal

Application Number:	12601275
Filing Date:	
Title of Invention:	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Filer:	Venkar Konda
Attorney Docket Number:	V-0045US

Filed as Small Entity

U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Basic National Stage Fee	2631	1	165	165
Pages:				
Natl Stage Appl Sz fee per 50 pgs >100	2681	1	135	135
Claims:				
Claims in excess of 20	2615	29	26	754
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1054**

Electronic Acknowledgement Receipt

EFS ID:	6694837
Application Number:	12601275
International Application Number:	
Confirmation Number:	6372
Title of Invention:	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Customer Number:	38139
Filer:	Venkar Konda
Filer Authorized By:	
Attorney Docket Number:	V-0045US
Receipt Date:	22-DEC-2009
Filing Date:	
Time Stamp:	19:05:08
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1054
RAM confirmation Number	6404
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Fee Worksheet (PTO-875)	fee-info.pdf	33527 86105945f3d107d6a07e8ca63ed220c3f09331a7	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	33527

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/05 (08-08)
Approved for use through 06/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office. U.S. DEPARTMENT OF COMMERCE

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	V-0045 US
First Inventor	Venkat Konda
Title	
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☑ **Fee Transmittal Form** (e.g., PTO/SB/17)
2. ☑ **Applicant claims small entity status.** See 37 CFR 1.27.
3. ☑ **Specification** [*Total Pages* 68]
   Both the claims and abstract must start on a new page
   (For information on the preferred arrangement, see MPEP 608.01(a))
4. ☑ **Drawing(s)** (*35 U.S.C. 113*) [*Total Sheets* 39]
5. **Oath or Declaration** [*Total Sheets* 1]
   a. ☑ Newly executed (original or copy)
   b. ☐ A copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 18 completed)
   i. ☐ DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) name in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. ☑ **Application Data Sheet.** See 37 CFR 1.76
7. ☐ **CD-ROM or CD-R** in duplicate, large table or Computer Program *(Appendix)*
   ☐ Landscape Table on CD
8. **Nucleotide and/or Amino Acid Sequence Submission**
   (if applicable, items a. – c. are required)
   a. ☐ Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ Paper
   c. ☐ Statements verifying identity of above copies

ADDRESS TO: **Commissioner for Patents**
P.O. Box 1450
Alexandria VA 22313-1450

ACCOMPANYING APPLICATION PARTS

9. ☐ **Assignment Papers** (cover sheet & document(s))
   Name of Assignee Konda Technologies Inc.
10. ☐ **37 CFR 3.73(b) Statement** *(when there is an assignee)* ☐ **Power of Attorney**
11. ☐ **English Translation Document** *(if applicable)*
12. ☐ **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
    ☐ Copies of citations attached
13. ☐ **Preliminary Amendment**
14. ☐ **Return Receipt Postcard** (MPEP 503)
    (*Should be specifically itemized)*
15. ☐ **Certified Copy of Priority Document(s)**
    (if foreign priority is claimed)
16. ☐ **Nonpublication Request** under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
17. ☐ Other:

18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76:*

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: .....

Prior application information: *Examiner* _____ *Art Unit:* _____

19. CORRESPONDENCE ADDRESS

☑ The address associated with Customer Number: 38139 ***OR*** ☐ Correspondence address below

Name	Venkat Konda				
Address	6278 Grand Oak Way				
City	San Jose	State	CA	Zip Code	95135
Country	USA	Telephone	408-472-3273	Email	venkat@kondatech.com

Signature	/Venkat Konda/	Date	11/22/2009
Name (Print/Type)	Venkat Konda	Registration No. (Attorney/Agent)	

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/01A (01-09)
Approved for use through 06/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS

As the below named inventor(s), I/we declare that:

This declaration is directed to:

☒ The attached application, or

☐ Application No. _____ filed on _____

☐ As amended on _____ (if applicable);

I/we believe that I/we am/are the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought;

I/we have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment specifically referred to above;

I/we acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me/us to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

All statements made herein of my/our own knowledge are true, all statements made herein on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and may jeopardize the validity of the application or any patent issuing thereon.

FULL NAME OF INVENTOR(S)

Inventor one: Venkat Konda Date: 11/22/2009

Signature: /Venkat Konda/ Citizen of: USA

Inventor two: _____ Date: _____

Signature: _____ Citizen of: _____

☐ Additional inventors or a legal representative are being named on _____ additional form(s) attached hereto.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Filer:	Venkar Konda
Attorney Docket Number:	V-0045US

Filed as Small Entity

U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Basic National Stage Fee	2631	1	165	165
Natl Stage Search - U.S. as IPEA or ISA	2640	1	0	0
Pages:				
Natl Stage Appl Sz fee per 50 pgs >100	2681	1	135	135
Claims:				
Claims in excess of 20	2615	29	26	754
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1054**

Electronic Acknowledgement Receipt

EFS ID:	6501767
Application Number:	12601275
International Application Number:	PCT/US08/64605
Confirmation Number:	6372
Title of Invention:	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Customer Number:	38139
Filer:	Venkar Konda
Filer Authorized By:	
Attorney Docket Number:	V-0045US
Receipt Date:	22-NOV-2009
Filing Date:	
Time Stamp:	23:28:30
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Specification	V-0045US.pdf	299380 debb4d8182a1df928e5922e1c44142090bba7555	no	69

Warnings:	
Information:	

2	Drawings-only black and white line drawings	V-0045US-FIGs.pdf	581351 9345637693e597fd4d92e2aa679baa691e95ca78	no	39
Warnings:					
Information:					
3	Transmittal of New Application	sb0005_fill.pdf	468829 959ba37f3439c0e68be3c2ba5915c1a196e60d2f	no	2
Warnings:					
Information:					
4	Application Data Sheet	sb0001a.pdf	545678 6fdc91490275bb543e412eafc4cd318937bc0281	no	2
Warnings:					
Information:					
This is not an USPTO supplied ADS fillable form					
5	Fee Worksheet (PTO-875)	fee-info.pdf	36986 f3996036a9d41e6a4b815016dd7db9f3066caa82	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1932224		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS

Venkat Konda

CROSS REFERENCE TO RELATED APPLICATIONS

This application is related to and claims priority of the PCT Application Serial No. PCT/US08/64605 entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 22, 2008, and the U.S. Provisional Patent Application Serial No. 60/940, 394 entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

This application is related to and incorporates by reference in its entirety the US Application Serial No. 12/530,207 entitled "FULLY CONNECTED GENERALIZED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed September 6, 2009, the PCT Application Serial No. PCT/US08/56064 entitled "FULLY CONNECTED GENERALIZED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed March 6, 2008, the U.S. Provisional Patent Application Serial No. 60/905,526 entitled "LARGE SCALE CROSSPOINT REDUCTION WITH NONBLOCKING UNICAST & MULTICAST IN ARBITRARILY LARGE MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed March 6, 2007, and the U.S. Provisional Patent Application Serial No. 60/940, 383 entitled "FULLY CONNECTED GENERALIZED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

This application is related to and incorporates by reference in its entirety the US Patent Application Docket No. V-0038US entitled "FULLY CONNECTED GENERALIZED BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application filed concurrently, the PCT Application Serial No. PCT/US08/64603 entitled "FULLY CONNECTED GENERALIZED BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 22, 2008, the U.S. Provisional Patent Application Serial No. 60/940, 387 entitled "FULLY CONNECTED GENERALIZED BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007, and the U.S. Provisional Patent Application Serial No. 60/940, 390 entitled "FULLY CONNECTED GENERALIZED MULTI-LINK BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

This application is related to and incorporates by reference in its entirety the US Patent Application Docket No. V-0039US entitled "FULLY CONNECTED GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application filed concurrently, the PCT Application Serial No. PCT/US08/64604 entitled "FULLY CONNECTED GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 22, 2008, the U.S. Provisional Patent Application Serial No. 60/940, 389 entitled "FULLY CONNECTED GENERALIZED REARRANGEABLY NONBLOCKING MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007, the U.S. Provisional Patent Application Serial No. 60/940, 391 entitled "FULLY CONNECTED GENERALIZED FOLDED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007 and the U.S. Provisional Patent Application Serial No. 60/940, 392 entitled "FULLY CONNECTED GENERALIZED STRICTLY NONBLOCKING MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

This application is related to and incorporates by reference in its entirety the U.S. Provisional Patent Application Serial No. 61/252, 603 entitled "VLSI LAYOUTS OF FULLY CONNECTED NETWORKS WITH LOCALITY EXPLOITATION" by Venkat Konda assigned to the same assignee as the current application, filed October 16, 2009.

This application is related to and incorporates by reference in its entirety the U.S. Provisional Patent Application Serial No. 61/252, 609 entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED AND PYRAMID NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed October 16, 2009.

BACKGROUND OF INVENTION

Multi-stage interconnection networks such as Benes networks and butterfly fat tree networks are widely useful in telecommunications, parallel and distributed computing. However VLSI layouts, known in the prior art, of these interconnection networks in an integrated circuit are inefficient and complicated.

Other multi-stage interconnection networks including butterfly fat tree networks, Banyan networks, Batcher-Banyan networks, Baseline networks, Delta networks, Omega networks and Flip networks have been widely studied particularly for self routing packet switching applications. Also Benes Networks with radix of two have been widely studied and it is known that Benes Networks of radix two are shown to be built with back to back baseline networks which are rearrangeably nonblocking for unicast connections.

The most commonly used VLSI layout in an integrated circuit is based on a two-dimensional grid model comprising only horizontal and vertical tracks. An intuitive interconnection network that utilizes two-dimensional grid model is 2D Mesh Network and its variations such as segmented mesh networks. Hence routing networks used in VLSI layouts are typically 2D mesh networks and its variations. However Mesh Networks require large scale cross points typically with a growth rate of $O(N^2)$ where N is the number of computing elements, ports, or logic elements depending on the application.

Multi-stage interconnection with a growth rate of $O(N \times \log N)$ requires significantly small number of cross points. U.S. Patent 6,185,220 entitled "Grid Layouts of Switching and Sorting Networks" granted to Muthukrishnan et al. describes a VLSI layout using existing VLSI grid model for Benes and Butterfly networks. U.S. Patent 6,940,308 entitled "Interconnection Network for a Field Programmable Gate Array" granted to Wong describes a VLSI layout where switches belonging to lower stage of Benes Network are layed out close to the logic cells and switches belonging to higher stages are layed out towards the center of the layout.

Due to the inefficient and in some cases impractical VLSI layout of Benes and butterfly fat tree networks on a semiconductor chip, today mesh networks and segmented mesh networks are widely used in the practical applications such as field programmable gate arrays (FPGAs), programmable logic devices (PLDs), and parallel computing interconnects. The prior art VLSI layouts of Benes and butterfly fat tree networks and VLSI layouts of mesh networks and segmented mesh networks require large area to implement the switches on the chip, large number of wires, longer wires, with increased power consumption, increased latency of the signals which effect the maximum clock speed of operation. Some networks may not even be implemented practically on a chip due to the lack of efficient layouts.

SUMMARY OF INVENTION

When large scale sub-integrated circuit blocks with inlet and outlet links are layed out in an integrated circuit device in a two-dimensional grid arrangement, (for example in an FPGA where the sub-integrated circuit blocks are Lookup Tables) the most intuitive routing network is a network that uses horizontal and vertical links only (the most often used such a network is one of the variations of a 2D Mesh network). A direct embedding of a generalized multi-stage network on to a 2D Mesh network is neither simple nor efficient.

In accordance with the invention, VLSI layouts of generalized multi-stage networks for broadcast, unicast and multicast connections are presented using only

horizontal and vertical links. The VLSI layouts employ shuffle exchange links where outlet links of cross links from switches in a stage in one sub-integrated circuit block are connected to inlet links of switches in the succeeding stage in another sub-integrated circuit block so that said cross links are either vertical links or horizontal and vice versa. In one embodiment the sub-integrated circuit blocks are arranged in a hypercube arrangement in a two-dimensional plane. The VLSI layouts exploit the benefits of significantly lower cross points, lower signal latency, lower power and full connectivity with significantly fast compilation.

The VLSI layouts presented are applicable to generalized multi-stage networks $V(N_1, N_2, d, s)$, generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$, generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$, generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$, and generalized hypercube networks $V_{hcube}(N_1, N_2, d, s)$ for s = 1,2,3 or any number in general. The embodiments of VLSI layouts are useful in wide target applications such as FPGAs, CPLDs, pSoCs, ASIC placement and route tools, networking applications, parallel & distributed computing, and reconfigurable computing.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1A is a diagram 100A of an exemplary symmetrical multi-link multi-stage network $V_{fold-mlink}(N, d, s)$ having inverse Benes connection topology of nine stages with N = 32, d = 2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1B is a diagram 100B of the equivalent symmetrical folded multi-link multi-stage network $V_{fold-mlink}(N, d, s)$ of the network 100A shown in FIG. 1A, having inverse Benes connection topology of five stages with N = 32, d = 2 and s=2, strictly nonblocking

network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1C is a diagram 100C layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 1D is a diagram 100D layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links ML(1,i) for i = [1, 64] and ML(8,i) for i = [1,64].

FIG. 1E is a diagram 100E layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links ML(2,i) for i = [1, 64] and ML(7,i) for i = [1,64].

FIG. 1F is a diagram 100F layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links ML(3,i) for i = [1, 64] and ML(6,i) for i = [1,64].

FIG. 1G is a diagram 100G layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links ML(4,i) for i = [1, 64] and ML(5,i) for i = [1,64].

FIG. 1H is a diagram 100H layout of a network $V_{fold-mlink}(N,d,s)$ where N = 128, d = 2, and s = 2, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 1I is a diagram 100I detailed connections of BLOCK 1_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing $V(N,d,s)$ or $V_{fold}(N,d,s)$.

FIG. 1J is a diagram 100J detailed connections of BLOCK 1_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing $V(N,d,s)$ or $V_{fold}(N,d,s)$.

FIG. 1K is a diagram 100K detailed connections of BLOCK 1_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing $V(N,d,s)$ or $V_{fold}(N,d,s)$.

FIG. 1K1 is a diagram 100M1 detailed connections of BLOCK 1_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing $V(N,d,s)$ or $V_{fold}(N,d,s)$ for s = 1.

FIG. 1L is a diagram 100L detailed connections of BLOCK 1_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing $V(N,d,s)$ or $V_{fold}(N,d,s)$.

FIG. 1L1 is a diagram 100L1 detailed connections of BLOCK 1_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing $V(N,d,s)$ or $V_{fold}(N,d,s)$ for s = 1.

FIG. 2A1 is a diagram 200A1 of an exemplary symmetrical multi-link multi-stage network $V_{fold-mlink}(N,d,s)$ having inverse Benes connection topology of one stage with N = 2, d = 2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention. FIG. 2A2 is a diagram 200A2 of the equivalent symmetrical folded multi-link multi-stage network $V_{fold-mlink}(N,d,s)$ of the network 200A1 shown in FIG. 2A1, having inverse Benes connection topology of one stage with N = 2, d = 2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention. FIG. 2A3 is a diagram 200A3 layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 2A2, in one embodiment, illustrating all the connection links.

FIG. 2B1 is a diagram 200B1 of an exemplary symmetrical multi-link multi-stage network $V_{fold-mlink}(N,d,s)$ having inverse Benes connection topology of one stage with N = 4, d = 2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention. FIG. 2B2 is a diagram 200B2 of the equivalent symmetrical folded multi-link multi-stage network $V_{fold-mlink}(N,d,s)$ of the network 200B1 shown in FIG. 2B1, having inverse Benes connection topology of one stage with N = 4, d = 2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention. FIG. 2B3 is a diagram 200B3 layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 2B2, in one embodiment, illustrating the connection links belonging with in each block only. FIG. 2B4 is a diagram 200B4 layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 2B2, in one embodiment, illustrating the connection links ML(1,i) for i = [1, 8] and ML(2,i) for i = [1,8].

FIG. 2C11 is a diagram 200C11 of an exemplary symmetrical multi-link multi-stage network $V_{fold-mlink}(N,d,s)$ having inverse Benes connection topology of one stage with N = 8, d = 2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention. FIG. 2C12 is a diagram 200C12 of the equivalent symmetrical folded multi-link multi-stage network $V_{fold-mlink}(N,d,s)$ of the network 200C11 shown in FIG. 2C11, having inverse Benes connection topology of one stage with N = 8, d = 2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 2C21 is a diagram 200C21 layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 2C12, in one embodiment, illustrating the connection links belonging with in each block only. FIG. 2C22 is a diagram 200C22 layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 2C12, in one embodiment, illustrating the connection links ML(1,i) for i =

[1, 16] and ML(4,i) for i = [1,16]. FIG. 2C23 is a diagram 200C23 layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 2C12, in one embodiment, illustrating the connection links ML(2,i) for i = [1, 16] and ML(3,i) for i = [1,16].

FIG. 2D1 is a diagram 200D1 of an exemplary symmetrical multi-link multi-stage network $V_{fold-mlink}(N,d,s)$ having inverse Benes connection topology of one stage with N = 16, d = 2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 2D2 is a diagram 200D2 of the equivalent symmetrical folded multi-link multi-stage network $V_{fold-mlink}(N,d,s)$ of the network 200D1 shown in FIG. 2D1, having inverse Benes connection topology of one stage with N = 16, d = 2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 2D3 is a diagram 200D3 layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 2D2, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 2D4 is a diagram 200D4 layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 2D2, in one embodiment, illustrating the connection links ML(1,i) for i = [1, 32] and ML(6,i) for i = [1,32].

FIG. 2D5 is a diagram 200D5 layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 2D2, in one embodiment, illustrating the connection links ML(2,i) for i = [1, 32] and ML(5,i) for i = [1,32].

FIG. 2D6 is a diagram 200D6 layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 2D2, in one embodiment, illustrating the connection links ML(3,i) for i = [1, 32] and ML(4,i) for i = [1,32].

FIG. 3A is a diagram 300A of an exemplary symmetrical multi-link multi-stage network $V_{hcube}(N,d,s)$ having inverse Benes connection topology of nine stages with N = 32, d = 2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 3B is a diagram 300B of the equivalent symmetrical folded multi-link multi-stage network $V_{hcube}(N,d,s)$ of the network 300A shown in FIG. 3A, having inverse Benes connection topology of five stages with N = 32, d = 2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 3C is a diagram 300C layout of the network $V_{hcube}(N,d,s)$ shown in FIG. 3B, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 3D is a diagram 100D layout of the network $V_{hcube}(N,d,s)$ shown in FIG. 3B, in one embodiment, illustrating the connection links ML(1,i) for i = [1, 64] and ML(8,i) for i = [1,64].

FIG. 3E is a diagram 300E layout of the network $V_{hcube}(N,d,s)$ shown in FIG. 3B, in one embodiment, illustrating the connection links ML(2,i) for i = [1, 64] and ML(7,i) for i = [1,64].

FIG. 3F is a diagram 300F layout of the network $V_{hcube}(N,d,s)$ shown in FIG. 3B, in one embodiment, illustrating the connection links ML(3,i) for i = [1, 64] and ML(6,i) for i = [1,64].

FIG. 3G is a diagram 300G layout of the network $V_{hcube}(N,d,s)$ shown in FIG. 3B, in one embodiment, illustrating the connection links ML(4,i) for i = [1, 64] and ML(5,i) for i = [1,64].

FIG. 3H is a diagram 300H layout of a network $V_{hcube}(N,d,s)$ where N = 128, d = 2, and s = 2, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 4A is a diagram 400A layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 4B is a diagram 400B layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links ML(1,i) for i = [1, 64] and ML(8,i) for i = [1,64].

FIG. 4C is a diagram 400C layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 4C, in one embodiment, illustrating the connection links ML(2,i) for i = [1, 64] and ML(7,i) for i = [1,64].

FIG. 4D is a diagram 400D layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 4D, in one embodiment, illustrating the connection links ML(3,i) for i = [1, 64] and ML(6,i) for i = [1,64].

FIG. 4E is a diagram 400E layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 4E, in one embodiment, illustrating the connection links ML(4,i) for i = [1, 64] and ML(5,i) for i = [1,64].

FIG. 4C1 is a diagram 400C1 layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 5A1 is a diagram 500A1 of an exemplary prior art implementation of a two by two switch; FIG. 5A2 is a diagram 500A2 for programmable integrated circuit prior art implementation of the diagram 500A1 of FIG. 5A1; FIG. 5A3 is a diagram 500A3 for one-time programmable integrated circuit prior art implementation of the diagram 500A1

of FIG. 5A1; FIG. 5A4 is a diagram 500A4 for integrated circuit placement and route implementation of the diagram 500A1 of FIG. 5A1.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is concerned with the VLSI layouts of arbitrarily large switching networks for broadcast, unicast and multicast connections. Particularly switching networks considered in the current invention include: generalized multi-stage networks $V(N_1, N_2, d, s)$, generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$, generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$, generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$, and generalized hypercube networks $V_{hcube}(N_1, N_2, d, s)$ for s = 1,2,3 or any number in general.

Efficient VLSI layout of networks on a semiconductor chip are very important and greatly influence many important design parameters such as the area taken up by the network on the chip, total number of wires, length of the wires, latency of the signals, capacitance and hence the maximum clock speed of operation. Some networks may not even be implemented practically on a chip due to the lack of efficient layouts. The different varieties of multi-stage networks described above have not been implemented previously on the semiconductor chips efficiently. For example in Field Programmable Gate Array (FPGA) designs, multi-stage networks described in the current invention have not been successfully implemented primarily due to the lack of efficient VLSI layouts. Current commercial FPGA products such as Xilinx Vertex, Altera's Stratix implement island-style architecture using mesh and segmented mesh routing interconnects using either full crossbars or sparse crossbars. These routing interconnects consume large silicon area for crosspoints, long wires, large signal propagation delay and hence consume lot of power.

The current invention discloses the VLSI layouts of numerous types of multi-stage networks which are very efficient. Moreover they can be embedded on to mesh and segmented mesh routing interconnects of current commercial FPGA products. The VLSI layouts disclosed in the current invention are applicable to including the numerous generalized multi-stage networks disclosed in the following patent applications, filed concurrently:

1) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-stage networks $V(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the PCT Application Serial No. PCT/US08/56064 that is incorporated by reference above.

2) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in PCT Application Serial No. PCT/US08/64603 that is incorporated by reference above.

3) Rearrangeably nonblocking for arbitrary fan-out multicast and unicast, and strictly nonblocking for unicast for generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$ and generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in PCT Application Serial No. PCT/US08/64604 that is incorporated by reference above.

4) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in PCT Application Serial No. PCT/US08/64603 that is incorporated by reference above.

5) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$ with numerous

connection topologies and the scheduling methods are described in detail in PCT Application Serial No. PCT/US08/64604 that is incorporated by reference above.

6) Strictly nonblocking for arbitrary fan-out multicast for generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$ and generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in PCT Application Serial No. PCT/US08/64604 that is incorporated by reference above.

7) VLSI layouts of numerous types of multi-stage networks with locality exploitation are described in U.S. Provisional Patent Application Serial No. 61/252, 603 that is incorporated by reference above.

8) VLSI layouts of numerous types of multistage pyramid networks are described in U.S. Provisional Patent Application Serial No. 61/252, 609 that is incorporated by reference above.

In addition the layouts of the current invention are also applicable to generalized multi-stage pyramid networks $V_p(N_1, N_2, d, s)$, generalized folded multi-stage pyramid networks $V_{fold-p}(N_1, N_2, d, s)$, generalized butterfly fat pyramid networks $V_{bfp}(N_1, N_2, d, s)$, generalized multi-link multi-stage pyramid networks $V_{mlink-p}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage pyramid networks $V_{fold-mlink-p}(N_1, N_2, d, s)$, generalized multi-link butterfly fat pyramid networks $V_{mlink-bfp}(N_1, N_2, d, s)$, and generalized hypercube networks $V_{hcube}(N_1, N_2, d, s)$ for s = 1,2,3 or any number in general.

Symmetric RNB generalized multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$:

Referring to diagram 100A in FIG. 1A, in one embodiment, an exemplary generalized multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d =

2; and s = 2 with nine stages of one hundred and forty four switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, 150, 160, 170, 180 and 190 is shown where input stage 110 consists of sixteen, two by four switches IS1-IS16 and output stage 120 consists of sixteen, four by two switches OS1-OS16. And all the middle stages namely the middle stage 130 consists of sixteen, four by four switches MS(1,1) - MS(1,16), middle stage 140 consists of sixteen, four by four switches MS(2,1) - MS(2,16), middle stage 150 consists of sixteen, four by four switches MS(3,1) - MS(3,16), middle stage 160 consists of sixteen, four by four switches MS(4,1) - MS(4,16), middle stage 170 consists of sixteen, four by four switches MS(5,1) - MS(5,16), middle stage 180 consists of sixteen, four by four switches MS(6,1) - MS(6,16), and middle stage 190 consists of sixteen, four by four switches MS(7,1) - MS(7,16).

As disclosed in PCT Application Serial No. PCT/US08/64604 that is incorporated by reference above, such a network can be operated in rearrangeably non-blocking manner for arbitrary fan-out multicast connections and also can be operated in strictly non-blocking manner for unicast connections.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N}{d}$, where N is the total number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by $\frac{N}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * 2d$ and each output switch OS1-OS4 can be denoted in general with the notation $2d * d$. Likewise, the size of each switch in any of the middle stages can be denoted as $2d * 2d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. A symmetric multi-stage network can be represented with the notation $V_{mlink}(N, d, s)$, where N represents the total number of inlet links of all input switches

(for example the links IL1-IL32), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Each of the $\frac{N}{d}$ input switches IS1 – IS16 are connected to exactly d switches in middle stage 130 through two links each for a total of $2 \times d$ links (for example input switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2), and also connected to middle switch MS(1,2) through the links ML(1,3) and ML(1,4)). The middle links which connect switches in the same row in two successive middle stages are called hereinafter straight middle links; and the middle links which connect switches in different rows in two successive middle stages are called hereinafter cross middle links. For example, the middle links ML(1,1) and ML(1,2) connect input switch IS1 and middle switch MS(1,1), so middle links ML(1,1) and ML(1,2) are straight middle links; where as the middle links ML(1,3) and ML(1,4) connect input switch IS1 and middle switch MS(1,2), since input switch IS1 and middle switch MS(1,2) belong to two different rows in diagram 100A of FIG. 1A, middle links ML(1,3) and ML(1,4) are cross middle links.

Each of the $\frac{N}{d}$ middle switches MS(1,1) – MS(1,16) in the middle stage 130 are connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(1,1) and ML(1,2) are connected to the middle switch MS(1,1) from input switch IS1, and the links ML(1,7) and ML(1,8) are connected to the middle switch MS(1,1) from input switch IS2) and also are connected to exactly d switches in middle stage 140 through two links each for a total of $2 \times d$ links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1), and the links ML(2,3) and ML(2,4) are connected from middle switch MS(1,1) to middle switch MS(2,3)).

Each of the $\frac{N}{d}$ middle switches MS(2,1) – MS(2,16) in the middle stage 140 are connected from exactly d input switches through two links each for a total of $2 \times d$ links

(for example the links ML(2,1) and ML(2,2) are connected to the middle switch MS(2,1) from input switch MS(1,1), and the links ML(1,11) and ML(1,12) are connected to the middle switch MS(2,1) from input switch MS(1,3)) and also are connected to exactly d switches in middle stage 150 through two links each for a total of $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1), and the links ML(3,3) and ML(3,4) are connected from middle switch MS(2,1) to middle switch MS(3,5)).

Each of the $\frac{N}{d}$ middle switches MS(3,1) – MS(3,16) in the middle stage 150 are connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected to the middle switch MS(3,1) from input switch MS(2,1), and the links ML(2,19) and ML(2,20) are connected to the middle switch MS(3,1) from input switch MS(2,5)) and also are connected to exactly d switches in middle stage 160 through two links each for a total of $2 \times d$ links (for example the links ML(4,1) and ML(4,2) are connected from middle switch MS(3,1) to middle switch MS(4,1), and the links ML(4,3) and ML(4,4) are connected from middle switch MS(3,1) to middle switch MS(4,9)).

Each of the $\frac{N}{d}$ middle switches MS(4,1) – MS(4,16) in the middle stage 160 are connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(4,1) and ML(4,2) are connected to the middle switch MS(4,1) from input switch MS(3,1), and the links ML(4,35) and ML(4,36) are connected to the middle switch MS(4,1) from input switch MS(3,9)) and also are connected to exactly d switches in middle stage 170 through two links each for a total of $2 \times d$ links (for example the links ML(5,1) and ML(5,2) are connected from middle switch MS(4,1) to middle switch MS(5,1), and the links ML(5,3) and ML(5,4) are connected from middle switch MS(4,1) to middle switch MS(5,9)).

Each of the $\frac{N}{d}$ middle switches MS(5,1) – MS(5,16) in the middle stage 170 are connected from exactly d input switches through two links each for a total of $2 \times d$ links

(for example the links ML(5,1) and ML(5,2) are connected to the middle switch MS(5,1) from input switch MS(4,1), and the links ML(5,35) and ML(5,36) are connected to the middle switch MS(5,1) from input switch MS(4,9)) and also are connected to exactly d switches in middle stage 180 through two links each for a total of $2 \times d$ links (for example the links ML(6,1) and ML(6,2) are connected from middle switch MS(5,1) to middle switch MS(6,1), and the links ML(6,3) and ML(6,4) are connected from middle switch MS(5,1) to middle switch MS(6,5)).

Each of the $\frac{N}{d}$ middle switches MS(6,1) – MS(6,16) in the middle stage 180 are connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(6,1) and ML(6,2) are connected to the middle switch MS(6,1) from input switch MS(5,1), and the links ML(6,19) and ML(6,20) are connected to the middle switch MS(6,1) from input switch MS(5,5)) and also are connected to exactly d switches in middle stage 190 through two links each for a total of $2 \times d$ links (for example the links ML(7,1) and ML(7,2) are connected from middle switch MS(6,1) to middle switch MS(7,1), and the links ML(7,3) and ML(7,4) are connected from middle switch MS(6,1) to middle switch MS(7,3)).

Each of the $\frac{N}{d}$ middle switches MS(7,1) – MS(7,16) in the middle stage 190 are connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(7,1) and ML(7,2) are connected to the middle switch MS(7,1) from input switch MS(6,1), and the links ML(7,11) and ML(7,12) are connected to the middle switch MS(7,1) from input switch MS(6,3)) and also are connected to exactly d switches in middle stage 120 through two links each for a total of $2 \times d$ links (for example the links ML(8,1) and ML(8,2) are connected from middle switch MS(7,1) to middle switch MS(8,1), and the links ML(8,3) and ML(8,4) are connected from middle switch MS(7,1) to middle switch OS2).

Each of the $\frac{N}{d}$ middle switches OS1 – OS16 in the middle stage 120 are connected from exactly d input switches through two links each for a total of $2 \times d$ links

(for example the links ML(8,1) and ML(8,2) are connected to the output switch OS1 from input switch MS(7,1), and the links ML(8,7) and ML(7,8) are connected to the output switch OS1 from input switch MS(7,2)).

Finally the connection topology of the network 100A shown in FIG. 1A is known to be back to back inverse Benes connection topology.

Referring to diagram 100B in FIG. 1B, is a folded version of the multi-link multi-stage network 100A shown in FIG. 1A. The network 100B in FIG. 1B shows input stage 110 and output stage 120 are placed together. That is input switch IS1 and output switch OS1 are placed together, input switch IS2 and output switch OS2 are placed together, and similarly input switch IS16 and output switch OS16 are placed together. All the right going middle links (hereinafter "forward connecting links") {i.e., inlet links IL1 – IL32 and middle links ML(1,1) - ML(1,64)} correspond to input switches IS1 - IS16, and all the left going middle links (hereinafter "backward connecting links") {i.e., middle links ML(8,1) - ML(8,64) and outlet links OL1-OL32} correspond to output switches OS1 - OS16.

Middle stage 130 and middle stage 190 are placed together. That is middle switches MS(1,1) and MS(7,1) are placed together, middle switches MS(1,2) and MS(7,2) are placed together, and similarly middle switches MS(1,16) and MS(7,16) are placed together. All the right going middle links {i.e., middle links ML(1,1) - ML(1,64) and middle links ML(2,1) – ML(2,64)} correspond to middle switches MS(1,1) – MS(1,16), and all the left going middle links {i.e., middle links ML(7,1) - ML(7,64) and middle links ML(8,1) and ML(8,64)} correspond to middle switches MS(7,1) – MS(7,16).

Middle stage 140 and middle stage 180 are placed together. That is middle switches MS(2,1) and MS(6,1) are placed together, middle switches MS(2,2) and MS(6,2) are placed together, and similarly middle switches MS(2,16) and MS(6,16) are placed together. All the right going middle links {i.e., middle links ML(2,1) - ML(2,64) and middle links ML(3,1) – ML(3,64)} correspond to middle switches MS(2,1) – MS(2,16), and all the left going middle links {i.e., middle links ML(6,1) - ML(6,64) and

middle links ML(7,1) and ML(7,64)} correspond to middle switches MS(6,1) – MS(6,16).

Middle stage 150 and middle stage 170 are placed together. That is middle switches MS(3,1) and MS(5,1) are placed together, middle switches MS(3,2) and MS(5,2) are placed together, and similarly middle switches MS(3,16) and MS(5,16) are placed together. All the right going middle links {i.e., middle links ML(3,1) - ML(3,64) and middle links ML(4,1) – ML(4,64)} correspond to middle switches MS(3,1) – MS(3,16), and all the left going middle links {i.e., middle links ML(5,1) - ML(5,64) and middle links ML(6,1) and ML(6,64)} correspond to middle switches MS(5,1) – MS(5,16).

Middle stage 160 is placed alone. All the right going middle links are the middle links ML(4,1) - ML(4,64) and all the left going middle links are middle links ML(5,1) - ML(5,64).

In one embodiment, in the network 100B of FIG. 1B, the switches that are placed together are implemented as separate switches then the network 100B is the generalized folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with nine stages as disclosed in PCT Application Serial No. PCT/US08/64604 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a two by four switch and a four by two switch. For example the switch input switch IS1 and output switch OS1 are placed together; so input switch IS1 is implemented as two by four switch with the inlet links IL1 and IL2 being the inputs of the input switch IS1 and middle links ML(1,1) – ML(1,4) being the outputs of the input switch IS1; and output switch OS1 is implemented as four by two switch with the middle links ML(8,1), ML(8,2), ML(8,7) and ML(8,8) being the inputs of the output switch OS1 and outlet links OL1 – OL2 being the outputs of the output switch OS1. Similarly in this embodiment of network 100B all the switches that are placed together in each middle stage are implemented as separate switches.

Hypercube Topology layout schemes:

Referring to layout 100C of FIG. 1C, in one embodiment, there are sixteen blocks namely Block 1_2, Block 3_4, Block 5_6, Block 7_8, Block 9_10, Block 11_12, Block 13_14, Block 15_16, Block 17_18, Block 19_20, Block 21_22, Block 23_24, Block 25_26, Block 27_28, Block 29_30, and Block 31_32. Each block implements all the switches in one row of the network 100B of FIG. 1B, one of the key aspects of the current invention. For example Block 1_2 implements the input switch IS1, output Switch OS1, middle switch MS(1,1), middle switch MS(7,1), middle switch MS(2,1), middle switch MS(6,1), middle switch MS(3,1), middle switch MS(5,1), and middle switch MS(4,1). For the simplification of illustration, Input switch IS1 and output switch OS1 together are denoted as switch 1; Middle switch MS(1,1) and middle switch MS(7,1) together are denoted by switch 2; Middle switch MS(2,1) and middle switch MS(6,1) together are denoted by switch 3; Middle switch MS(3,1) and middle switch MS(5,1) together are denoted by switch 4; Middle switch MS(4,1) is denoted by switch 5.

All the straight middle links are illustrated in layout 100C of FIG. 1C. For example in Block 1_2, inlet links IL1 – IL2, outlet links OL1 – OL2, middle link ML(1,1), middle link ML(1,2), middle link ML(8,1), middle link ML(8,2), middle link ML(2,1), middle link ML(2,2), middle link ML(7,1), middle link ML(7,2), middle link ML(3,1), middle link ML(3,2), middle link ML(6,1), middle link ML(6,2), middle link ML(4,1), middle link ML(4,2), middle link ML(5,1) and middle link ML(5,2) are illustrated in layout 100C of FIG. 1C.

Even though it is not illustrated in layout 100C of FIG. 1C, in each block, in addition to the switches there may be Configurable Logic Blocks (CLB) or any arbitrary digital circuit (hereinafter "sub-integrated circuit block") depending on the applications in different embodiments. There are four quadrants in the layout 100C of FIG. 1C namely top-left, bottom-left, top-right and bottom-right quadrants. Top-left quadrant implements Block 1_2, Block 3_4, Block 5_6, and Block 7_8. Bottom-left quadrant implements Block 9_10, Block 11_12, Block 13_14, and Block 15_16. Top-right quadrant implements Block 17_18, Block 19_20, Block 21_22, and Block 23_24. Bottom-right quadrant implements Block 25_26, Block 27_28, Block 29_30, and Block 31_32. There

are two halves in layout 100C of FIG. 1C namely left-half and right-half. Left-half consists of top-left and bottom-left quadrants. Right-half consists of top-right and bottom-right quadrants.

Recursively in each quadrant there are four sub-quadrants. For example in top-left quadrant there are four sub-quadrants namely top-left sub-quadrant, bottom-left sub-quadrant, top-right sub-quadrant and bottom-right sub-quadrant. Top-left sub-quadrant of top-left quadrant implements Block 1_2. Bottom-left sub-quadrant of top-left quadrant implements Block 3_4. Top-right sub-quadrant of top-left quadrant implements Block 5_6. Finally bottom-right sub-quadrant of top-left quadrant implements Block 7_8. Similarly there are two sub-halves in each quadrant. For example in top-left quadrant there are two sub-halves namely left-sub-half and right-sub-half. Left-sub-half of top-left quadrant implements Block 1_2 and Block 3_4. Right-sub-half of top-left quadrant implements Block 5_6 and Block 7_8. Finally applicant notes that in each quadrant or half the blocks are arranged as a general binary hypercube. Recursively in larger multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 > 32$, the layout in this embodiment in accordance with the current invention, will be such that the super-quadrants will also be arranged in d-ary hypercube manner. (In the embodiment of the layout 100C of FIG. 1C, it is binary hypercube manner since d = 2, in the network $V_{fold-mlink}(N_1, N_2, d, s)$ 100B of FIG. 1B).

Layout 100D of FIG. 1D illustrates the inter-block links between switches 1 and 2 of each block. For example middle links ML(1,3), ML(1,4), ML(8,7), and ML(8,8) are connected between switch 1 of Block 1_2 and switch 2 of Block 3_4. Similarly middle links ML(1,7), ML(1,8), ML(8,3), and ML(8,4) are connected between switch 2 of Block 1_2 and switch 1 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 100D of FIG. 1D can be implemented as vertical tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(1,4) and ML(8,8) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(1,4) and ML(8,8) are implemented as a time division multiplexed single track).

Layout 100E of FIG. 1E illustrates the inter-block links between switches 2 and 3 of each block. For example middle links ML(2,3), ML(2,4), ML(7,11), and ML(7,12) are connected between switch 2 of Block 1_2 and switch 3 of Block 3_4. Similarly middle links ML(2,11), ML(2,12), ML(7,3), and ML(7,4) are connected between switch 3 of Block 1_2 and switch 2 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 100E of FIG. 1E can be implemented as horizontal tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(2,12) and ML(7,4) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(2,12) and ML(7,4) are implemented as a time division multiplexed single track).

Layout 100F of FIG. 1F illustrates the inter-block links between switches 3 and 4 of each block. For example middle links ML(3,3), ML(3,4), ML(6,19), and ML(6,20) are connected between switch 3 of Block 1_2 and switch 4 of Block 3_4. Similarly middle links ML(3,19), ML(3,20), ML(6,3), and ML(6,4) are connected between switch 4 of Block 1_2 and switch 3 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 100F of FIG. 1F can be implemented as vertical tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(3,4) and ML(6,20) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(3,4) and ML(6,20) are implemented as a time division multiplexed single track).

Layout 100G of FIG. 1G illustrates the inter-block links between switches 4 and 5 of each block. For example middle links ML(4,3), ML(4,4), ML(5,35), and ML(5,36) are connected between switch 4 of Block 1_2 and switch 5 of Block 3_4. Similarly middle links ML(4,35), ML(4,36), ML(5,3), and ML(5,4) are connected between switch 5 of Block 1_2 and switch 4 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 100G of FIG. 1G can be implemented as horizontal tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(4,4) and ML(5,36) are implemented as two different tracks); or

in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(4,4) and ML(5,36) are implemented as a time division multiplexed single track).

The complete layout for the network 100B of FIG. 1B is given by combining the links in layout diagrams of 100C, 100D, 100E, 100F, and 100G. Applicant notes that in the layout 100C of FIG. 1C, the inter-block links between switch 1 and switch 2 of corresponding blocks are vertical tracks as shown in layout 100D of FIG. 1D; the inter-block links between switch 2 and switch 3 of corresponding blocks are horizontal tracks as shown in layout 100E of FIG. 1E; the inter-block links between switch 3 and switch 4 of corresponding blocks are vertical tracks as shown in layout 100F of FIG. 1F; and finally the inter-block links between switch 4 and switch 5 of corresponding blocks are horizontal tracks as shown in layout 100G of FIG. 1G. The pattern is alternate vertical tracks and horizontal tracks. It continues recursively for larger networks of N > 32 as will be illustrated later.

Some of the key aspects of the current invention are discussed. 1) All the switches in one row of the multi-stage network 100B are implemented in a single block. 2) The blocks are placed in such a way that all the inter-block links are either horizontal tracks or vertical tracks; 3) Since all the inter-block links are either horizontal or vertical tracks, all the inter-block links can be mapped on to island-style architectures in current commercial FPGA's; 4) The length of the longest wire is about half of the width (or length) of the complete layout (For example middle link ML(4,4) is about half the width of the complete layout).

In accordance with the current invention, the layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ the sub-quadrants, quadrants, and super-quadrants are arranged in d-ary hypercube manner and also the inter-blocks are accordingly connected in d-ary hypercube topology. Even though all the embodiments in the current invention are illustrated for $N_1 = N_2$, the embodiments can be extended for $N_1 \neq N_2$.

Referring to layout 100H of FIG. 1H, illustrates the extension of layout 100C for the network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 128$; d = 2; and s = 2. There are four super-quadrants in layout 100H namely top-left super-quadrant, bottom-left super-quadrant, top-right super-quadrant, bottom-right super-quadrant. Total number of blocks in the layout 100H is sixty four. Top-left super-quadrant implements the blocks from block 1_2 to block 31_32. Each block in all the super-quadrants has two more switches namely switch 6 and switch 7 in addition to the switches [1-5] illustrated in layout 100C of FIG. 1C. The inter-block link connection topology is the exactly the same between the switches 1 and 2; switches 2 and 3; switches 3 and 4; switches 4 and 5 as it is shown in the layouts of FIG. 1D, FIG. 1E, FIG. 1F, and FIG. 1G respectively.

Bottom-left super-quadrant implements the blocks from block 33_34 to block 63_64. Top-right super-quadrant implements the blocks from block 65_66 to block 95_96. And bottom-right super-quadrant implements the blocks from block 97_98 to block 127_128. In all these three super-quadrants also, the inter-block link connection topology is the exactly the same between the switches 1 and 2; switches 2 and 3; switches 3 and 4; switches 4 and 5 as that of the top-left super-quadrant.

Recursively in accordance with the current invention, the inter-block links connecting the switch 5 and switch 6 will be vertical tracks between the corresponding switches of top-left super-quadrant and bottom-left super-quadrant. And similarly the inter-block links connecting the switch 5 and switch 6 will be vertical tracks between the corresponding switches of top-right super-quadrant and bottom-right super-quadrant. The inter-block links connecting the switch 6 and switch 7 will be horizontal tracks between the corresponding switches of top-left super-quadrant and top-right super-quadrant. And similarly the inter-block links connecting the switch 6 and switch 7 will be horizontal tracks between the corresponding switches of bottom-left super-quadrant and bottom-right super-quadrant.

Referring to diagram 100I of FIG. 1I illustrates a high-level implementation of Block 1_2 (Each of the other blocks have similar implementation) of the layout 100C of FIG. 1C which represents a generalized folded multi-link multi-stage network

$V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 2. Block 1_2 in 100I illustrates both the intra-block and inter-block links connected to Block 1_2. The layout diagram 100I corresponds to the embodiment where the switches that are placed together are implemented as separate switches in the network 100B of FIG. 1B. As noted before then the network 100B is the generalized folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 2 with nine stages as disclosed in PCT Application Serial No. PCT/US08/64604 that is incorporated by reference above.

That is the switches that are placed together in Block 1_2 as shown in FIG. 1I are namely input switch IS1 and output switch OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the switches implemented are input switch IS1 and output switch OS1); middle switch MS(1,1) and middle switch MS(7,1) belonging to switch 2; middle switch MS(2,1) and middle switch MS(6,1) belonging to switch 3; middle switch MS(3,1) and middle switch MS(5,1) belonging to switch 4; And middle switch MS(4,1) belonging to switch 5.

Input switch IS1 is implemented as two by four switch with the inlet links IL1 and IL2 being the inputs of the input switch IS1 and middle links ML(1,1) – ML(1,4) being the outputs of the input switch IS1; and output switch OS1 is implemented as four by two switch with the middle links ML(8,1) – ML(8,4) being the inputs of the output switch OS1 and outlet links OL1 – OL2 being the outputs of the output switch OS1.

Middle switch MS(1,1) is implemented as four by four switch with the middle links ML(1,1), ML(1,2), ML(1,7) and ML(1,8) being the inputs and middle links ML(2,1) – ML(2,4) being the outputs; and middle switch MS(7,1) is implemented as four by four switch with the middle links ML(7,1), ML(7,2), ML(7,11) and ML(7,12) being the inputs and middle links ML(8,1) – ML(8,4) being the outputs. Similarly all the other middle switches are also implemented as four by four switches as illustrated in 100I of FIG. 1I.

Now the VLSI layouts of generalized multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 < 32$; d = 2; s = 2 and its corresponding version of

folded generalized multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 < 32$; d = 2; s = 2 are discussed. Referring to diagram 200A1 of FIG. 2A1 is generalized multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 2$; d = 2. Diagram 200A2 of FIG. 2A2 illustrates the corresponding folded generalized multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 2$; d = 2, version of the diagram 200A1 of FIG. 2A1. Layout 200A3 of FIG. 2A3 illustrates the VLSI layout of the network 200A2 of FIG. 2A2. There is only one block i.e., Block 1_2 comprising switch 1. Just like in the layout 100C of FIG. 1C, switch 1 consists of input switch IS1 and output switch OS1.

Referring to diagram 200B1 of FIG. 2B1 is generalized multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 4$; d = 2; s = 2. Diagram 200B2 of FIG. 2B2 illustrates the corresponding folded generalized multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 4$; d = 2; s = 2, version of the diagram 200B1 of FIG. 2B1. Layout 200B3 of FIG. 2B3 illustrates the VLSI layout of the network 200B2 of FIG. 2B2. There are two blocks i.e., Block 1_2 and Block 3_4 each comprising switch 1 and switch 2. Switch 1 in each block consists of the corresponding input switch and output switch. For example switch 1 in Block 1_2 consists of input switch IS1 and output switch OS1. Similarly switch 2 in Block 1_2 consists of middle switch (1,1). Layout 200B4 of FIG. 2B4 illustrates the inter-block links of the VLSI layout diagram 200B3 of FIG. 2B3. For example middle links ML(1,4) and ML(2,8). It must be noted that all the inter-block links are vertical tracks in this layout. (Alternatively all the inter-blocks can also be implemented as horizontal tracks).

Referring to diagram 200C11 of FIG. 2C11 is generalized multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 8$; d = 2; s = 2. Diagram 200C12 of FIG. 2C12 illustrates the corresponding folded generalized multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 8$; d = 2; s = 2, version of the diagram 200C11 of FIG. 2C11. Layout 200C21 of FIG. 2C21 illustrates the VLSI layout of the network 200C12 of FIG. 2C12. There are four blocks i.e., Block 1_2, Block 3_4, Block 5_6, and Block 7_8 each comprising switch 1, switch 2 and switch 3. For example switch 1 in

Block 1_2 consists of input switch IS1 and output switch OS1; Switch 2 in Block 1_2 consists of MS(1,1) and MS(3,1). Switch 3 in Block 1_2 consists of MS(2,1).

Layout 200C22 of FIG. 2C22 illustrates the inter-block links between the switch 1 and switch 2 of the VLSI layout diagram 200C21 of FIG. 2C21. For example middle links ML(1,4) and ML(4,8) are connected between Block 1_2 and Block 3_4. It must be noted that all the inter-block links between switch 1 and switch 2 of all blocks are vertical tracks in this layout. Layout 200C23 of FIG. 2C23 illustrates the inter-block links between the switch 2 and switch 3 of the VLSI layout diagram 200C21 of FIG. 2C21. For example middle links ML(2,12) and ML(3,4) are connected between Block 1_2 and Block 5_6. It must be noted that all the inter-block links between switch 2 and switch 3 of all blocks are horizontal tracks in this layout

Referring to diagram 200D1 of FIG. 2D1 is generalized multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 16$; d = 2; s = 2. Diagram 200D2 of FIG. 2D2 illustrates the corresponding folded generalized multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 16$; d = 2; s = 2, version of the diagram 200D1 of FIG. 2D1. Layout 200D3 of FIG. 2D3 illustrates the VLSI layout of the network 200D2 of FIG. 2D2. There are eight blocks i.e., Block 1_2, Block 3_4, Block 5_6, Block 7_8, Block 9_10, Block 11_12, Block 13_14 and Block 15_16 each comprising switch 1, switch 2, switch 3 and switch 4. For example switch 1 in Block 1_2 consists of input switch IS1 and output switch OS1; Switch 2 in Block 1_2 consists of MS(1,1) and MS(5,1). Switch 3 in Block 1_2 consists of MS(2,1) and MS(4,1), and switch 4 in Block 1_2 consists of MS(3,1).

Layout 200D4 of FIG. 2D4 illustrates the inter-block links between the switch 1 and switch 2 of the VLSI layout diagram 200D3 of FIG. 2D3. For example middle links ML(1,4) and ML(6,8) are connected between Block 1_2 and Block 3_4. It must be noted that all the inter-block links between switch 1 and switch 2 of all blocks are vertical tracks in this layout. Layout 200D5 of FIG. 2D5 illustrates the inter-block links between the switch 2 and switch 3 of the VLSI layout diagram 200D3 of FIG. 2D3. For example middle links ML(2,12) and ML(5,4) are connected between Block 1_2 and Block 5_6. It

must be noted that all the inter-block links between switch 2 and switch 3 of all blocks are horizontal tracks in this layout. Layout 200D6 of FIG. 2D6 illustrates the inter-block links between the switch 3 and switch 4 of the VLSI layout diagram 200D3 of FIG. 2D3. For example middle links ML(3,4) and ML(4,20) are connected between Block 1_2 and Block 9_10. It must be noted that all the inter-block links between switch 3 and switch 4 of all blocks are vertical tracks in this layout.

Generalized Multi-link Butterfly Fat Tree Network Embodiment:

In another embodiment in the network 100B of FIG. 1B, the switches that are placed together are implemented as combined switch then the network 100B is the generalized multi-link butterfly fat tree network $V_{mlink-bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with five stages as disclosed in PCT Application Serial No. PCT/US08/64603 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a six by six switch. For example the input switch IS1 and output switch OS1 are placed together; so input switch IS1 and output OS1 are implemented as a six by six switch with the inlet links IL1, IL2, ML(8,1), ML(8,2), ML(8,7) and ML(8,8) being the inputs of the combined switch (denoted as IS1&OS1) and middle links ML(1,1), ML(1,2), ML(1,3), ML(1,4), OL1 and OL2 being the outputs of the combined switch IS1&OS1. Similarly in this embodiment of network 100B all the switches that are placed together are implemented as a combined switch.

Layout diagrams 100C in FIG. 1C, 100D in FIG. 1D, 100E in FIG. 1E, 100F in FIG. 1G are also applicable to generalized multi-link butterfly fat tree network $V_{mlink-bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with five stages. The layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized multi-link butterfly fat tree network $V_{mlink-bft}(N_1, N_2, d, s)$. Accordingly layout 100H of FIG. 1H is also applicable to generalized multi-link butterfly fat tree network $V_{mlink-bft}(N_1, N_2, d, s)$.

Referring to diagram 100J of FIG. 1J illustrates a high-level implementation of Block 1_2 (Each of the other blocks have similar implementation) of the layout 100C of FIG. 1C which represents a generalized multi-link butterfly fat tree network $V_{mlink-bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 2. Block 1_2 in 100J illustrates both the intra-block and inter-block links. The layout diagram 100J corresponds to the embodiment where the switches that are placed together are implemented as combined switch in the network 100B of FIG. 1B. As noted before then the network 100B is the generalized multi-link butterfly fat tree network $V_{mlink-bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 2 with five stages as disclosed in PCT Application Serial No. PCT/US08/64603 that is incorporated by reference above.

That is the switches that are placed together in Block 1_2 as shown in FIG. 1J are namely the combined input and output switch IS1&OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the switch implemented is combined input and output switch IS1&OS1); middle switch MS(1,1) belonging to switch 2; middle switch MS(2,1) belonging to switch 3; middle switch MS(3,1) belonging to switch 4; And middle switch MS(4,1) belonging to switch 5.

Combined input and output switch IS1&OS1 is implemented as six by six switch with the inlet links IL1, IL2 and ML(8,1) – ML(8,4) being the inputs and middle links ML(1,1) – ML(1,4), and outlet links OL1 – OL2 being the outputs.

Middle switch MS(1,1) is implemented as eight by eight switch with the middle links ML(1,1), ML(1,2), ML(1,7), ML(1,8), ML(7,1), ML(7,2), ML(7,11) and ML(7,12) being the inputs and middle links ML(2,1) – ML(2,4) and middle links ML(8,1) – ML(8,4) being the outputs. Similarly all the other middle switches are also implemented as eight by eight switches as illustrated in 100J of FIG. 1J. Applicant observes that in middle switch MS(1,1) any one of the right going middle links can be switched to any one of the left going middle links and hereinafter middle switch MS(1,1) provides U-turn links. In general, in the network $V_{mlink-bft}(N_1, N_2, d, s)$ each input switch, each output switch and each middle switch provides U-turn links.

In another embodiment, middle switch MS(1,1) (or the middle switches in any of the middle stage excepting the root middle stage) of Block 1_2 of $V_{mlink-bft}(N_1, N_2, d, s)$ can be implemented as a four by eight switch and a four by four switch to save cross points. This is because the left going middle links of these middle switches are never setup to the right going middle links. For example, in middle switch MS(1,1) of Block 1_2 as shown FIG. 1J, the left going middle links namely ML(7,1), ML(7,2), ML(7,11), and ML(7,12) are never switched to the right going middle links ML(2,1), ML(2,2), ML(2,3), and ML(2,4). And hence to implement MS(1,1) two switches namely: 1) a four by eight switch with the middle links ML(1,1), ML(1,2), ML(1,7), and ML(1,8) as inputs and the middle links ML(2,1), ML(2,2), ML(2,3), ML(2,4), ML(8,1), ML(8,2), ML(8,3), and ML(8,4) as outputs and 2) a four by four switch with the middle links ML(7,1), ML(7,2), ML(7,11), and ML(7,12) as inputs and the middle links ML(8,1), ML(8,2), ML(8,3), and ML(8,4) as outputs are sufficient without loosing any connectivity of the embodiment of MS(1,1) being implemented as an eight by eight switch as described before.)

Generalized multi-stage network Embodiment:

In one embodiment, in the network 100B of FIG. 1B, the switches that are placed together are implemented as two separate switches in input stage 110 and output stage 120; and as four separate switches in all the middle stages, then the network 100B is the generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with nine stages as disclosed in PCT Application Serial No. PCT/US08/64604 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a two by four switch and a four by two switch respectively. For example the switch input switch IS1 and output switch OS1 are placed together; so input switch IS1 is implemented as two by four switch with the inlet links IL1 and IL2 being the inputs and middle links ML(1,1) – ML(1,4) being the outputs; and output switch OS1 is implemented as four by two switch with the middle links ML(8,1), ML(8,4), ML(8,7) and ML(8,8) being the inputs and outlet links OL1 – OL2 being the outputs.

The switches, corresponding to the middle stages that are placed together are implemented as four two by two switches. For example middle switches MS(1,1), MS(1,17), MS(7,1), and MS(7,17) are placed together; so middle switch MS(1,1) is implemented as two by two switch with middle links ML(1,1) and ML(1,7) being the inputs and middle links ML(2,1) and ML(2,3) being the outputs; middle switch MS(1,17) is implemented as two by two switch with the middle links ML(1,2) and ML(1,8) being the inputs and middle links ML(2,2) and ML(2,4) being the outputs; middle switch MS(7,1) is implemented as two by two switch with middle links ML(7,1) and ML(7,11) being the inputs and middle links ML(8,1) and ML(8,3) being the outputs; And middle switch MS(7,17) is implemented as two by two switch with the middle links ML(7,2) and ML(7,12) being the inputs and middle links ML(8,2) and ML(8,4) being the outputs; Similarly in this embodiment of network 100B all the switches that are placed together are implemented as separate switches.

Layout diagrams 100C in FIG. 1C, 100D in FIG. 1D, 100E in FIG. 1E, 100F in FIG. 1G are also applicable to generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with nine stages. The layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$. Accordingly layout 100H of FIG. 1H is also applicable to generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$.

Referring to diagram 100K of FIG. 1K illustrates a high-level implementation of Block 1_2 (Each of the other blocks have similar implementation) of the layout 100C of FIG. 1C which represents a generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$. Block 1_2 in 100K illustrates both the intra-block and inter-block links. The layout diagram 100K corresponds to the embodiment where the switches that are placed together are implemented as separate switches in the network 100B of FIG. 1B. As noted before then the network 100B is the generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with nine stages as disclosed in PCT Application Serial No. PCT/US08/64604 that is incorporated by reference above.

That is the switches that are placed together in Block 1_2 as shown in FIG. 1K are namely the input switch IS1 and output switch OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the switches implemented are input switch IS1 and output switch OS1); middle switches MS(1,1), MS(1,17), MS(7,1) and MS(7,17) belonging to switch 2; middle switches MS(2,1), MS(2,17), MS(6,1) and MS(6,17) belonging to switch 3; middle switches MS(3,1), MS(3,17), MS(5,1) and MS(5,17) belonging to switch 4; And middle switches MS(4,1), and MS(4,17) belonging to switch 5.

Input switch IS1 and output switch OS1 are placed together; so input switch IS1 is implemented as two by four switch with the inlet links IL1 and IL2 being the inputs and middle links ML(1,1) – ML(1,4) being the outputs; and output switch OS1 is implemented as four by two switch with the middle links ML(8,1), ML(8,4), ML(8,7) and ML(8,8) being the inputs and outlet links OL1 – OL2 being the outputs.

Middle switches MS(1,1), MS(1,17), MS(7,1), and MS(7,17) are placed together; so middle switch MS(1,1) is implemented as two by two switch with middle links ML(1,1) and ML(1,7) being the inputs and middle links ML(2,1) and ML(2,3) being the outputs; middle switch MS(1,17) is implemented as two by two switch with the middle links ML(1,2) and ML(1,8) being the inputs and middle links ML(2,2) and ML(2,4) being the outputs; middle switch MS(7,1) is implemented as two by two switch with middle links ML(7,1) and ML(7,11) being the inputs and middle links ML(8,1) and ML(8,3) being the outputs; And middle switch MS(7,17) is implemented as two by two switch with the middle links ML(7,2) and ML(7,12) being the inputs and middle links ML(8,2) and ML(8,4) being the outputs. Similarly all the other middle switches are also implemented as two by two switches as illustrated in 100K of FIG. 1K.

Generalized multi-stage network Embodiment with S = 1:

In one embodiment, in the network 100B of FIG. 1B (where it is implemented with s = 1), the switches that are placed together are implemented as two separate switches in input stage 110 and output stage 120; and as two separate switches in all the middle stages, then the network 100B is the generalized folded multi-stage network

$V_{fold}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 1 with nine stages as disclosed in PCT Application Serial No. PCT/US08/64604 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a two by two switch and a two by two switch. For example the switch input switch IS1 and output switch OS1 are placed together; so input switch IS1 is implemented as two by two switch with the inlet links IL1 and IL2 being the inputs and middle links ML(1,1) – ML(1,2) being the outputs; and output switch OS1 is implemented as two by two switch with the middle links ML(8,1) and ML(8,3) being the inputs and outlet links OL1 – OL2 being the outputs.

The switches, corresponding to the middle stages that are placed together are implemented as two, two by two switches. For example middle switches MS(1,1) and MS(7,1) are placed together; so middle switch MS(1,1) is implemented as two by two switch with middle links ML(1,1) and ML(1,3) being the inputs and middle links ML(2,1) and ML(2,2) being the outputs; middle switch MS(7,1) is implemented as two by two switch with middle links ML(7,1) and ML(7,5) being the inputs and middle links ML(8,1) and ML(8,2) being the outputs; Similarly in this embodiment of network 100B all the switches that are placed together are implemented as two separate switches.

Layout diagrams 100C in FIG. 1C, 100D in FIG. 1D, 100E in FIG. 1E, 100F in FIG. 1G are also applicable to generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 1 with nine stages. The layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$. Accordingly layout 100H of FIG. 1H is also applicable to generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$.

Referring to diagram 100K1 of FIG. 1K1 illustrates a high-level implementation of Block 1_2 (Each of the other blocks have similar implementation) for the layout 100C of FIG. 1C when s = 1 which represents a generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 1 (All the double links are replaced by single links when s = 1). Block 1_2 in 100K1 illustrates both the intra-block and inter-

block links. The layout diagram 100K1 corresponds to the embodiment where the switches that are placed together are implemented as separate switches in the network 100B of FIG. 1B when s = 1. As noted before then the network 100B is the generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 1 with nine stages as disclosed in PCT Application Serial No. PCT/US08/64604 that is incorporated by reference above.

That is the switches that are placed together in Block 1_2 as shown in FIG. 1K1 are namely the input switch IS1 and output switch OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the switches implemented are input switch IS1 and output switch OS1); middle switches MS(1,1) and MS(7,1) belonging to switch 2; middle switches MS(2,1) and MS(6,1) belonging to switch 3; middle switches MS(3,1) and MS(5,1) belonging to switch 4; And middle switch MS(4,1) belonging to switch 5.

Input switch IS1 and output switch OS1 are placed together; so input switch IS1 is implemented as two by two switch with the inlet links IL1 and IL2 being the inputs and middle links ML(1,1) – ML(1,2) being the outputs; and output switch OS1 is implemented as two by two switch with the middle links ML(8,1) and ML(8,3) being the inputs and outlet links OL1 – OL2 being the outputs.

Middle switches MS(1,1) and MS(7,1) are placed together; so middle switch MS(1,1) is implemented as two by two switch with middle links ML(1,1) and ML(1,3) being the inputs and middle links ML(2,1) and ML(2,2) being the outputs; And middle switch MS(7,1) is implemented as two by two switch with middle links ML(7,1) and ML(7,5) being the inputs and middle links ML(8,1) and ML(8,2) being the outputs. Similarly all the other middle switches are also implemented as two by two switches as illustrated in 100K1 of FIG. 1K1.

Generalized Butterfly Fat Tree Network Embodiment:

In another embodiment in the network 100B of FIG. 1B, the switches that are placed together are implemented as two combined switches then the network 100B is the

generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 2 with five stages as disclosed in PCT Application Serial No. PCT/US08/64603 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a six by six switch. For example the input switch IS1 and output switch OS1 are placed together; so input output switch IS1&OS1 are implemented as a six by six switch with the inlet links IL1, IL2, ML(8,1), ML(8,2), ML(8,7) and ML(8,8) being the inputs of the combined switch (denoted as IS1&OS1) and middle links ML(1,1), ML(1,2), ML(1,3), ML(1,4), OL1 and OL2 being the outputs of the combined switch IS1&OS1.

The switches, corresponding to the middle stages that are placed together are implemented as two four by four switches. For example middle switches MS(1,1) and MS(1,17) are placed together; so middle switch MS(1,1) is implemented as four by four switch with middle links ML(1,1), ML(1,7), ML(7,1) and ML(7,11) being the inputs and middle links ML(2,1), ML(2,3), ML(8,1) and ML(8,3) being the outputs; middle switch MS(1,17) is implemented as four by four switch with the middle links ML(1,2), ML(1,8), ML(7,2) and ML(7,12) being the inputs and middle links ML(2,2), ML(2,4), ML(8,2) and ML(8,4) being the outputs. Similarly in this embodiment of network 100B all the switches that are placed together are implemented as a two combined switches.

Layout diagrams 100C in FIG. 1C, 100D in FIG. 1D, 100E in FIG. 1E, 100F in FIG. 1G are also applicable to generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 2 with five stages. The layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$. Accordingly layout 100H of FIG. 1H is also applicable to generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$.

Referring to diagram 100L of FIG. 1L illustrates a high-level implementation of Block 1_2 (Each of the other blocks have similar implementation) of the layout 100C of FIG. 1C which represents a generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 2. Block 1_2 in 100L illustrates both the intra-block and

inter-block links. The layout diagram 100L corresponds to the embodiment where the switches that are placed together are implemented as two combined switches in the network 100B of FIG. 1B. As noted before then the network 100B is the generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with five stages as disclosed in PCT Application Serial No. PCT/US08/64603 that is incorporated by reference above.

That is the switches that are placed together in Block 1_2 as shown in FIG. 1L are namely the combined input and output switch IS1&OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the switch implemented is combined input and output switch IS1&OS1); middle switch MS(1,1) and MS(1,17) belonging to switch 2; middle switch MS(2,1) and MS(2,17) belonging to switch 3; middle switch MS(3,1) and MS(3,17) belonging to switch 4; And middle switch MS(4,1) belonging to switch 5.

Combined input and output switch IS1&OS1 is implemented as six by six switch with the inlet links IL1, IL2, ML(8,1) , ML(8,2), ML(8,7) and ML(8,8) being the inputs and middle links ML(1,1) – ML(1,4) and outlet links OL1 – OL2 being the outputs.

Middle switch MS(1,1) is implemented as four by four switch with middle links ML(1,1), ML(1,7), ML(7,1) and ML(7,11) being the inputs and middle links ML(2,1), ML(2,3), ML(8,1) and ML(8,3) being the outputs; And middle switch MS(1,17) is implemented as four by four switch with the middle links ML(1,2), ML(1,8), ML(7,2) and ML(7,12) being the inputs and middle links ML(2,2), ML(2,4), ML(8,2) and ML(8,4) being the outputs. Similarly all the other middle switches are also implemented as two four by four switches as illustrated in 100L of FIG. 1L. Applicant observes that in middle switch MS(1,1) any one of the right going middle links can be switched to any one of the left going middle links and hereinafter middle switch MS(1,1) provides U-turn links. In general, in the network $V_{bft}(N_1, N_2, d, s)$ each input switch, each output switch and each middle switch provides U-turn links.

In another embodiment, middle switch MS(1,1) (or the middle switches in any of the middle stage excepting the root middle stage) of Block 1_2 of $V_{bft}(N_1, N_2, d, s)$ can be implemented as a two by four switch and a two by two switch to save cross points. This is because the left going middle links of these middle switches are never setup to the right going middle links. For example, in middle switch MS(1,1) of Block 1_2 as shown FIG. 1L, the left going middle links namely ML(7,1) and ML(7,11) are never switched to the right going middle links ML(2,1) and ML(2,3). And hence to implement MS(1,1) two switches namely: 1) a two by four switch with the middle links ML(1,1) and ML(1,7) as inputs and the middle links ML(2,1), ML(2,3), ML(8,1), and ML(8,3) as outputs and 2) a two by two switch with the middle links ML(7,1) and ML(7,11) as inputs and the middle links ML(8,1) and ML(8,3) as outputs are sufficient without loosing any connectivity of the embodiment of MS(1,1) being implemented as an eight by eight switch as described before.)

Generalized Butterfly Fat Tree Network Embodiment with S = 1:

In one embodiment, in the network 100B of FIG. 1B (where it is implemented with s = 1), the switches that are placed together are implemented as a combined switch in input stage 110 and output stage 120; and as a combined switch in all the middle stages, then the network 100B is the generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 1 with five stages as disclosed in PCT Application Serial No. PCT/US08/64603 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a four by four switch. For example the switch input switch IS1 and output switch OS1 are placed together; so input and output switch IS1&OS1 is implemented as four by four switch with the inlet links IL1, IL2, ML(8,1) and ML(8,3) being the inputs and middle links ML(1,1) – ML(1,2) and outlet links OL1 – OL2 being the outputs

The switches, corresponding to the middle stages that are placed together are implemented as a four by four switch. For example middle switches MS(1,1) is

implemented as four by four switch with middle links ML(1,1), ML(1,3), ML(7,1) and ML(7,5) being the inputs and middle links ML(2,1), ML(2,2), ML(8,1) and ML(8,2) being the outputs..

Layout diagrams 100C in FIG. 1C, 100D in FIG. 1D, 100E in FIG. 1E, 100F in FIG. 1G are also applicable to generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 1 with five stages. The layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$. Accordingly layout 100H of FIG. 1H is also applicable to generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$.

Referring to diagram 100L1 of FIG. 1L1 illustrates a high-level implementation of Block 1_2 (Each of the other blocks have similar implementation) for the layout 100C of FIG. 1C when s = 1 which represents a generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 1 (All the double links are replaced by single links when s = 1). Block 1_2 in 100K1 illustrates both the intra-block and inter-block links. The layout diagram 100L1 corresponds to the embodiment where the switches that are placed together are implemented as a combined switch in the network 100B of FIG. 1B when s = 1. As noted before then the network 100B is the generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 1 with nine stages as disclosed in PCT Application Serial No. PCT/US08/64603 that is incorporated by reference above.

That is the switches that are placed together in Block 1_2 as shown in FIG. 1L1 are namely the input and output switch IS1&OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the switches implemented are input switch IS1 and output switch OS1); middle switch MS(1,1) belonging to switch 2; middle switch MS(2,1) belonging to switch 3; middle switch MS(3,1) belonging to switch 4; And middle switch MS(4,1) belonging to switch 5.

Input and output switch IS1&OS1 are placed together; so input and output switch IS1&OS1 is implemented as four by four switch with the inlet links IL1, IL2, ML(8,1)

and ML(8,3) being the inputs and middle links ML(1,1) – ML(1,2) and outlet links OL1 – OL2 being the outputs.

Middle switch MS(1,1) is implemented as four by four switch with middle links ML(1,1), ML(1,3), ML(7,1) and ML(7,5) being the inputs and middle links ML(2,1), ML(2,2), ML(8,1) and ML(8,2) being the outputs. Similarly all the other middle switches are also implemented as four by four switches as illustrated in 100L1 of FIG. 1L1.

In another embodiment, middle switch MS(1,1) (or the middle switches in any of the middle stage excepting the root middle stage) of Block 1_2 of $V_{mlink-bft}(N_1, N_2, d, s)$ can be implemented as a two by four switch and a two by two switch to save cross points. This is because the left going middle links of these middle switches are never setup to the right going middle links. For example, in middle switch MS(1,1) of Block 1_2 as shown FIG. 1L1, the left going middle links namely ML(7,1) and ML(7,5) are never switched to the right going middle links ML(2,1) and ML(2,2). And hence to implement MS(1,1) two switches namely: 1) a two by four switch with the middle links ML(1,1) and ML(1,3) as inputs and the middle links ML(2,1), ML(2,2), ML(8,1), and ML(8,2) as outputs and 2) a two by two switch with the middle links ML(7,1) and ML(7,5) as inputs and the middle links ML(8,1) and ML(8,2) as outputs are sufficient without loosing any connectivity of the embodiment of MS(1,1) being implemented as an eight by eight switch as described before.)

Hypercube-like Topology layout schemes:

Referring to diagram 300A in FIG. 3A, in one embodiment, an exemplary generalized multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 2 with nine stages of one hundred and forty four switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, 150, 170, 170, 180 and 190 is shown where input stage 110

consists of sixteen, two by four switches IS1-IS16 and output stage 120 consists of sixteen, four by two switches OS1-OS16.

As disclosed in PCT Application Serial No. PCT/US08/64604 that is incorporated by reference above, such a network can be operated in rearrangeably non-blocking manner for arbitrary fan-out multicast connections and also can be operated in strictly non-blocking manner for unicast connections.

The diagram 300A in FIG. 3A is exactly the same as the diagram 100A in FIG. 1A excepting the connection links between middle stage 150 and middle stage 160 as well as between middle stage 160 and middle stage 170.

Each of the $\frac{N}{d}$ middle switches are connected to exactly d switches in middle stage 160 through two links each for a total of $2 \times d$ links (for example the links ML(4,1) and ML(4,2) are connected from middle switch MS(3,1) to middle switch MS(4,1), and the links ML(4,3) and ML(4,4) are connected from middle switch MS(3,1) to middle switch MS(4,15)).

Each of the $\frac{N}{d}$ middle switches MS(4,1) – MS(4,16) in the middle stage 160 are connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(4,1) and ML(4,2) are connected to the middle switch MS(4,1) from input switch MS(3,1), and the links ML(4,59) and ML(4,60) are connected to the middle switch MS(4,1) from input switch MS(3,15)) and also are connected to exactly d switches in middle stage 170 through two links each for a total of $2 \times d$ links (for example the links ML(5,1) and ML(5,2) are connected from middle switch MS(4,1) to middle switch MS(5,1), and the links ML(5,3) and ML(5,4) are connected from middle switch MS(4,1) to middle switch MS(5,15)).

Each of the $\frac{N}{d}$ middle switches MS(5,1) – MS(5,16) in the middle stage 170 are connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(5,1) and ML(5,2) are connected to the middle switch MS(5,1)

from input switch MS(4,1), and the links ML(5,59) and ML(5,60) are connected to the middle switch MS(5,1) from input switch MS(4,15)).

Finally the connection topology of the network 100A shown in FIG. 1A is also basically back to back inverse Benes connection topology but with a slight variation. All the cross middle links from middle switches MS(3,1) - MS(3,8) connect to middle switches MS(4,9) – MS(4,16) and all the cross middle links from middle switches MS(3,9) - MS(3,16) connect to middle switches MS(4,1) – MS(4,8). Applicant makes a key observation that there are many combinations of connections possible using this property. The difference in the connection topology between diagram 100A of FIG. 1A and diagram 300A of FIG. 3A is that the connections formed by cross middle links between middle stage 150 and middle stage 160 are made of two different combinations otherwise both the diagrams 100A and 300A implement back to back inverse Benes connection topology. Since these networks implement back to back inverse Benes topologies since there is difference in the connections of cross middle links between middle stage 150 and middle stage 160, the same difference in the connections of cross middle links between 160 and middle stage 170 occurs.

Referring to diagram 300B in FIG. 3B, is a folded version of the multi-link multi-stage network 300A shown in FIG. 3A. The network 300B in FIG. 3B shows input stage 110 and output stage 120 are placed together. That is input switch IS1 and output switch OS1 are placed together, input switch IS2 and output switch OS2 are placed together, and similarly input switch IS16 and output switch OS16 are placed together. All the right going middle links {i.e., inlet links IL1 – IL32 and middle links ML(1,1) - ML(1,64)} correspond to input switches IS1 - IS16, and all the left going middle links {i.e., middle links ML(7,1) - ML(7,64) and outlet links OL1-OL32} correspond to output switches OS1 - OS16.

Just the same way there is difference in the connection topology between diagram 100A of FIG. 1A and diagram 300A of FIG. 3A in the way the connections are formed by cross middle links between middle stage 150 and middle stage 160 and also between middle stage 160 and middle stage 170, the exact similar difference is there between the diagram 100B of FIG. 1B and the diagram 300B of FIG. 3B, i.e., in the way the

connections are formed by cross middle links between middle stage 150 and middle stage 160 and also between middle stage 160 and middle stage 170.

In one embodiment, in the network 300B of FIG. 3B, the switches that are placed together are implemented as separate switches then the network 300B is the generalized folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with nine stages as disclosed in PCT Application Serial No. PCT/US08/64604 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a two by four switch and a four by two switch. For example the switch input switch IS1 and output switch OS1 are placed together; so input switch IS1 is implemented as two by four switch with the inlet links IL1 and IL2 being the inputs of the input switch IS1 and middle links ML(1,1) – ML(1,4) being the outputs of the input switch IS1; and output switch OS1 is implemented as four by two switch with the middle links ML(8,1), ML(8,2), ML(8,7) and ML(8,8) being the inputs of the output switch OS1 and outlet links OL1 – OL2 being the outputs of the output switch OS1. Similarly in this embodiment of network 300B all the switches that are placed together are implemented as separate switches.

Referring to layout 300C of FIG. 3C, in one embodiment, there are sixteen blocks namely Block 1_2, Block 3_4, Block 5_6, Block 7_8, Block 9_10, Block 11_12, Block 13_14, Block 15_16, Block 17_18, Block 19_20, Block 21_22, Block 23_24, Block 25_26, Block 27_28, Block 29_30, and Block 31_32. Each block implements all the switches in one row of the network 300B of FIG. 3B, one of the key aspects of the current invention. For example Block 1_2 implements the input switch IS1, output Switch OS1, middle switch MS(1,1), middle switch MS(7,1), middle switch MS(2,1), middle switch MS(6,1), middle switch MS(3,1), middle switch MS(5,1), and middle switch MS(4,1). For the simplification of illustration, Input switch IS1 and output switch OS1 together are denoted as switch 1; Middle switch MS(1,1) and middle switch MS(7,1) together are denoted by switch 2; Middle switch MS(2,1) and middle switch MS(6,1) together are denoted by switch 3; Middle switch MS(3,1) and middle switch MS(5,1) together are denoted by switch 4; And middle switch MS(4,1) is denoted by switch 5.

All the straight middle links are illustrated in layout 300C of FIG. 3C. For example in Block 1_2, inlet links IL1 – IL2, outlet links OL1 – OL2, middle link ML(1,1), middle link ML(1,2), middle link ML(8,1), middle link ML(8,2), middle link ML(2,1), middle link ML(2,2), middle link ML(7,1), middle link ML(7,2), middle link ML(3,1), middle link ML(3,2), middle link ML(6,1), middle link ML(6,2), middle link ML(4,1), middle link ML(4,2), middle link ML(5,1) and middle link ML(5,2) are illustrated in layout 300C of FIG. 3C.

Even though it is not illustrated in layout 300C of FIG. 3C, in each block, in addition to the switches there may be Configurable Logic Blocks (CLB) or any arbitrary digital circuit or sub-integrated circuit block depending on the applications in different embodiments. There are four quadrants in the layout 300C of FIG. 3C namely top-left, bottom-left, top-right and bottom-right quadrants. Top-left quadrant implements Block 1_2, Block 3_4, Block 5_6, and Block 7_8. Bottom-left quadrant implements Block 9_10, Block 11_12, Block 13_14, and Block 15_16. Top-right quadrant implements Block 25_26, Block 27_28, Block 29_30, and Block 31_32. Bottom-right quadrant implements Block 17_18, Block 19_20, Block 21_22, and Block 23_24. There are two halves in layout 300C of FIG. 3C namely left-half and right-half. Left-half consists of top-left and bottom-left quadrants. Right-half consists of top-right and bottom-right quadrants.

Recursively in each quadrant there are four sub-quadrants. For example in top-left quadrant there are four sub-quadrants namely top-left sub-quadrant, bottom-left sub-quadrant, top-right sub-quadrant and bottom-right sub-quadrant. Top-left sub-quadrant of top-left quadrant implements Block 1_2. Bottom-left sub-quadrant of top-left quadrant implements Block 3_4. Top-right sub-quadrant of top-left quadrant implements Block 7_8. Finally bottom-right sub-quadrant of top-left quadrant implements Block 5_6. Similarly there are two sub-halves in each quadrant. For example in top-left quadrant there are two sub-halves namely left-sub-half and right-sub-half. Left-sub-half of top-left quadrant implements Block 1_2 and Block 3_4. Right-sub-half of top-left quadrant implements Block 7_8 and Block 5_6. Recursively in larger multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 > 32$, the layout in this embodiment in accordance

with the current invention, will be such that the super-quadrants will also be arranged in a similar manner.

Layout 300D of FIG. 3D illustrates the inter-block links (in the layout 300C of FIG. 3C all the cross middle links are inter-block links) between switches 1 and 2 of each block. For example middle links ML(1,3), ML(1,4), ML(8,7), and ML(8,8) are connected between switch 1 of Block 1_2 and switch 2 of Block 3_4. Similarly middle links ML(1,7), ML(1,8), ML(8,3), and ML(8,4) are connected between switch 2 of Block 1_2 and switch 1 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 100D of FIG. 1D can be implemented as vertical tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(1,4) and ML(8,8) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(1,4) and ML(8,8) are implemented as a time division multiplexed single track).

Layout 300E of FIG. 3E illustrates the inter-block links between switches 2 and 3 of each block. For example middle links ML(2,3), ML(2,4), ML(7,11), and ML(7,12) are connected between switch 2 of Block 1_2 and switch 3 of Block 3_4. Similarly middle links ML(2,11), ML(2,12), ML(7,3), and ML(7,4) are connected between switch 3 of Block 1_2 and switch 2 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 300E of FIG. 3E can be implemented as diagonal tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(2,12) and ML(7,4) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(2,12) and ML(7,4) are implemented as a time division multiplexed single track).

Layout 300F of FIG. 3F illustrates the inter-block links between switches 3 and 4 of each block. For example middle links ML(3,3), ML(3,4), ML(6,19), and ML(6,20) are connected between switch 3 of Block 1_2 and switch 4 of Block 3_4. Similarly middle links ML(3,19), ML(3,20), ML(6,3), and ML(6,4) are connected between switch 4 of Block 1_2 and switch 3 of Block 3_4. Applicant notes that the inter-block links illustrated

in layout 300F of FIG. 3F can be implemented as vertical tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(3,4) and ML(6,20) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(3,4) and ML(6,20) are implemented as a time division multiplexed single track).

Layout 300G of FIG. 3G illustrates the inter-block links between switches 4 and 5 of each block. For example middle links ML(4,3), ML(4,4), ML(5,35), and ML(5,36) are connected between switch 4 of Block 1_2 and switch 5 of Block 3_4. Similarly middle links ML(4,35), ML(4,36), ML(5,3), and ML(5,4) are connected between switch 5 of Block 1_2 and switch 4 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 300G of FIG. 3G can be implemented as horizontal tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(4,4) and ML(5,36) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(4,4) and ML(5,36) are implemented as a time division multiplexed single track).

The complete layout for the network 300B of FIG. 3B is given by combining the links in layout diagrams of 300C, 300D, 300E, 300F, and 300G. Applicant notes that in the layout 300C of FIG. 3C, the inter-block links between switch 1 and switch 2 are vertical tracks as shown in layout 300D of FIG. 3D; the inter-block links between switch 2 and switch 3 are horizontal tracks as shown in layout 300E of FIG. 3E; the inter-block links between switch 3 and switch 4 are vertical tracks as shown in layout 300F of FIG. 3F; and finally the inter-block links between switch 4 and switch 5 are horizontal tracks as shown in layout 300G of FIG. 3G. The pattern is either vertical tracks, horizontal tracks or diagonal tracks. It continues recursively for larger networks of $N > 32$ as will be illustrated later.

Some of the key aspects of the current invention related to layout diagram 300C of IFG. 3C are noted. 1) All the switches in one row of the multi-stage network 300B are implemented in a single block. 2) The blocks are placed in such a way that all the inter-

block links are either horizontal tracks, vertical tracks or diagonal tracks; 3) The length of the longest wire is about half of the width (or length) of the complete layout (For example middle link ML(4,4) is about half the width of the complete layout.);

The layout 300C in FIG. 3C can be recursively extended for any arbitrarily large generalized folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$. Referring to layout 300H of FIG. 3H, illustrates the extension of layout 300C for the network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 128$; d = 2; and s = 2. There are four super-quadrants in layout 300H namely top-left super-quadrant, bottom-left super-quadrant, top-right super-quadrant, bottom-right super-quadrant. Total number of blocks in the layout 300H is sixty four. Top-left super-quadrant implements the blocks from block 1_2 to block 31_32. Each block in all the super-quadrants has two more switches namely switch 6 and switch 7 in addition to the switches [1-5] illustrated in layout 300C of FIG. 3C. The inter-block link connection topology is the exactly the same between the switches 1 and 2; switches 2 and 3; switches 3 and 4; switches 4 and 5 as it is shown in the layouts of FIG. 3D, FIG. 3E, FIG. 3F, and FIG. 3G respectively.

Bottom-left super-quadrant implements the blocks from block 33_34 to block 63_64. Top-right super-quadrant implements the blocks from block 65_66 to block 95_96. And bottom-right super-quadrant implements the blocks from block 97_98 to block 127_128. In all these three super-quadrants also, the inter-block link connection topology is the exactly the same between the switches 1 and 2; switches 2 and 3; switches 3 and 4; switches 4 and 5 as that of the top-left super-quadrant.

Recursively in accordance with the current invention, the inter-block links connecting the switch 5 and switch 6 will be vertical tracks between the corresponding switches of top-left super-quadrant and bottom-left super-quadrant. And similarly the inter-block links connecting the switch 5 and switch 6 will be vertical tracks between the corresponding switches of top-right super-quadrant and bottom-right super-quadrant. The inter-block links connecting the switch 6 and switch 7 will be horizontal tracks between the corresponding switches of top-left super-quadrant and top-right super-quadrant. And similarly the inter-block links connecting the switch 6 and switch 7 will be horizontal

tracks between the corresponding switches of bottom-left super-quadrant and bottom-right super-quadrant.

Ring Topology layout schemes:

Layout diagram 400C of FIG. 4C is another embodiment for the generalized folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ diagram 100B in FIG. 1B.

Referring to layout 400C of FIG. 4C, there are sixteen blocks namely Block 1_2, Block 3_4, Block 5_6, Block 7_8, Block 9_10, Block 11_12, Block 13_14, Block 15_16, Block 17_18, Block 19_20, Block 21_22, Block 23_24, Block 25_26, Block 27_28, Block 29_30, and Block 31_32. Each block implements all the switches in one row of the network 100B of FIG. 1B, one of the key aspects of the current invention. For example Block 1_2 implements the input switch IS1, output Switch OS1, middle switch MS(1,1), middle switch MS(7,1), middle switch MS(2,1), middle switch MS(6,1), middle switch MS(3,1), middle switch MS(5,1), and middle switch MS(4,1). For the simplification of illustration, Input switch IS1 and output switch OS1 together are denoted as switch 1; Middle switch MS(1,1) and middle switch MS(7,1) together are denoted by switch 2; Middle switch MS(2,1) and middle switch MS(6,1) together are denoted by switch 3; Middle switch MS(3,1) and middle switch MS(5,1) together are denoted by switch 4; And middle switch MS(4,1) is denoted by switch 5.

All the straight middle links are illustrated in layout 400C of FIG. 4C. For example in Block 1_2, inlet links IL1 – IL2, outlet links OL1 – OL2, middle link ML(1,1), middle link ML(1,2), middle link ML(8,1), middle link ML(8,2), middle link ML(2,1), middle link ML(2,2), middle link ML(7,1), middle link ML(7,2), middle link ML(3,1), middle link ML(3,2), middle link ML(6,1), middle link ML(6,2), middle link ML(4,1), middle link ML(4,2), middle link ML(5,1) and middle link ML(5,2) are illustrated in layout 400C of FIG. 4C.

Even though it is not illustrated in layout 400C of FIG. 4C, in each block, in addition to the switches there may be Configurable Logic Blocks (CLB) or any arbitrary

digital circuit or sub-integrated circuit block depending on the applications in different embodiments. The topology of the layout 400C in FIG. 4C is a ring. For each of the neighboring rows in diagram 100B of FIG. 1B the corresponding blocks are also physically neighbors in layout diagram 400C of FIG. 4C. In addition the topmost row is also logically considered as neighbor to the bottommost row. For example Block 1_2 (implementing the switches belonging to a row in diagram 100B of FIG. 1B) has Block 3_4 as neighbor since Block 3_4 implements the switches in its neighboring row. Similarly Block 1_2 also has Block 31_32 as neighbor since Block 1_2 implements topmost row of switches and Block 31_32 implements bottommost row of switches in diagram 100B of FIG. 1B. The ring layout scheme illustrated in 400C of FIG. 4C can be generalized for a large multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 > 32$, in accordance with the current invention.

Layout 400B of FIG. 4B illustrates the inter-block links (in the layout 400A of FIG. 4A all the cross middle links are inter-block links) between switches 1 and 2 of each block. For example middle links ML(1,3), ML(1,4), ML(8,7), and ML(8,8) are connected between switch 1 of Block 1_2 and switch 2 of Block 3_4. Similarly middle links ML(1,7), ML(1,8), ML(8,3), and ML(8,4) are connected between switch 2 of Block 1_2 and switch 1 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 400B of FIG. 4B are implemented as vertical tracks or horizontal tracks or diagonal tracks. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(1,4) and ML(8,8) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(1,4) and ML(8,8) are implemented as a time division multiplexed single track).

Layout 400C of FIG. 4C illustrates the inter-block links between switches 2 and 3 of each block. For example middle links ML(2,3), ML(2,4), ML(7,11), and ML(7,12) are connected between switch 2 of Block 1_2 and switch 3 of Block 3_4. Similarly middle links ML(2,11), ML(2,12), ML(7,3), and ML(7,4) are connected between switch 3 of Block 1_2 and switch 2 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 400C of FIG. 4C are implemented as vertical tracks or horizontal tracks or

diagonal tracks. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(2,12) and ML(7,4) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(2,12) and ML(7,4) are implemented as a time division multiplexed single track).

Layout 400D of FIG. 4D illustrates the inter-block links between switches 3 and 4 of each block. For example middle links ML(3,3), ML(3,4), ML(6,19), and ML(6,20) are connected between switch 3 of Block 1_2 and switch 4 of Block 3_4. Similarly middle links ML(3,19), ML(3,20), ML(6,3), and ML(6,4) are connected between switch 4 of Block 1_2 and switch 3 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 400D of FIG. 4D are implemented as vertical tracks or horizontal tracks or diagonal tracks. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(3,4) and ML(6,20) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(3,4) and ML(6,20) are implemented as a time division multiplexed single track).

Layout 400E of FIG. 4E illustrates the inter-block links between switches 4 and 5 of each block. For example middle links ML(4,3), ML(4,4), ML(5,35), and ML(5,36) are connected between switch 4 of Block 1_2 and switch 5 of Block 3_4. Similarly middle links ML(4,35), ML(4,36), ML(5,3), and ML(5,4) are connected between switch 5 of Block 1_2 and switch 4 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 400E of FIG. 4E are implemented as vertical tracks or horizontal tracks or diagonal tracks. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(4,4) and ML(5,36) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(4,4) and ML(5,36) are implemented as a time division multiplexed single track).

The complete layout for the network 100B of FIG. 1B is given by combining the links in layout diagrams of 400A, 400B, 400C, 400D, and 400E.

Some of the key aspects of the current invention related to layout diagram 400A of FIG. 4A are noted. 1) All the switches in one row of the multi-stage network 100B are implemented in a single block. 2) The blocks are placed in such a way that all the inter-block links are either horizontal tracks, vertical tracks or diagonal tracks; 3) Length of the different wires between the same two middle stages is not the same. However it gives an opportunity to implement the most connected circuits to place and route through the blocks which have shorter wires.

Layout diagram 400C1 of FIG. 4C1 is another embodiment for the generalized folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ diagram 100B in FIG. 1B. Referring to layout 400C1 of FIG. 4C1, there are sixteen blocks namely Block 1_2, Block 3_4, Block 5_6, Block 7_8, Block 9_10, Block 11_12, Block 13_14, Block 15_16, Block 17_18, Block 19_20, Block 21_22, Block 23_24, Block 25_26, Block 27_28, Block 29_30, and Block 31_32. Each block implements all the switches in one row of the network 100B of FIG. 1B, one of the key aspects of the current invention. For example Block 1_2 implements the input switch IS1, output Switch OS1, middle switch MS(1,1), middle switch MS(7,1), middle switch MS(2,1), middle switch MS(6,1), middle switch MS(3,1), middle switch MS(5,1), and middle switch MS(4,1). For the simplification of illustration, Input switch IS1 and output switch OS1 together are denoted as switch 1; Middle switch MS(1,1) and middle switch MS(7,1) together are denoted by switch 2; Middle switch MS(2,1) and middle switch MS(6,1) together are denoted by switch 3; Middle switch MS(3,1) and middle switch MS(5,1) together are denoted by switch 4; And middle switch MS(4,1) is denoted by switch 5.

All the straight middle links are illustrated in layout 400C1 of FIG. 4C1. For example in Block 1_2, inlet links IL1 – IL2, outlet links OL1 – OL2, middle link ML(1,1), middle link ML(1,2), middle link ML(8,1), middle link ML(8,2), middle link ML(2,1), middle link ML(2,2), middle link ML(7,1), middle link ML(7,2), middle link ML(3,1), middle link ML(3,2), middle link ML(6,1), middle link ML(6,2), middle link ML(4,1), middle link ML(4,2), middle link ML(5,1) and middle link ML(5,2) are illustrated in layout 400C1 of FIG. 4C1.

Even though it is not illustrated in layout 400C1 of FIG. 4C1, in each block, in addition to the switches there may be Configurable Logic Blocks (CLB) or any arbitrary digital circuit or sub-integrated circuit block depending on the applications in different embodiments. The topology of the layout 400C1 in FIG. 4C1 is another embodiment of ring layout topology. For each of the neighboring rows in diagram 100B of FIG. 1B the corresponding blocks are also physically neighbors in layout diagram 400C of FIG. 4C. In addition the topmost row is also logically considered as neighbor to the bottommost row. For example Block 1_2 (implementing the switches belonging to a row in diagram 100B of FIG. 1B) has Block 3_4 as neighbor since Block 3_4 implements the switches in its neighboring row. Similarly Block 1_2 also has Block 31_32 as neighbor since Block 1_2 implements topmost row of switches and Block 31_32 implements bottommost row of switches in diagram 100B of FIG. 1B. The ring layout scheme illustrated in 400C of FIG. 4C can be generalized for a large multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 > 32$, in accordance with the current invention.

All the layout embodiments disclosed in the current invention are applicable to generalized multi-stage networks $V(N_1, N_2, d, s)$, generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$, generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$, generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$, and generalized hypercube networks $V_{hcube}(N_1, N_2, d, s)$ for s = 1,2,3 or any number in general, and for both $N_1 = N_2 = N$ .and $N_1 \neq N_2$, and d is any integer.

Conversely applicant makes another important observation that generalized hypercube networks $V_{hcube}(N_1, N_2, d, s)$ are implemented with the layout topology being the hypercube topology shown in layout 100C of FIG. 1C with large scale cross point reduction as any one of the networks described in the current invention namely: generalized multi-stage networks $V(N_1, N_2, d, s)$, generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$, generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$,

generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$ for s = 1,2,3 or any number in general, and for both $N_1 = N_2 = N$ .and $N_1 \neq N_2$, and d is any integer.

Applications Embodiments:

All the embodiments disclosed in the current invention are useful in many varieties of applications. FIG. 5A1 illustrates the diagram of 500A1 which is a typical two by two switch with two inlet links namely IL1 and IL2, and two outlet links namely OL1 and OL2. The two by two switch also implements four crosspoints namely CP(1,1), CP(1,2), CP(2,1) and CP(2,2) as illustrated in FIG. 5A1. For example the diagram of 500A1 may the implementation of middle switch MS(1,1) of the diagram 100K of FIG. 1K where inlet link IL1 of diagram 500A1 corresponds to middle link ML(1,1) of diagram 100K, inlet link IL2 of diagram 500A1 corresponds to middle link ML(1,7) of diagram 100K, outlet link OL1 of diagram 500A1 corresponds to middle link ML(2,1) of diagram 100K, outlet link OL2 of diagram 500A1 corresponds to middle link ML(2,3) of diagram 100K.

1) Programmable Integrated Circuit Embodiments:

All the embodiments disclosed in the current invention are useful in programmable integrated circuit applications. FIG. 5A2 illustrates the detailed diagram 500A2 for the implementation of the diagram 500A1 in programmable integrated circuit embodiments. Each crosspoint is implemented by a transistor coupled between the corresponding inlet link and outlet link, and a programmable cell in programmable integrated circuit embodiments. Specifically crosspoint CP(1,1) is implemented by transistor C(1,1) coupled between inlet link IL1 and outlet link OL1, and programmable cell P(1,1); crosspoint CP(1,2) is implemented by transistor C(1,2) coupled between inlet

link IL1 and outlet link OL2, and programmable cell P(1,2); crosspoint CP(2,1) is implemented by transistor C(2,1) coupled between inlet link IL2 and outlet link OL1, and programmable cell P(2,1); and crosspoint CP(2,2) is implemented by transistor C(2,2) coupled between inlet link IL2 and outlet link OL2, and programmable cell P(2,2).

If the programmable cell is programmed ON, the corresponding transistor couples the corresponding inlet link and outlet link. If the programmable cell is programmed OFF, the corresponding inlet link and outlet link are not connected. For example if the programmable cell P(1,1) is programmed ON, the corresponding transistor C(1,1) couples the corresponding inlet link IL1 and outlet link OL1. If the programmable cell P(1,1) is programmed OFF, the corresponding inlet link IL1 and outlet link OL1 are not connected. In volatile programmable integrated circuit embodiments the programmable cell may be an SRAM (Static Random Address Memory) cell. In non-volatile programmable integrated circuit embodiments the programmable cell may be a Flash memory cell. Also the programmable integrated circuit embodiments may implement field programmable logic arrays (FPGA) devices, or programmable Logic devices (PLD), or Application Specific Integrated Circuits (ASIC) embedded with programmable logic circuits or 3D-FPGAs.

FIG. 5A2 also illustrates a buffer B1 on inlet link IL2. The signals driven along inlet link IL2 are amplified by buffer B1. Buffer B1 can be inverting or non-inverting buffer. Buffers such as B1 are used to amplify the signal in links which are usually long.

2) One-time Programmable Integrated Circuit Embodiments:

All the embodiments disclosed in the current invention are useful in one-time programmable integrated circuit applications. FIG. 5A3 illustrates the detailed diagram 500A3 for the implementation of the diagram 500A1 in one-time programmable integrated circuit embodiments. Each crosspoint is implemented by a via coupled between the corresponding inlet link and outlet link in one-time programmable integrated circuit embodiments. Specifically crosspoint CP(1,1) is implemented by via V(1,1) coupled between inlet link IL1 and outlet link OL1; crosspoint CP(1,2) is implemented by via V(1,2) coupled between inlet link IL1 and outlet link OL2; crosspoint CP(2,1) is

implemented by via V(2,1) coupled between inlet link IL2 and outlet link OL1; and crosspoint CP(2,2) is implemented by via V(2,2) coupled between inlet link IL2 and outlet link OL2.

If the via is programmed ON, the corresponding inlet link and outlet link are permanently connected which is denoted by thick circle at the intersection of inlet link and outlet link. If the via is programmed OFF, the corresponding inlet link and outlet link are not connected which is denoted by the absence of thick circle at the intersection of inlet link and outlet link. For example in the diagram 500A3 the via V(1,1) is programmed ON, and the corresponding inlet link IL1 and outlet link OL1 are connected as denoted by thick circle at the intersection of inlet link IL1 and outlet link OL1; the via V(2,2) is programmed ON, and the corresponding inlet link IL2 and outlet link OL2 are connected as denoted by thick circle at the intersection of inlet link IL2 and outlet link OL2; the via V(1,2) is programmed OFF, and the corresponding inlet link IL1 and outlet link OL2 are not connected as denoted by the absence of thick circle at the intersection of inlet link IL1 and outlet link OL2; the via V(2,1) is programmed OFF, and the corresponding inlet link IL2 and outlet link OL1 are not connected as denoted by the absence of thick circle at the intersection of inlet link IL2 and outlet link OL1. One-time programmable integrated circuit embodiments may be anti-fuse based programmable integrated circuit devices or mask programmable structured ASIC devices.

3) Integrated Circuit Placement and Route Embodiments:

All the embodiments disclosed in the current invention are useful in Integrated Circuit Placement and Route applications, for example in ASIC backend Placement and Route tools. FIG. 5A4 illustrates the detailed diagram 500A4 for the implementation of the diagram 500A1 in Integrated Circuit Placement and Route embodiments. In an integrated circuit since the connections are known a-priori, the switch and crosspoints are actually virtual. However the concept of virtual switch and virtal crosspoint using the embodiments disclosed in the current invention reduces the number of required wires, wire length needed to connect the inputs and outputs of different netlists and the time required by the tool for placement and route of netlists in the integrated circuit.

Each virtual crosspoint is used to either to hardwire or provide no connectivity between the corresponding inlet link and outlet link. Specifically crosspoint CP(1,1) is implemented by direct connect point DCP(1,1) to hardwire (i.e., to permanently connect) inlet link IL1 and outlet link OL1 which is denoted by the thick circle at the intersection of inlet link IL1 and outlet link OL1; crosspoint CP(2,2) is implemented by direct connect point DCP(2,2) to hardwire inlet link IL2 and outlet link OL2 which is denoted by the thick circle at the intersection of inlet link IL2 and outlet link OL2. The diagram 500A4 does not show direct connect point DCP(1,2) and direct connect point DCP(1,3) since they are not needed and in the hardware implementation they are eliminated. Alternatively inlet link IL1 needs to be connected to outlet link OL1 and inlet link IL1 does not need to be connected to outlet link OL2. Also inlet link IL2 needs to be connected to outlet link OL2 and inlet link IL2 does not need to be connected to outlet link OL1. Furthermore in the example of the diagram 500A4, there is no need to drive the signal of inlet link IL1 horizontally beyond outlet link OL1 and hence the inlet link IL1 is not even extended horizontally until the outlet link OL2. Also the absence of direct connect point DCP(2,1) illustrates there is no need to connect inlet link IL2 and outlet link OL1.

In summary in integrated circuit placement and route tools, the concept of virtual switches and virtual cross points is used during the implementation of the placement & routing algorithmically in software, however during the hardware implementation cross points in the cross state are implemented as hardwired connections between the corresponding inlet link and outlet link, and in the bar state are implemented as no connection between inlet link and outlet link.

3) More Application Embodiments:

All the embodiments disclosed in the current invention are also useful in the design of SoC interconnects, Field programmable interconnect chips, parallel computer systems and in time-space-time switches.

Numerous modifications and adaptations of the embodiments, implementations, and examples described herein will be apparent to the skilled artisan in view of the disclosure.

CLAIMS

What is claimed is:

1. An integrated circuit device comprising a plurality of sub-integrated circuit blocks and a routing network, and

Said each plurality of sub-integrated circuit blocks comprising a plurality of inlet links and a plurality of outlet links; and

Said routing network interconnects any one of said outlet link of one of said sub-integrated circuit block to one or more said inlet links of one or more of said sub-integrated circuit blocks; and

Said routing network comprising of a plurality of stages y, starting from the lowest stage to the highest stage; and

Said routing network comprising a plurality of switches of size $d \times d$, where $d \geq 2$, in each said stage and each said switch of size $d \times d$ having d inlet links and d outlet links; and

Said each sub-integrated circuit block comprising a plurality of said switches corresponding to each said stage; and

Said each sub-integrated circuit block comprising a plurality of forward connecting links connecting from switches in lower stage to switches in the immediate succeeding higher stage, and also comprising a plurality of backward connecting links connecting from switches in higher stage to switches in the immediate preceding lower stage; and

Said each sub-integrated circuit block comprising a plurality straight links in said forward connecting links from switches in lower stage to switches in the immediate succeeding higher stage and a plurality cross links in said forward connecting links from switches in lower stage to switches in the immediate succeeding higher stage, and further comprising a plurality of straight links in said backward connecting links from switches

in higher stage to switches in the immediate preceding lower stage and a plurality of cross links in said backward connecting links from switches in higher stage to switches in the immediate preceding lower stage.

2. The integrated circuit device of claim 1, wherein said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and

said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks.

3. The integrated circuit device of claim 2, wherein said plurality of sub-integrated circuit blocks arranged in a two-dimensional grid.

4. The integrated circuit device of claim 3, wherein said cross links in succeeding stages are connecting as alternative vertical and horizontal links between switches in said sub-integrated circuit blocks.

5. The integrated circuit device of claim 4, wherein said cross links from switches in a stage in one of said sub-integrated circuit blocks are connecting to switches in the succeeding stage in another of said sub-integrated circuit blocks so that said cross links are either vertical links or horizontal and vice versa, and hereinafter such cross links are "shuffle exchange links").

6. The integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are substantially of equal length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are substantially of equal length in the entire said integrated circuit device.

7. The integrated circuit device of claim 6, wherein the shortest horizontal shuffle exchange links are connecting at the lowest stage and between switches in two

nearest neighboring said sub-integrated circuit blocks, and length of the horizontal shuffle exchange links is doubled in each succeeding stage; and the shortest vertical shuffle exchange links are connecting at the lowest stage and between switches in two nearest neighboring said sub-integrated circuit blocks, and length of the vertical shuffle exchange links is doubled in each succeeding stage.

8. The integrated circuit device of claim 7, wherein $y \geq (\log_2 N)$ so that the length of the horizontal shuffle exchange links in the highest stage is equal to half the size of the horizontal size of said two dimensional grid of sub-integrated circuit blocks and the length of the vertical shuffle exchange links in the highest stage is equal to half the size of the vertical size of said two dimensional grid of sub-integrated circuit blocks.

9. The integrated circuit device of claim 8, wherein $d = 2$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast Benes network with full bandwidth.

10. The integrated circuit device of claim 8, wherein $d = 2$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast Benes network and rearrangeably nonblocking for arbitrary fan-out multicast Benes network with full bandwidth.

11. The integrated circuit device of claim 8, wherein $d = 2$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast Benes network with full bandwidth.

12. The integrated circuit device of claim 7, wherein $y \geq (\log_2 N)$ so that the length of the horizontal shuffle exchange links in the highest stage is equal to half the size of the horizontal size of said two dimensional grid of sub-integrated circuit blocks and the length of the vertical shuffle exchange links in the highest stage is equal to half the size of the vertical size of said two dimensional grid of sub-integrated circuit blocks, and

said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks.

13. The integrated circuit device of claim 12, wherein $d = 2$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast butterfly fat tree network with full bandwidth.

14. The integrated circuit device of claim 12, wherein $d = 2$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast butterfly fat tree network and rearrangeably nonblocking for arbitrary fan-out multicast butterfly fat tree network with full bandwidth.

15. The integrated circuit device of claim 12, wherein $d = 2$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast butterfly fat tree network with full bandwidth.

16. The integrated circuit device of claim 1, wherein said horizontal and vertical links are implemented on two or more metal layers.

17. The integrated circuit device of claim 1, wherein said switches comprising active and reprogrammable cross points and said each cross point is programmable by an SRAM cell or a Flash Cell.

18. The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks are of equal die size.

19. The integrated circuit device of claim 16, wherein said sub-integrated circuit blocks are Lookup Tables (hereinafter "LUTs") and said integrated circuit device is a field programmable gate array (FPGA) device or field programmable gate array (FPGA) block embedded in another integrated circuit device.

20. The integrated circuit device of claim 16, wherein said sub-integrated circuit blocks are AND or OR gates and said integrated circuit device is a programmable logic device (PLD).

21. The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks comprising any arbitrary hardware logic or memory circuits.

22. The integrated circuit device of claim 1, wherein said switches comprising active one-time programmable cross points and said integrated circuit device is a mask programmable gate array (MPGA) device or a structured ASIC device.

23. The integrated circuit device of claim 1, wherein said switches comprising passive cross points or just connection of two links or not and said integrated circuit device is a Application Specific Integrated Circuit (ASIC) device.

24. The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks further recursively comprise one or more super-sub-integrated circuit blocks and a sub-routing network.

25. The integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and $y \geq (\log_2 N)$.

26. The integrated circuit device of claim 25, wherein $d = 2$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized multi-stage network with full bandwidth.

27. The integrated circuit device of claim 25, wherein $d = 2$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized multi-stage network and rearrangeably nonblocking for arbitrary fan-out multicast generalized multi-stage network with full bandwidth.

28. The integrated circuit device of claim 25, wherein $d = 2$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized multi-stage network with full bandwidth.

29. The integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and $y \geq (\log_2 N)$, and

said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks.

30. The integrated circuit device of claim 29, wherein $d = 2$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized butterfly fat tree network with full bandwidth.

31. The integrated circuit device of claim 29, wherein $d = 2$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized butterfly fat tree Network and rearrangeably nonblocking for arbitrary fan-out multicast generalized butterfly fat tree network with full bandwidth.

32. The integrated circuit device of claim 29, wherein $d = 2$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized butterfly fat tree network with full bandwidth.

33. The integrated circuit device of claim 1, wherein said straight links connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and

said cross links are connecting as vertical or horizontal or diagonal links between two different said sub-integrated circuit blocks.

34. The integrated circuit device of claim 8, wherein $d = 4$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast multi-link Benes network with full bandwidth.

35. The integrated circuit device of claim 8, wherein $d = 4$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast multi-link Benes network and rearrangeably nonblocking for arbitrary fan-out multicast multi-link Benes network with full bandwidth.

36. The integrated circuit device of claim 8, wherein $d = 4$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast multi-link Benes network with full bandwidth.

37. The integrated circuit device of claim 12, wherein $d = 4$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast multi-link butterfly fat tree network with full bandwidth.

38. The integrated circuit device of claim 12, wherein $d = 4$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in

each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast multi-link butterfly fat tree network and rearrangeably nonblocking for arbitrary fan-out multicast multi-link butterfly fat tree network with full bandwidth.

39. The integrated circuit device of claim 12, wherein $d = 4$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast multi-link butterfly fat tree network with full bandwidth.

40. The integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and $y \geq (\log_2 N)$.

41. The integrated circuit device of claim 40, wherein $d = 4$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized multi-link multi-stage network with full bandwidth.

42. The integrated circuit device of claim 40, wherein $d = 4$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized multi-link multi-stage network and rearrangeably nonblocking for arbitrary fan-out multicast generalized multi-link multi-stage network with full bandwidth.

43. The integrated circuit device of claim 40, wherein $d = 4$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized multi-link multi-stage network with full bandwidth.

44. The integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and $y \geq (\log_2 N)$, and

said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks.

45. The integrated circuit device of claim 44, wherein $d = 4$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized multi-link butterfly fat tree network with full bandwidth.

46. The integrated circuit device of claim 44, wherein $d = 4$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized multi-link butterfly fat tree Network and rearrangeably nonblocking for arbitrary fan-out multicast generalized multi-link butterfly fat tree network with full bandwidth.

47. The integrated circuit device of claim 44, wherein $d = 4$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting

said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized multi-link butterfly fat tree network with full bandwidth.

48. The integrated circuit device of claim 1, wherein said plurality of forward connecting links use a plurality of buffers to amplify signals driven through them and said plurality of backward connecting links use a plurality of buffers to amplify signals driven through them; and said buffers can be inverting or non-inverting buffers.

49. The integrated circuit device of claim 1, wherein said wherein said all switches of size $d \times d$ are either fully populated or partially populated.

VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS

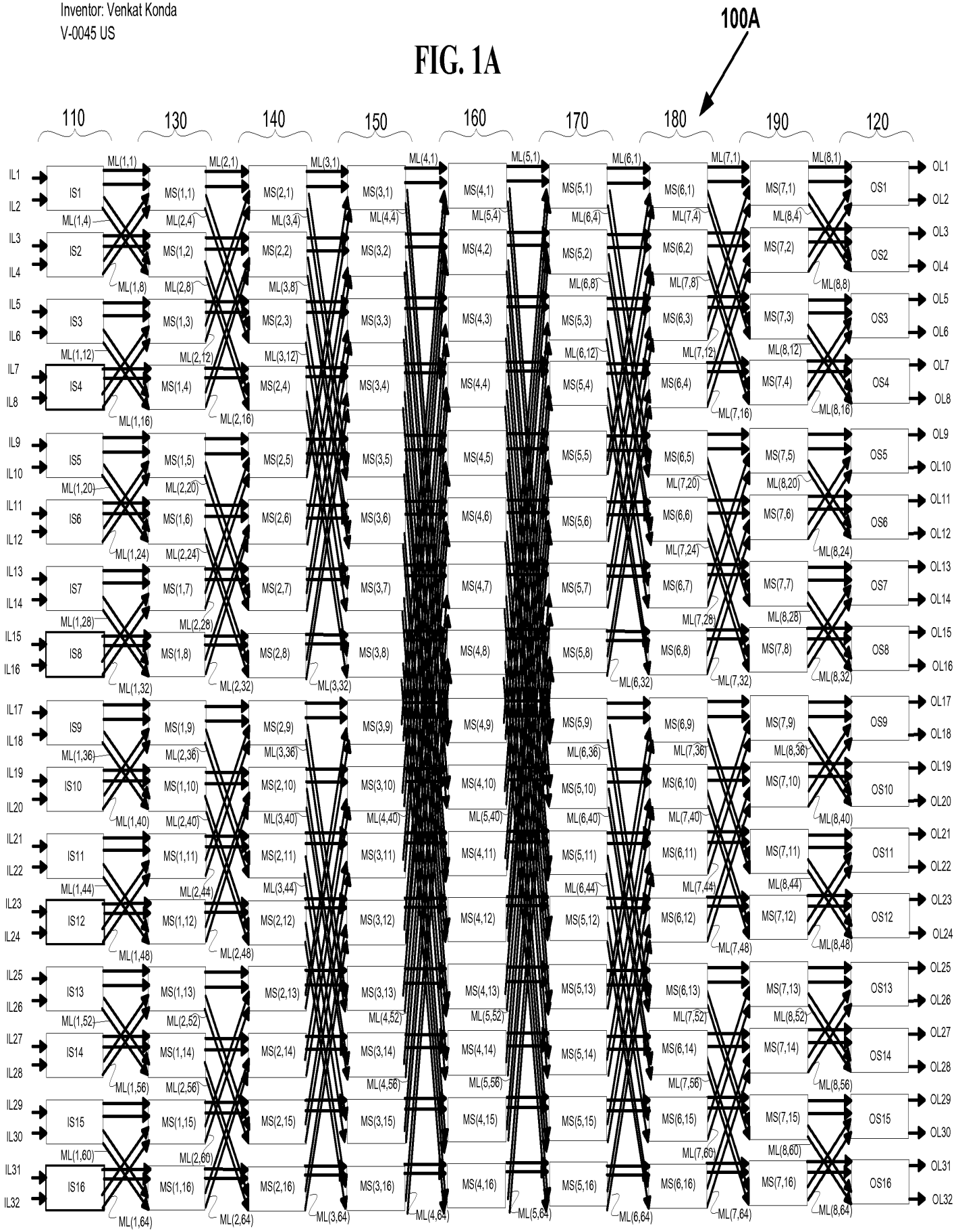
Venkat Konda

ABSTRACT OF DISCLOSURE

In accordance with the invention, VLSI layouts of generalized multi-stage networks for broadcast, unicast and multicast connections are presented using only horizontal and vertical links. The VLSI layouts employ shuffle exchange links where outlet links of cross links from switches in a stage in one sub-integrated circuit block are connected to inlet links of switches in the succeeding stage in another sub-integrated circuit block so that said cross links are either vertical links or horizontal and vice versa. In one embodiment the sub-integrated circuit blocks are arranged in a hypercube arrangement in a two-dimensional plane. The VLSI layouts exploit the benefits of significantly lower cross points, lower signal latency, lower power and full connectivity with significantly fast compilation.

The VLSI layouts presented are applicable to generalized multi-stage networks $V(N_1, N_2, d, s)$, generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$, generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$, generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$, and generalized hypercube networks $V_{hcube}(N_1, N_2, d, s)$ for s = 1,2,3 or any number in general. The embodiments of VLSI layouts are useful in wide target applications such as FPGAs, CPLDs, pSoCs, ASIC placement and route tools, networking applications, parallel & distributed computing, and reconfigurable computing.

FIG. 1A


100A
110
130
140
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IL1
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IL8
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MS(5,11)
MS(5,12)
MS(5,13)
MS(5,14)
MS(5,15)
MS(5,16)
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MS(6,5)
MS(6,6)
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MS(6,10)
MS(6,11)
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MS(6,14)
MS(6,15)
MS(6,16)
MS(7,1)
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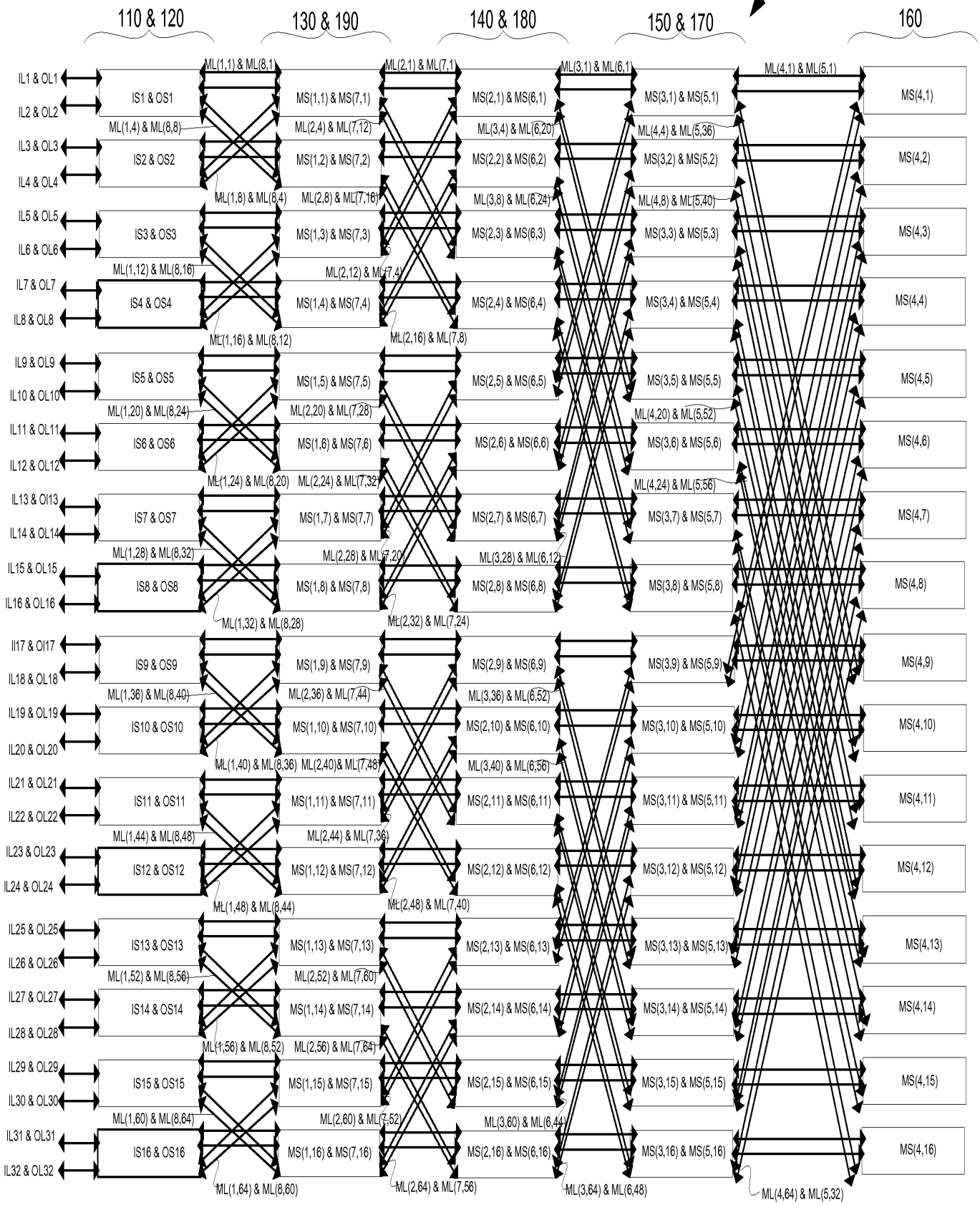
MS(7,6)
MS(7,7)
MS(7,8)
MS(7,9)
MS(7,10)
MS(7,11)
MS(7,12)
MS(7,13)
MS(7,14)
MS(7,15)
MS(7,16)
OS1
OS2
OS3
OS4
OS5
OS6
OS7
OS8
OS9
OS10
OS11
OS12
OS13
OS14
OS15
OS16
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
OL9
OL10
OL11
OL12
OL13
OL14
OL15
OL16
OL17
OL18
OL19
OL20
OL21
OL22
OL23
OL24
OL25
OL26
OL27
OL28
OL29
OL30
OL31
OL32

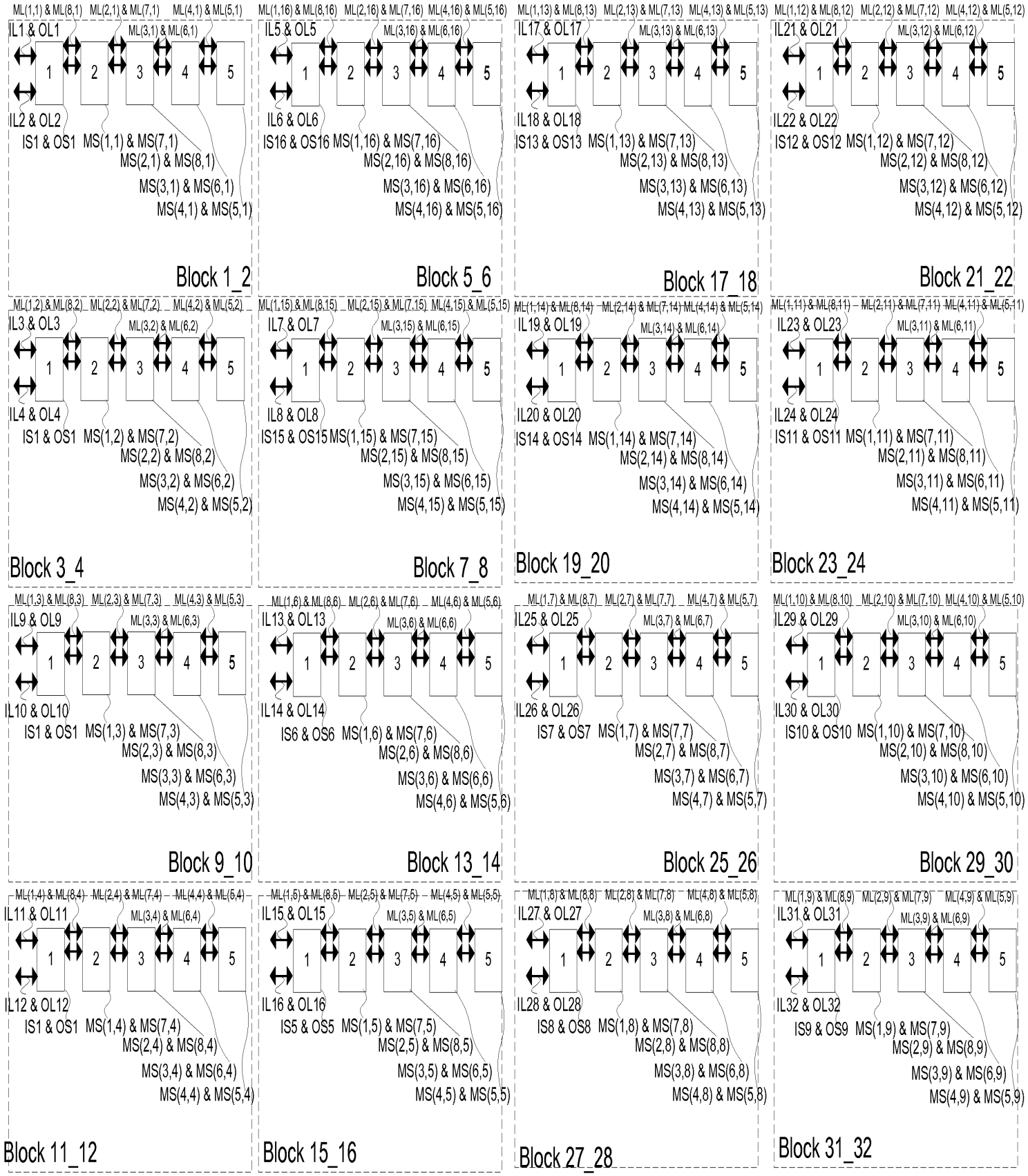
100B

FIG. 1B


110 & 120
130 & 190
140 & 180
150 & 170
160
IL1 & OL1
IL2 & OL2
IL3 & OL3
IL4 & OL4
IL5 & OL5
IL6 & OL6
IL7 & OL7
IL8 & OL8
IL9 & OL9
IL10 & OL10
IL11 & OL11
IL12 & OL12
IL13 & OI13
IL14 & OL14
IL15 & OL15
IL16 & OL16
II17 & OI17
IL18 & OL18
IL19 & OL19
IL20 & OL20
IL21 & OL21
IL22 & OL22
IL23 & OL23
IL24 & OL24
IL25 & OL25
IL26 & OL26
IL27 & OL27
IL28 & OL28
IL29 & OL29
IL30 & OL30
IL31 & OL31
IL32 & OL32
IS1 & OS1
IS2 & OS2
IS3 & OS3
IS4 & OS4
IS5 & OS5
IS6 & OS6
IS7 & OS7
IS8 & OS8
IS9 & OS9
IS10 & OS10
IS11 & OS11
IS12 & OS12
IS13 & OS13
IS14 & OS14
IS15 & OS15
IS16 & OS16
ML(1,1) & ML(8,1)
ML(1,4) & ML(8,8)
ML(1,8) & ML(8,4)
ML(1,12) & ML(8,16)
ML(1,16) & ML(8,12)
ML(1,20) & ML(8,24)
ML(1,24) & ML(8,20)
ML(1,28) & ML(8,32)
ML(1,32) & ML(8,28)
ML(1,36) & ML(8,40)
ML(1,40) & ML(8,36)
ML(1,44) & ML(8,48)
ML(1,48) & ML(8,44)
ML(1,52) & ML(8,56)
ML(1,56) & ML(8,52)
ML(1,60) & ML(8,64)
ML(1,64) & ML(8,60)
MS(1,1) & MS(7,1)
MS(1,2) & MS(7,2)
MS(1,3) & MS(7,3)
MS(1,4) & MS(7,4)
MS(1,5) & MS(7,5)
MS(1,6) & MS(7,6)
MS(1,7) & MS(7,7)
MS(1,8) & MS(7,8)
MS(1,9) & MS(7,9)
MS(1,10) & MS(7,10)
MS(1,11) & MS(7,11)
MS(1,12) & MS(7,12)
MS(1,13) & MS(7,13)
MS(1,14) & MS(7,14)
MS(1,15) & MS(7,15)
MS(1,16) & MS(7,16)
ML(2,1) & ML(7,1)
ML(2,4) & ML(7,12)
ML(2,8) & ML(7,16)
ML(2,12) & ML(7,4)
ML(2,16) & ML(7,8)
ML(2,20) & ML(7,28)
ML(2,24) & ML(7,32)
ML(2,28) & ML(7,20)
ML(2,32) & ML(7,24)
ML(2,36) & ML(7,44)
ML(2,40)& ML(7,48)
ML(2,44) & ML(7,36)
ML(2,48) & ML(7,40)
ML(2,52) & ML(7,60)
ML(2,56) & ML(7,64)
ML(2,60) & ML(7,52)
ML(2,64) & ML(7,56)
MS(2,1) & MS(6,1)
MS(2,2) & MS(6,2)
MS(2,3) & MS(6,3)
MS(2,4) & MS(6,4)
MS(2,5) & MS(6,5)
MS(2,6) & MS(6,6)
MS(2,7) & MS(6,7)
MS(2,8) & MS(6,8)
MS(2,9) & MS(6,9)
MS(2,10) & MS(6,10)
MS(2,11) & MS(6,11)
MS(2,12) & MS(6,12)
MS(2,13) & MS(6,13)
MS(2,14) & MS(6,14)
MS(2,15) & MS(6,15)
MS(2,16) & MS(6,16)
ML(3,1) & ML(6,1)
ML(3,4) & ML(6,20)
ML(3,8) & ML(6,24)
ML(3,12) & ML(6,4)
ML(3,28) & ML(6,12)
ML(3,36) & ML(6,52)
ML(3,40) & ML(6,56)
ML(3,60) & ML(6,44)
ML(3,64) & ML(6,48)
MS(3,1) & MS(5,1)
MS(3,2) & MS(5,2)
MS(3,3) & MS(5,3)
MS(3,4) & MS(5,4)
MS(3,5) & MS(5,5)
MS(3,6) & MS(5,6)
MS(3,7) & MS(5,7)
MS(3,8) & MS(5,8)
MS(3,9) & MS(5,9)
MS(3,10) & MS(5,10)
MS(3,11) & MS(5,11)
MS(3,12) & MS(5,12)
MS(3,13) & MS(5,13)
MS(3,14) & MS(5,14)
MS(3,15) & MS(5,15)
MS(3,16) & MS(5,16)
ML(4,1) & ML(5,1)
ML(4,4) & ML(5,36)
ML(4,8) & ML(5,40)
ML(4,20) & ML(5,52)
ML(4,24) & ML(5,56)
ML(4,64) & ML(5,32)
MS(4,1)
MS(4,2)
MS(4,3)
MS(4,4)
MS(4,5)
MS(4,6)
MS(4,7)
MS(4,8)
MS(4,9)
MS(4,10)
MS(4,11)
MS(4,12)
MS(4,13)
MS(4,14)
MS(4,15)
MS(4,16)

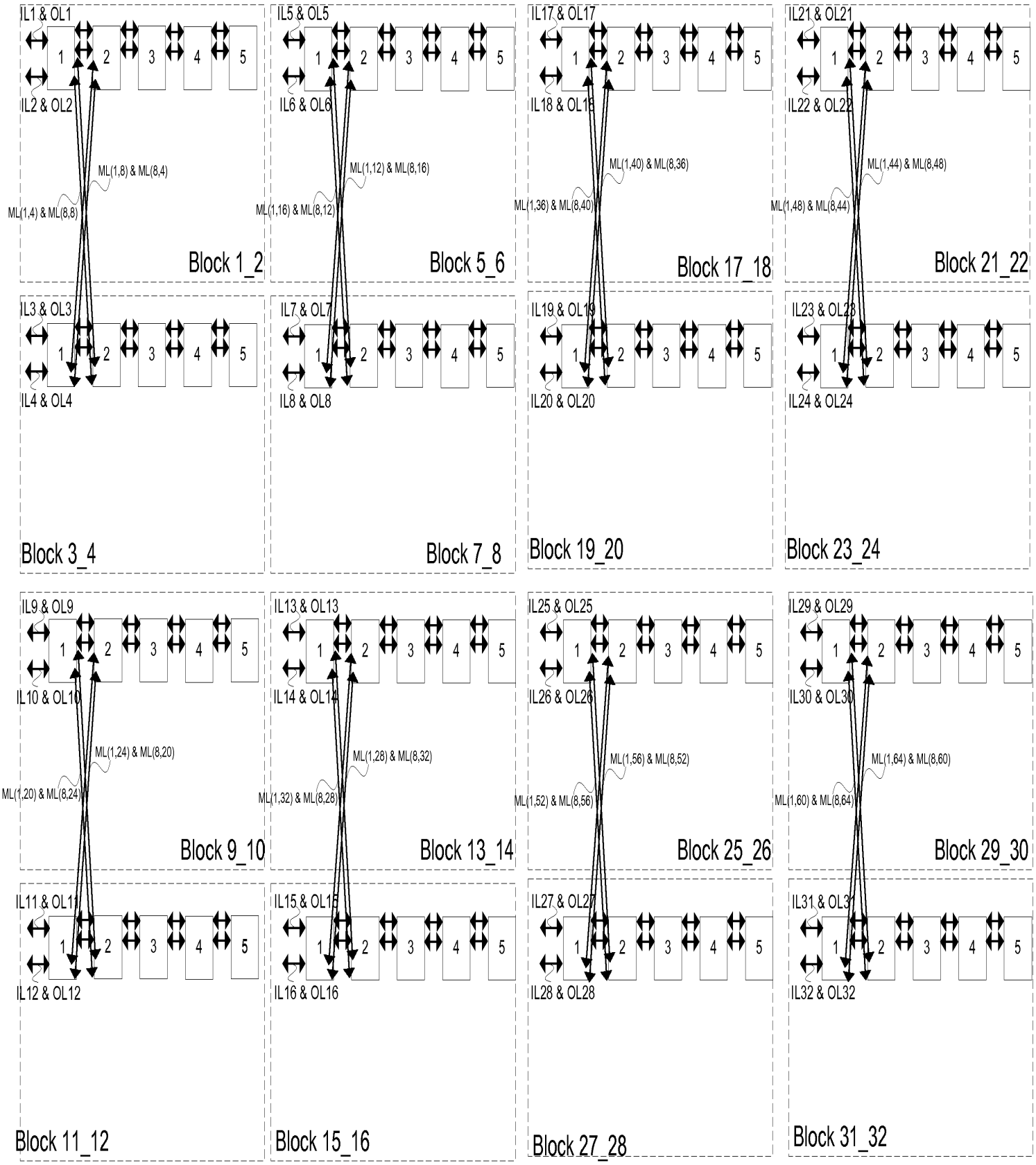
100C

FIG. 1C


ML(1,1) & ML(8,1) ML(2,1) & ML(7,1) ML(4,1) & ML(5,1)
IL1 & OL1
ML(3,1) & ML(6,1)
1 2 3 4 5
IL2 & OL2
IS1 & OS1 MS(1,1) & MS(7,1)
MS(2,1) & MS(8,1)
MS(3,1) & MS(6,1)
MS(4,1) & MS(5,1)
Block 1_2
ML(1,16) & ML(8,16) ML(2,16) & ML(7,16) ML(4,16) & ML(5,16)
IL5 & OL5
ML(3,16) & ML(6,16)
1 2 3 4 5
IL6 & OL6
IS16 & OS16 MS(1,16) & MS(7,16)
MS(2,16) & MS(8,16)
MS(3,16) & MS(6,16)
MS(4,16) & MS(5,16)
Block 5_6
ML(1,13) & ML(8,13) ML(2,13) & ML(7,13) ML(4,13) & ML(5,13)
IL17 & OL17
ML(3,13) & ML(6,13)
1 2 3 4 5
IL18 & OL18
IS13 & OS13 MS(1,13) & MS(7,13)
MS(2,13) & MS(8,13)
MS(3,13) & MS(6,13)
MS(4,13) & MS(5,13)
Block 17_18
ML(1,12) & ML(8,12) ML(2,12) & ML(7,12) ML(4,12) & ML(5,12)
IL21 & OL21
ML(3,12) & ML(6,12)
1 2 3 4 5
IL22 & OL22
IS12 & OS12 MS(1,12) & MS(7,12)
MS(2,12) & MS(8,12)
MS(3,12) & MS(6,12)
MS(4,12) & MS(5,12)
Block 21_22
ML(1,2) & ML(8,2) ML(2,2) & ML(7,2) ML(4,2) & ML(5,2)
IL3 & OL3
ML(3,2) & ML(6,2)
1 2 3 4 5
IL4 & OL4
IS1 & OS1 MS(1,2) & MS(7,2)
MS(2,2) & MS(8,2)
MS(3,2) & MS(6,2)
MS(4,2) & MS(5,2)
Block 3_4
ML(1,15) & ML(8,15) ML(2,15) & ML(7,15) ML(4,15) & ML(5,15)
IL7 & OL7
ML(3,15) & ML(6,15)
1 2 3 4 5
IL8 & OL8
IS15 & OS15 MS(1,15) & MS(7,15)
MS(2,15) & MS(8,15)
MS(3,15) & MS(6,15)
MS(4,15) & MS(5,15)
Block 7_8
ML(1,14) & ML(8,14) ML(2,14) & ML(7,14) ML(4,14) & ML(5,14)
IL19 & OL19
ML(3,14) & ML(6,14)
1 2 3 4 5
IL20 & OL20
IS14 & OS14 MS(1,14) & MS(7,14)
MS(2,14) & MS(8,14)
MS(3,14) & MS(6,14)
MS(4,14) & MS(5,14)
Block 19_20
ML(1,11) & ML(8,11) ML(2,11) & ML(7,11) ML(4,11) & ML(5,11)
IL23 & OL23
ML(3,11) & ML(6,11)
1 2 3 4 5
IL24 & OL24
IS11 & OS11 MS(1,11) & MS(7,11)
MS(2,11) & MS(8,11)
MS(3,11) & MS(6,11)
MS(4,11) & MS(5,11)
Block 23_24
ML(1,3) & ML(8,3) ML(2,3) & ML(7,3) ML(4,3) & ML(5,3)
IL9 & OL9
ML(3,3) & ML(6,3)
1 2 3 4 5
IL10 & OL10
IS1 & OS1 MS(1,3) & MS(7,3)
MS(2,3) & MS(8,3)
MS(3,3) & MS(6,3)
MS(4,3) & MS(5,3)
Block 9_10
ML(1,6) & ML(8,6) ML(2,6) & ML(7,6) ML(4,6) & ML(5,6)
IL13 & OL13
ML(3,6) & ML(6,6)
1 2 3 4 5
IL14 & OL14
IS6 & OS6 MS(1,6) & MS(7,6)
MS(2,6) & MS(8,6)
MS(3,6) & MS(6,6)
MS(4,6) & MS(5,6)
Block 13_14
ML(1,7) & ML(8,7) ML(2,7) & ML(7,7) ML(4,7) & ML(5,7)
IL25 & OL25
ML(3,7) & ML(6,7)
1 2 3 4 5
IL26 & OL26
IS7 & OS7 MS(1,7) & MS(7,7)
MS(2,7) & MS(8,7)
MS(3,7) & MS(6,7)
MS(4,7) & MS(5,7)
Block 25_26
ML(1,10) & ML(8,10) ML(2,10) & ML(7,10) ML(4,10) & ML(5,10)
IL29 & OL29
ML(3,10) & ML(6,10)
1 2 3 4 5
IL30 & OL30
IS10 & OS10 MS(1,10) & MS(7,10)
MS(2,10) & MS(8,10)
MS(3,10) & MS(6,10)
MS(4,10) & MS(5,10)
Block 29_30
ML(1,4) & ML(8,4) ML(2,4) & ML(7,4) ML(4,4) & ML(5,4)
IL11 & OL11
ML(3,4) & ML(6,4)
1 2 3 4 5
IL12 & OL12
IS1 & OS1 MS(1,4) & MS(7,4)
MS(2,4) & MS(8,4)
MS(3,4) & MS(6,4)
MS(4,4) & MS(5,4)
Block 11_12
ML(1,5) & ML(8,5) ML(2,5) & ML(7,5) ML(4,5) & ML(5,5)
IL15 & OL15
ML(3,5) & ML(6,5)
1 2 3 4 5
IL16 & OL16
IS5 & OS5 MS(1,5) & MS(7,5)
MS(2,5) & MS(8,5)
MS(3,5) & MS(6,5)
MS(4,5) & MS(5,5)
Block 15_16
ML(1,8) & ML(8,8) ML(2,8) & ML(7,8) ML(4,8) & ML(5,8)
IL27 & OL27
ML(3,8) & ML(6,8)
1 2 3 4 5
IL28 & OL28
IS8 & OS8 MS(1,8) & MS(7,8)
MS(2,8) & MS(8,8)
MS(3,8) & MS(6,8)
MS(4,8) & MS(5,8)
Block 27_28
ML(1,9) & ML(8,9) ML(2,9) & ML(7,9) ML(4,9) & ML(5,9)
IL31 & OL31
ML(3,9) & ML(6,9)
1 2 3 4 5
IL32 & OL32
IS9 & OS9 MS(1,9) & MS(7,9)
MS(2,9) & MS(8,9)
MS(3,9) & MS(6,9)
MS(4,9) & MS(5,9)
Block 31_32

100D

FIG. 1D


IL1 & OL1
IL2 & OL2
ML(1,8) & ML(8,4)
ML(1,4) & ML(8,8)
Block 1_2
IL5 & OL5
IL6 & OL6
ML(1,12) & ML(8,16)
ML(1,16) & ML(8,12)
Block 5_6
IL17 & OL17
IL18 & OL18
ML(1,40) & ML(8,36)
ML(1,36) & ML(8,40)
Block 17_18
IL21 & OL21
IL22 & OL22
ML(1,44) & ML(8,48)
ML(1,48) & ML(8,44)
Block 21_22
IL3 & OL3
IL4 & OL4
Block 3_4
IL7 & OL7
IL8 & OL8
Block 7_8
IL19 & OL19
IL20 & OL20
Block 19_20
IL23 & OL23
IL24 & OL24
Block 23_24
IL9 & OL9
IL10 & OL10
ML(1,24) & ML(8,20)
ML(1,20) & ML(8,24)
Block 9_10
IL13 & OL13
IL14 & OL14
ML(1,28) & ML(8,32)
ML(1,32) & ML(8,28)
Block 13_14
IL25 & OL25
IL26 & OL26
ML(1,56) & ML(8,52)
ML(1,52) & ML(8,56)
Block 25_26
IL29 & OL29
IL30 & OL30
ML(1,64) & ML(8,60)
ML(1,60) & ML(8,64)
Block 29_30
IL11 & OL11
IL12 & OL12
Block 11_12
IL15 & OL15
IL16 & OL16
Block 15_16
IL27 & OL27
IL28 & OL28
Block 27_28
IL31 & OL31
IL32 & OL32
Block 31_32

100E

FIG. 1E

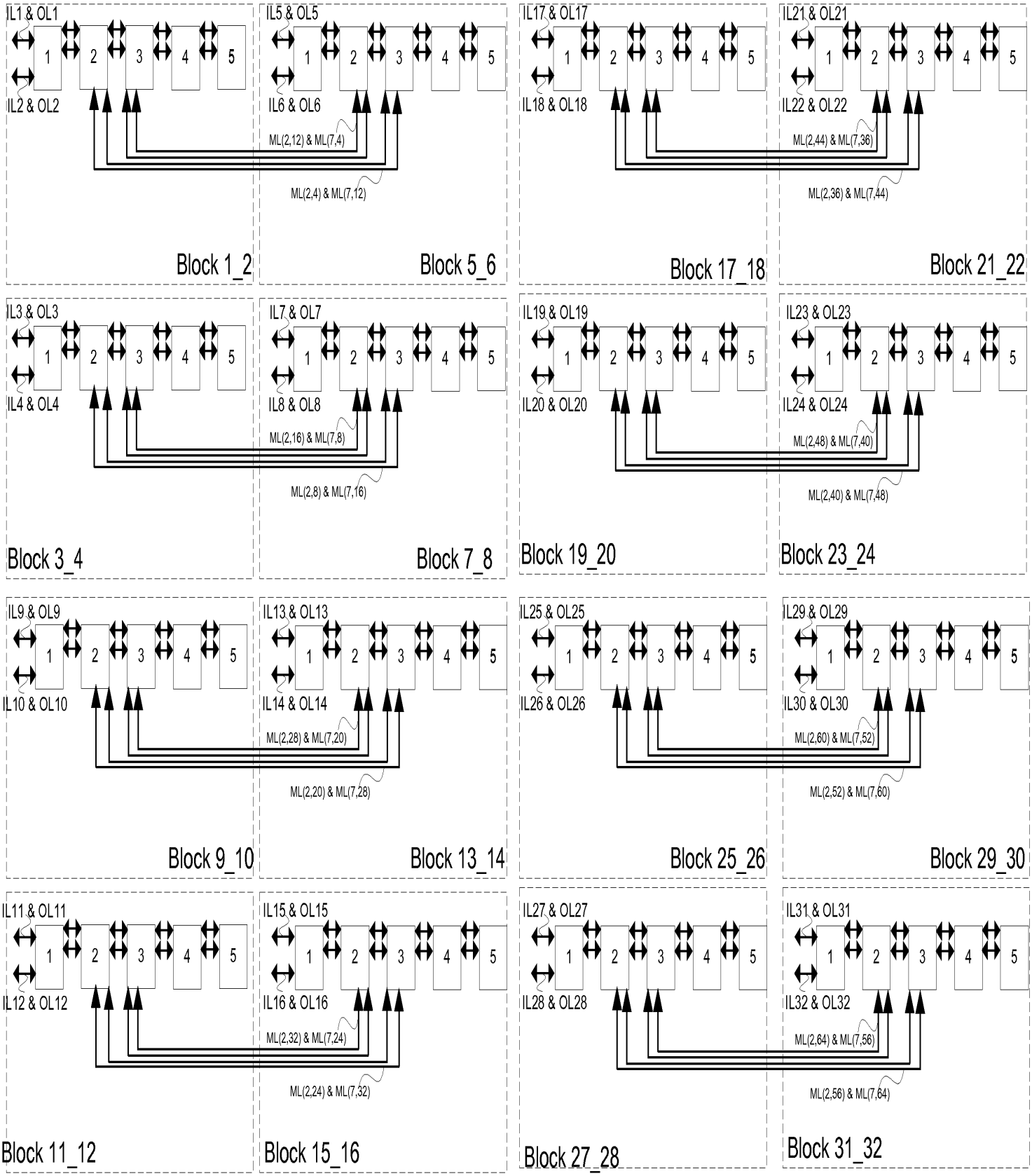

IL1 & OL1
IL2 & OL2
ML(2,12) & ML(7,4)
ML(2,4) & ML(7,12)
Block 1_2
IL5 & OL5
IL6 & OL6
Block 5_6
IL17 & OL17
IL18 & OL18
ML(2,44) & ML(7,36)
ML(2,36) & ML(7,44)
Block 17_18
IL21 & OL21
IL22 & OL22
Block 21_22
IL3 & OL3
IL4 & OL4
ML(2,16) & ML(7,8)
ML(2,8) & ML(7,16)
Block 3_4
IL7 & OL7
IL8 & OL8
Block 7_8
IL19 & OL19
IL20 & OL20
ML(2,48) & ML(7,40)
ML(2,40) & ML(7,48)
Block 19_20
IL23 & OL23
IL24 & OL24
Block 23_24
IL9 & OL9
IL10 & OL10
ML(2,28) & ML(7,20)
ML(2,20) & ML(7,28)
Block 9_10
IL13 & OL13
IL14 & OL14
Block 13_14
IL25 & OL25
IL26 & OL26
ML(2,60) & ML(7,52)
ML(2,52) & ML(7,60)
Block 25_26
IL29 & OL29
IL30 & OL30
Block 29_30
IL11 & OL11
IL12 & OL12
ML(2,32) & ML(7,24)
ML(2,24) & ML(7,32)
Block 11_12
IL15 & OL15
IL16 & OL16
Block 15_16
IL27 & OL27
IL28 & OL28
ML(2,64) & ML(7,56)
ML(2,56) & ML(7,64)
Block 27_28
IL31 & OL31
IL32 & OL32
Block 31_32

FIG. 1F

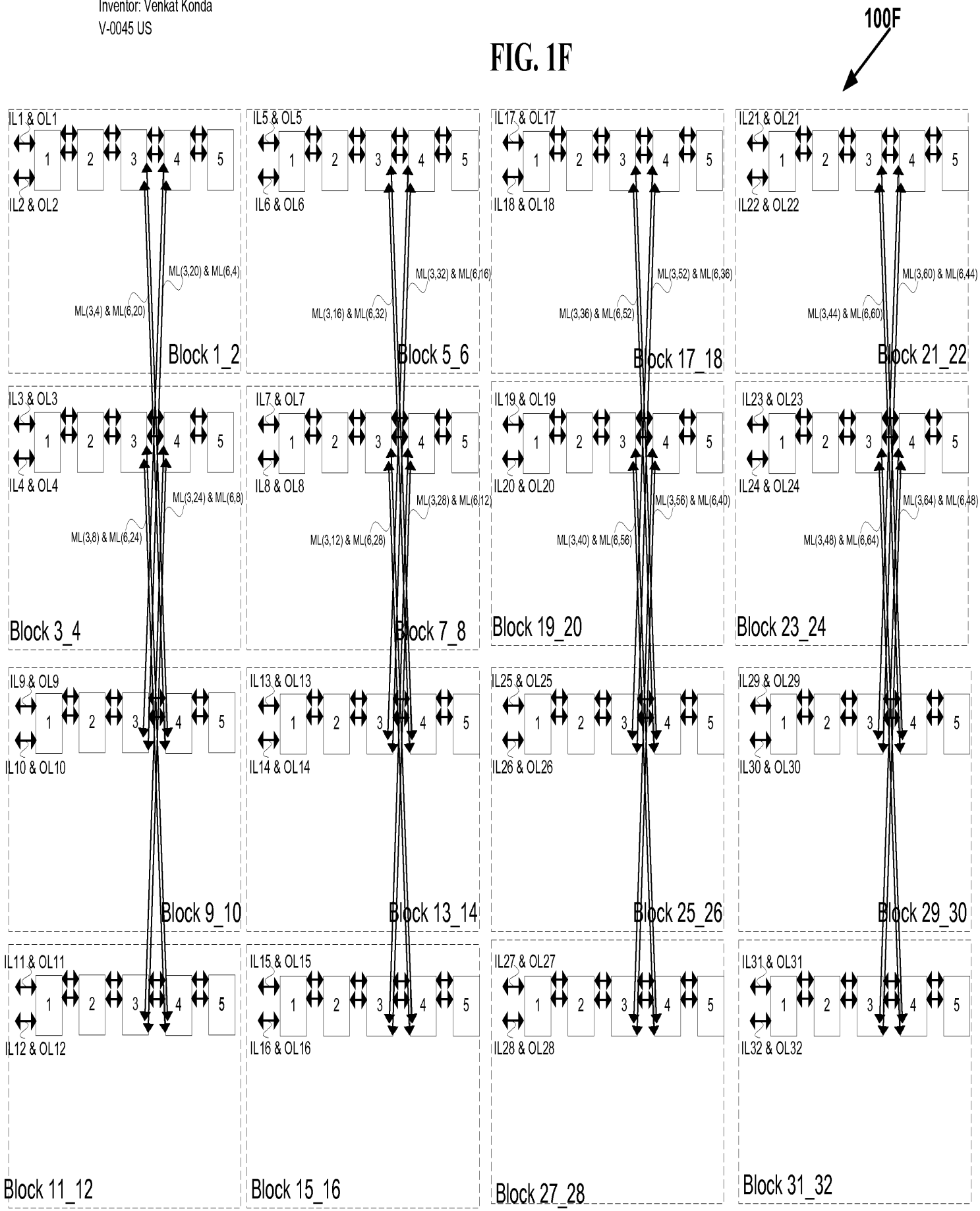

100F
IL1 & OL1
IL2 & OL2
ML(3,20) & ML(6,4)
ML(3,4) & ML(6,20)
Block 1_2
IL5 & OL5
IL6 & OL6
ML(3,32) & ML(6,16)
ML(3,16) & ML(6,32)
Block 5_6
IL17 & OL17
IL18 & OL18
ML(3,52) & ML(6,36)
ML(3,36) & ML(6,52)
Block 17_18
IL21 & OL21
IL22 & OL22
ML(3,60) & ML(6,44)
ML(3,44) & ML(6,60)
Block 21_22
IL3 & OL3
IL4 & OL4
ML(3,24) & ML(6,8)
ML(3,8) & ML(6,24)
Block 3_4
IL7 & OL7
IL8 & OL8
ML(3,28) & ML(6,12)
ML(3,12) & ML(6,28)
Block 7_8
IL19 & OL19
IL20 & OL20
ML(3,56) & ML(6,40)
ML(3,40) & ML(6,56)
Block 19_20
IL23 & OL23
IL24 & OL24
ML(3,64) & ML(6,48)
ML(3,48) & ML(6,64)
Block 23_24
IL9 & OL9
IL10 & OL10
Block 9_10
IL13 & OL13
IL14 & OL14
Block 13_14
IL25 & OL25
IL26 & OL26
Block 25_26
IL29 & OL29
IL30 & OL30
Block 29_30
IL11 & OL11
IL12 & OL12
Block 11_12
IL15 & OL15
IL16 & OL16
Block 15_16
IL27 & OL27
IL28 & OL28
Block 27_28
IL31 & OL31
IL32 & OL32
Block 31_32

FIG. 1G

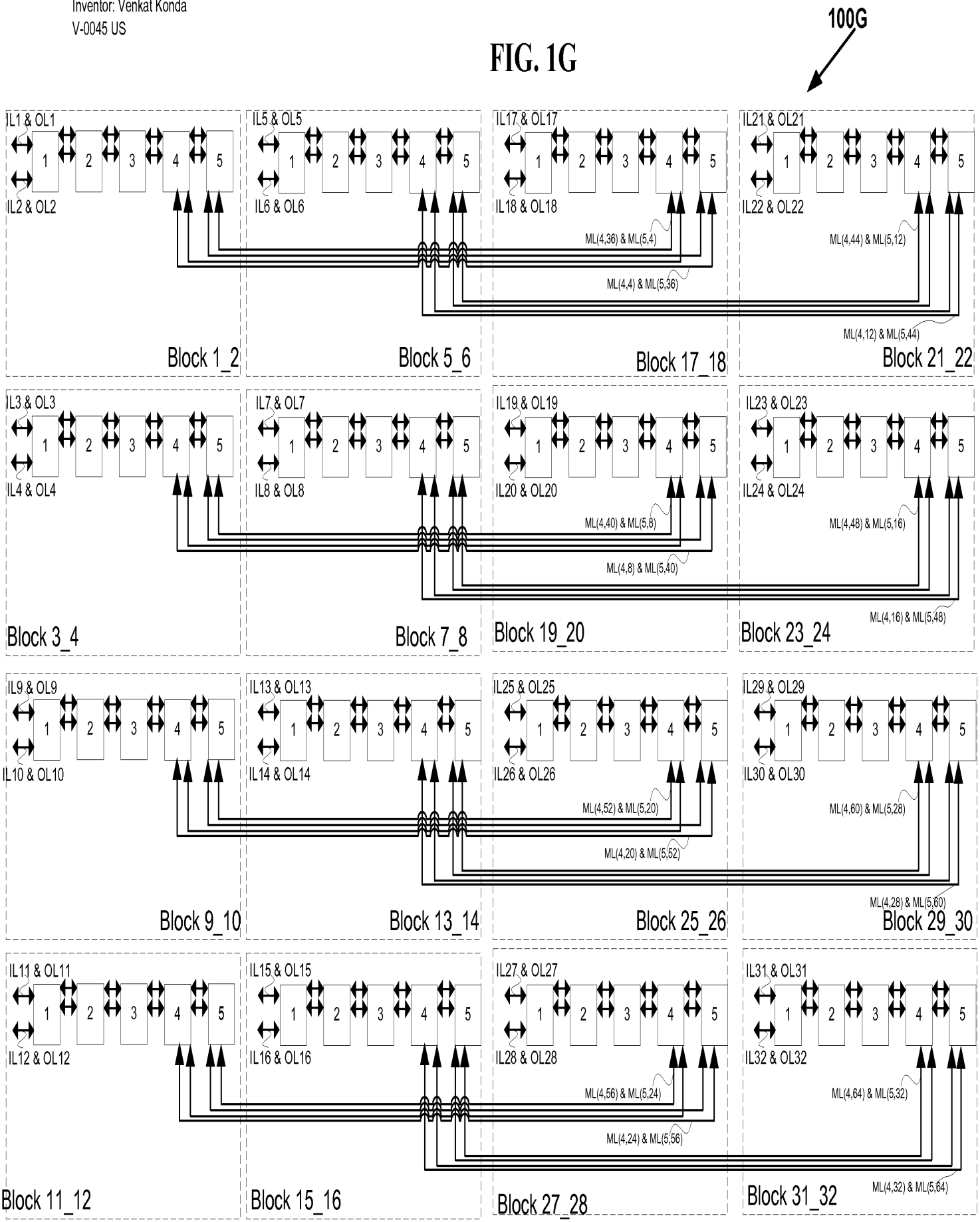

100G
IL1 & OL1
IL2 & OL2
IL5 & OL5
IL6 & OL6
IL17 & OL17
IL18 & OL18
IL21 & OL21
IL22 & OL22
ML(4,36) & ML(5,4)
ML(4,4) & ML(5,36)
ML(4,44) & ML(5,12)
ML(4,12) & ML(5,44)
Block 1_2
Block 5_6
Block 17_18
Block 21_22
IL3 & OL3
IL4 & OL4
IL7 & OL7
IL8 & OL8
IL19 & OL19
IL20 & OL20
IL23 & OL23
IL24 & OL24
ML(4,40) & ML(5,8)
ML(4,8) & ML(5,40)
ML(4,48) & ML(5,16)
ML(4,16) & ML(5,48)
Block 3_4
Block 7_8
Block 19_20
Block 23_24
IL9 & OL9
IL10 & OL10
IL13 & OL13
IL14 & OL14
IL25 & OL25
IL26 & OL26
IL29 & OL29
IL30 & OL30
ML(4,52) & ML(5,20)
ML(4,20) & ML(5,52)
ML(4,60) & ML(5,28)
ML(4,28) & ML(5,60)
Block 9_10
Block 13_14
Block 25_26
Block 29_30
IL11 & OL11
IL12 & OL12
IL15 & OL15
IL16 & OL16
IL27 & OL27
IL28 & OL28
IL31 & OL31
IL32 & OL32
ML(4,56) & ML(5,24)
ML(4,24) & ML(5,56)
ML(4,64) & ML(5,32)
ML(4,32) & ML(5,64)
Block 11_12
Block 15_16
Block 27_28
Block 31_32

FIG. 1H

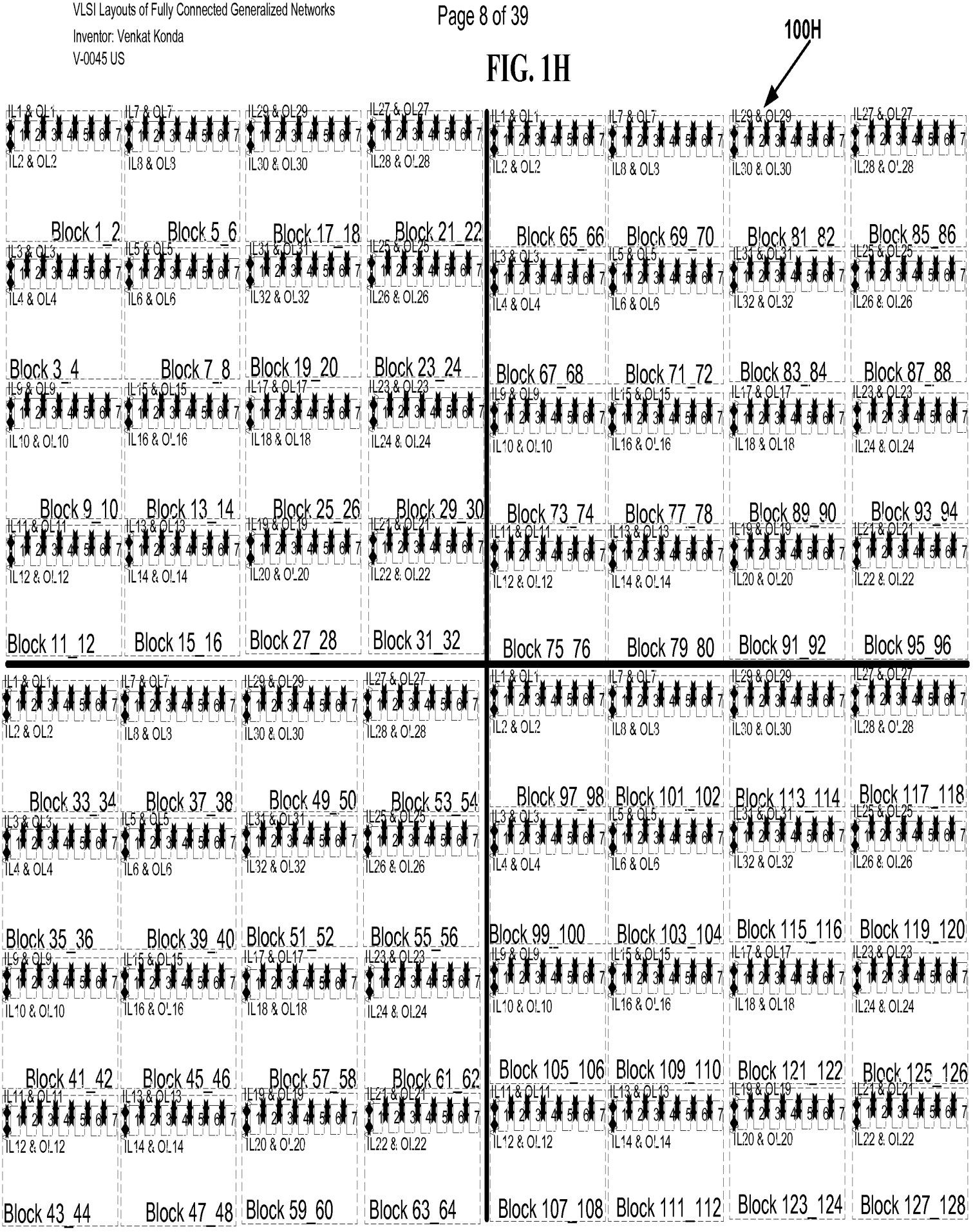
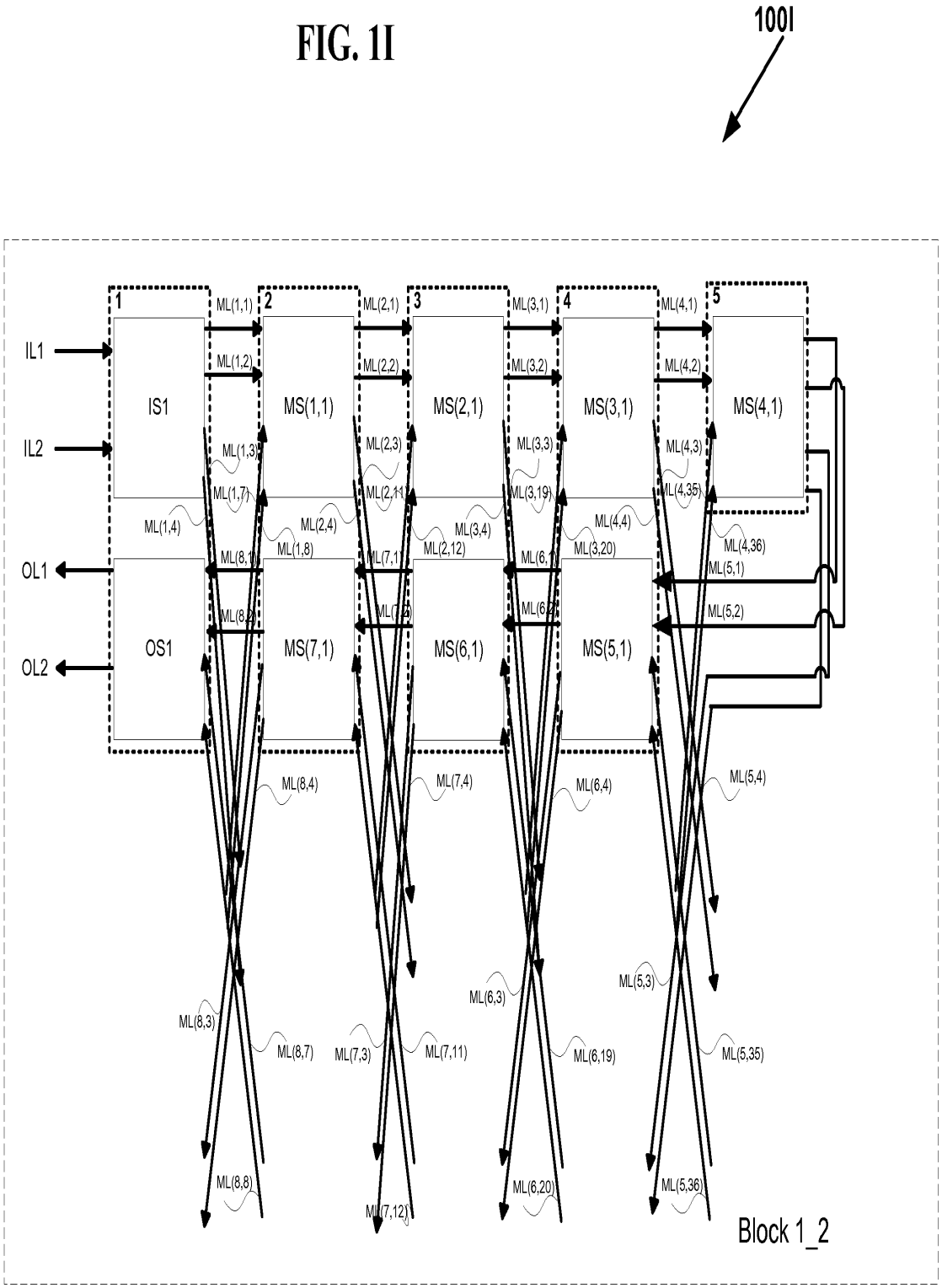

100H
Block 1_2
Block 5_6
Block 17_18
Block 21_22
Block 65_66
Block 69_70
Block 81_82
Block 85_86
Block 3_4
Block 7_8
Block 19_20
Block 23_24
Block 67_68
Block 71_72
Block 83_84
Block 87_88
Block 9_10
Block 13_14
Block 25_26
Block 29_30
Block 73_74
Block 77_78
Block 89_90
Block 93_94
Block 11_12
Block 15_16
Block 27_28
Block 31_32
Block 75_76
Block 79_80
Block 91_92
Block 95_96
Block 33_34
Block 37_38
Block 49_50
Block 53_54
Block 97_98
Block 101_102
Block 113_114
Block 117_118
Block 35_36
Block 39_40
Block 51_52
Block 55_56
Block 99_100
Block 103_104
Block 115_116
Block 119_120
Block 41_42
Block 45_46
Block 57_58
Block 61_62
Block 105_106
Block 109_110
Block 121_122
Block 125_126
Block 43_44
Block 47_48
Block 59_60
Block 63_64
Block 107_108
Block 111_112
Block 123_124
Block 127_128

FIG. 1I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OL1
OL2
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MS(6,1)
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ML(7,12)
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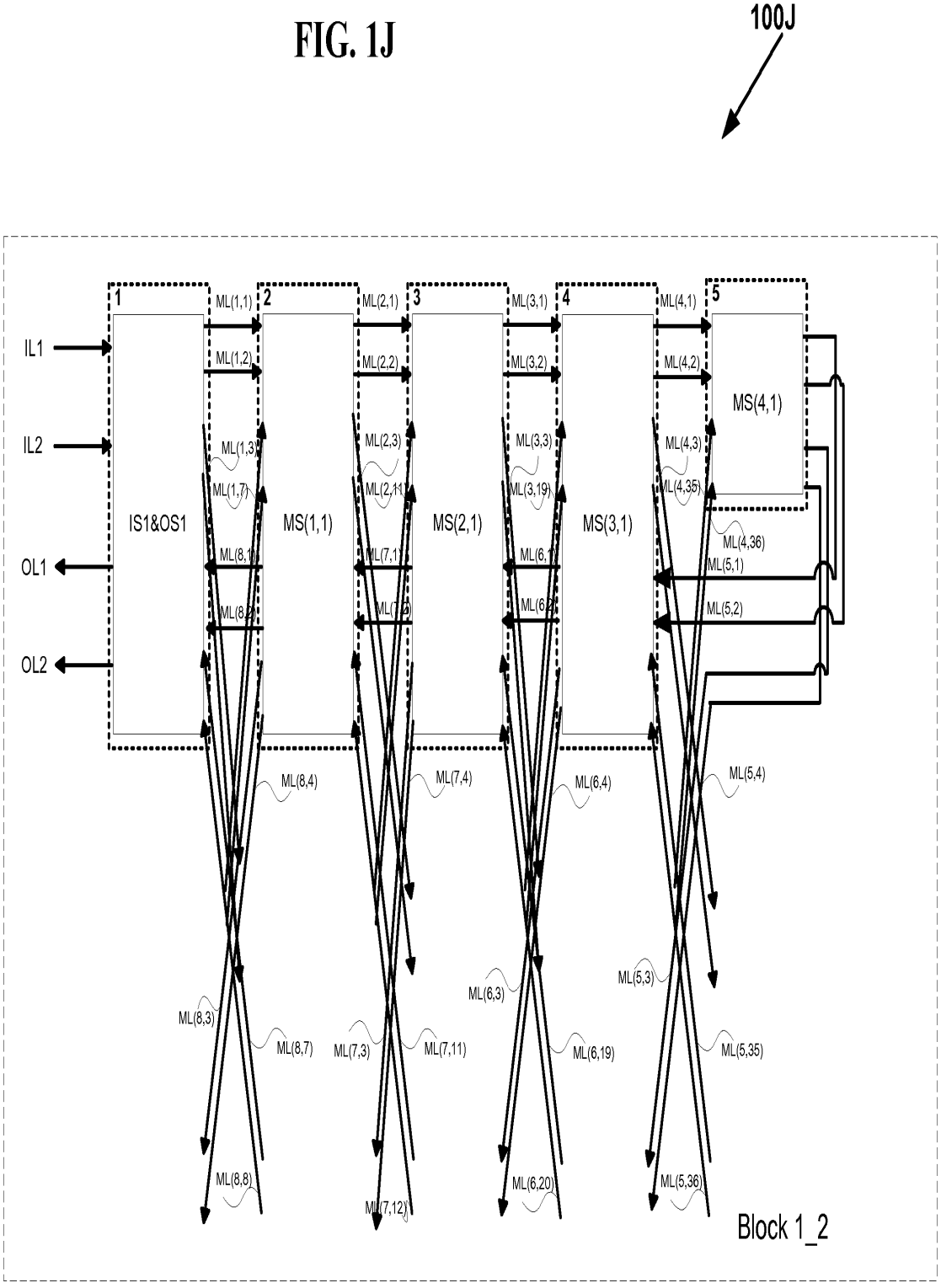
ML(8,8)
Block 1_2

FIG. 1J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4
5
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IL2
OL1
OL2
IS1&OS1
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ML(2,2)
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ML(2,11)
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ML(4,35)
ML(4,36)
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ML(8,3)
ML(8,7)
ML(7,3)
ML(7,11)
ML(6,3)
ML(6,19)
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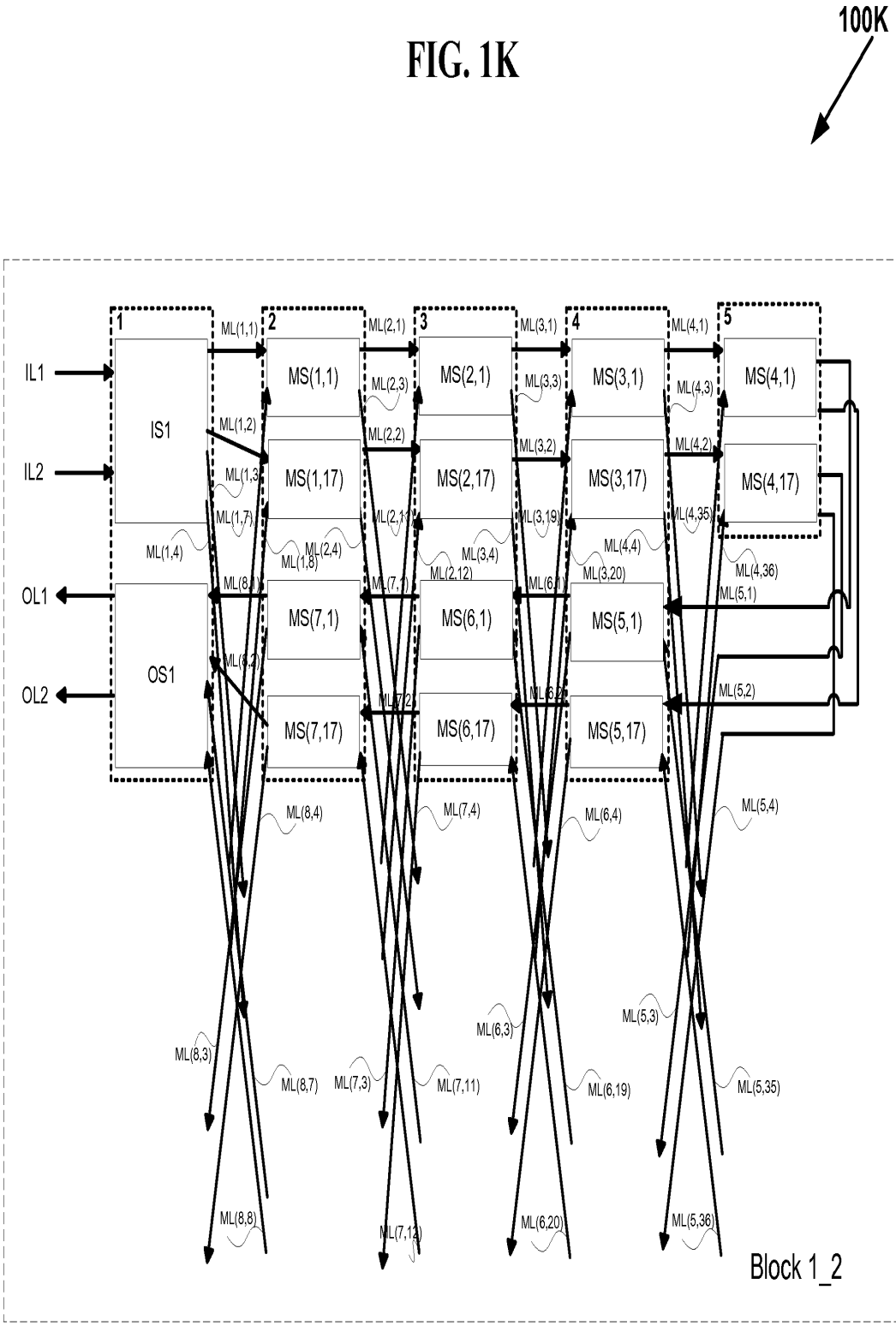
ML(5,36)
Block 1_2

FIG. 1K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OL1
OL2
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OS1
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ML(7,12)
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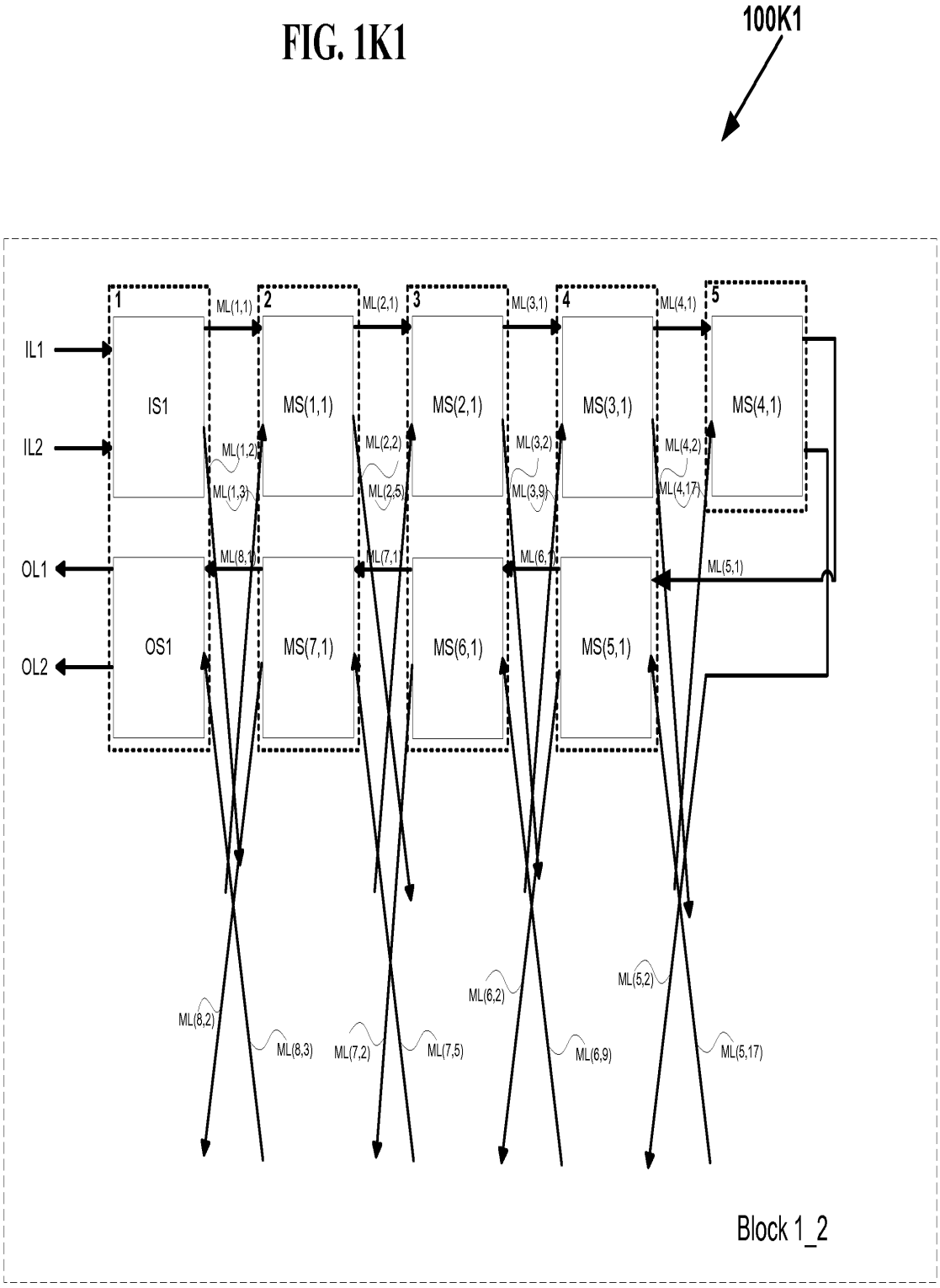
ML(8,8)
Block 1_2

FIG. 1K1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IL2
OL1
OL2
IS1
OS1
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MS(2,1)
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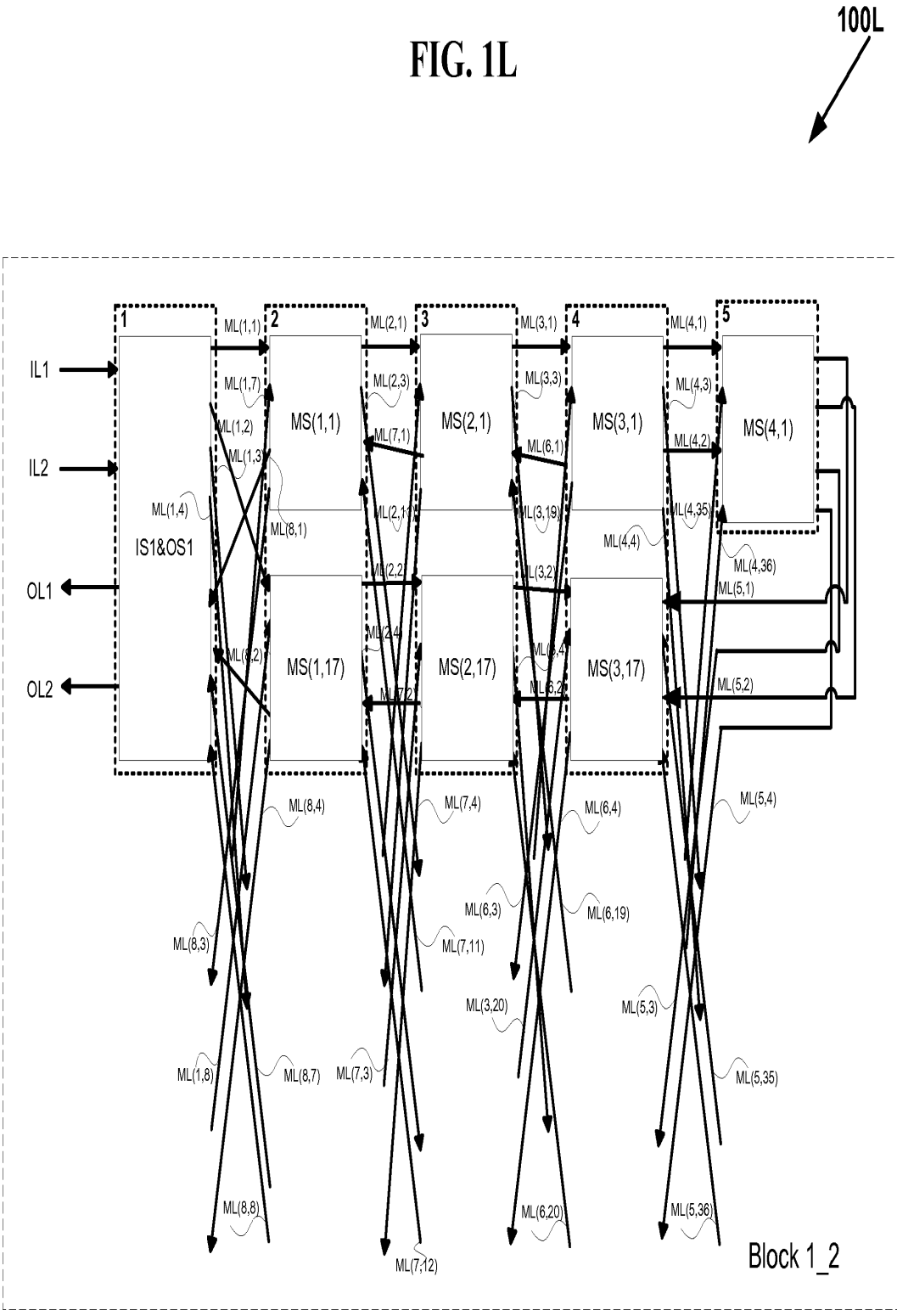
ML(7,1)
ML(6,1)
ML(5,1)
ML(8,2)
ML(8,3)
ML(7,2)
ML(7,5)
ML(6,2)
ML(6,9)
ML(5,2)
ML(5,17)
Block 1_2

FIG. 1L


100L
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IL2
OL1
OL2
IS1&OS1
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MS(1,17)
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ML(8,1)
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ML(8,3)
ML(8,4)
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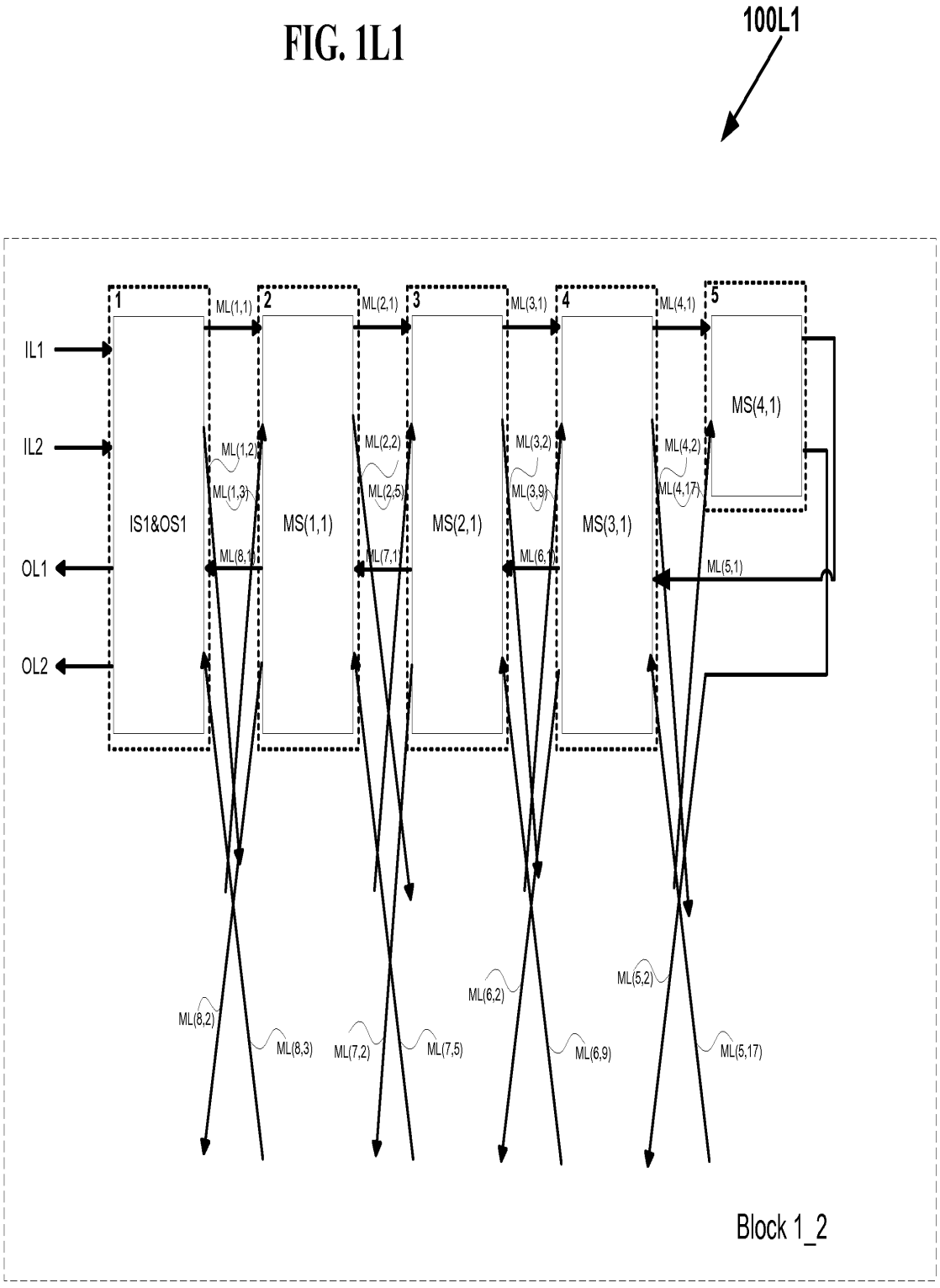
ML(3,2)
ML(3,19)
ML(3,20)
Block 1_2

FIG. 1L1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IL2
OL1
OL2
IS1&OS1
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MS(4,1)
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ML(3,9)
ML(6,1)
ML(4,2)
ML(4,17)
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ML(8,2)
ML(8,3)
ML(7,2)
ML(7,5)
ML(6,2)
ML(6,9)
ML(5,2)
ML(5,17)
Block 1_2

FIG. 2A1

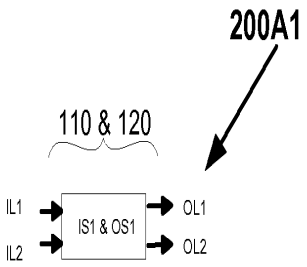


FIG. 2A2

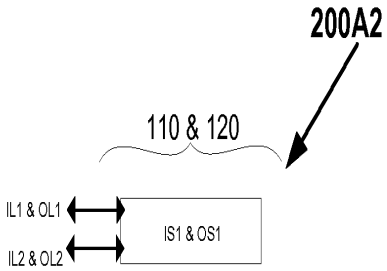


FIG. 2A3

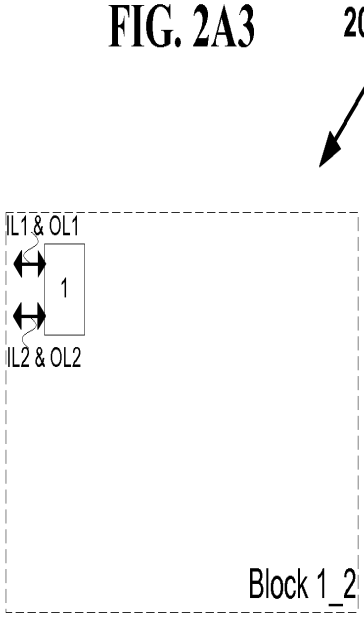


FIG. 2B1

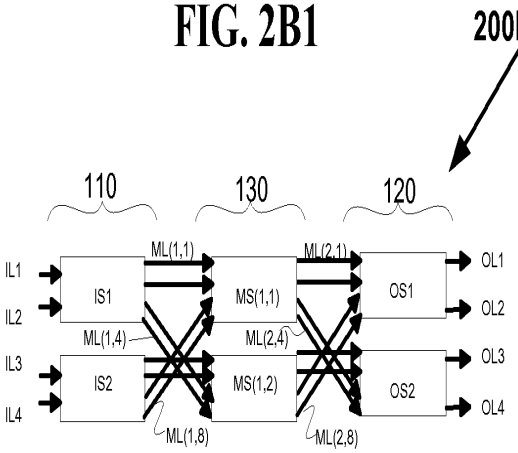


FIG. 2B2

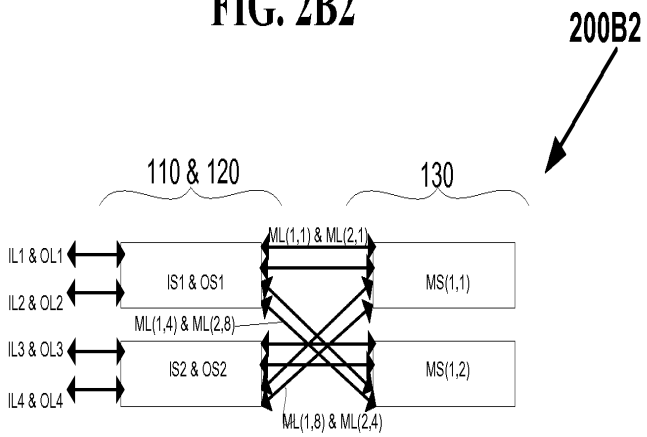


FIG. 2B3

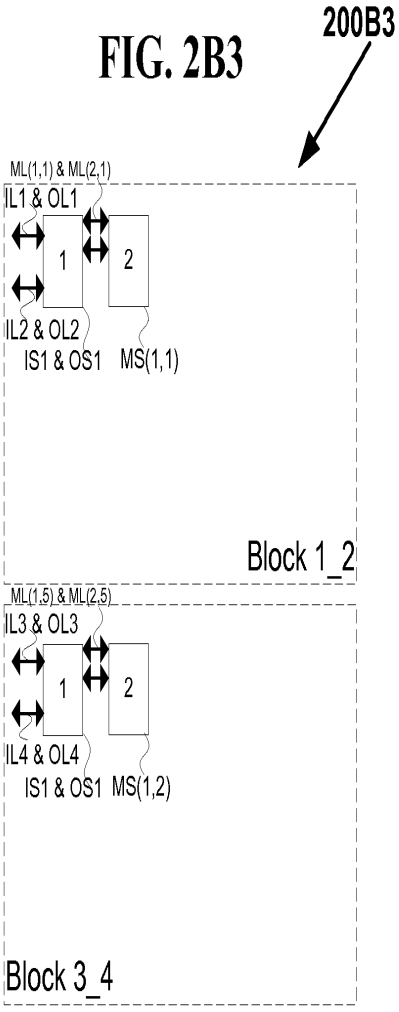


FIG. 2B4

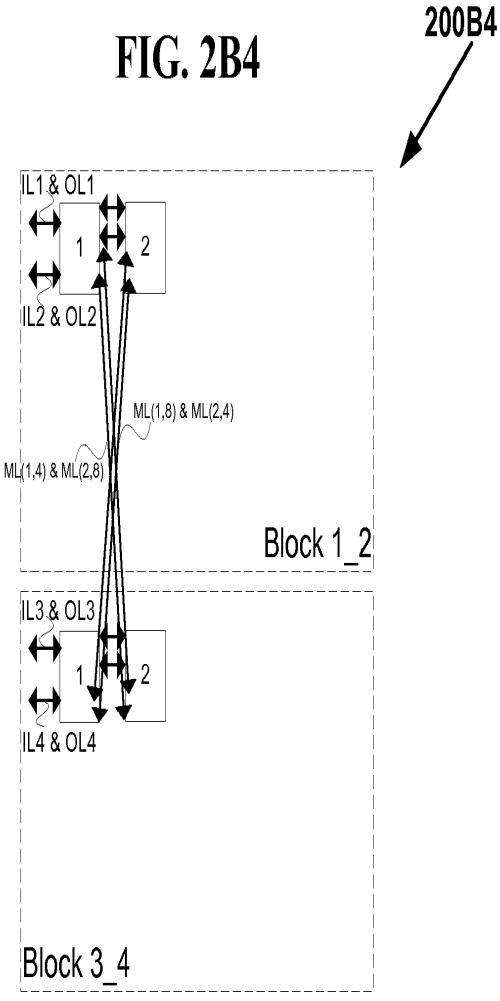


FIG. 2C11

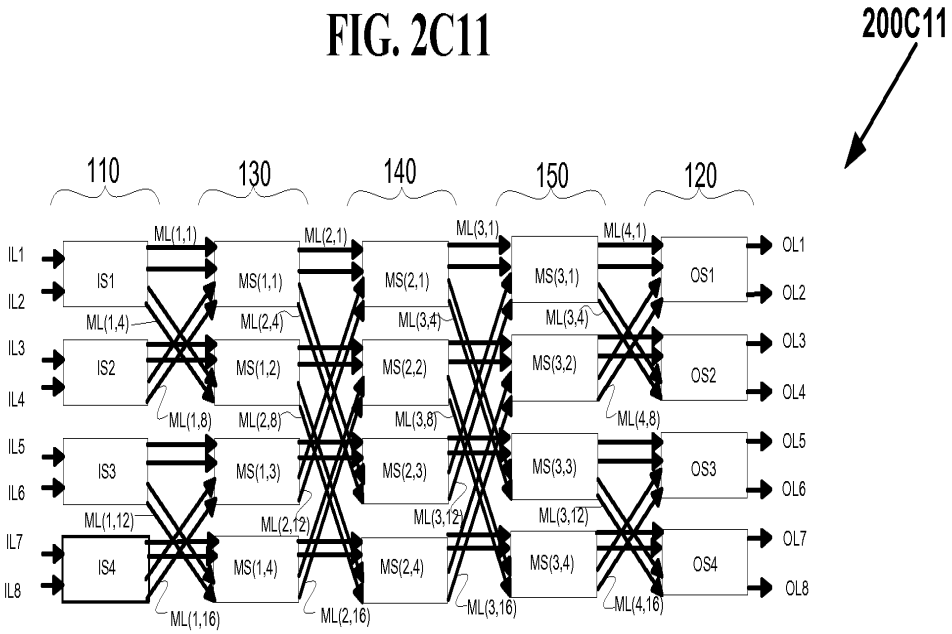


FIG. 2C12

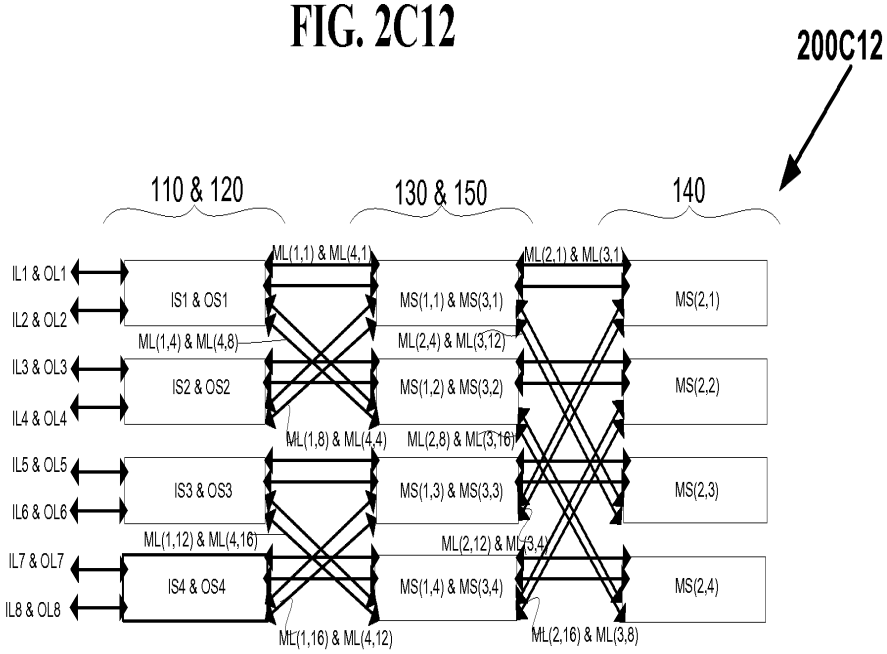


FIG. 2C21

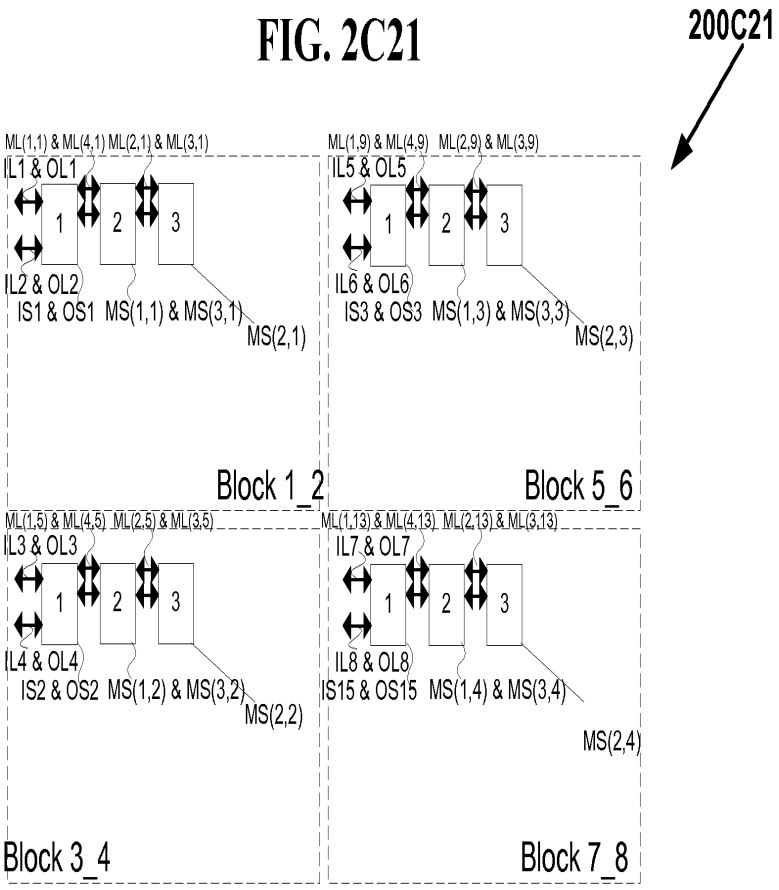


FIG. 2C22

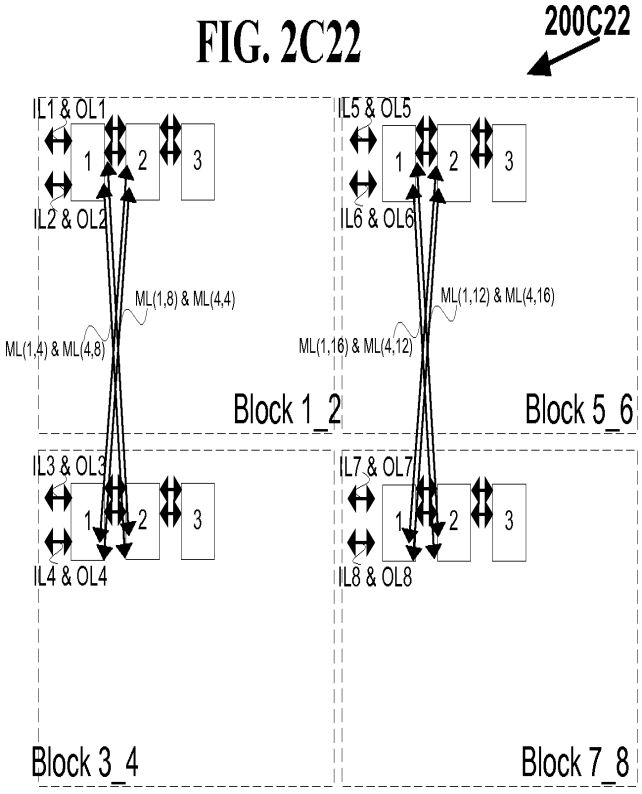


FIG. 2C23

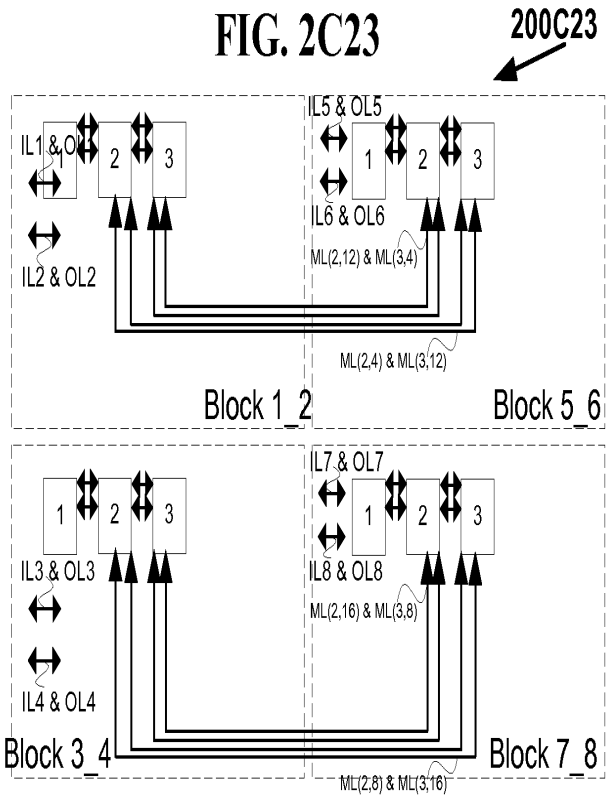
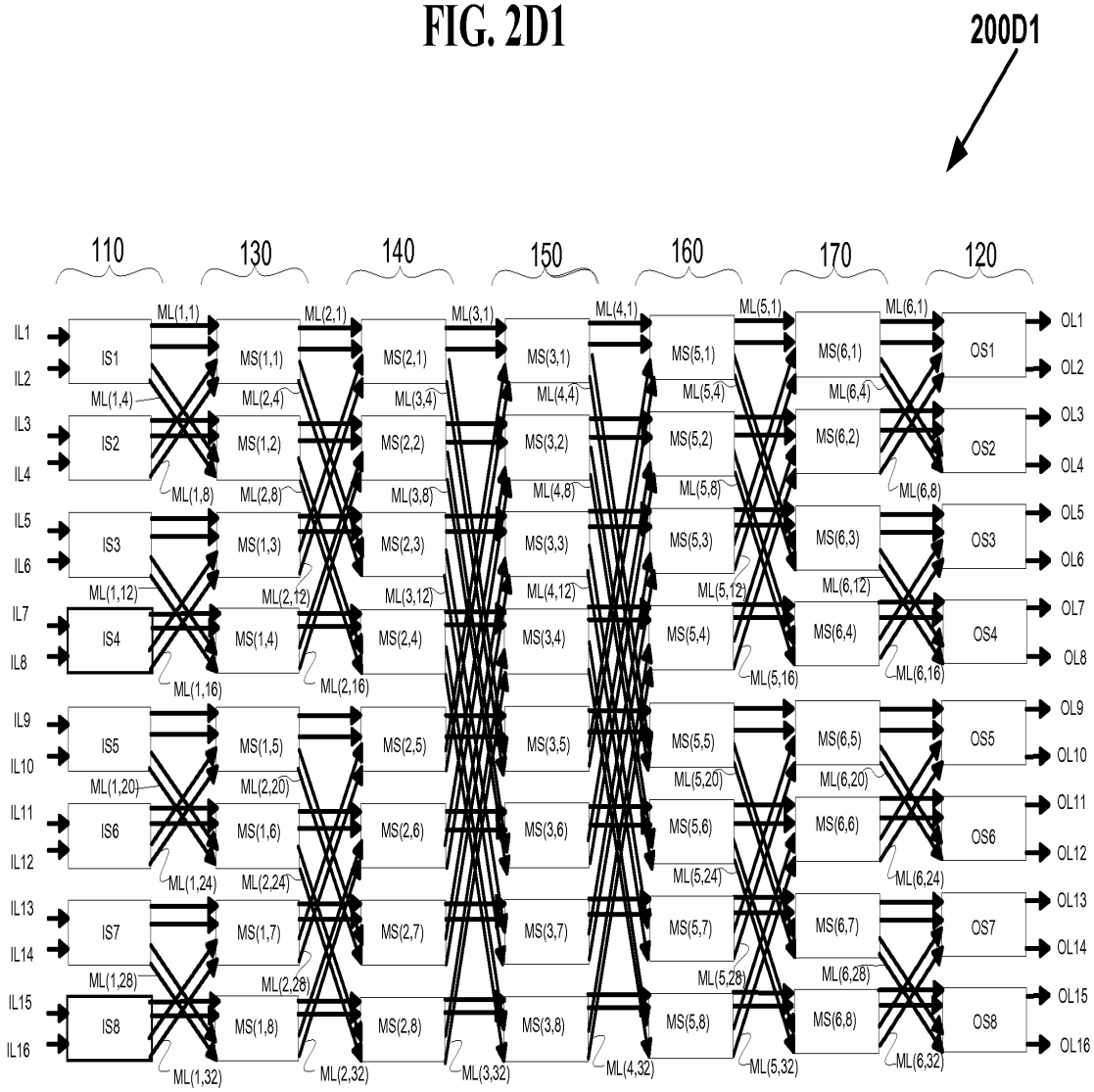


FIG. 2D1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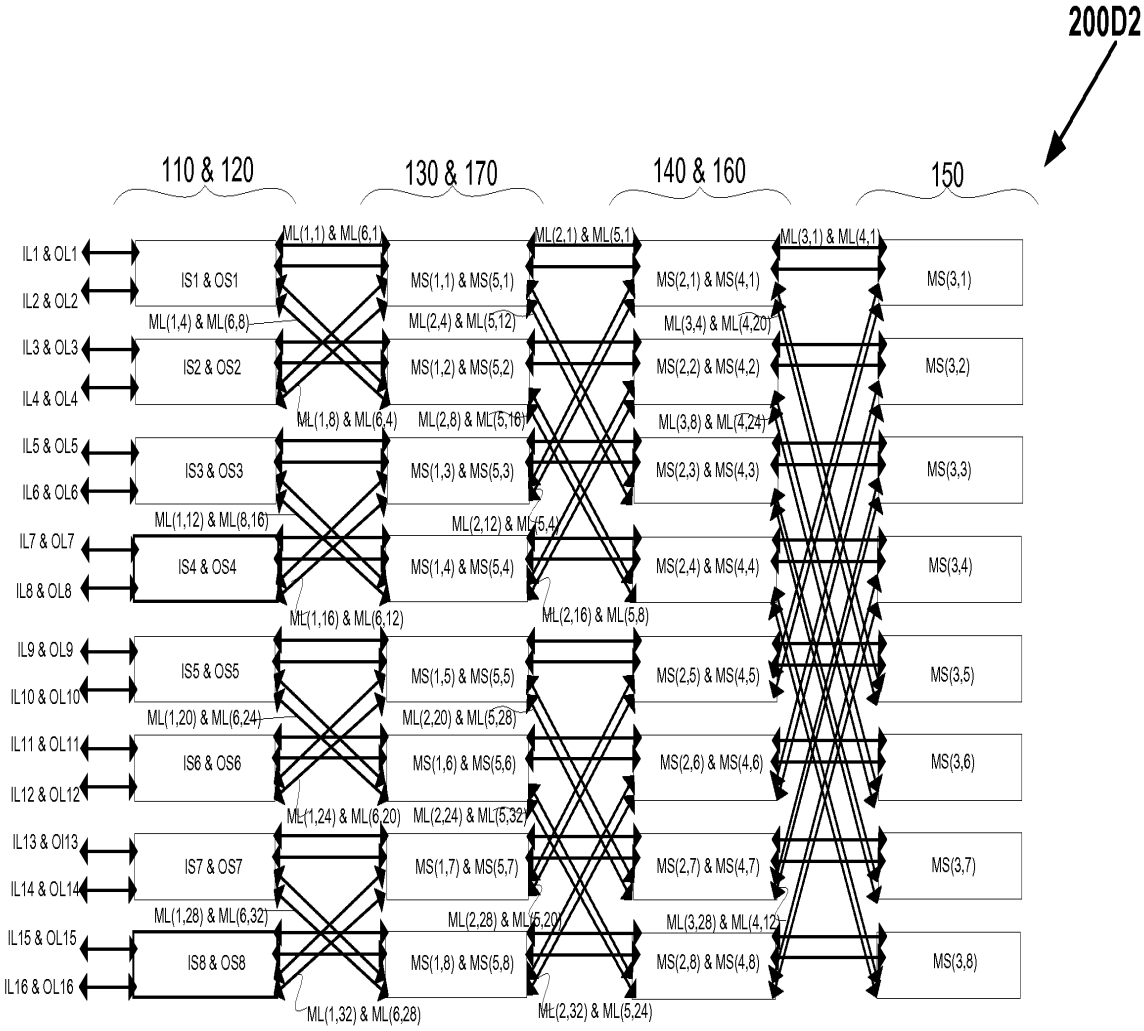
ML(6,28)
ML(6,32)

FIG. 2D2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140 & 160
150
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IL2 & OL2
IL3 & OL3
IL4 & OL4
IL5 & OL5
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IL7 & OL7
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IL11 & OL11
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IL13 & OI13
IL14 & OL14
IL15 & OL15
IL16 & OL16
IS1 & OS1
IS2 & OS2
IS3 & OS3
IS4 & OS4
IS5 & OS5
IS6 & OS6
IS7 & OS7
IS8 & OS8
ML(1,1) & ML(6,1)
ML(1,4) & ML(6,8)
ML(1,8) & ML(6,4)
ML(1,12) & ML(8,16)
ML(1,16) & ML(6,12)
ML(1,20) & ML(6,24)
ML(1,24) & ML(6,20)
ML(1,28) & ML(6,32)
ML(1,32) & ML(6,28)
MS(1,1) & MS(5,1)
MS(1,2) & MS(5,2)
MS(1,3) & MS(5,3)
MS(1,4) & MS(5,4)
MS(1,5) & MS(5,5)
MS(1,6) & MS(5,6)
MS(1,7) & MS(5,7)
MS(1,8) & MS(5,8)
ML(2,1) & ML(5,1)
ML(2,4) & ML(5,12)
ML(2,8) & ML(5,16)
ML(2,12) & ML(5,4)
ML(2,16) & ML(5,8)
ML(2,20) & ML(5,28)
ML(2,24) & ML(5,32)
ML(2,28) & ML(5,20)
ML(2,32) & ML(5,24)
MS(2,1) & MS(4,1)
MS(2,2) & MS(4,2)
MS(2,3) & MS(4,3)
MS(2,4) & MS(4,4)
MS(2,5) & MS(4,5)
MS(2,6) & MS(4,6)
MS(2,7) & MS(4,7)
MS(2,8) & MS(4,8)
ML(3,1) & ML(4,1)
ML(3,4) & ML(4,20)
ML(3,8) & ML(4,24)
ML(3,28) & ML(4,12)
MS(3,1)
MS(3,2)
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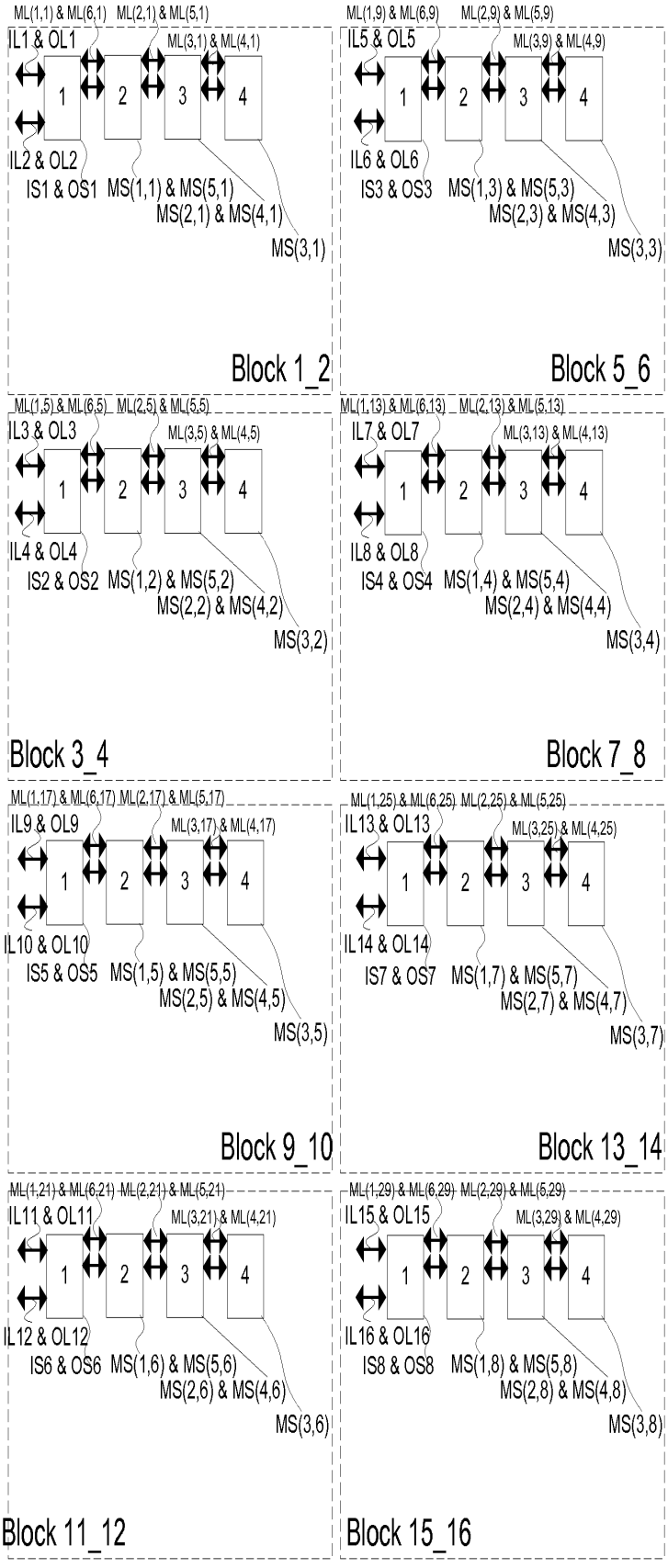
MS(3,5)
MS(3,6)
MS(3,7)
MS(3,8)

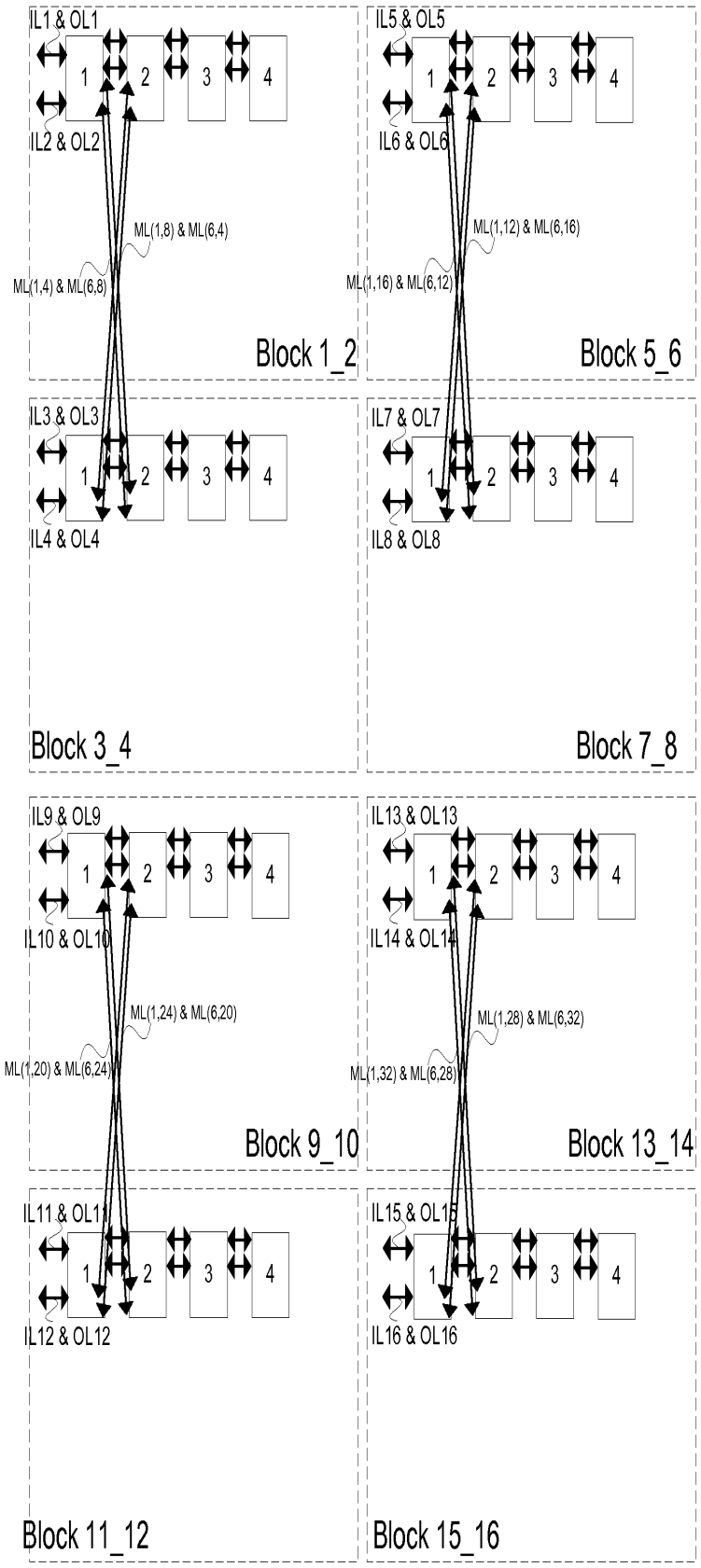
200D3

FIG. 2D3



200D4

FIG. 2D4



200D5

FIG. 2D5

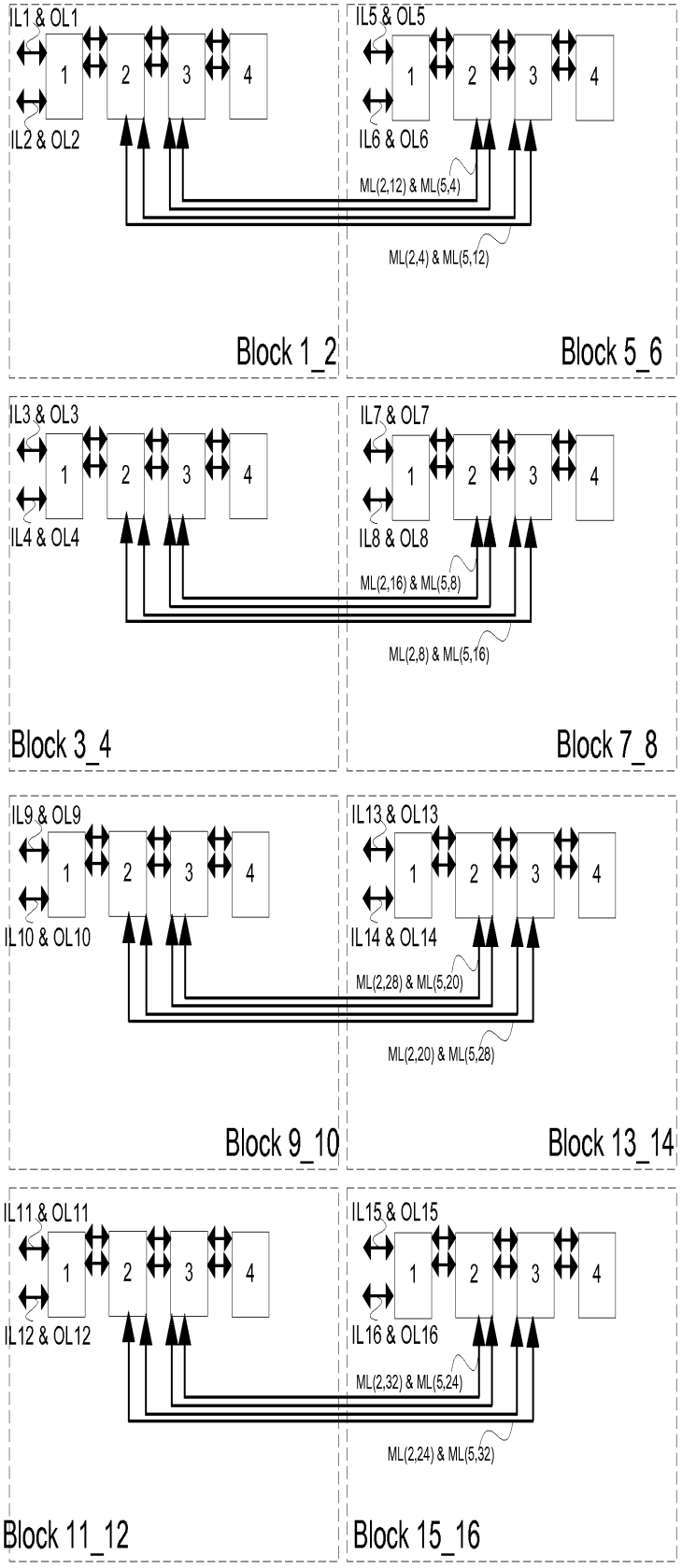


FIG. 2D6

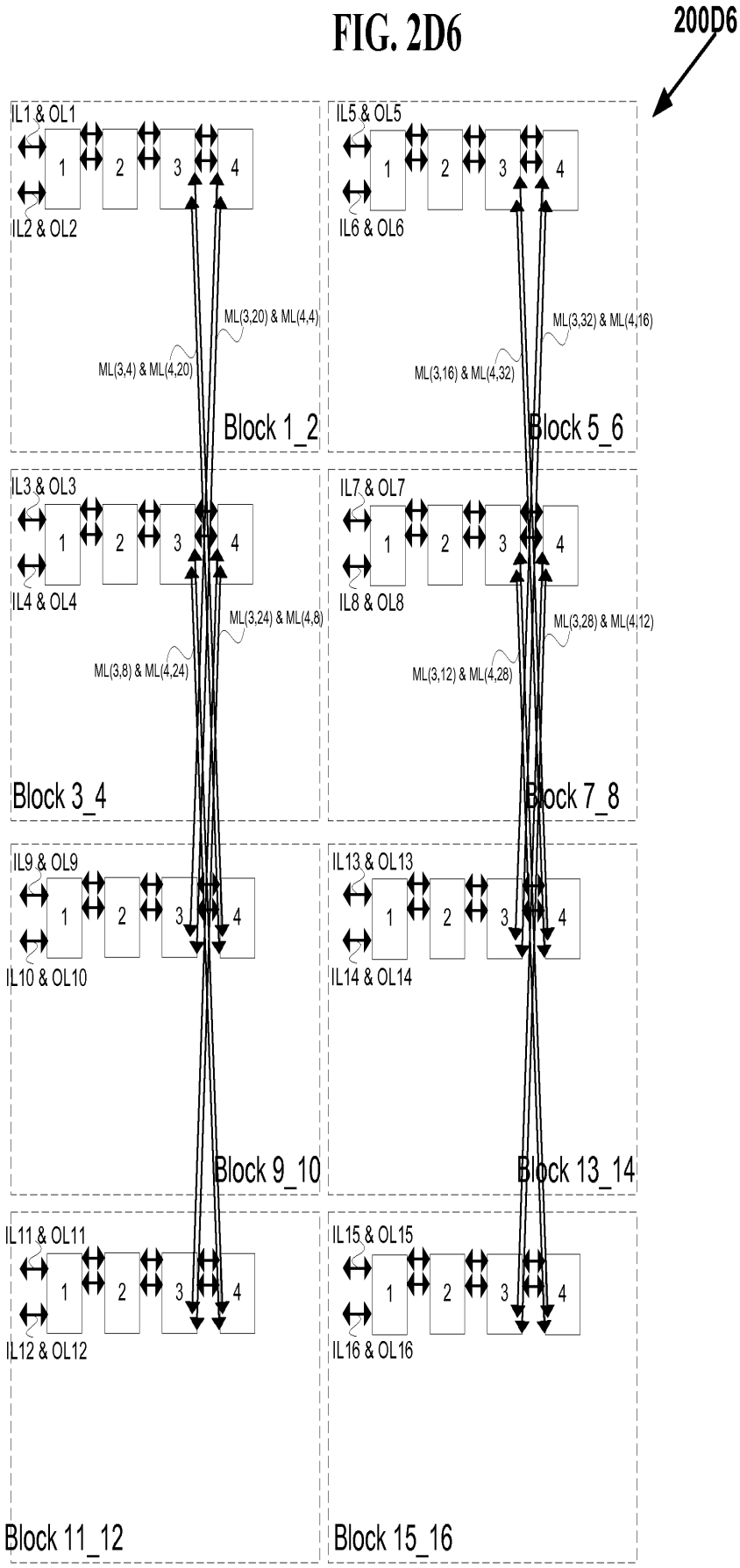

200D6
IL1 & OL1
IL2 & OL2
IL5 & OL5
IL6 & OL6
ML(3,20) & ML(4,4)
ML(3,4) & ML(4,20)
ML(3,32) & ML(4,16)
ML(3,16) & ML(4,32)
Block 1_2
Block 5_6
IL3 & OL3
IL4 & OL4
IL7 & OL7
IL8 & OL8
ML(3,24) & ML(4,8)
ML(3,8) & ML(4,24)
ML(3,28) & ML(4,12)
ML(3,12) & ML(4,28)
Block 3_4
Block 7_8
IL9 & OL9
IL10 & OL10
IL13 & OL13
IL14 & OL14
Block 9_10
Block 13_14
IL11 & OL11
IL12 & OL12
IL15 & OL15
IL16 & OL16
Block 11_12
Block 15_16

FIG. 3A

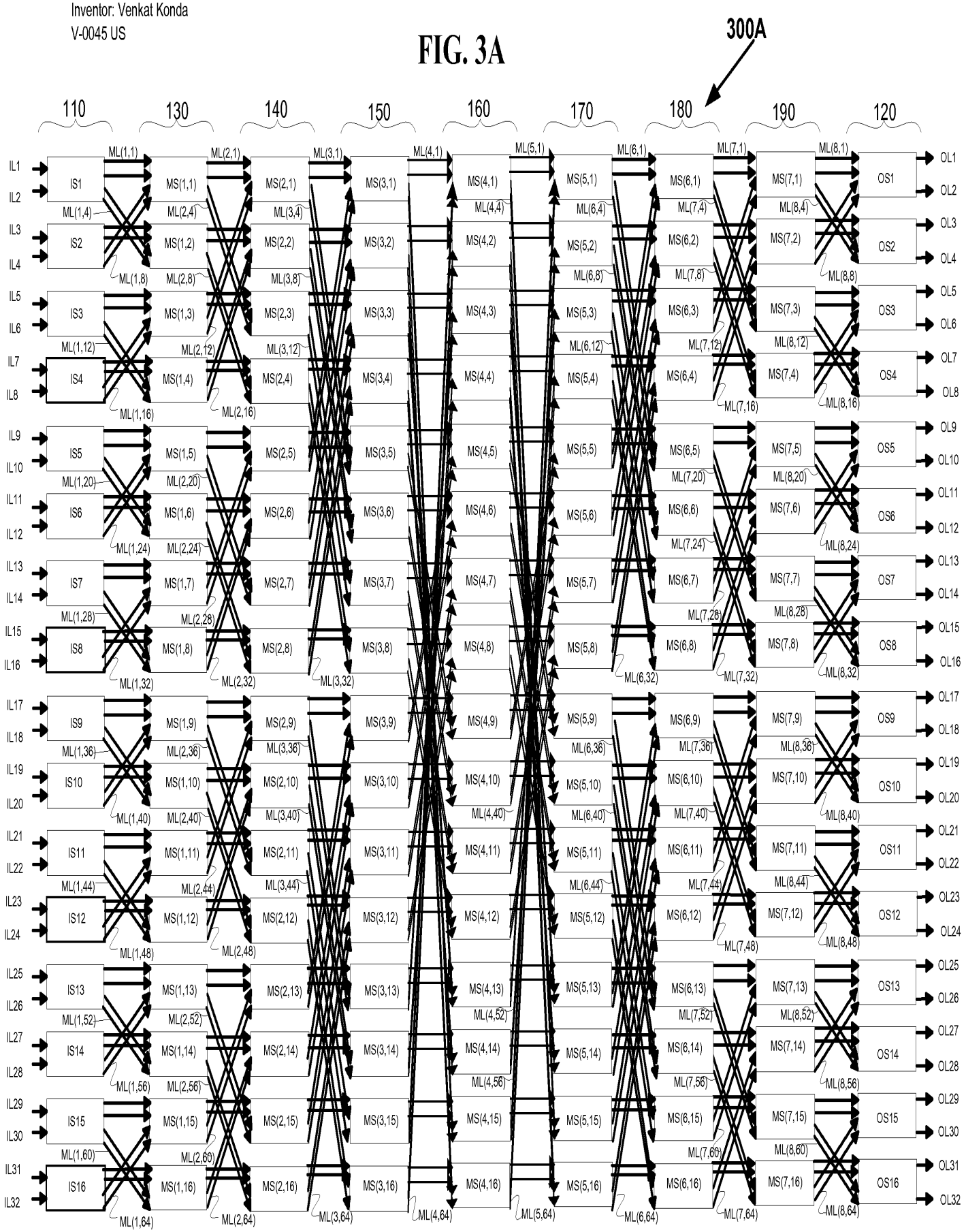
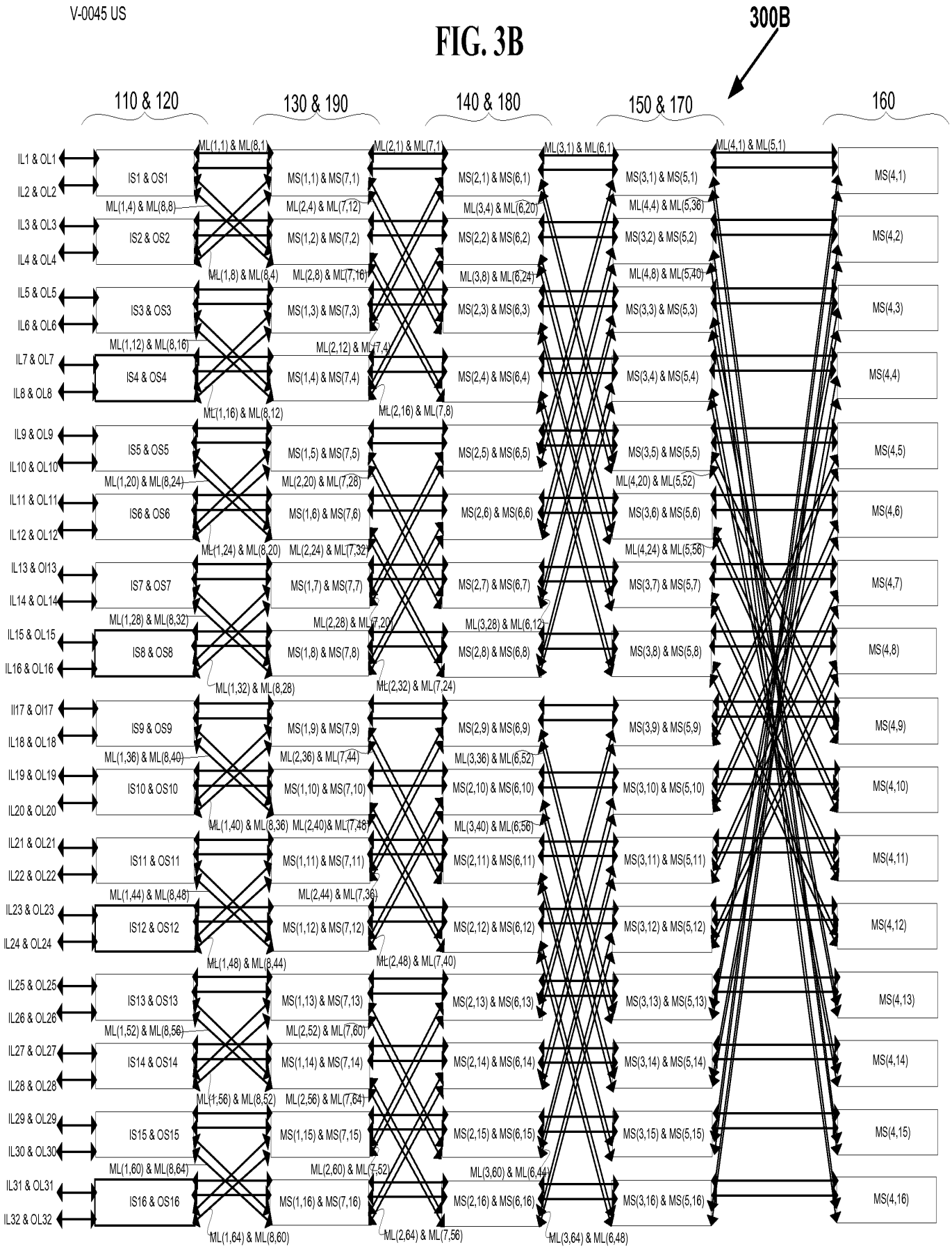
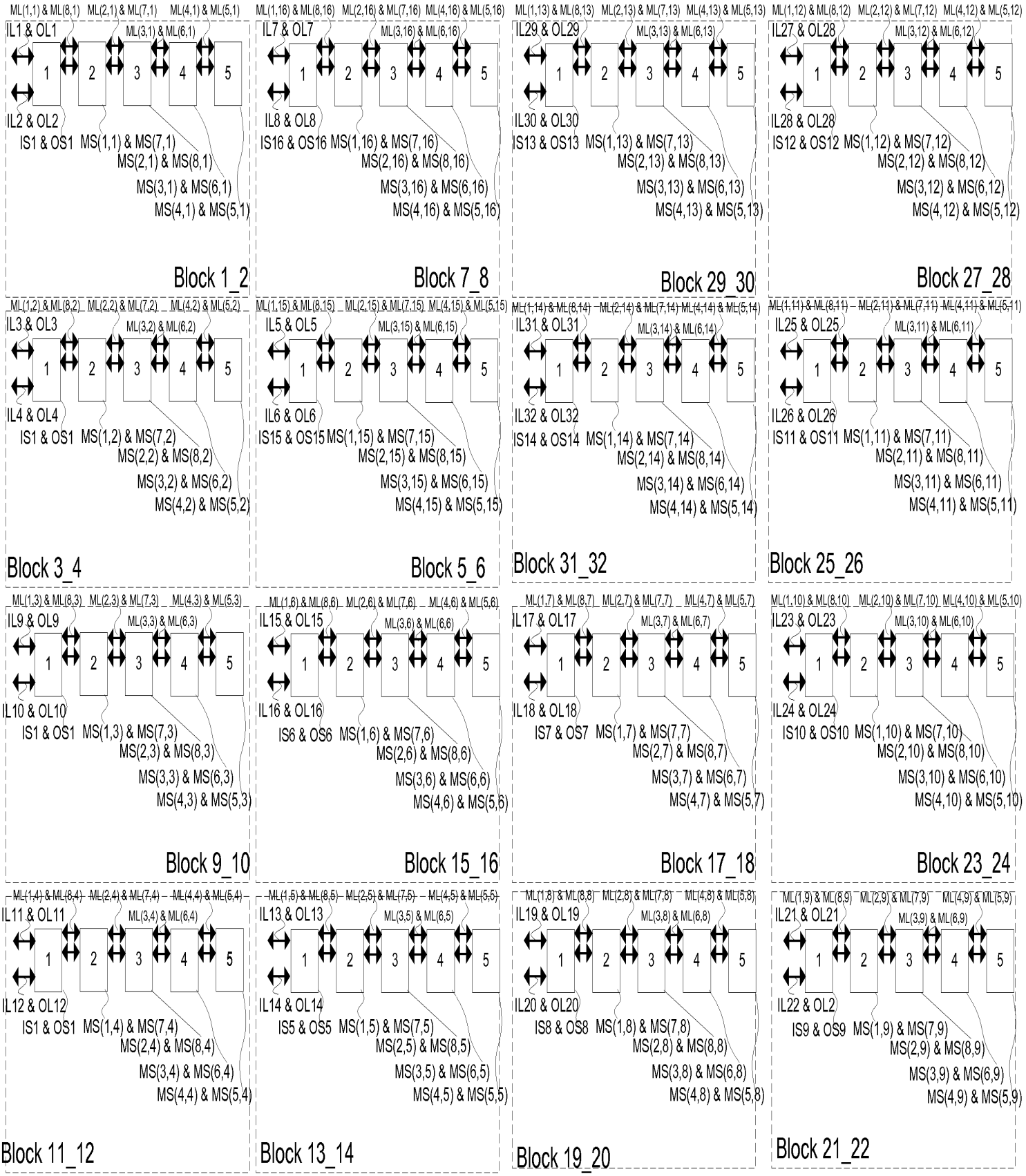

300A
110
130
140
150
160
170
180
190
120
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
IL9
IL10
IL11
IL12
IL13
IL14
IL15
IL16
IL17
IL18
IL19
IL20
IL21
IL22
IL23
IL24
IL25
IL26
IL27
IL28
IL29
IL30
IL31
IL32
IS1
IS2
IS3
IS4
IS5
IS6
IS7
IS8
IS9
IS10
IS11
IS12
IS13
IS14
IS15
IS16
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
OL9
OL10
OL11
OL12
OL13
OL14
OL15
OL16
OL17
OL18
OL19
OL20
OL21
OL22
OL23
OL24
OL25
OL26
OL27
OL28
OL29
OL30
OL31
OL32
OS1
OS2
OS3
OS4
OS5
OS6
OS7
OS8
OS9
OS10
OS11
OS12
OS13
OS14
OS15
OS16

FIG. 3B


300B
110 & 120
130 & 190
140 & 180
150 & 170
160
IL1 & OL1
IL2 & OL2
IL3 & OL3
IL4 & OL4
IL5 & OL5
IL6 & OL6
IL7 & OL7
IL8 & OL8
IL9 & OL9
IL10 & OL10
IL11 & OL11
IL12 & OL12
IL13 & OI13
IL14 & OL14
IL15 & OL15
IL16 & OL16
II17 & OI17
IL18 & OL18
IL19 & OL19
IL20 & OL20
IL21 & OL21
IL22 & OL22
IL23 & OL23
IL24 & OL24
IL25 & OL25
IL26 & OL26
IL27 & OL27
IL28 & OL28
IL29 & OL29
IL30 & OL30
IL31 & OL31
IL32 & OL32
IS1 & OS1
IS2 & OS2
IS3 & OS3
IS4 & OS4
IS5 & OS5
IS6 & OS6
IS7 & OS7
IS8 & OS8
IS9 & OS9
IS10 & OS10
IS11 & OS11
IS12 & OS12
IS13 & OS13
IS14 & OS14
IS15 & OS15
IS16 & OS16
ML(1,1) & ML(8,1)
ML(1,4) & ML(8,8)
ML(1,8) & ML(8,4)
ML(1,12) & ML(8,16)
ML(1,16) & ML(8,12)
ML(1,20) & ML(8,24)
ML(1,24) & ML(8,20)
ML(1,28) & ML(8,32)
ML(1,32) & ML(8,28)
ML(1,36) & ML(8,40)
ML(1,40) & ML(8,36)
ML(1,44) & ML(8,48)
ML(1,48) & ML(8,44)
ML(1,52) & ML(8,56)
ML(1,56) & ML(8,52)
ML(1,60) & ML(8,64)
ML(1,64) & ML(8,60)
ML(2,1) & ML(7,1)
ML(2,4) & ML(7,12)
ML(2,8) & ML(7,16)
ML(2,12) & ML(7,4)
ML(2,16) & ML(7,8)
ML(2,20) & ML(7,28)
ML(2,24) & ML(7,32)
ML(2,28) & ML(7,20)
ML(2,32) & ML(7,24)
ML(2,36) & ML(7,44)
ML(2,40)& ML(7,48)
ML(2,44) & ML(7,36)
ML(2,48) & ML(7,40)
ML(2,52) & ML(7,60)
ML(2,56) & ML(7,64)
ML(2,60) & ML(7,52)
ML(2,64) & ML(7,56)
ML(3,1) & ML(6,1)
ML(3,4) & ML(6,20)
ML(3,8) & ML(6,24)
ML(3,12) & ML(6,4)
ML(3,16) & ML(6,8)
ML(3,20) & ML(6,28)
ML(3,24) & ML(6,32)
ML(3,28) & ML(6,12)
ML(3,32) & ML(6,16)
ML(3,36) & ML(6,52)
ML(3,40) & ML(6,56)
ML(3,44) & ML(6,36)
ML(3,48) & ML(6,40)
ML(3,52) & ML(6,60)
ML(3,56) & ML(6,64)
ML(3,60) & ML(6,44)
ML(3,64) & ML(6,48)
ML(4,1) & ML(5,1)
ML(4,4) & ML(5,36)
ML(4,8) & ML(5,40)
ML(4,12) & ML(5,4)
ML(4,16) & ML(5,8)
ML(4,20) & ML(5,52)
ML(4,24) & ML(5,56)
ML(4,28) & ML(5,20)
ML(4,32) & ML(5,24)
ML(4,36) & ML(5,44)
ML(4,40) & ML(5,48)
ML(4,44) & ML(5,28)
ML(4,48) & ML(5,32)
ML(4,52) & ML(5,12)
ML(4,56) & ML(5,16)
ML(4,60) & ML(5,60)
ML(4,64) & ML(5,64)
MS(1,1) & MS(7,1)
MS(1,2) & MS(7,2)
MS(1,3) & MS(7,3)
MS(1,4) & MS(7,4)
MS(1,5) & MS(7,5)
MS(1,6) & MS(7,6)
MS(1,7) & MS(7,7)
MS(1,8) & MS(7,8)
MS(1,9) & MS(7,9)
MS(1,10) & MS(7,10)
MS(1,11) & MS(7,11)
MS(1,12) & MS(7,12)
MS(1,13) & MS(7,13)
MS(1,14) & MS(7,14)
MS(1,15) & MS(7,15)
MS(1,16) & MS(7,16)
MS(2,1) & MS(6,1)
MS(2,2) & MS(6,2)
MS(2,3) & MS(6,3)
MS(2,4) & MS(6,4)
MS(2,5) & MS(6,5)
MS(2,6) & MS(6,6)
MS(2,7) & MS(6,7)
MS(2,8) & MS(6,8)
MS(2,9) & MS(6,9)
MS(2,10) & MS(6,10)
MS(2,11) & MS(6,11)
MS(2,12) & MS(6,12)
MS(2,13) & MS(6,13)
MS(2,14) & MS(6,14)
MS(2,15) & MS(6,15)
MS(2,16) & MS(6,16)
MS(3,1) & MS(5,1)
MS(3,2) & MS(5,2)
MS(3,3) & MS(5,3)
MS(3,4) & MS(5,4)
MS(3,5) & MS(5,5)
MS(3,6) & MS(5,6)
MS(3,7) & MS(5,7)
MS(3,8) & MS(5,8)
MS(3,9) & MS(5,9)
MS(3,10) & MS(5,10)
MS(3,11) & MS(5,11)
MS(3,12) & MS(5,12)
MS(3,13) & MS(5,13)
MS(3,14) & MS(5,14)
MS(3,15) & MS(5,15)
MS(3,16) & MS(5,16)
MS(4,1)
MS(4,2)
MS(4,3)
MS(4,4)
MS(4,5)
MS(4,6)
MS(4,7)
MS(4,8)
MS(4,9)
MS(4,10)
MS(4,11)
MS(4,12)
MS(4,13)
MS(4,14)
MS(4,15)
MS(4,16)

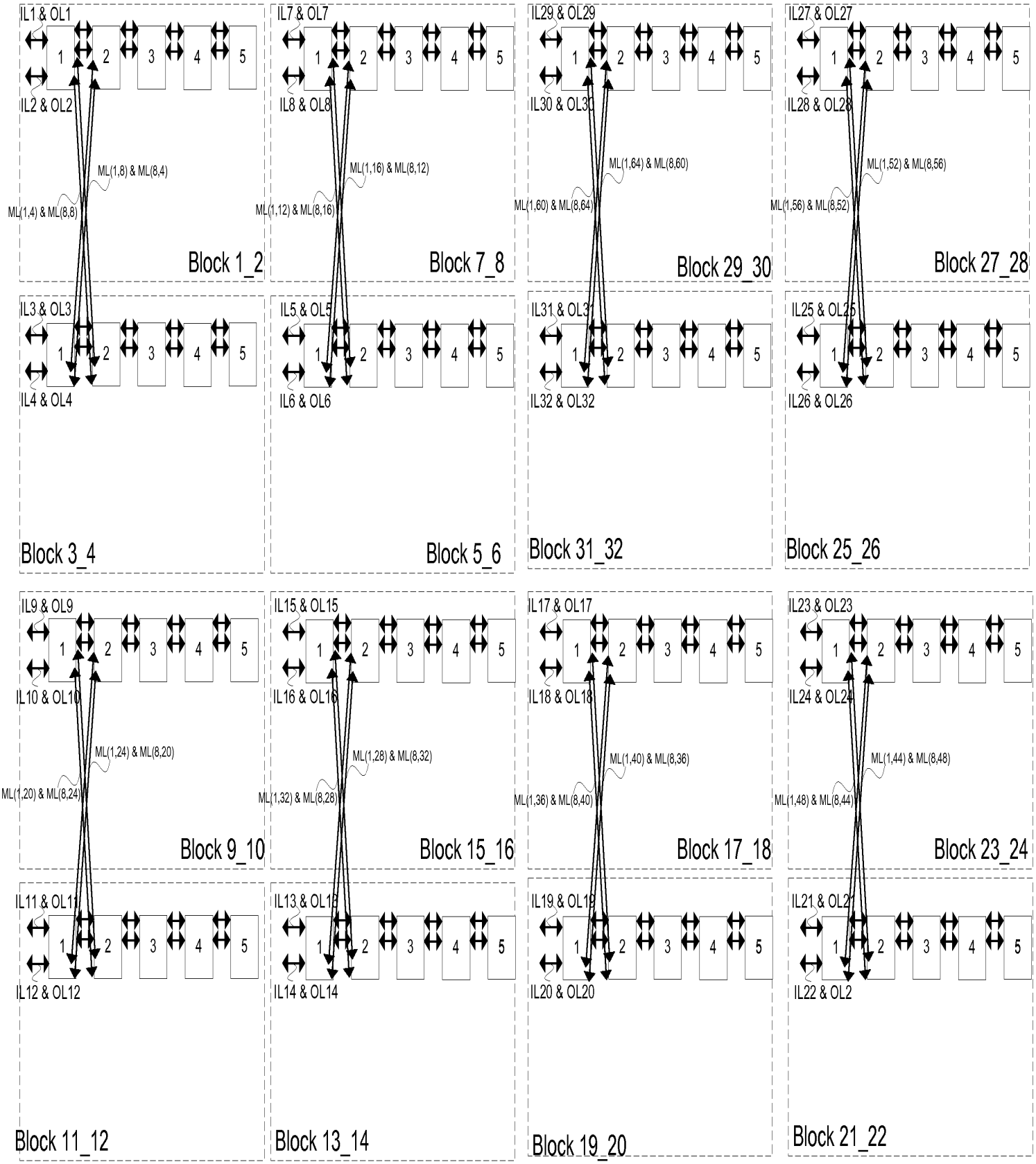
300C

FIG. 3C


ML(1,1) & ML(8,1) ML(2,1) & ML(7,1) ML(4,1) & ML(5,1)
IL1 & OL1
ML(3,1) & ML(6,1)
IL2 & OL2
IS1 & OS1 MS(1,1) & MS(7,1)
MS(2,1) & MS(8,1)
MS(3,1) & MS(6,1)
MS(4,1) & MS(5,1)
Block 1_2
ML(1,16) & ML(8,16) ML(2,16) & ML(7,16) ML(4,16) & ML(5,16)
IL7 & OL7
ML(3,16) & ML(6,16)
IL8 & OL8
IS16 & OS16 MS(1,16) & MS(7,16)
MS(2,16) & MS(8,16)
MS(3,16) & MS(6,16)
MS(4,16) & MS(5,16)
Block 7_8
ML(1,13) & ML(8,13) ML(2,13) & ML(7,13) ML(4,13) & ML(5,13)
IL29 & OL29
ML(3,13) & ML(6,13)
IL30 & OL30
IS13 & OS13 MS(1,13) & MS(7,13)
MS(2,13) & MS(8,13)
MS(3,13) & MS(6,13)
MS(4,13) & MS(5,13)
Block 29_30
ML(1,12) & ML(8,12) ML(2,12) & ML(7,12) ML(4,12) & ML(5,12)
IL27 & OL28
ML(3,12) & ML(6,12)
IL28 & OL28
IS12 & OS12 MS(1,12) & MS(7,12)
MS(2,12) & MS(8,12)
MS(3,12) & MS(6,12)
MS(4,12) & MS(5,12)
Block 27_28
ML(1,2) & ML(8,2) ML(2,2) & ML(7,2) ML(4,2) & ML(5,2)
IL3 & OL3
ML(3,2) & ML(6,2)
IL4 & OL4
IS1 & OS1 MS(1,2) & MS(7,2)
MS(2,2) & MS(8,2)
MS(3,2) & MS(6,2)
MS(4,2) & MS(5,2)
Block 3_4
ML(1,15) & ML(8,15) ML(2,15) & ML(7,15) ML(4,15) & ML(5,15)
IL5 & OL5
ML(3,15) & ML(6,15)
IL6 & OL6
IS15 & OS15 MS(1,15) & MS(7,15)
MS(2,15) & MS(8,15)
MS(3,15) & MS(6,15)
MS(4,15) & MS(5,15)
Block 5_6
ML(1,14) & ML(8,14) ML(2,14) & ML(7,14) ML(4,14) & ML(5,14)
IL31 & OL31
ML(3,14) & ML(6,14)
IL32 & OL32
IS14 & OS14 MS(1,14) & MS(7,14)
MS(2,14) & MS(8,14)
MS(3,14) & MS(6,14)
MS(4,14) & MS(5,14)
Block 31_32
ML(1,11) & ML(8,11) ML(2,11) & ML(7,11) ML(4,11) & ML(5,11)
IL25 & OL25
ML(3,11) & ML(6,11)
IL26 & OL26
IS11 & OS11 MS(1,11) & MS(7,11)
MS(2,11) & MS(8,11)
MS(3,11) & MS(6,11)
MS(4,11) & MS(5,11)
Block 25_26
ML(1,3) & ML(8,3) ML(2,3) & ML(7,3) ML(4,3) & ML(5,3)
IL9 & OL9
ML(3,3) & ML(6,3)
IL10 & OL10
IS1 & OS1 MS(1,3) & MS(7,3)
MS(2,3) & MS(8,3)
MS(3,3) & MS(6,3)
MS(4,3) & MS(5,3)
Block 9_10
ML(1,6) & ML(8,6) ML(2,6) & ML(7,6) ML(4,6) & ML(5,6)
IL15 & OL15
ML(3,6) & ML(6,6)
IL16 & OL16
IS6 & OS6 MS(1,6) & MS(7,6)
MS(2,6) & MS(8,6)
MS(3,6) & MS(6,6)
MS(4,6) & MS(5,6)
Block 15_16
ML(1,7) & ML(8,7) ML(2,7) & ML(7,7) ML(4,7) & ML(5,7)
IL17 & OL17
ML(3,7) & ML(6,7)
IL18 & OL18
IS7 & OS7 MS(1,7) & MS(7,7)
MS(2,7) & MS(8,7)
MS(3,7) & MS(6,7)
MS(4,7) & MS(5,7)
Block 17_18
ML(1,10) & ML(8,10) ML(2,10) & ML(7,10) ML(4,10) & ML(5,10)
IL23 & OL23
ML(3,10) & ML(6,10)
IL24 & OL24
IS10 & OS10 MS(1,10) & MS(7,10)
MS(2,10) & MS(8,10)
MS(3,10) & MS(6,10)
MS(4,10) & MS(5,10)
Block 23_24
ML(1,4) & ML(8,4) ML(2,4) & ML(7,4) ML(4,4) & ML(5,4)
IL11 & OL11
ML(3,4) & ML(6,4)
IL12 & OL12
IS1 & OS1 MS(1,4) & MS(7,4)
MS(2,4) & MS(8,4)
MS(3,4) & MS(6,4)
MS(4,4) & MS(5,4)
Block 11_12
ML(1,5) & ML(8,5) ML(2,5) & ML(7,5) ML(4,5) & ML(5,5)
IL13 & OL13
ML(3,5) & ML(6,5)
IL14 & OL14
IS5 & OS5 MS(1,5) & MS(7,5)
MS(2,5) & MS(8,5)
MS(3,5) & MS(6,5)
MS(4,5) & MS(5,5)
Block 13_14
ML(1,8) & ML(8,8) ML(2,8) & ML(7,8) ML(4,8) & ML(5,8)
IL19 & OL19
ML(3,8) & ML(6,8)
IL20 & OL20
IS8 & OS8 MS(1,8) & MS(7,8)
MS(2,8) & MS(8,8)
MS(3,8) & MS(6,8)
MS(4,8) & MS(5,8)
Block 19_20
ML(1,9) & ML(8,9) ML(2,9) & ML(7,9) ML(4,9) & ML(5,9)
IL21 & OL21
ML(3,9) & ML(6,9)
IL22 & OL2
IS9 & OS9 MS(1,9) & MS(7,9)
MS(2,9) & MS(8,9)
MS(3,9) & MS(6,9)
MS(4,9) & MS(5,9)
Block 21_22

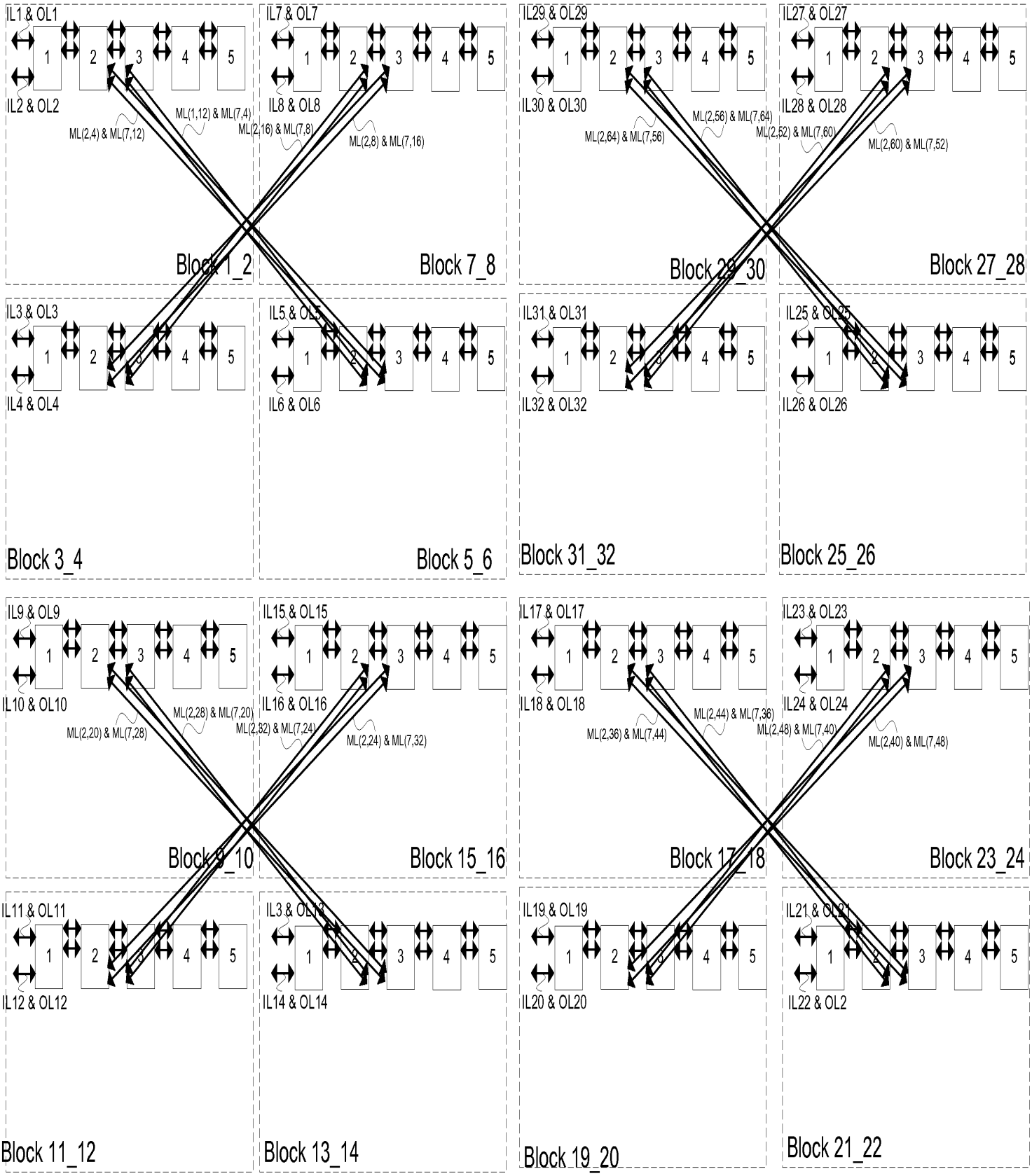
300D

FIG. 3D


IL1 & OL1
IL2 & OL2
ML(1,8) & ML(8,4)
ML(1,4) & ML(8,8)
Block 1_2
IL7 & OL7
IL8 & OL8
ML(1,16) & ML(8,12)
ML(1,12) & ML(8,16)
Block 7_8
IL29 & OL29
IL30 & OL30
ML(1,64) & ML(8,60)
ML(1,60) & ML(8,64)
Block 29_30
IL27 & OL27
IL28 & OL28
ML(1,52) & ML(8,56)
ML(1,56) & ML(8,52)
Block 27_28
IL3 & OL3
IL4 & OL4
Block 3_4
IL5 & OL5
IL6 & OL6
Block 5_6
IL31 & OL31
IL32 & OL32
Block 31_32
IL25 & OL25
IL26 & OL26
Block 25_26
IL9 & OL9
IL10 & OL10
ML(1,24) & ML(8,20)
ML(1,20) & ML(8,24)
Block 9_10
IL15 & OL15
IL16 & OL16
ML(1,28) & ML(8,32)
ML(1,32) & ML(8,28)
Block 15_16
IL17 & OL17
IL18 & OL18
ML(1,40) & ML(8,36)
ML(1,36) & ML(8,40)
Block 17_18
IL23 & OL23
IL24 & OL24
ML(1,44) & ML(8,48)
ML(1,48) & ML(8,44)
Block 23_24
IL11 & OL11
IL12 & OL12
Block 11_12
IL13 & OL13
IL14 & OL14
Block 13_14
IL19 & OL19
IL20 & OL20
Block 19_20
IL21 & OL21
IL22 & OL22
Block 21_22

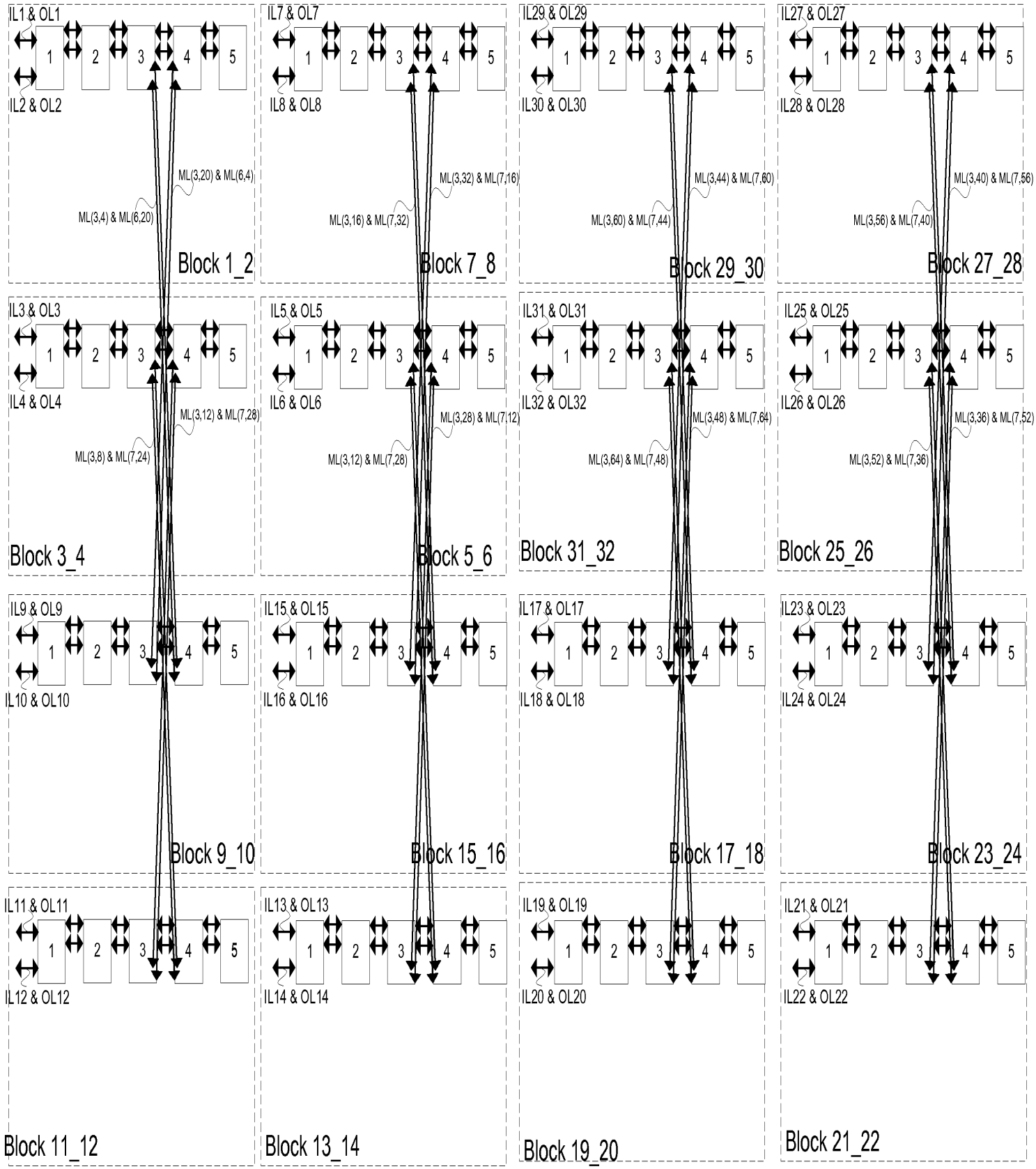
300E

FIG. 3E


IL1 & OL1
IL2 & OL2
ML(1,12) & ML(7,4)
ML(2,4) & ML(7,12)
IL7 & OL7
IL8 & OL8
ML(2,16) & ML(7,8)
ML(2,8) & ML(7,16)
Block 1_2
Block 7_8
IL29 & OL29
IL30 & OL30
ML(2,56) & ML(7,64)
ML(2,64) & ML(7,56)
IL27 & OL27
IL28 & OL28
ML(2,52) & ML(7,60)
ML(2,60) & ML(7,52)
Block 29_30
Block 27_28
IL3 & OL3
IL4 & OL4
IL5 & OL5
IL6 & OL6
Block 3_4
Block 5_6
IL31 & OL31
IL32 & OL32
IL25 & OL25
IL26 & OL26
Block 31_32
Block 25_26
IL9 & OL9
IL10 & OL10
ML(2,28) & ML(7,20)
ML(2,20) & ML(7,28)
IL15 & OL15
IL16 & OL16
ML(2,32) & ML(7,24)
ML(2,24) & ML(7,32)
Block 9_10
Block 15_16
IL17 & OL17
IL18 & OL18
ML(2,44) & ML(7,36)
ML(2,36) & ML(7,44)
IL23 & OL23
IL24 & OL24
ML(2,48) & ML(7,40)
ML(2,40) & ML(7,48)
Block 17_18
Block 23_24
IL11 & OL11
IL12 & OL12
IL13 & OL13
IL14 & OL14
Block 11_12
Block 13_14
IL19 & OL19
IL20 & OL20
IL21 & OL21
IL22 & OL2
Block 19_20
Block 21_22

300F

FIG. 3F


IL1 & OL1
IL2 & OL2
ML(3,20) & ML(6,4)
ML(3,4) & ML(6,20)
Block 1_2
IL7 & OL7
IL8 & OL8
ML(3,32) & ML(7,16)
ML(3,16) & ML(7,32)
Block 7_8
IL29 & OL29
IL30 & OL30
ML(3,44) & ML(7,60)
ML(3,60) & ML(7,44)
Block 29_30
IL27 & OL27
IL28 & OL28
ML(3,40) & ML(7,56)
ML(3,56) & ML(7,40)
Block 27_28
IL3 & OL3
IL4 & OL4
ML(3,12) & ML(7,28)
ML(3,8) & ML(7,24)
Block 3_4
IL5 & OL5
IL6 & OL6
ML(3,28) & ML(7,12)
ML(3,12) & ML(7,28)
Block 5_6
IL31 & OL31
IL32 & OL32
ML(3,48) & ML(7,64)
ML(3,64) & ML(7,48)
Block 31_32
IL25 & OL25
IL26 & OL26
ML(3,36) & ML(7,52)
ML(3,52) & ML(7,36)
Block 25_26
IL9 & OL9
IL10 & OL10
Block 9_10
IL15 & OL15
IL16 & OL16
Block 15_16
IL17 & OL17
IL18 & OL18
Block 17_18
IL23 & OL23
IL24 & OL24
Block 23_24
IL11 & OL11
IL12 & OL12
Block 11_12
IL13 & OL13
IL14 & OL14
Block 13_14
IL19 & OL19
IL20 & OL20
Block 19_20
IL21 & OL21
IL22 & OL22
Block 21_22

300G

FIG. 3G

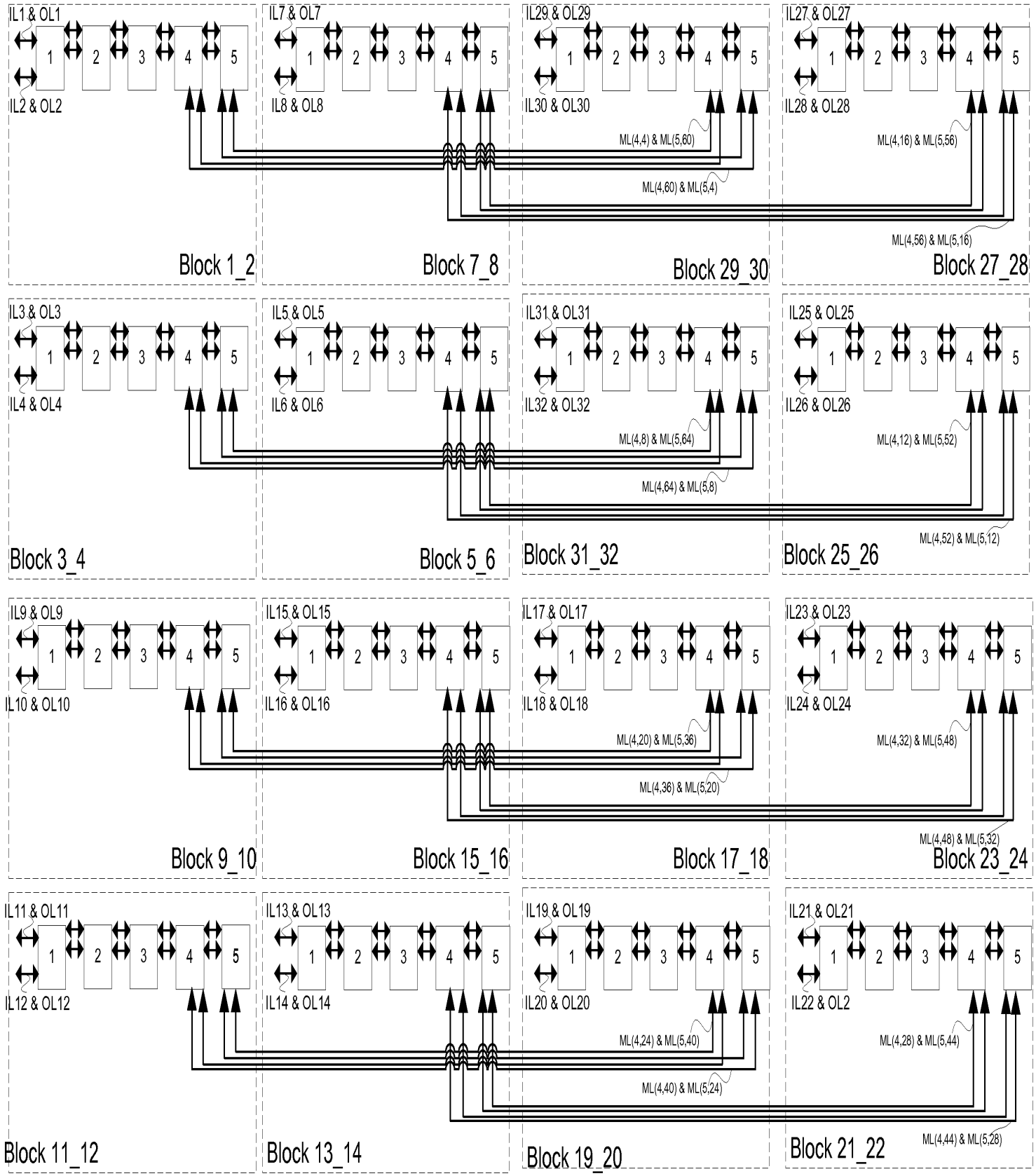
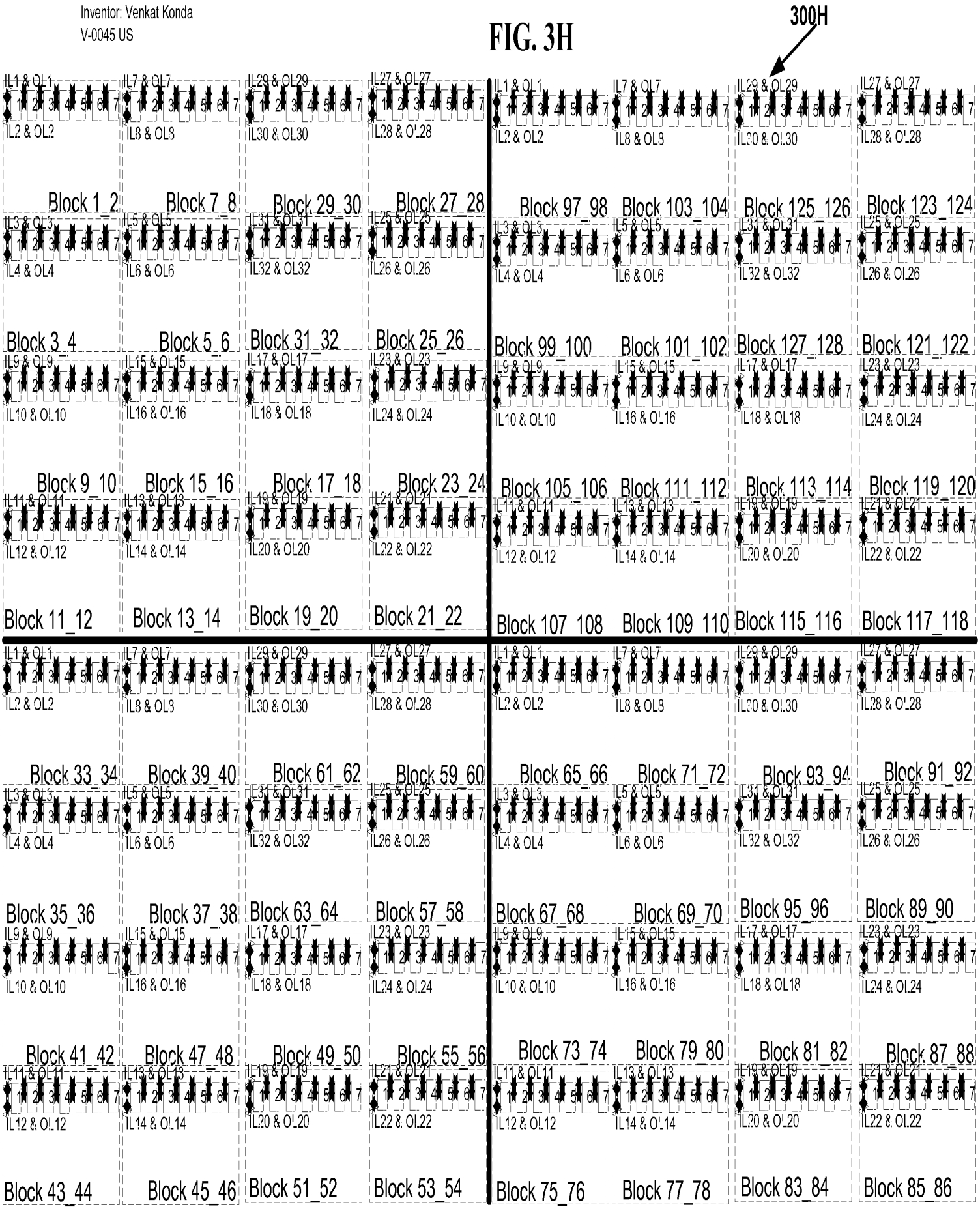

IL1 & OL1
IL2 & OL2
IL7 & OL7
IL8 & OL8
IL29 & OL29
IL30 & OL30
IL27 & OL27
IL28 & OL28
ML(4,4) & ML(5,60)
ML(4,60) & ML(5,4)
ML(4,16) & ML(5,56)
ML(4,56) & ML(5,16)
Block 1_2
Block 7_8
Block 29_30
Block 27_28
IL3 & OL3
IL4 & OL4
IL5 & OL5
IL6 & OL6
IL31 & OL31
IL32 & OL32
IL25 & OL25
IL26 & OL26
ML(4,8) & ML(5,64)
ML(4,64) & ML(5,8)
ML(4,12) & ML(5,52)
ML(4,52) & ML(5,12)
Block 3_4
Block 5_6
Block 31_32
Block 25_26
IL9 & OL9
IL10 & OL10
IL15 & OL15
IL16 & OL16
IL17 & OL17
IL18 & OL18
IL23 & OL23
IL24 & OL24
ML(4,20) & ML(5,36)
ML(4,36) & ML(5,20)
ML(4,32) & ML(5,48)
ML(4,48) & ML(5,32)
Block 9_10
Block 15_16
Block 17_18
Block 23_24
IL11 & OL11
IL12 & OL12
IL13 & OL13
IL14 & OL14
IL19 & OL19
IL20 & OL20
IL21 & OL21
IL22 & OL2
ML(4,24) & ML(5,40)
ML(4,40) & ML(5,24)
ML(4,28) & ML(5,44)
ML(4,44) & ML(5,28)
Block 11_12
Block 13_14
Block 19_20
Block 21_22

FIG. 3H


300H
Block 1_2
Block 7_8
Block 29_30
Block 27_28
Block 97_98
Block 103_104
Block 125_126
Block 123_124
Block 3_4
Block 5_6
Block 31_32
Block 25_26
Block 99_100
Block 101_102
Block 127_128
Block 121_122
Block 9_10
Block 15_16
Block 17_18
Block 23_24
Block 105_106
Block 111_112
Block 113_114
Block 119_120
Block 11_12
Block 13_14
Block 19_20
Block 21_22
Block 107_108
Block 109_110
Block 115_116
Block 117_118
Block 33_34
Block 39_40
Block 61_62
Block 59_60
Block 65_66
Block 71_72
Block 93_94
Block 91_92
Block 35_36
Block 37_38
Block 63_64
Block 57_58
Block 67_68
Block 69_70
Block 95_96
Block 89_90
Block 41_42
Block 47_48
Block 49_50
Block 55_56
Block 73_74
Block 79_80
Block 81_82
Block 87_88
Block 43_44
Block 45_46
Block 51_52
Block 53_54
Block 75_76
Block 77_78
Block 83_84
Block 85_86

400A

FIG. 4A


ML(1,1) & ML(8,1) ML(2,1) & ML(7,1) ML(4,1) & ML(5,1)
IL1 & OL1
ML(3,1) & ML(6,1)
1 2 3 4 5
IL2 & OL2
IS1 & OS1 MS(1,1) & MS(7,1)
MS(2,1) & MS(8,1)
MS(3,1) & MS(6,1)
MS(4,1) & MS(5,1)
Block 1_2
ML(1,16) & ML(8,16) ML(2,16) & ML(7,16) ML(4,16) & ML(5,16)
IL31 & OL31
ML(3,16) & ML(6,16)
1 2 3 4 5
IL32 & OL32
IS16 & OS16 MS(1,16) & MS(7,16)
MS(2,16) & MS(8,16)
MS(3,16) & MS(6,16)
MS(4,16) & MS(5,16)
Block 31_32
ML(1,13) & ML(8,13) ML(2,13) & ML(7,13) ML(4,13) & ML(5,13)
IL25 & OL25
ML(3,13) & ML(6,13)
1 2 3 4 5
IL26 & OL26
IS13 & OS13 MS(1,13) & MS(7,13)
MS(2,13) & MS(8,13)
MS(3,13) & MS(6,13)
MS(4,13) & MS(5,13)
Block 25_26
ML(1,12) & ML(8,12) ML(2,12) & ML(7,12) ML(4,12) & ML(5,12)
IL23 & OL23
ML(3,12) & ML(6,12)
1 2 3 4 5
IL24 & OL24
IS12 & OS12 MS(1,12) & MS(7,12)
MS(2,12) & MS(8,12)
MS(3,12) & MS(6,12)
MS(4,12) & MS(5,12)
Block 23_24
ML(1,2) & ML(8,2) ML(2,2) & ML(7,2) ML(4,2) & ML(5,2)
IL3 & OL3
ML(3,2) & ML(6,2)
1 2 3 4 5
IL4 & OL4
IS1 & OS1 MS(1,2) & MS(7,2)
MS(2,2) & MS(8,2)
MS(3,2) & MS(6,2)
MS(4,2) & MS(5,2)
Block 3_4
ML(1,15) & ML(8,15) ML(2,15) & ML(7,15) ML(4,15) & ML(5,15)
IL29 & OL29
ML(3,15) & ML(6,15)
1 2 3 4 5
IL30 & OL30
IS15 & OS15 MS(1,15) & MS(7,15)
MS(2,15) & MS(8,15)
MS(3,15) & MS(6,15)
MS(4,15) & MS(5,15)
Block 29_30
ML(1,14) & ML(8,14) ML(2,14) & ML(7,14) ML(4,14) & ML(5,14)
IL27 & OL27
ML(3,14) & ML(6,14)
1 2 3 4 5
IL28 & OL28
IS14 & OS14 MS(1,14) & MS(7,14)
MS(2,14) & MS(8,14)
MS(3,14) & MS(6,14)
MS(4,14) & MS(5,14)
Block 27_28
ML(1,11) & ML(8,11) ML(2,11) & ML(7,11) ML(4,11) & ML(5,11)
IL21 & OL21
ML(3,11) & ML(6,11)
1 2 3 4 5
IL22 & OL22
IS11 & OS11 MS(1,11) & MS(7,11)
MS(2,11) & MS(8,11)
MS(3,11) & MS(6,11)
MS(4,11) & MS(5,11)
Block 21_22
ML(1,3) & ML(8,3) ML(2,3) & ML(7,3) ML(4,3) & ML(5,3)
IL5 & OL5
ML(3,3) & ML(6,3)
1 2 3 4 5
IL6 & OL6
IS1 & OS1 MS(1,3) & MS(7,3)
MS(2,3) & MS(8,3)
MS(3,3) & MS(6,3)
MS(4,3) & MS(5,3)
Block 5_6
ML(1,6) & ML(8,6) ML(2,6) & ML(7,6) ML(4,6) & ML(5,6)
IL11 & OL11
ML(3,6) & ML(6,6)
1 2 3 4 5
IL12 & OL12
IS6 & OS6 MS(1,6) & MS(7,6)
MS(2,6) & MS(8,6)
MS(3,6) & MS(6,6)
MS(4,6) & MS(5,6)
Block 11_12
ML(1,7) & ML(8,7) ML(2,7) & ML(7,7) ML(4,7) & ML(5,7)
IL13 & OL13
ML(3,7) & ML(6,7)
1 2 3 4 5
IL14 & OL14
IS7 & OS7 MS(1,7) & MS(7,7)
MS(2,7) & MS(8,7)
MS(3,7) & MS(6,7)
MS(4,7) & MS(5,7)
Block 13_14
ML(1,10) & ML(8,10) ML(2,10) & ML(7,10) ML(4,10) & ML(5,10)
IL19 & OL19
ML(3,10) & ML(6,10)
1 2 3 4 5
IL20 & OL20
IS10 & OS10 MS(1,10) & MS(7,10)
MS(2,10) & MS(8,10)
MS(3,10) & MS(6,10)
MS(4,10) & MS(5,10)
Block 19_20
ML(1,4) & ML(8,4) ML(2,4) & ML(7,4) ML(4,4) & ML(5,4)
IL7 & OL7
ML(3,4) & ML(6,4)
1 2 3 4 5
IL8 & OL8
IS1 & OS1 MS(1,4) & MS(7,4)
MS(2,4) & MS(8,4)
MS(3,4) & MS(6,4)
MS(4,4) & MS(5,4)
Block 7_8
ML(1,5) & ML(8,5) ML(2,5) & ML(7,5) ML(4,5) & ML(5,5)
IL9 & OL10
ML(3,5) & ML(6,5)
1 2 3 4 5
IL9 & OL10
IS5 & OS5 MS(1,5) & MS(7,5)
MS(2,5) & MS(8,5)
MS(3,5) & MS(6,5)
MS(4,5) & MS(5,5)
Block 9_10
ML(1,8) & ML(8,8) ML(2,8) & ML(7,8) ML(4,8) & ML(5,8)
IL15 & OL15
ML(3,8) & ML(6,8)
1 2 3 4 5
IL16 & OL16
IS8 & OS8 MS(1,8) & MS(7,8)
MS(2,8) & MS(8,8)
MS(3,8) & MS(6,8)
MS(4,8) & MS(5,8)
Block 15_16
ML(1,9) & ML(8,9) ML(2,9) & ML(7,9) ML(4,9) & ML(5,9)
IL17 & OL17
ML(3,9) & ML(6,9)
1 2 3 4 5
IL18 & OL18
IS9 & OS9 MS(1,9) & MS(7,9)
MS(2,9) & MS(8,9)
MS(3,9) & MS(6,9)
MS(4,9) & MS(5,9)
Block 17_18

FIG. 4B

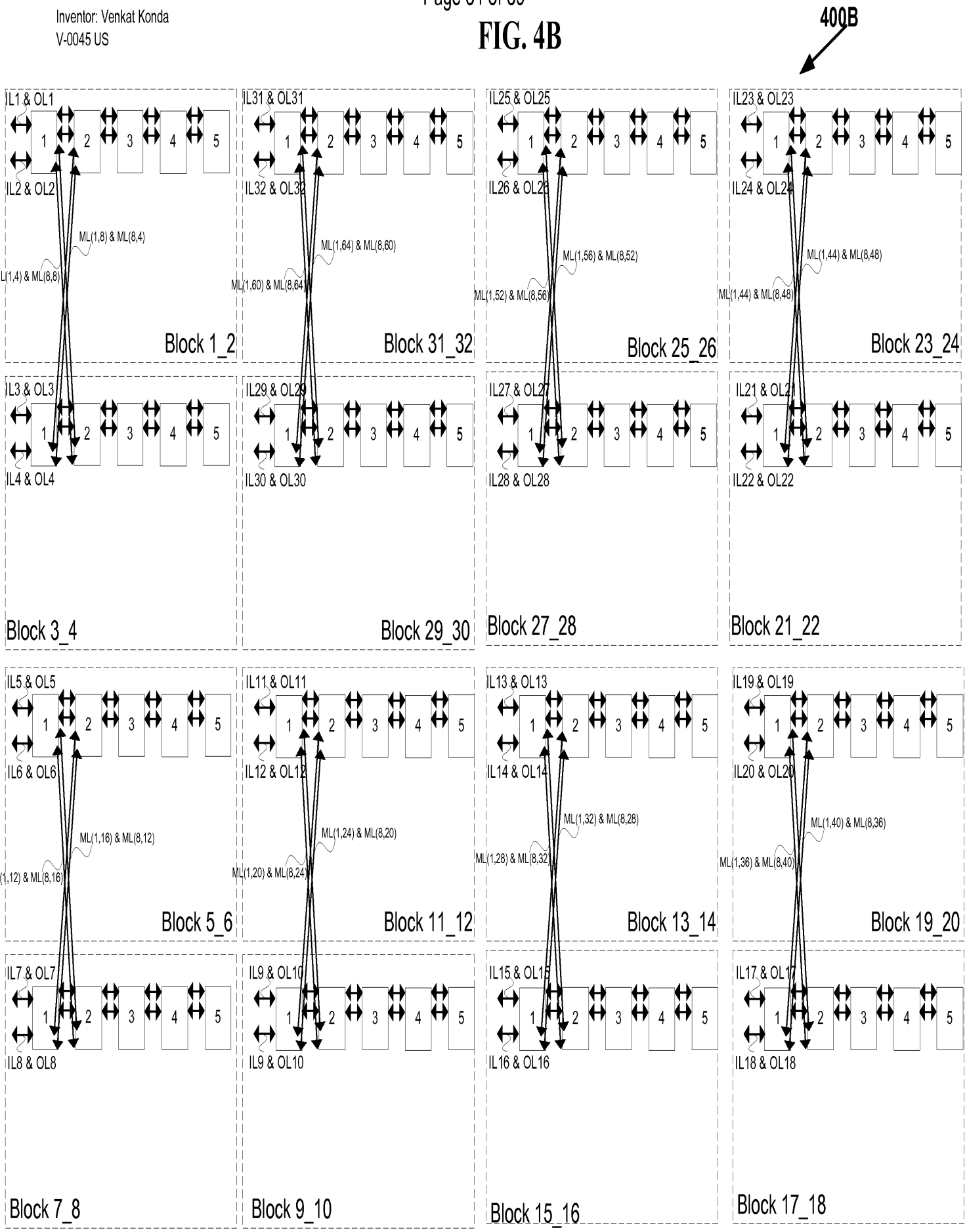

400B
IL1 & OL1
IL2 & OL2
ML(1,8) & ML(8,4)
ML(1,4) & ML(8,8)
Block 1_2
IL31 & OL31
IL32 & OL32
ML(1,64) & ML(8,60)
ML(1,60) & ML(8,64)
Block 31_32
IL25 & OL25
IL26 & OL26
ML(1,56) & ML(8,52)
ML(1,52) & ML(8,56)
Block 25_26
IL23 & OL23
IL24 & OL24
ML(1,44) & ML(8,48)
ML(1,44) & ML(8,48)
Block 23_24
IL3 & OL3
IL4 & OL4
Block 3_4
IL29 & OL29
IL30 & OL30
Block 29_30
IL27 & OL27
IL28 & OL28
Block 27_28
IL21 & OL21
IL22 & OL22
Block 21_22
IL5 & OL5
IL6 & OL6
ML(1,16) & ML(8,12)
ML(1,12) & ML(8,16)
Block 5_6
IL11 & OL11
IL12 & OL12
ML(1,24) & ML(8,20)
ML(1,20) & ML(8,24)
Block 11_12
IL13 & OL13
IL14 & OL14
ML(1,32) & ML(8,28)
ML(1,28) & ML(8,32)
Block 13_14
IL19 & OL19
IL20 & OL20
ML(1,40) & ML(8,36)
ML(1,36) & ML(8,40)
Block 19_20
IL7 & OL7
IL8 & OL8
Block 7_8
IL9 & OL10
IL9 & OL10
Block 9_10
IL15 & OL15
IL16 & OL16
Block 15_16
IL17 & OL17
IL18 & OL18
Block 17_18

FIG. 4C

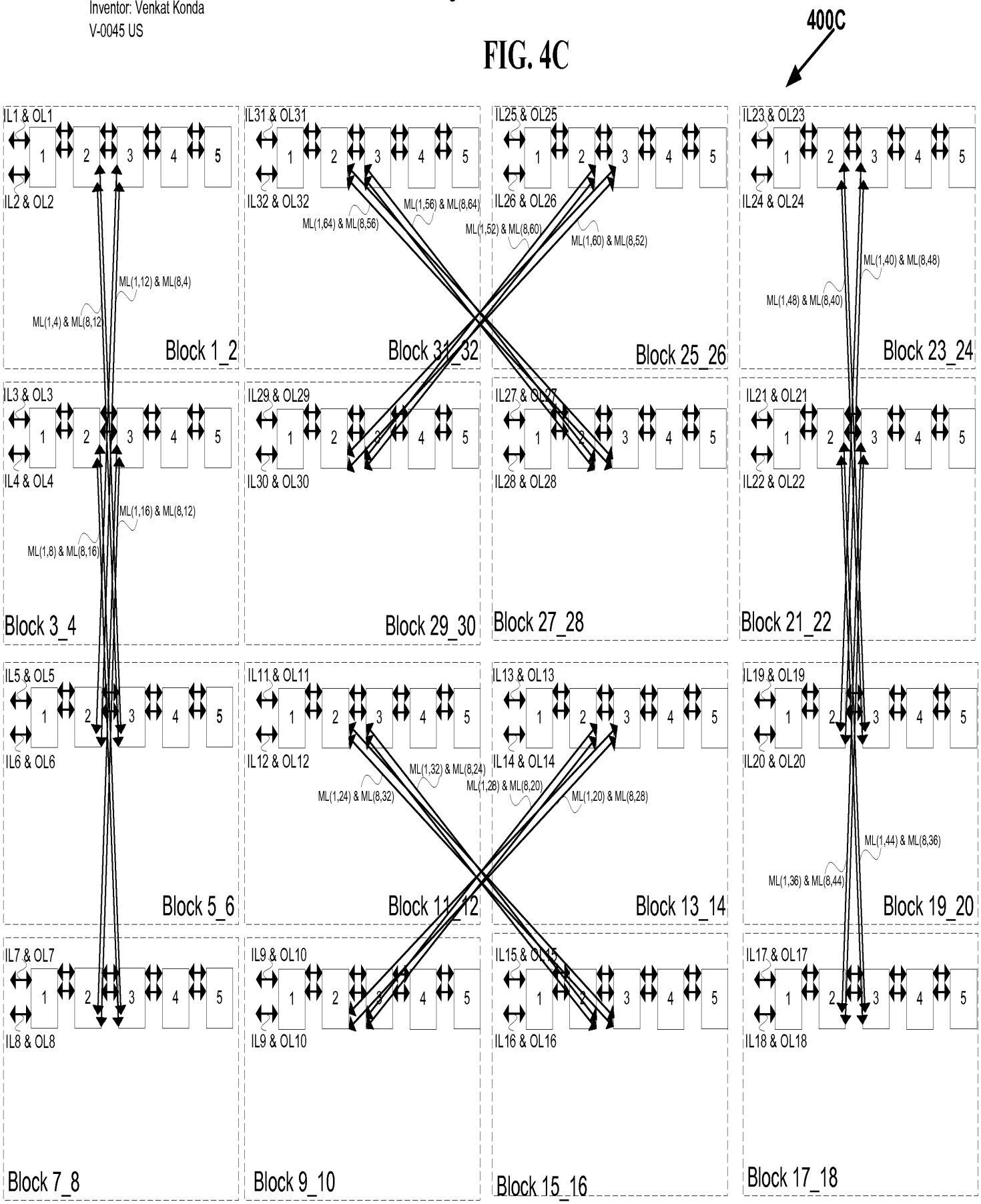
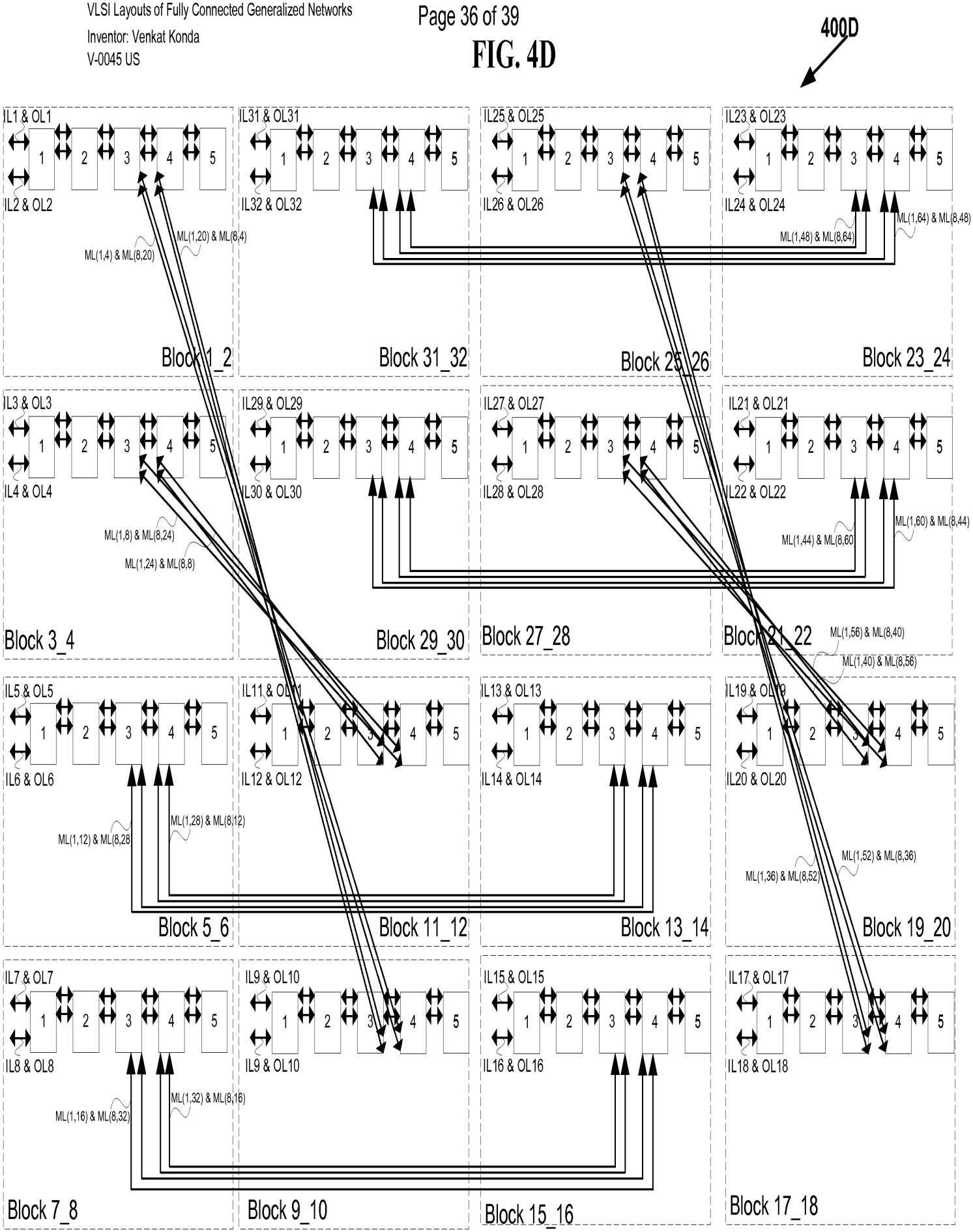
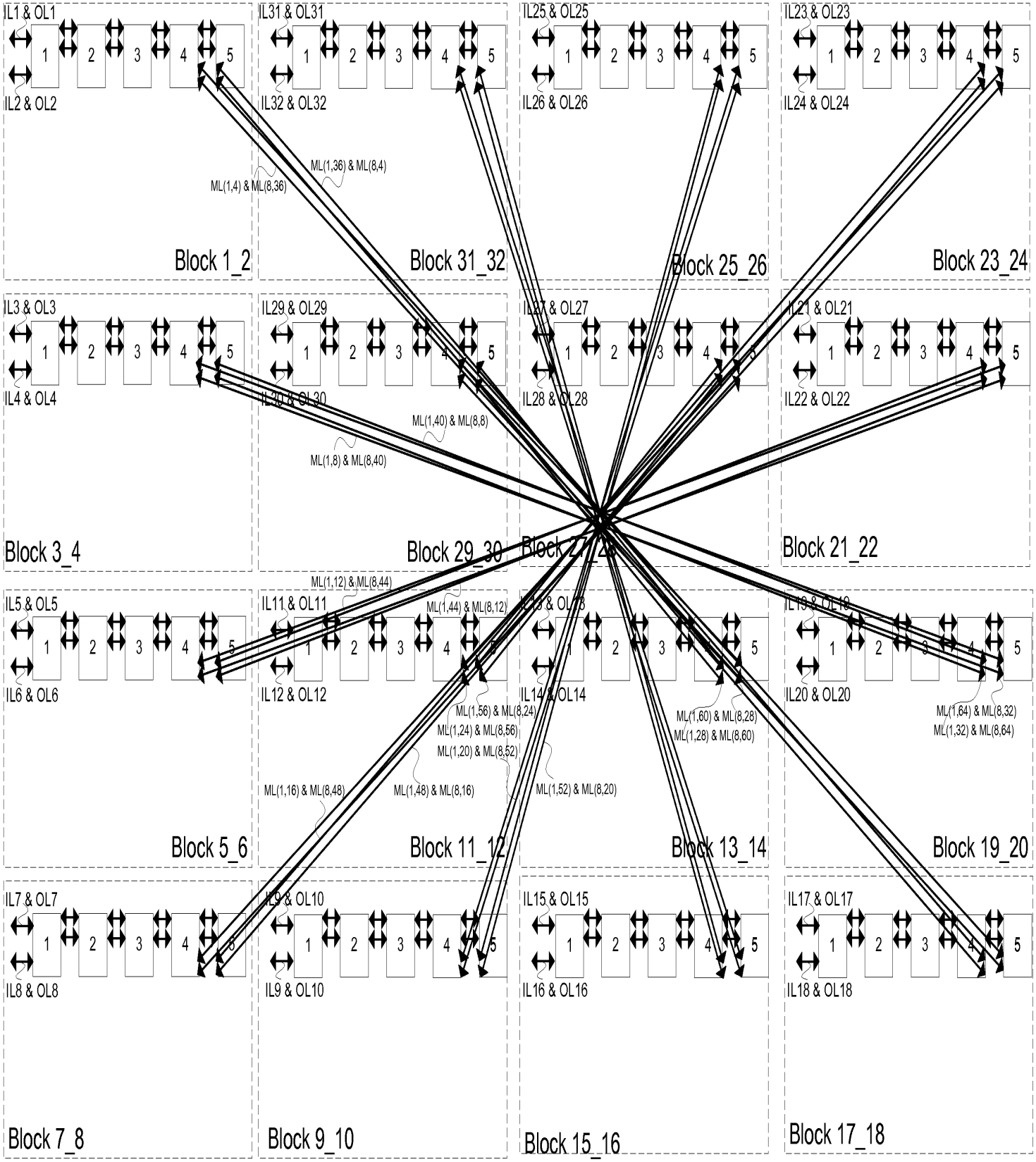

400C
IL1 & OL1
IL2 & OL2
ML(1,12) & ML(8,4)
ML(1,4) & ML(8,12)
Block 1_2
IL31 & OL31
IL32 & OL32
ML(1,56) & ML(8,64)
ML(1,64) & ML(8,56)
Block 31_32
IL25 & OL25
IL26 & OL26
ML(1,52) & ML(8,60)
ML(1,60) & ML(8,52)
Block 25_26
IL23 & OL23
IL24 & OL24
ML(1,40) & ML(8,48)
ML(1,48) & ML(8,40)
Block 23_24
IL3 & OL3
IL4 & OL4
ML(1,16) & ML(8,12)
ML(1,8) & ML(8,16)
Block 3_4
IL29 & OL29
IL30 & OL30
Block 29_30
IL27 & OL27
IL28 & OL28
Block 27_28
IL21 & OL21
IL22 & OL22
Block 21_22
IL5 & OL5
IL6 & OL6
Block 5_6
IL11 & OL11
IL12 & OL12
ML(1,32) & ML(8,24)
ML(1,28) & ML(8,20)
ML(1,24) & ML(8,32)
Block 11_12
IL13 & OL13
IL14 & OL14
ML(1,20) & ML(8,28)
Block 13_14
IL19 & OL19
IL20 & OL20
ML(1,44) & ML(8,36)
ML(1,36) & ML(8,44)
Block 19_20
IL7 & OL7
IL8 & OL8
Block 7_8
IL9 & OL10
IL9 & OL10
Block 9_10
IL15 & OL15
IL16 & OL16
Block 15_16
IL17 & OL17
IL18 & OL18
Block 17_18

FIG. 4D


400D
IL1 & OL1
IL2 & OL2
IL31 & OL31
IL32 & OL32
IL25 & OL25
IL26 & OL26
IL23 & OL23
IL24 & OL24
ML(1,4) & ML(8,20)
ML(1,20) & ML(8,4)
ML(1,48) & ML(8,64)
ML(1,64) & ML(8,48)
Block 1_2
Block 31_32
Block 25_26
Block 23_24
IL3 & OL3
IL4 & OL4
IL29 & OL29
IL30 & OL30
IL27 & OL27
IL28 & OL28
IL21 & OL21
IL22 & OL22
ML(1,8) & ML(8,24)
ML(1,24) & ML(8,8)
ML(1,44) & ML(8,60)
ML(1,60) & ML(8,44)
Block 3_4
Block 29_30
Block 27_28
Block 21_22
ML(1,56) & ML(8,40)
ML(1,40) & ML(8,56)
IL5 & OL5
IL6 & OL6
IL11 & OL11
IL12 & OL12
IL13 & OL13
IL14 & OL14
IL19 & OL19
IL20 & OL20
ML(1,12) & ML(8,28)
ML(1,28) & ML(8,12)
ML(1,36) & ML(8,52)
ML(1,52) & ML(8,36)
Block 5_6
Block 11_12
Block 13_14
Block 19_20
IL7 & OL7
IL8 & OL8
IL9 & OL10
IL9 & OL10
IL15 & OL15
IL16 & OL16
IL17 & OL17
IL18 & OL18
ML(1,16) & ML(8,32)
ML(1,32) & ML(8,16)
Block 7_8
Block 9_10
Block 15_16
Block 17_18

400E

FIG. 4E


IL1 & OL1
IL2 & OL2
IL31 & OL31
IL32 & OL32
IL25 & OL25
IL26 & OL26
IL23 & OL23
IL24 & OL24
ML(1,36) & ML(8,4)
ML(1,4) & ML(8,36)
Block 1_2
Block 31_32
Block 25_26
Block 23_24
IL3 & OL3
IL4 & OL4
IL29 & OL29
IL30 & OL30
IL27 & OL27
IL28 & OL28
IL21 & OL21
IL22 & OL22
ML(1,40) & ML(8,8)
ML(1,8) & ML(8,40)
Block 3_4
Block 29_30
Block 27_28
Block 21_22
ML(1,12) & ML(8,44)
ML(1,44) & ML(8,12)
IL5 & OL5
IL6 & OL6
IL11 & OL11
IL12 & OL12
IL13 & OL13
IL14 & OL14
IL19 & OL19
IL20 & OL20
ML(1,56) & ML(8,24)
ML(1,24) & ML(8,56)
ML(1,20) & ML(8,52)
ML(1,60) & ML(8,28)
ML(1,28) & ML(8,60)
ML(1,64) & ML(8,32)
ML(1,32) & ML(8,64)
ML(1,16) & ML(8,48)
ML(1,48) & ML(8,16)
ML(1,52) & ML(8,20)
Block 5_6
Block 11_12
Block 13_14
Block 19_20
IL7 & OL7
IL8 & OL8
IL9 & OL10
IL15 & OL15
IL16 & OL16
IL17 & OL17
IL18 & OL18
Block 7_8
Block 9_10
Block 15_16
Block 17_18

400C1

FIG. 4C1

FIG. 5A

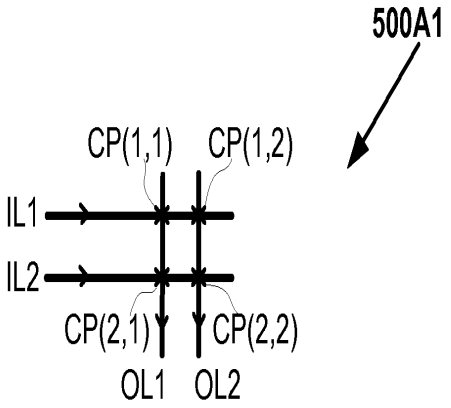


FIG. 5A1
(Prior Art)

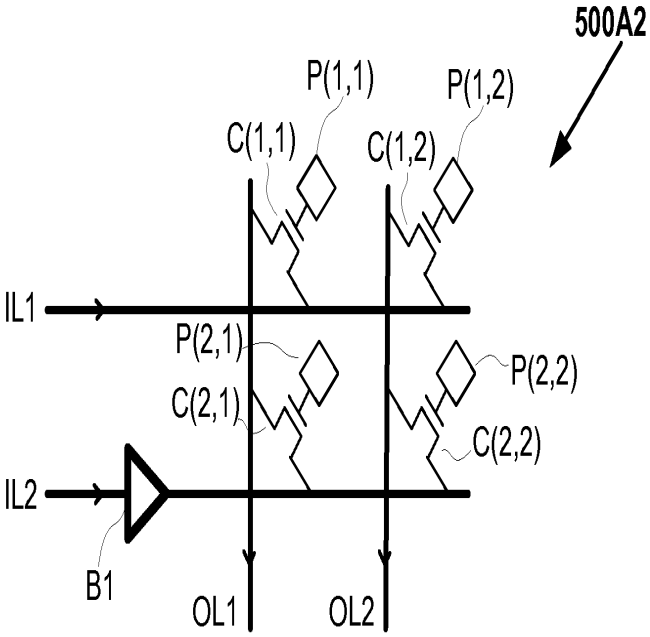


FIG. 5A2
(Prior Art)

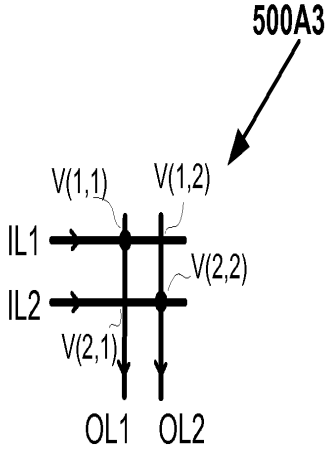


FIG. 5A3
(Prior Art)

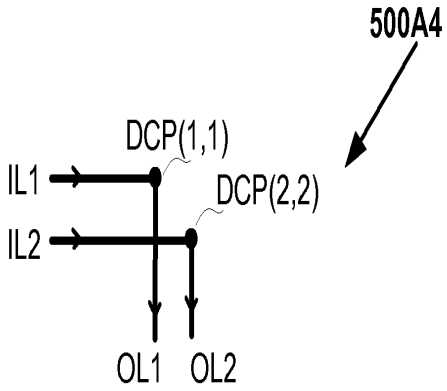


FIG. 5A4

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(71) Applicant and
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(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

(54) **Title:** VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS

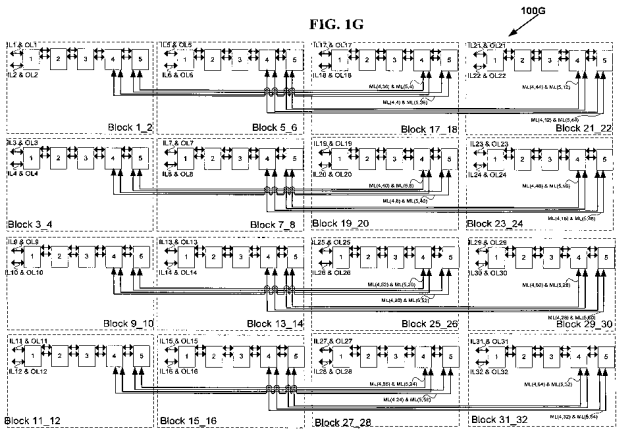

FIG. 1G

(57) **Abstract:** In accordance with the invention, VLSI layouts of generalized multi-stage networks for broadcast, unicast and multicast connections are presented using only horizontal and vertical links. The VLSI layouts employ shuffle exchange links where outlet links of cross links from switches in a stage in one sub-integrated circuit block are connected to inlet links of switches in the succeeding stage in another sub- integrated circuit block so that said cross links are either vertical links or horizontal and vice versa. In one embodiment the sub- integrated circuit blocks are arranged in a hypercube arrangement in a two-dimensional plane. The VLSI layouts exploit the benefits of significantly lower cross points, lower signal latency, lower power and full connectivity with significantly fast compilation.

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VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS

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CROSS REFERENCE TO RELATED APPLICATIONS

This application is Continuation In Part PCT Application to and incorporates by reference in its entirety the U.S. Provisional Patent Application Serial No. 60/940, 394 entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

This application is related to and incorporates by reference in its entirety the PCT Application Serial No. PCT/US08/56064 entitled "FULLY CONNECTED GENERALIZED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed March 6, 2008, the U.S. Provisional Patent Application Serial No. 60/905,526 entitled "LARGE SCALE CROSSPOINT REDUCTION WITH NONBLOCKING UNICAST & MULTICAST IN ARBITRARILY LARGE MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed March 6, 2007, and the U.S. Provisional Patent Application Serial No. 60/940, 383 entitled "FULLY CONNECTED GENERALIZED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

This application is related to and incorporates by reference in its entirety the PCT Application Docket No. S-0038PCT entitled "FULLY CONNECTED GENERALIZED BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed concurrently, the U.S. Provisional Patent Application Serial No. 60/940, 387 entitled "FULLY CONNECTED GENERALIZED BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same

assignee as the current application, filed May 25, 2007, and the U.S. Provisional Patent Application Serial No. 60/940, 390 entitled "FULLY CONNECTED GENERALIZED MULTI-LINK BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007

This application is related to and incorporates by reference in its entirety the PCT Application Docket No. S-0039PCT entitled "FULLY CONNECTED GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed concurrently, the U.S. Provisional Patent Application Serial No. 60/940, 389 entitled "FULLY CONNECTED GENERALIZED REARRANGEABLY NONBLOCKING MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007, the U.S. Provisional Patent Application Serial No. 60/940, 391 entitled "FULLY CONNECTED GENERALIZED FOLDED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007 and the U.S. Provisional Patent Application Serial No. 60/940, 392 entitled "FULLY CONNECTED GENERALIZED STRICTLY NONBLOCKING MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

This application is related to and incorporates by reference in its entirety the U.S. Provisional Patent Application Serial No. 60/984, 724 entitled "VLSI LAYOUTS OF FULLY CONNECTED NETWORKS WITH LOCALITY EXPLOITATION" by Venkat Konda assigned to the same assignee as the current application, filed November 2, 2007.

This application is related to and incorporates by reference in its entirety the U.S. Provisional Patent Application Serial No. 61/018, 494 entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED AND PYRAMID NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed January 1, 2008.

BACKGROUND OF INVENTION

Multi-stage interconnection networks such as Benes networks and butterfly fat tree networks are widely useful in telecommunications, parallel and distributed computing. However VLSI layouts, known in the prior art, of these interconnection networks in an integrated circuit are inefficient and complicated.

Other multi-stage interconnection networks including butterfly fat tree networks, Banyan networks, Batcher-Banyan networks, Baseline networks, Delta networks, Omega networks and Flip networks have been widely studied particularly for self routing packet switching applications. Also Benes Networks with radix of two have been widely studied and it is known that Benes Networks of radix two are shown to be built with back to back baseline networks which are rearrangeably nonblocking for unicast connections.

The most commonly used VLSI layout in an integrated circuit is based on a two-dimensional grid model comprising only horizontal and vertical tracks. An intuitive interconnection network that utilizes two-dimensional grid model is 2D Mesh Network and its variations such as segmented mesh networks. Hence routing networks used in VLSI layouts are typically 2D mesh networks and its variations. However Mesh Networks require large scale cross points typically with a growth rate of $O(N^2)$ where N is the number of computing elements, ports, or logic elements depending on the application.

Multi-stage interconnection with a growth rate of $O(N \times \log N)$ requires significantly small number of cross points. U.S. Patent 6,185,220 entitled "Grid Layouts of Switching and Sorting Networks" granted to Muthukrishnan et al. describes a VLSI layout using existing VLSI grid model for Benes and Butterfly networks. U.S. Patent 6,940,308 entitled "Interconnection Network for a Field Programmable Gate Array" granted to Wong describes a VLSI layout where switches belonging to lower stage of Benes Network are layed out close to the logic cells and switches belonging to higher stages are layed out towards the center of the layout.

Due to the inefficient and in some cases impractical VLSI layout of Benes and butterfly fat tree networks on a semiconductor chip, today mesh networks and segmented mesh networks are widely used in the practical applications such as field programmable gate arrays (FPGAs), programmable logic devices (PLDs), and parallel computing interconnects. The prior art VLSI layouts of Benes and butterfly fat tree networks and VLSI layouts of mesh networks and segmented mesh networks require large area to implement the switches on the chip, large number of wires, longer wires, with increased power consumption, increased latency of the signals which effect the maximum clock speed of operation. Some networks may not even be implemented practically on a chip due to the lack of efficient layouts.

SUMMARY OF INVENTION

When large scale sub-integrated circuit blocks with inlet and outlet links are layed out in an integrated circuit device in a two-dimensional grid arrangement, (for example in an FPGA where the sub-integrated circuit blocks are Lookup Tables) the most intuitive routing network is a network that uses horizontal and vertical links only (the most often used such a network is one of the variations of a 2D Mesh network). A direct embedding of a generalized multi-stage network on to a 2D Mesh network is neither simple nor efficient.

In accordance with the invention, VLSI layouts of generalized multi-stage networks for broadcast, unicast and multicast connections are presented using only horizontal and vertical links. The VLSI layouts employ shuffle exchange links where outlet links of cross links from switches in a stage in one sub-integrated circuit block are connected to inlet links of switches in the succeeding stage in another sub-integrated circuit block so that said cross links are either vertical links or horizontal and vice versa. In one embodiment the sub-integrated circuit blocks are arranged in a hypercube arrangement in a two-dimensional plane. The VLSI layouts exploit the benefits of significantly lower cross points, lower signal latency, lower power and full connectivity with significantly fast compilation.

The VLSI layouts presented are applicable to generalized multi-stage networks $V(N_1, N_2, d, s)$, generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$, generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$, generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$, and generalized hypercube networks $V_{hcube}(N_1, N_2, d, s)$ for s = 1,2,3 or any number in general. The embodiments of VLSI layouts are useful in wide target applications such as FPGAs, CPLDs, pSoCs, ASIC placement and route tools, networking applications, parallel & distributed computing, and reconfigurable computing.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1A is a diagram 100A of an exemplary symmetrical multi-link multi-stage network $V_{fold-mlink}(N, d, s)$ having inverse Benes connection topology of nine stages with N = 32, d = 2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1B is a diagram 100B of the equivalent symmetrical folded multi-link multi-stage network $V_{fold-mlink}(N, d, s)$ of the network 100A shown in FIG. 1A, having inverse Benes connection topology of five stages with N = 32, d = 2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1C is a diagram 100C layout of the network $V_{fold-mlink}(N, d, s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 1D is a diagram 100D layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links ML(1,i) for i = [1, 64] and ML(8,i) for i = [1,64].

FIG. 1E is a diagram 100E layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links ML(2,i) for i = [1, 64] and ML(7,i) for i = [1,64].

FIG. 1F is a diagram 100F layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links ML(3,i) for i = [1, 64] and ML(6,i) for i = [1,64].

FIG. 1G is a diagram 100G layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links ML(4,i) for i = [1, 64] and ML(5,i) for i = [1,64].

FIG. 1H is a diagram 100H layout of a network $V_{fold-mlink}(N,d,s)$ where N = 128, d = 2, and s = 2, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 1I is a diagram 100I detailed connections of BLOCK 1_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing $V(N,d,s)$ or $V_{fold}(N,d,s)$.

FIG. 1J is a diagram 100J detailed connections of BLOCK 1_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing $V(N,d,s)$ or $V_{fold}(N,d,s)$.

FIG. 1K is a diagram 100K detailed connections of BLOCK 1_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing $V(N,d,s)$ or $V_{fold}(N,d,s)$.

FIG. 1K1 is a diagram 100M1 detailed connections of BLOCK 1_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing $V(N,d,s)$ or $V_{fold}(N,d,s)$ for s = 1.

FIG. 1L is a diagram 100L detailed connections of BLOCK 1_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing $V(N,d,s)$ or $V_{fold}(N,d,s)$.

FIG. 1L1 is a diagram 100L1 detailed connections of BLOCK 1_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing $V(N,d,s)$ or $V_{fold}(N,d,s)$ for s = 1.

FIG. 2A1 is a diagram 200A1 of an exemplary symmetrical multi-link multi-stage network $V_{fold-mlink}(N,d,s)$ having inverse Benes connection topology of one stage with N = 2, d = 2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention. FIG. 2A2 is a diagram 200A2 of the equivalent symmetrical folded multi-link multi-stage network $V_{fold-mlink}(N,d,s)$ of the network 200A1 shown in FIG. 2A1, having inverse Benes connection topology of one stage with N = 2, d = 2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention. FIG. 2A3 is a diagram 200A3 layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 2A2, in one embodiment, illustrating all the connection links.

FIG. 2B1 is a diagram 200B1 of an exemplary symmetrical multi-link multi-stage network $V_{fold-mlink}(N,d,s)$ having inverse Benes connection topology of one stage with N = 4, d = 2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention. FIG. 2B2 is a diagram 200B2 of the equivalent symmetrical folded multi-link multi-stage network $V_{fold-mlink}(N,d,s)$ of the network

200B1 shown in FIG. 2B1, having inverse Benes connection topology of one stage with N = 4, d = 2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention. FIG. 2B3 is a diagram 200B3 layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 2B2, in one embodiment, illustrating the connection links belonging with in each block only. FIG. 2B4 is a diagram 200B4 layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 2B2, in one embodiment, illustrating the connection links ML(1,i) for i = [1, 8] and ML(2,i) for i = [1,8].

FIG. 2C11 is a diagram 200C11 of an exemplary symmetrical multi-link multi-stage network $V_{fold-mlink}(N,d,s)$ having inverse Benes connection topology of one stage with N = 8, d = 2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention. FIG. 2C12 is a diagram 200C12 of the equivalent symmetrical folded multi-link multi-stage network $V_{fold-mlink}(N,d,s)$ of the network 200C11 shown in FIG. 2C11, having inverse Benes connection topology of one stage with N = 8, d = 2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 2C21 is a diagram 200C21 layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 2C12, in one embodiment, illustrating the connection links belonging with in each block only. FIG. 2C22 is a diagram 200C22 layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 2C12, in one embodiment, illustrating the connection links ML(1,i) for i = [1, 16] and ML(4,i) for i = [1,16]. FIG. 2C23 is a diagram 200C23 layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 2C12, in one embodiment, illustrating the connection links ML(2,i) for i = [1, 16] and ML(3,i) for i = [1,16].

FIG. 2D1 is a diagram 200D1 of an exemplary symmetrical multi-link multi-stage network $V_{fold-mlink}(N,d,s)$ having inverse Benes connection topology of one stage with N = 16, d = 2 and s=2, strictly nonblocking network for unicast connections and

rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 2D2 is a diagram 200D2 of the equivalent symmetrical folded multi-link multi-stage network $V_{fold-mlink}(N,d,s)$ of the network 200D1 shown in FIG. 2D1, having inverse Benes connection topology of one stage with N = 16, d = 2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 2D3 is a diagram 200D3 layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 2D2, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 2D4 is a diagram 200D4 layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 2D2, in one embodiment, illustrating the connection links ML(1,i) for i = [1, 32] and ML(6,i) for i = [1,32].

FIG. 2D5 is a diagram 200D5 layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 2D2, in one embodiment, illustrating the connection links ML(2,i) for i = [1, 32] and ML(5,i) for i = [1,32].

FIG. 2D6 is a diagram 200D6 layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 2D2, in one embodiment, illustrating the connection links ML(3,i) for i = [1, 32] and ML(4,i) for i = [1,32].

FIG. 3A is a diagram 300A of an exemplary symmetrical multi-link multi-stage network $V_{hcube}(N,d,s)$ having inverse Benes connection topology of nine stages with N = 32, d = 2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 3B is a diagram 300B of the equivalent symmetrical folded multi-link multi-stage network $V_{hcube}(N,d,s)$ of the network 300A shown in FIG. 3A, having inverse

Benes connection topology of five stages with N = 32, d = 2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 3C is a diagram 300C layout of the network $V_{hcube}(N,d,s)$ shown in FIG. 3B, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 3D is a diagram 100D layout of the network $V_{hcube}(N,d,s)$ shown in FIG. 3B, in one embodiment, illustrating the connection links ML(1,i) for i = [1, 64] and ML(8,i) for i = [1,64].

FIG. 3E is a diagram 300E layout of the network $V_{hcube}(N,d,s)$ shown in FIG. 3B, in one embodiment, illustrating the connection links ML(2,i) for i = [1, 64] and ML(7,i) for i = [1,64].

FIG. 3F is a diagram 300F layout of the network $V_{hcube}(N,d,s)$ shown in FIG. 3B, in one embodiment, illustrating the connection links ML(3,i) for i = [1, 64] and ML(6,i) for i = [1,64].

FIG. 3G is a diagram 300G layout of the network $V_{hcube}(N,d,s)$ shown in FIG. 3B, in one embodiment, illustrating the connection links ML(4,i) for i = [1, 64] and ML(5,i) for i = [1,64].

FIG. 3H is a diagram 300H layout of a network $V_{hcube}(N,d,s)$ where N = 128, d = 2, and s = 2, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 4A is a diagram 400A layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 4B is a diagram 400B layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links ML(1,i) for i = [1, 64] and ML(8,i) for i = [1,64].

FIG. 4C is a diagram 400C layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 4C, in one embodiment, illustrating the connection links ML(2,i) for i = [1, 64] and ML(7,i) for i = [1,64].

FIG. 4D is a diagram 400D layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 4D, in one embodiment, illustrating the connection links ML(3,i) for i = [1, 64] and ML(6,i) for i = [1,64].

FIG. 4E is a diagram 400E layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 4E, in one embodiment, illustrating the connection links ML(4,i) for i = [1, 64] and ML(5,i) for i = [1,64].

FIG. 4C1 is a diagram 400C1 layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 5A1 is a diagram 500A1 of an exemplary prior art implementation of a two by two switch; FIG. 5A2 is a diagram 500A2 for programmable integrated circuit prior art implementation of the diagram 500A1 of FIG. 5A1; FIG. 5A3 is a diagram 500A3 for one-time programmable integrated circuit prior art implementation of the diagram 500A1 of FIG. 5A1; FIG. 5A4 is a diagram 500A4 for integrated circuit placement and route implementation of the diagram 500A1 of FIG. 5A1.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is concerned with the VLSI layouts of arbitrarily large switching networks for broadcast, unicast and multicast connections. Particularly switching networks considered in the current invention include: generalized multi-stage

networks $V(N_1, N_2, d, s)$, generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$, generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$, generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$, and generalized hypercube networks $V_{hcube}(N_1, N_2, d, s)$ for s = 1,2,3 or any number in general.

Efficient VLSI layout of networks on a semiconductor chip are very important and greatly influence many important design parameters such as the area taken up by the network on the chip, total number of wires, length of the wires, latency of the signals, capacitance and hence the maximum clock speed of operation. Some networks may not even be implemented practically on a chip due to the lack of efficient layouts. The different varieties of multi-stage networks described above have not been implemented previously on the semiconductor chips efficiently. For example in Field Programmable Gate Array (FPGA) designs, multi-stage networks described in the current invention have not been successfully implemented primarily due to the lack of efficient VLSI layouts. Current commercial FPGA products such as Xilinx Vertex, Altera's Stratix implement island-style architecture using mesh and segmented mesh routing interconnects using either full crossbars or sparse crossbars. These routing interconnects consume large silicon area for crosspoints, long wires, large signal propagation delay and hence consume lot of power.

The current invention discloses the VLSI layouts of numerous types of multi-stage networks which are very efficient. Moreover they can be embedded on to mesh and segmented mesh routing interconnects of current commercial FPGA products. The VLSI layouts disclosed in the current invention are applicable to including the numerous generalized multi-stage networks disclosed in the following patent applications, filed concurrently:

1) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-stage networks $V(N_1, N_2, d, s)$ with numerous connection

topologies and the scheduling methods are described in detail in the PCT Application Serial No. PCT/US08/56064 that is incorporated by reference above.

2) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in U.S. Provisional Patent Application Serial No. 60/940, 387 that is incorporated by reference above.

3) Rearrangeably nonblocking for arbitrary fan-out multicast and unicast, and strictly nonblocking for unicast for generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$ and generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in U.S. Provisional Patent Application Serial No. 60/940, 389 that is incorporated by reference above.

4) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in U.S. Provisional Patent Application Serial No. 60/940, 390 that is incorporated by reference above.

5) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in U.S. Provisional Patent Application Serial No. 60/940, 391 that is incorporated by reference above.

6) Strictly nonblocking for arbitrary fan-out multicast for generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$ and generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling

methods are described in detail in U.S. Provisional Patent Application Serial No. 60/940, 392 that is incorporated by reference above.

7) VLSI layouts of numerous types of multi-stage networks with locality exploitation are described in U.S. Provisional Patent Application Serial No. 60/984, 724 that is incorporated by reference above.

8) VLSI layouts of numerous types of multistage pyramid networks are described in U.S. Provisional Patent Application Serial No. 61/018, 494 that is incorporated by reference above.

In addition the layouts of the current invention are also applicable to generalized multi-stage pyramid networks $V_p(N_1, N_2, d, s)$, generalized folded multi-stage pyramid networks $V_{fold-p}(N_1, N_2, d, s)$, generalized butterfly fat pyramid networks $V_{bfp}(N_1, N_2, d, s)$, generalized multi-link multi-stage pyramid networks $V_{mlink-p}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage pyramid networks $V_{fold-mlink-p}(N_1, N_2, d, s)$, generalized multi-link butterfly fat pyramid networks $V_{mlink-bfp}(N_1, N_2, d, s)$, and generalized hypercube networks $V_{hcube}(N_1, N_2, d, s)$ for s = 1,2,3 or any number in general.

Symmetric RNB generalized multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$:

Referring to diagram 100A in FIG. 1A, in one embodiment, an exemplary generalized multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 2 with nine stages of one hundred and forty four switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, 150, 160, 170, 180 and 190 is shown where input stage 110 consists of sixteen, two by four switches IS1-IS16 and output stage 120 consists of sixteen, four by two switches OS1-OS16. And all the middle stages namely the middle

stage 130 consists of sixteen, four by four switches MS(1,1) - MS(1,16), middle stage 140 consists of sixteen, four by four switches MS(2,1) - MS(2,16), middle stage 150 consists of sixteen, four by four switches MS(3,1) - MS(3,16), middle stage 160 consists of sixteen, four by four switches MS(4,1) - MS(4,16), middle stage 170 consists of sixteen, four by four switches MS(5,1) - MS(5,16), middle stage 180 consists of sixteen, four by four switches MS(6,1) - MS(6,16), and middle stage 190 consists of sixteen, four by four switches MS(7,1) - MS(7,16).

As disclosed in U.S. Provisional Patent Application Serial No. 60/940,389 that is incorporated by reference above, such a network can be operated in rearrangeably non-blocking manner for arbitrary fan-out multicast connections and also can be operated in strictly non-blocking manner for unicast connections.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N}{d}$, where N is the total number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by $\frac{N}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * 2d$ and each output switch OS1-OS4 can be denoted in general with the notation $2d * d$. Likewise, the size of each switch in any of the middle stages can be denoted as $2d * 2d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. A symmetric multi-stage network can be represented with the notation $V_{mlink}(N, d, s)$, where N represents the total number of inlet links of all input switches (for example the links IL1-IL32), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Each of the $\frac{N}{d}$ input switches IS1 – IS16 are connected to exactly d switches in middle stage 130 through two links each for a total of $2 \times d$ links (for example input

switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2), and also connected to middle switch MS(1,2) through the links ML(1,3) and ML(1,4)). The middle links which connect switches in the same row in two successive middle stages are called hereinafter straight middle links; and the middle links which connect switches in different rows in two successive middle stages are called hereinafter cross middle links. For example, the middle links ML(1,1) and ML(1,2) connect input switch IS1 and middle switch MS(1,1), so middle links ML(1,1) and ML(1,2) are straight middle links; where as the middle links ML(1,3) and ML(1,4) connect input switch IS1 and middle switch MS(1,2), since input switch IS1 and middle switch MS(1,2) belong to two different rows in diagram 100A of FIG. 1A, middle links ML(1,3) and ML(1,4) are cross middle links.

Each of the $\frac{N}{d}$ middle switches MS(1,1) – MS(1,16) in the middle stage 130 are connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(1,1) and ML(1,2) are connected to the middle switch MS(1,1) from input switch IS1, and the links ML(1,7) and ML(1,8) are connected to the middle switch MS(1,1) from input switch IS2) and also are connected to exactly d switches in middle stage 140 through two links each for a total of $2 \times d$ links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1), and the links ML(2,3) and ML(2,4) are connected from middle switch MS(1,1) to middle switch MS(2,3)).

Each of the $\frac{N}{d}$ middle switches MS(2,1) – MS(2,16) in the middle stage 140 are connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(2,1) and ML(2,2) are connected to the middle switch MS(2,1) from input switch MS(1,1), and the links ML(1,11) and ML(1,12) are connected to the middle switch MS(2,1) from input switch MS(1,3)) and also are connected to exactly d switches in middle stage 150 through two links each for a total of $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1), and the links ML(3,3) and ML(3,4) are connected from middle switch MS(2,1) to middle switch MS(3,5)).

Each of the $\frac{N}{d}$ middle switches MS(3,1) – MS(3,16) in the middle stage 150 are connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected to the middle switch MS(3,1) from input switch MS(2,1), and the links ML(2,19) and ML(2,20) are connected to the middle switch MS(3,1) from input switch MS(2,5)) and also are connected to exactly d switches in middle stage 160 through two links each for a total of $2 \times d$ links (for example the links ML(4,1) and ML(4,2) are connected from middle switch MS(3,1) to middle switch MS(4,1), and the links ML(4,3) and ML(4,4) are connected from middle switch MS(3,1) to middle switch MS(4,9)).

Each of the $\frac{N}{d}$ middle switches MS(4,1) – MS(4,16) in the middle stage 160 are connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(4,1) and ML(4,2) are connected to the middle switch MS(4,1) from input switch MS(3,1), and the links ML(4,35) and ML(4,36) are connected to the middle switch MS(4,1) from input switch MS(3,9)) and also are connected to exactly d switches in middle stage 170 through two links each for a total of $2 \times d$ links (for example the links ML(5,1) and ML(5,2) are connected from middle switch MS(4,1) to middle switch MS(5,1), and the links ML(5,3) and ML(5,4) are connected from middle switch MS(4,1) to middle switch MS(5,9)).

Each of the $\frac{N}{d}$ middle switches MS(5,1) – MS(5,16) in the middle stage 170 are connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(5,1) and ML(5,2) are connected to the middle switch MS(5,1) from input switch MS(4,1), and the links ML(5,35) and ML(5,36) are connected to the middle switch MS(5,1) from input switch MS(4,9)) and also are connected to exactly d switches in middle stage 180 through two links each for a total of $2 \times d$ links (for example the links ML(6,1) and ML(6,2) are connected from middle switch MS(5,1) to middle switch MS(6,1), and the links ML(6,3) and ML(6,4) are connected from middle switch MS(5,1) to middle switch MS(6,5)).

Each of the $\frac{N}{d}$ middle switches MS(6,1) – MS(6,16) in the middle stage 180 are connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(6,1) and ML(6,2) are connected to the middle switch MS(6,1) from input switch MS(5,1), and the links ML(6,19) and ML(6,20) are connected to the middle switch MS(6,1) from input switch MS(5,5)) and also are connected to exactly d switches in middle stage 190 through two links each for a total of $2 \times d$ links (for example the links ML(7,1) and ML(7,2) are connected from middle switch MS(6,1) to middle switch MS(7,1), and the links ML(7,3) and ML(7,4) are connected from middle switch MS(6,1) to middle switch MS(7,3)).

Each of the $\frac{N}{d}$ middle switches MS(7,1) – MS(7,16) in the middle stage 190 are connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(7,1) and ML(7,2) are connected to the middle switch MS(7,1) from input switch MS(6,1), and the links ML(7,11) and ML(7,12) are connected to the middle switch MS(7,1) from input switch MS(6,3)) and also are connected to exactly d switches in middle stage 120 through two links each for a total of $2 \times d$ links (for example the links ML(8,1) and ML(8,2) are connected from middle switch MS(7,1) to middle switch MS(8,1), and the links ML(8,3) and ML(8,4) are connected from middle switch MS(7,1) to middle switch OS2).

Each of the $\frac{N}{d}$ middle switches OS1 – OS16 in the middle stage 120 are connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(8,1) and ML(8,2) are connected to the output switch OS1 from input switch MS(7,1), and the links ML(8,7) and ML(7,8) are connected to the output switch OS1 from input switch MS(7,2)).

Finally the connection topology of the network 100A shown in FIG. 1A is known to be back to back inverse Benes connection topology.

Referring to diagram 100B in FIG. 1B, is a folded version of the multi-link multi-stage network 100A shown in FIG. 1A. The network 100B in FIG. 1B shows input stage

110 and output stage 120 are placed together. That is input switch IS1 and output switch OS1 are placed together, input switch IS2 and output switch OS2 are placed together, and similarly input switch IS16 and output switch OS16 are placed together. All the right going middle links (hereinafter "forward connecting links") {i.e., inlet links IL1 – IL32 and middle links ML(1,1) - ML(1,64)} correspond to input switches IS1 - IS16, and all the left going middle links (hereinafter "backward connecting links") {i.e., middle links ML(8,1) - ML(8,64) and outlet links OL1-OL32} correspond to output switches OS1 - OS16.

Middle stage 130 and middle stage 190 are placed together. That is middle switches MS(1,1) and MS(7,1) are placed together, middle switches MS(1,2) and MS(7,2) are placed together, and similarly middle switches MS(1,16) and MS(7,16) are placed together. All the right going middle links {i.e., middle links ML(1,1) - ML(1,64) and middle links ML(2,1) – ML(2,64)} correspond to middle switches MS(1,1) – MS(1,16), and all the left going middle links {i.e., middle links ML(7,1) - ML(7,64) and middle links ML(8,1) and ML(8,64)} correspond to middle switches MS(7,1) – MS(7,16).

Middle stage 140 and middle stage 180 are placed together. That is middle switches MS(2,1) and MS(6,1) are placed together, middle switches MS(2,2) and MS(6,2) are placed together, and similarly middle switches MS(2,16) and MS(6,16) are placed together. All the right going middle links {i.e., middle links ML(2,1) - ML(2,64) and middle links ML(3,1) – ML(3,64)} correspond to middle switches MS(2,1) – MS(2,16), and all the left going middle links {i.e., middle links ML(6,1) - ML(6,64) and middle links ML(7,1) and ML(7,64)} correspond to middle switches MS(6,1) – MS(6,16).

Middle stage 150 and middle stage 170 are placed together. That is middle switches MS(3,1) and MS(5,1) are placed together, middle switches MS(3,2) and MS(5,2) are placed together, and similarly middle switches MS(3,16) and MS(5,16) are placed together. All the right going middle links {i.e., middle links ML(3,1) - ML(3,64) and middle links ML(4,1) – ML(4,64)} correspond to middle switches MS(3,1) – MS(3,16), and all the left going middle links {i.e., middle links ML(5,1) - ML(5,64) and

middle links ML(6,1) and ML(6,64)} correspond to middle switches MS(5,1) – MS(5,16).

Middle stage 160 is placed alone. All the right going middle links are the middle links ML(4,1) - ML(4,64) and all the left going middle links are middle links ML(5,1) - ML(5,64).

In one embodiment, in the network 100B of FIG. 1B, the switches that are placed together are implemented as separate switches then the network 100B is the generalized folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with nine stages as disclosed in U.S. Provisional Patent Application Serial No. 60/940,389 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a two by four switch and a four by two switch. For example the switch input switch IS1 and output switch OS1 are placed together; so input switch IS1 is implemented as two by four switch with the inlet links IL1 and IL2 being the inputs of the input switch IS1 and middle links ML(1,1) – ML(1,4) being the outputs of the input switch IS1; and output switch OS1 is implemented as four by two switch with the middle links ML(8,1), ML(8,2), ML(8,7) and ML(8,8) being the inputs of the output switch OS1 and outlet links OL1 – OL2 being the outputs of the output switch OS1. Similarly in this embodiment of network 100B all the switches that are placed together in each middle stage are implemented as separate switches.

Hypercube Topology layout schemes:

Referring to layout 100C of FIG. 1C, in one embodiment, there are sixteen blocks namely Block 1_2, Block 3_4, Block 5_6, Block 7_8, Block 9_10, Block 11_12, Block 13_14, Block 15_16, Block 17_18, Block 19_20, Block 21_22, Block 23_24, Block 25_26, Block 27_28, Block 29_30, and Block 31_32. Each block implements all the switches in one row of the network 100B of FIG. 1B, one of the key aspects of the current invention. For example Block 1_2 implements the input switch IS1, output Switch OS1,

middle switch MS(1,1), middle switch MS(7,1), middle switch MS(2,1), middle switch MS(6,1), middle switch MS(3,1), middle switch MS(5,1), and middle switch MS(4,1). For the simplification of illustration, Input switch IS1 and output switch OS1 together are denoted as switch 1; Middle switch MS(1,1) and middle switch MS(7,1) together are denoted by switch 2; Middle switch MS(2,1) and middle switch MS(6,1) together are denoted by switch 3; Middle switch MS(3,1) and middle switch MS(5,1) together are denoted by switch 4; Middle switch MS(4,1) is denoted by switch 5.

All the straight middle links are illustrated in layout 100C of FIG. 1C. For example in Block 1_2, inlet links IL1 – IL2, outlet links OL1 – OL2, middle link ML(1,1), middle link ML(1,2), middle link ML(8,1), middle link ML(8,2), middle link ML(2,1), middle link ML(2,2), middle link ML(7,1), middle link ML(7,2), middle link ML(3,1), middle link ML(3,2), middle link ML(6,1), middle link ML(6,2), middle link ML(4,1), middle link ML(4,2), middle link ML(5,1) and middle link ML(5,2) are illustrated in layout 100C of FIG. 1C.

Even though it is not illustrated in layout 100C of FIG. 1C, in each block, in addition to the switches there may be Configurable Logic Blocks (CLB) or any arbitrary digital circuit (hereinafter "sub-integrated circuit block") depending on the applications in different embodiments. There are four quadrants in the layout 100C of FIG. 1C namely top-left, bottom-left, top-right and bottom-right quadrants. Top-left quadrant implements Block 1_2, Block 3_4, Block 5_6, and Block 7_8. Bottom-left quadrant implements Block 9_10, Block 11_12, Block 13_14, and Block 15_16. Top-right quadrant implements Block 17_18, Block 19_20, Block 21_22, and Block 23_24. Bottom-right quadrant implements Block 25_26, Block 27_28, Block 29_30, and Block 31_32. There are two halves in layout 100C of FIG. 1C namely left-half and right-half. Left-half consists of top-left and bottom-left quadrants. Right-half consists of top-right and bottom-right quadrants.

Recursively in each quadrant there are four sub-quadrants. For example in top-left quadrant there are four sub-quadrants namely top-left sub-quadrant, bottom-left sub-quadrant, top-right sub-quadrant and bottom-right sub-quadrant. Top-left sub-quadrant of top-left quadrant implements Block 1_2. Bottom-left sub-quadrant of top-left quadrant

implements Block 3_4. Top-right sub-quadrant of top-left quadrant implements Block 5_6. Finally bottom-right sub-quadrant of top-left quadrant implements Block 7_8. Similarly there are two sub-halves in each quadrant. For example in top-left quadrant there are two sub-halves namely left-sub-half and right-sub-half. Left-sub-half of top-left quadrant implements Block 1_2 and Block 3_4. Right-sub-half of top-left quadrant implements Block 5_6 and Block 7_8. Finally applicant notes that in each quadrant or half the blocks are arranged as a general binary hypercube. Recursively in larger multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 > 32$, the layout in this embodiment in accordance with the current invention, will be such that the super-quadrants will also be arranged in d-ary hypercube manner. (In the embodiment of the layout 100C of FIG. 1C, it is binary hypercube manner since d = 2, in the network $V_{fold-mlink}(N_1, N_2, d, s)$ 100B of FIG. 1B).

Layout 100D of FIG. 1D illustrates the inter-block links between switches 1 and 2 of each block. For example middle links ML(1,3), ML(1,4), ML(8,7), and ML(8,8) are connected between switch 1 of Block 1_2 and switch 2 of Block 3_4. Similarly middle links ML(1,7), ML(1,8), ML(8,3), and ML(8,4) are connected between switch 2 of Block 1_2 and switch 1 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 100D of FIG. 1D can be implemented as vertical tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(1,4) and ML(8,8) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(1,4) and ML(8,8) are implemented as a time division multiplexed single track).

Layout 100E of FIG. 1E illustrates the inter-block links between switches 2 and 3 of each block. For example middle links ML(2,3), ML(2,4), ML(7,11), and ML(7,12) are connected between switch 2 of Block 1_2 and switch 3 of Block 3_4. Similarly middle links ML(2,11), ML(2,12), ML(7,3), and ML(7,4) are connected between switch 3 of Block 1_2 and switch 2 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 100E of FIG. 1E can be implemented as horizontal tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for

example middle links ML(2,12) and ML(7,4) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(2,12) and ML(7,4) are implemented as a time division multiplexed single track).

Layout 100F of FIG. 1F illustrates the inter-block links between switches 3 and 4 of each block. For example middle links ML(3,3), ML(3,4), ML(6,19), and ML(6,20) are connected between switch 3 of Block 1_2 and switch 4 of Block 3_4. Similarly middle links ML(3,19), ML(3,20), ML(6,3), and ML(6,4) are connected between switch 4 of Block 1_2 and switch 3 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 100F of FIG. 1F can be implemented as vertical tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(3,4) and ML(6,20) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(3,4) and ML(6,20) are implemented as a time division multiplexed single track).

Layout 100G of FIG. 1G illustrates the inter-block links between switches 4 and 5 of each block. For example middle links ML(4,3), ML(4,4), ML(5,35), and ML(5,36) are connected between switch 4 of Block 1_2 and switch 5 of Block 3_4. Similarly middle links ML(4,35), ML(4,36), ML(5,3), and ML(5,4) are connected between switch 5 of Block 1_2 and switch 4 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 100G of FIG. 1G can be implemented as horizontal tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(4,4) and ML(5,36) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(4,4) and ML(5,36) are implemented as a time division multiplexed single track).

The complete layout for the network 100B of FIG. 1B is given by combining the links in layout diagrams of 100C, 100D, 100E, 100F, and 100G. Applicant notes that in the layout 100C of FIG. 1C, the inter-block links between switch 1 and switch 2 of corresponding blocks are vertical tracks as shown in layout 100D of FIG. 1D; the inter-

block links between switch 2 and switch 3 of corresponding blocks are horizontal tracks as shown in layout 100E of FIG. 1E; the inter-block links between switch 3 and switch 4 of corresponding blocks are vertical tracks as shown in layout 100F of FIG. 1F; and finally the inter-block links between switch 4 and switch 5 of corresponding blocks are horizontal tracks as shown in layout 100G of FIG. 1G. The pattern is alternate vertical tracks and horizontal tracks. It continues recursively for larger networks of N > 32 as will be illustrated later.

Some of the key aspects of the current invention are discussed. 1) All the switches in one row of the multi-stage network 100B are implemented in a single block. 2) The blocks are placed in such a way that all the inter-block links are either horizontal tracks or vertical tracks; 3) Since all the inter-block links are either horizontal or vertical tracks, all the inter-block links can be mapped on to island-style architectures in current commercial FPGA's; 4) The length of the longest wire is about half of the width (or length) of the complete layout (For example middle link ML(4,4) is about half the width of the complete layout).

In accordance with the current invention, the layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ the sub-quadrants, quadrants, and super-quadrants are arranged in d-ary hypercube manner and also the inter-blocks are accordingly connected in d-ary hypercube topology. Even though all the embodiments in the current invention are illustrated for $N_1 = N_2$, the embodiments can be extended for $N_1 \neq N_2$.

Referring to layout 100H of FIG. 1H, illustrates the extension of layout 100C for the network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 128$; $d = 2$; and $s = 2$. There are four super-quadrants in layout 100H namely top-left super-quadrant, bottom-left super-quadrant, top-right super-quadrant, bottom-right super-quadrant. Total number of blocks in the layout 100H is sixty four. Top-left super-quadrant implements the blocks from block 1_2 to block 31_32. Each block in all the super-quadrants has two more switches namely switch 6 and switch 7 in addition to the switches [1-5] illustrated in layout 100C of FIG. 1C. The inter-block link connection topology is the exactly the same between the

switches 1 and 2; switches 2 and 3; switches 3 and 4; switches 4 and 5 as it is shown in the layouts of FIG. 1D, FIG. 1E, FIG. 1F, and FIG. 1G respectively.

Bottom-left super-quadrant implements the blocks from block 33_34 to block 63_64. Top-right super-quadrant implements the blocks from block 65_66 to block 95_96. And bottom-right super-quadrant implements the blocks from block 97_98 to block 127_128. In all these three super-quadrants also, the inter-block link connection topology is the exactly the same between the switches 1 and 2; switches 2 and 3; switches 3 and 4; switches 4 and 5 as that of the top-left super-quadrant.

Recursively in accordance with the current invention, the inter-block links connecting the switch 5 and switch 6 will be vertical tracks between the corresponding switches of top-left super-quadrant and bottom-left super-quadrant. And similarly the inter-block links connecting the switch 5 and switch 6 will be vertical tracks between the corresponding switches of top-right super-quadrant and bottom-right super-quadrant. The inter-block links connecting the switch 6 and switch 7 will be horizontal tracks between the corresponding switches of top-left super-quadrant and top-right super-quadrant. And similarly the inter-block links connecting the switch 6 and switch 7 will be horizontal tracks between the corresponding switches of bottom-left super-quadrant and bottom-right super-quadrant.

Referring to diagram 100I of FIG. 1I illustrates a high-level implementation of Block 1_2 (Each of the other blocks have similar implementation) of the layout 100C of FIG. 1C which represents a generalized folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$. Block 1_2 in 100I illustrates both the intra-block and inter-block links connected to Block 1_2. The layout diagram 100I corresponds to the embodiment where the switches that are placed together are implemented as separate switches in the network 100B of FIG. 1B. As noted before then the network 100B is the generalized folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with nine stages as disclosed in U.S. Provisional Patent Application Serial No. 60/940,389 that is incorporated by reference above.

That is the switches that are placed together in Block 1_2 as shown in FIG. 1I are namely input switch IS1 and output switch OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the switches implemented are input switch IS1 and output switch OS1); middle switch MS(1,1) and middle switch MS(7,1) belonging to switch 2; middle switch MS(2,1) and middle switch MS(6,1) belonging to switch 3; middle switch MS(3,1) and middle switch MS(5,1) belonging to switch 4; And middle switch MS(4,1) belonging to switch 5.

Input switch IS1 is implemented as two by four switch with the inlet links IL1 and IL2 being the inputs of the input switch IS1 and middle links ML(1,1) – ML(1,4) being the outputs of the input switch IS1; and output switch OS1 is implemented as four by two switch with the middle links ML(8,1) – ML(8,4) being the inputs of the output switch OS1 and outlet links OL1 – OL2 being the outputs of the output switch OS1.

Middle switch MS(1,1) is implemented as four by four switch with the middle links ML(1,1), ML(1,2), ML(1,7) and ML(1,8) being the inputs and middle links ML(2,1) – ML(2,4) being the outputs; and middle switch MS(7,1) is implemented as four by four switch with the middle links ML(7,1), ML(7,2), ML(7,11) and ML(7,12) being the inputs and middle links ML(8,1) – ML(8,4) being the outputs. Similarly all the other middle switches are also implemented as four by four switches as illustrated in 100I of FIG. 1I.

Now the VLSI layouts of generalized multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 < 32$; d = 2; s = 2 and its corresponding version of folded generalized multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 < 32$; d = 2; s = 2 are discussed. Referring to diagram 200A1 of FIG. 2A1 is generalized multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 2$; d = 2. Diagram 200A2 of FIG. 2A2 illustrates the corresponding folded generalized multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 2$; d = 2, version of the diagram 200A1 of FIG. 2A1. Layout 200A3 of FIG. 2A3 illustrates the VLSI layout of the network 200A2 of FIG. 2A2. There is only one block i.e., Block 1_2 comprising switch 1. Just like in the layout 100C of FIG. 1C, switch 1 consists of input switch IS1 and output switch OS1.

Referring to diagram 200B1 of FIG. 2B1 is generalized multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 4$; d = 2; s = 2. Diagram 200B2 of FIG. 2B2 illustrates the corresponding folded generalized multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 4$; d = 2; s = 2, version of the diagram 200B1 of FIG. 2B1. Layout 200B3 of FIG. 2B3 illustrates the VLSI layout of the network 200B2 of FIG. 2B2. There are two blocks i.e., Block 1_2 and Block 3_4 each comprising switch 1 and switch 2. Switch 1 in each block consists of the corresponding input switch and output switch. For example switch 1 in Block 1_2 consists of input switch IS1 and output switch OS1. Similarly switch 2 in Block 1_2 consists of middle switch (1,1). Layout 200B4 of FIG. 2B4 illustrates the inter-block links of the VLSI layout diagram 200B3 of FIG. 2B3. For example middle links ML(1,4) and ML(2,8). It must be noted that all the inter-block links are vertical tracks in this layout. (Alternatively all the inter-blocks can also be implemented as horizontal tracks).

Referring to diagram 200C11 of FIG. 2C11 is generalized multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 8$; d = 2; s = 2. Diagram 200C12 of FIG. 2C12 illustrates the corresponding folded generalized multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 8$; d = 2; s = 2, version of the diagram 200C11 of FIG. 2C11. Layout 200C21 of FIG. 2C21 illustrates the VLSI layout of the network 200C12 of FIG. 2C12. There are four blocks i.e., Block 1_2, Block 3_4, Block 5_6, and Block 7_8 each comprising switch 1, switch 2 and switch 3. For example switch 1 in Block 1_2 consists of input switch IS1 and output switch OS1; Switch 2 in Block 1_2 consists of MS(1,1) and MS(3,1). Switch 3 in Block 1_2 consists of MS(2,1).

Layout 200C22 of FIG. 2C22 illustrates the inter-block links between the switch 1 and switch 2 of the VLSI layout diagram 200C21 of FIG. 2C21. For example middle links ML(1,4) and ML(4,8) are connected between Block 1_2 and Block 3_4. It must be noted that all the inter-block links between switch 1 and switch 2 of all blocks are vertical tracks in this layout. Layout 200C23 of FIG. 2C23 illustrates the inter-block links between the switch 2 and switch 3 of the VLSI layout diagram 200C21 of FIG. 2C21. For example middle links ML(2,12) and ML(3,4) are connected between Block 1_2 and

Block 5_6. It must be noted that all the inter-block links between switch 2 and switch 3 of all blocks are horizontal tracks in this layout

Referring to diagram 200D1 of FIG. 2D1 is generalized multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 16$; d = 2; s = 2. Diagram 200D2 of FIG. 2D2 illustrates the corresponding folded generalized multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 16$; d = 2; s = 2, version of the diagram 200D1 of FIG. 2D1. Layout 200D3 of FIG. 2D3 illustrates the VLSI layout of the network 200D2 of FIG. 2D2. There are eight blocks i.e., Block 1_2, Block 3_4, Block 5_6, Block 7_8, Block 9_10, Block 11_12, Block 13_14 and Block 15_16 each comprising switch 1, switch 2, switch 3 and switch 4. For example switch 1 in Block 1_2 consists of input switch IS1 and output switch OS1; Switch 2 in Block 1_2 consists of MS(1,1) and MS(5,1). Switch 3 in Block 1_2 consists of MS(2,1) and MS(4,1), and switch 4 in Block 1_2 consists of MS(3,1).

Layout 200D4 of FIG. 2D4 illustrates the inter-block links between the switch 1 and switch 2 of the VLSI layout diagram 200D3 of FIG. 2D3. For example middle links ML(1,4) and ML(6,8) are connected between Block 1_2 and Block 3_4. It must be noted that all the inter-block links between switch 1 and switch 2 of all blocks are vertical tracks in this layout. Layout 200D5 of FIG. 2D5 illustrates the inter-block links between the switch 2 and switch 3 of the VLSI layout diagram 200D3 of FIG. 2D3. For example middle links ML(2,12) and ML(5,4) are connected between Block 1_2 and Block 5_6. It must be noted that all the inter-block links between switch 2 and switch 3 of all blocks are horizontal tracks in this layout. Layout 200D6 of FIG. 2D6 illustrates the inter-block links between the switch 3 and switch 4 of the VLSI layout diagram 200D3 of FIG. 2D3. For example middle links ML(3,4) and ML(4,20) are connected between Block 1_2 and Block 9_10. It must be noted that all the inter-block links between switch 3 and switch 4 of all blocks are vertical tracks in this layout.

Generalized Multi-link Butterfly Fat Tree Network Embodiment:

In another embodiment in the network 100B of FIG. 1B, the switches that are placed together are implemented as combined switch then the network 100B is the

generalized multi-link butterfly fat tree network $V_{mlink-bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with five stages as disclosed in U.S. Provisional Patent Application Serial No. 60/940,390 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a six by six switch. For example the input switch IS1 and output switch OS1 are placed together; so input switch IS1 and output OS1 are implemented as a six by six switch with the inlet links IL1, IL2, ML(8,1), ML(8,2), ML(8,7) and ML(8,8) being the inputs of the combined switch (denoted as IS1&OS1) and middle links ML(1,1), ML(1,2), ML(1,3), ML(1,4), OL1 and OL2 being the outputs of the combined switch IS1&OS1. Similarly in this embodiment of network 100B all the switches that are placed together are implemented as a combined switch.

Layout diagrams 100C in FIG. 1C, 100D in FIG. 1D, 100E in FIG. 1E, 100F in FIG. 1G are also applicable to generalized multi-link butterfly fat tree network $V_{mlink-bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with five stages. The layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized multi-link butterfly fat tree network $V_{mlink-bft}(N_1, N_2, d, s)$. Accordingly layout 100H of FIG. 1H is also applicable to generalized multi-link butterfly fat tree network $V_{mlink-bft}(N_1, N_2, d, s)$.

Referring to diagram 100J of FIG. 1J illustrates a high-level implementation of Block 1_2 (Each of the other blocks have similar implementation) of the layout 100C of FIG. 1C which represents a generalized multi-link butterfly fat tree network $V_{mlink-bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$. Block 1_2 in 100J illustrates both the intra-block and inter-block links. The layout diagram 100J corresponds to the embodiment where the switches that are placed together are implemented as combined switch in the network 100B of FIG. 1B. As noted before then the network 100B is the generalized multi-link butterfly fat tree network $V_{mlink-bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with five stages as disclosed in U.S. Provisional Patent Application Serial No. 60/940,390 that is incorporated by reference above.

That is the switches that are placed together in Block 1_2 as shown in FIG. 1J are namely the combined input and output switch IS1&OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the switch implemented is combined input and output switch IS1&OS1); middle switch MS(1,1) belonging to switch 2; middle switch MS(2,1) belonging to switch 3; middle switch MS(3,1) belonging to switch 4; And middle switch MS(4,1) belonging to switch 5.

Combined input and output switch IS1&OS1 is implemented as six by six switch with the inlet links IL1, IL2 and ML(8,1) – ML(8,4) being the inputs and middle links ML(1,1) – ML(1,4), and outlet links OL1 – OL2 being the outputs.

Middle switch MS(1,1) is implemented as eight by eight switch with the middle links ML(1,1), ML(1,2), ML(1,7), ML(1,8), ML(7,1), ML(7,2), ML(7,11) and ML(7,12) being the inputs and middle links ML(2,1) – ML(2,4) and middle links ML(8,1) – ML(8,4) being the outputs. Similarly all the other middle switches are also implemented as eight by eight switches as illustrated in 100J of FIG. 1J. Applicant observes that in middle switch MS(1,1) any one of the right going middle links can be switched to any one of the left going middle links and hereinafter middle switch MS(1,1) provides U-turn links. In general, in the network $V_{mlink-bft}(N_1, N_2, d, s)$ each input switch, each output switch and each middle switch provides U-turn links.

In another embodiment, middle switch MS(1,1) (or the middle switches in any of the middle stage excepting the root middle stage) of Block 1_2 of $V_{mlink-bft}(N_1, N_2, d, s)$ can be implemented as a four by eight switch and a four by four switch to save cross points. This is because the left going middle links of these middle switches are never setup to the right going middle links. For example, in middle switch MS(1,1) of Block 1_2 as shown FIG. 1J, the left going middle links namely ML(7,1), ML(7,2), ML(7,11), and ML(7,12) are never switched to the right going middle links ML(2,1), ML(2,2), ML(2,3), and ML(2,4). And hence to implement MS(1,1) two switches namely: 1) a four by eight switch with the middle links ML(1,1), ML(1,2), ML(1,7), and ML(1,8) as inputs and the middle links ML(2,1), ML(2,2), ML(2,3), ML(2,4), ML(8,1), ML(8,2), ML(8,3), and ML(8,4) as outputs and 2) a four by four

switch with the middle links ML(7,1), ML(7,2), ML(7,11), and ML(7,12) as inputs and the middle links ML(8,1), ML(8,2), ML(8,3), and ML(8,4) as outputs are sufficient without loosing any connectivity of the embodiment of MS(1,1) being implemented as an eight by eight switch as described before.)

Generalized multi-stage network Embodiment:

In one embodiment, in the network 100B of FIG. 1B, the switches that are placed together are implemented as two separate switches in input stage 110 and output stage 120; and as four separate switches in all the middle stages, then the network 100B is the generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with nine stages as disclosed in U.S. Provisional Patent Application Serial No. 60/940,391 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a two by four switch and a four by two switch respectively. For example the switch input switch IS1 and output switch OS1 are placed together; so input switch IS1 is implemented as two by four switch with the inlet links IL1 and IL2 being the inputs and middle links ML(1,1) – ML(1,4) being the outputs; and output switch OS1 is implemented as four by two switch with the middle links ML(8,1), ML(8,4), ML(8,7) and ML(8,8) being the inputs and outlet links OL1 – OL2 being the outputs.

The switches, corresponding to the middle stages that are placed together are implemented as four two by two switches. For example middle switches MS(1,1), MS(1,17), MS(7,1), and MS(7,17) are placed together; so middle switch MS(1,1) is implemented as two by two switch with middle links ML(1,1) and ML(1,7) being the inputs and middle links ML(2,1) and ML(2,3) being the outputs; middle switch MS(1,17) is implemented as two by two switch with the middle links ML(1,2) and ML(1,8) being the inputs and middle links ML(2,2) and ML(2,4) being the outputs; middle switch MS(7,1) is implemented as two by two switch with middle links ML(7,1) and ML(7,11) being the inputs and middle links ML(8,1) and ML(8,3) being the outputs; And middle switch MS(7,17) is implemented as two by two switch with the middle links ML(7,2) and ML(7,12) being the inputs and middle links ML(8,2) and ML(8,4) being the outputs;

Similarly in this embodiment of network 100B all the switches that are placed together are implemented as separate switches.

Layout diagrams 100C in FIG. 1C, 100D in FIG. 1D, 100E in FIG. 1E, 100F in FIG. 1G are also applicable to generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 2 with nine stages. The layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$. Accordingly layout 100H of FIG. 1H is also applicable to generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$.

Referring to diagram 100K of FIG. 1K illustrates a high-level implementation of Block 1_2 (Each of the other blocks have similar implementation) of the layout 100C of FIG. 1C which represents a generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 2. Block 1_2 in 100K illustrates both the intra-block and inter-block links. The layout diagram 100K corresponds to the embodiment where the switches that are placed together are implemented as separate switches in the network 100B of FIG. 1B. As noted before then the network 100B is the generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 2 with nine stages as disclosed in U.S. Provisional Patent Application Serial No. 60/940,391 that is incorporated by reference above.

That is the switches that are placed together in Block 1_2 as shown in FIG. 1K are namely the input switch IS1 and output switch OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the switches implemented are input switch IS1 and output switch OS1); middle switches MS(1,1), MS(1,17), MS(7,1) and MS(7,17) belonging to switch 2; middle switches MS(2,1), MS(2,17), MS(6,1) and MS(6,17) belonging to switch 3; middle switches MS(3,1), MS(3,17), MS(5,1) and MS(5,17) belonging to switch 4; And middle switches MS(4,1), and MS(4,17) belonging to switch 5.

Input switch IS1 and output switch OS1 are placed together; so input switch IS1 is implemented as two by four switch with the inlet links IL1 and IL2 being the inputs and

middle links ML(1,1) – ML(1,4) being the outputs; and output switch OS1 is implemented as four by two switch with the middle links ML(8,1), ML(8,4), ML(8,7) and ML(8,8) being the inputs and outlet links OL1 – OL2 being the outputs.

Middle switches MS(1,1), MS(1,17), MS(7,1), and MS(7,17) are placed together; so middle switch MS(1,1) is implemented as two by two switch with middle links ML(1,1) and ML(1,7) being the inputs and middle links ML(2,1) and ML(2,3) being the outputs; middle switch MS(1,17) is implemented as two by two switch with the middle links ML(1,2) and ML(1,8) being the inputs and middle links ML(2,2) and ML(2,4) being the outputs; middle switch MS(7,1) is implemented as two by two switch with middle links ML(7,1) and ML(7,11) being the inputs and middle links ML(8,1) and ML(8,3) being the outputs; And middle switch MS(7,17) is implemented as two by two switch with the middle links ML(7,2) and ML(7,12) being the inputs and middle links ML(8,2) and ML(8,4) being the outputs. Similarly all the other middle switches are also implemented as two by two switches as illustrated in 100K of FIG. 1K.

Generalized multi-stage network Embodiment with S = 1:

In one embodiment, in the network 100B of FIG. 1B (where it is implemented with s = 1), the switches that are placed together are implemented as two separate switches in input stage 110 and output stage 120; and as two separate switches in all the middle stages, then the network 100B is the generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 1 with nine stages as disclosed in U.S. Provisional Patent Application Serial No. 60/940,391 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a two by two switch and a two by two switch. For example the switch input switch IS1 and output switch OS1 are placed together; so input switch IS1 is implemented as two by two switch with the inlet links IL1 and IL2 being the inputs and middle links ML(1,1) – ML(1,2) being the outputs; and output switch OS1 is implemented as two by two switch with the middle links ML(8,1) and ML(8,3) being the inputs and outlet links OL1 – OL2 being the outputs.

The switches, corresponding to the middle stages that are placed together are implemented as two, two by two switches. For example middle switches MS(1,1) and MS(7,1) are placed together; so middle switch MS(1,1) is implemented as two by two switch with middle links ML(1,1) and ML(1,3) being the inputs and middle links ML(2,1) and ML(2,2) being the outputs; middle switch MS(7,1) is implemented as two by two switch with middle links ML(7,1) and ML(7,5) being the inputs and middle links ML(8,1) and ML(8,2) being the outputs; Similarly in this embodiment of network 100B all the switches that are placed together are implemented as two separate switches.

Layout diagrams 100C in FIG. 1C, 100D in FIG. 1D, 100E in FIG. 1E, 100F in FIG. 1G are also applicable to generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 1 with nine stages. The layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$. Accordingly layout 100H of FIG. 1H is also applicable to generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$.

Referring to diagram 100K1 of FIG. 1K1 illustrates a high-level implementation of Block 1_2 (Each of the other blocks have similar implementation) for the layout 100C of FIG. 1C when s = 1 which represents a generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 1 (All the double links are replaced by single links when s = 1). Block 1_2 in 100K1 illustrates both the intra-block and inter-block links. The layout diagram 100K1 corresponds to the embodiment where the switches that are placed together are implemented as separate switches in the network 100B of FIG. 1B when s = 1. As noted before then the network 100B is the generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 1 with nine stages as disclosed in U.S. Provisional Patent Application Serial No. 60/940,391 that is incorporated by reference above.

That is the switches that are placed together in Block 1_2 as shown in FIG. 1K1 are namely the input switch IS1 and output switch OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the switches implemented are input switch IS1 and output switch OS1); middle switches

MS(1,1) and MS(7,1) belonging to switch 2; middle switches MS(2,1) and MS(6,1) belonging to switch 3; middle switches MS(3,1) and MS(5,1) belonging to switch 4; And middle switch MS(4,1) belonging to switch 5.

Input switch IS1 and output switch OS1 are placed together; so input switch IS1 is implemented as two by two switch with the inlet links IL1 and IL2 being the inputs and middle links ML(1,1) – ML(1,2) being the outputs; and output switch OS1 is implemented as two by two switch with the middle links ML(8,1) and ML(8,3) being the inputs and outlet links OL1 – OL2 being the outputs.

Middle switches MS(1,1) and MS(7,1) are placed together; so middle switch MS(1,1) is implemented as two by two switch with middle links ML(1,1) and ML(1,3) being the inputs and middle links ML(2,1) and ML(2,2) being the outputs; And middle switch MS(7,1) is implemented as two by two switch with middle links ML(7,1) and ML(7,5) being the inputs and middle links ML(8,1) and ML(8,2) being the outputs. Similarly all the other middle switches are also implemented as two by two switches as illustrated in 100K1 of FIG. 1K1.

Generalized Butterfly Fat Tree Network Embodiment:

In another embodiment in the network 100B of FIG. 1B, the switches that are placed together are implemented as two combined switches then the network 100B is the generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with five stages as disclosed in U.S. Provisional Patent Application Serial No. 60/940,387 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a six by six switch. For example the input switch IS1 and output switch OS1 are placed together; so input output switch IS1&OS1 are implemented as a six by six switch with the inlet links IL1, IL2, ML(8,1), ML(8,2), ML(8,7) and ML(8,8) being the inputs of the combined switch (denoted as IS1&OS1) and middle links ML(1,1), ML(1,2), ML(1,3), ML(1,4), OL1 and OL2 being the outputs of the combined switch IS1&OS1.

The switches, corresponding to the middle stages that are placed together are implemented as two four by four switches. For example middle switches MS(1,1) and MS(1,17) are placed together; so middle switch MS(1,1) is implemented as four by four switch with middle links ML(1,1), ML(1,7), ML(7,1) and ML(7,11) being the inputs and middle links ML(2,1), ML(2,3), ML(8,1) and ML(8,3) being the outputs; middle switch MS(1,17) is implemented as four by four switch with the middle links ML(1,2), ML(1,8), ML(7,2) and ML(7,12) being the inputs and middle links ML(2,2), ML(2,4), ML(8,2) and ML(8,4) being the outputs. Similarly in this embodiment of network 100B all the switches that are placed together are implemented as a two combined switches.

Layout diagrams 100C in FIG. 1C, 100D in FIG. 1D, 100E in FIG. 1E, 100F in FIG. 1G are also applicable to generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 2 with five stages. The layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$. Accordingly layout 100H of FIG. 1H is also applicable to generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$.

Referring to diagram 100L of FIG. 1L illustrates a high-level implementation of Block 1_2 (Each of the other blocks have similar implementation) of the layout 100C of FIG. 1C which represents a generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 2. Block 1_2 in 100L illustrates both the intra-block and inter-block links. The layout diagram 100L corresponds to the embodiment where the switches that are placed together are implemented as two combined switches in the network 100B of FIG. 1B. As noted before then the network 100B is the generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 2 with five stages as disclosed in U.S. Provisional Patent Application Serial No. 60/940,387 that is incorporated by reference above.

That is the switches that are placed together in Block 1_2 as shown in FIG. 1L are namely the combined input and output switch IS1&OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the switch implemented is combined input and output switch IS1&OS1); middle switch

MS(1,1) and MS(1,17) belonging to switch 2; middle switch MS(2,1) and MS(2,17) belonging to switch 3; middle switch MS(3,1) and MS(3,17) belonging to switch 4; And middle switch MS(4,1) belonging to switch 5.

Combined input and output switch IS1&OS1 is implemented as six by six switch with the inlet links IL1, IL2, ML(8,1) , ML(8,2), ML(8,7) and ML(8,8) being the inputs and middle links ML(1,1) – ML(1,4) and outlet links OL1 – OL2 being the outputs.

Middle switch MS(1,1) is implemented as four by four switch with middle links ML(1,1), ML(1,7), ML(7,1) and ML(7,11) being the inputs and middle links ML(2,1), ML(2,3), ML(8,1) and ML(8,3) being the outputs; And middle switch MS(1,17) is implemented as four by four switch with the middle links ML(1,2), ML(1,8), ML(7,2) and ML(7,12) being the inputs and middle links ML(2,2), ML(2,4), ML(8,2) and ML(8,4) being the outputs. Similarly all the other middle switches are also implemented as two four by four switches as illustrated in 100L of FIG. 1L. Applicant observes that in middle switch MS(1,1) any one of the right going middle links can be switched to any one of the left going middle links and hereinafter middle switch MS(1,1) provides U-turn links. In general, in the network $V_{bft}(N_1, N_2, d, s)$ each input switch, each output switch and each middle switch provides U-turn links.

In another embodiment, middle switch MS(1,1) (or the middle switches in any of the middle stage excepting the root middle stage) of Block 1_2 of $V_{bft}(N_1, N_2, d, s)$ can be implemented as a two by four switch and a two by two switch to save cross points. This is because the left going middle links of these middle switches are never setup to the right going middle links. For example, in middle switch MS(1,1) of Block 1_2 as shown FIG. 1L, the left going middle links namely ML(7,1) and ML(7,11) are never switched to the right going middle links ML(2,1) and ML(2,3). And hence to implement MS(1,1) two switches namely: 1) a two by four switch with the middle links ML(1,1) and ML(1,7) as inputs and the middle links ML(2,1), ML(2,3), ML(8,1), and ML(8,3) as outputs and 2) a two by two switch with the middle links ML(7,1) and ML(7,11) as inputs and the middle links ML(8,1) and ML(8,3) as outputs are sufficient without loosing any

connectivity of the embodiment of MS(1,1) being implemented as an eight by eight switch as described before.)

Generalized Butterfly Fat Tree Network Embodiment with S = 1:

In one embodiment, in the network 100B of FIG. 1B (where it is implemented with s = 1), the switches that are placed together are implemented as a combined switch in input stage 110 and output stage 120; and as a combined switch in all the middle stages, then the network 100B is the generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 1 with five stages as disclosed in U.S. Provisional Patent Application Serial No. 60/940,387 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a four by four switch. For example the switch input switch IS1 and output switch OS1 are placed together; so input and output switch IS1&OS1 is implemented as four by four switch with the inlet links IL1, IL2, ML(8,1) and ML(8,3) being the inputs and middle links ML(1,1) – ML(1,2) and outlet links OL1 – OL2 being the outputs

The switches, corresponding to the middle stages that are placed together are implemented as a four by four switch. For example middle switches MS(1,1) is implemented as four by four switch with middle links ML(1,1), ML(1,3), ML(7,1) and ML(7,5) being the inputs and middle links ML(2,1), ML(2,2), ML(8,1) and ML(8,2) being the outputs..

Layout diagrams 100C in FIG. 1C, 100D in FIG. 1D, 100E in FIG. 1E, 100F in FIG. 1G are also applicable to generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 1 with five stages. The layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$. Accordingly layout 100H of FIG. 1H is also applicable to generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$.

Referring to diagram 100L1 of FIG. 1L1 illustrates a high-level implementation of Block 1_2 (Each of the other blocks have similar implementation) for the layout 100C of FIG. 1C when s = 1 which represents a generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 1 (All the double links are replaced by single links when s = 1). Block 1_2 in 100K1 illustrates both the intra-block and inter-block links. The layout diagram 100L1 corresponds to the embodiment where the switches that are placed together are implemented as a combined switch in the network 100B of FIG. 1B when s = 1. As noted before then the network 100B is the generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 1 with nine stages as disclosed in U.S. Provisional Patent Application Serial No. 60/940,387 that is incorporated by reference above.

That is the switches that are placed together in Block 1_2 as shown in FIG. 1L1 are namely the input and output switch IS1&OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the switches implemented are input switch IS1 and output switch OS1); middle switch MS(1,1) belonging to switch 2; middle switch MS(2,1) belonging to switch 3; middle switch MS(3,1) belonging to switch 4; And middle switch MS(4,1) belonging to switch 5.

Input and output switch IS1&OS1 are placed together; so input and output switch IS1&OS1 is implemented as four by four switch with the inlet links IL1, IL2, ML(8,1) and ML(8,3) being the inputs and middle links ML(1,1) – ML(1,2) and outlet links OL1 – OL2 being the outputs.

Middle switch MS(1,1) is implemented as four by four switch with middle links ML(1,1), ML(1,3), ML(7,1) and ML(7,5) being the inputs and middle links ML(2,1), ML(2,2), ML(8,1) and ML(8,2) being the outputs. Similarly all the other middle switches are also implemented as four by four switches as illustrated in 100L1 of FIG. 1L1.

In another embodiment, middle switch MS(1,1) (or the middle switches in any of the middle stage excepting the root middle stage) of Block 1_2 of $V_{mlink-bft}(N_1, N_2, d, s)$ can be implemented as a two by four switch and a two by two

switch to save cross points. This is because the left going middle links of these middle switches are never setup to the right going middle links. For example, in middle switch MS(1,1) of Block 1_2 as shown FIG. 1L1, the left going middle links namely ML(7,1) and ML(7,5) are never switched to the right going middle links ML(2,1) and ML(2,2). And hence to implement MS(1,1) two switches namely: 1) a two by four switch with the middle links ML(1,1) and ML(1,3) as inputs and the middle links ML(2,1), ML(2,2), ML(8,1), and ML(8,2) as outputs and 2) a two by two switch with the middle links ML(7,1) and ML(7,5) as inputs and the middle links ML(8,1) and ML(8,2) as outputs are sufficient without loosing any connectivity of the embodiment of MS(1,1) being implemented as an eight by eight switch as described before.)

Hypercube-like Topology layout schemes:

Referring to diagram 300A in FIG. 3A, in one embodiment, an exemplary generalized multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; d = 2; and s = 2 with nine stages of one hundred and forty four switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, 150, 170, 170, 180 and 190 is shown where input stage 110 consists of sixteen, two by four switches IS1-IS16 and output stage 120 consists of sixteen, four by two switches OS1-OS16.

As disclosed in U.S. Provisional Patent Application Serial No. 60/940,389 that is incorporated by reference above, such a network can be operated in rearrangeably non-blocking manner for arbitrary fan-out multicast connections and also can be operated in strictly non-blocking manner for unicast connections.

The diagram 300A in FIG. 3A is exactly the same as the diagram 100A in FIG. 1A excepting the connection links between middle stage 150 and middle stage 160 as well as between middle stage 160 and middle stage 170.

Each of the $\frac{N}{d}$ middle switches are connected to exactly d switches in middle stage 160 through two links each for a total of $2 \times d$ links (for example the links ML(4,1) and ML(4,2) are connected from middle switch MS(3,1) to middle switch MS(4,1), and the links ML(4,3) and ML(4,4) are connected from middle switch MS(3,1) to middle switch MS(4,15)).

Each of the $\frac{N}{d}$ middle switches MS(4,1) – MS(4,16) in the middle stage 160 are connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(4,1) and ML(4,2) are connected to the middle switch MS(4,1) from input switch MS(3,1), and the links ML(4,59) and ML(4,60) are connected to the middle switch MS(4,1) from input switch MS(3,15)) and also are connected to exactly d switches in middle stage 170 through two links each for a total of $2 \times d$ links (for example the links ML(5,1) and ML(5,2) are connected from middle switch MS(4,1) to middle switch MS(5,1), and the links ML(5,3) and ML(5,4) are connected from middle switch MS(4,1) to middle switch MS(5,15)).

Each of the $\frac{N}{d}$ middle switches MS(5,1) – MS(5,16) in the middle stage 170 are connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(5,1) and ML(5,2) are connected to the middle switch MS(5,1) from input switch MS(4,1), and the links ML(5,59) and ML(5,60) are connected to the middle switch MS(5,1) from input switch MS(4,15)).

Finally the connection topology of the network 100A shown in FIG. 1A is also basically back to back inverse Benes connection topology but with a slight variation. All the cross middle links from middle switches MS(3,1) - MS(3,8) connect to middle switches MS(4,9) – MS(4,16) and all the cross middle links from middle switches MS(3,9) - MS(3,16) connect to middle switches MS(4,1) – MS(4,8). Applicant makes a key observation that there are many combinations of connections possible using this property. The difference in the connection topology between diagram 100A of FIG. 1A and diagram 300A of FIG. 3A is that the connections formed by cross middle links

between middle stage 150 and middle stage 160 are made of two different combinations otherwise both the diagrams 100A and 300A implement back to back inverse Benes connection topology. Since these networks implement back to back inverse Benes topologies since there is difference in the connections of cross middle links between middle stage 150 and middle stage 160, the same difference in the connections of cross middle links between 160 and middle stage 170 occurs.

Referring to diagram 300B in FIG. 3B, is a folded version of the multi-link multi-stage network 300A shown in FIG. 3A. The network 300B in FIG. 3B shows input stage 110 and output stage 120 are placed together. That is input switch IS1 and output switch OS1 are placed together, input switch IS2 and output switch OS2 are placed together, and similarly input switch IS16 and output switch OS16 are placed together. All the right going middle links {i.e., inlet links IL1 – IL32 and middle links ML(1,1) - ML(1,64)} correspond to input switches IS1 - IS16, and all the left going middle links {i.e., middle links ML(7,1) - ML(7,64) and outlet links OL1-OL32} correspond to output switches OS1 - OS16.

Just the same way there is difference in the connection topology between diagram 100A of FIG. 1A and diagram 300A of FIG. 3A in the way the connections are formed by cross middle links between middle stage 150 and middle stage 160 and also between middle stage 160 and middle stage 170, the exact similar difference is there between the diagram 100B of FIG. 1B and the diagram 300B of FIG. 3B, i.e., in the way the connections are formed by cross middle links between middle stage 150 and middle stage 160 and also between middle stage 160 and middle stage 170.

In one embodiment, in the network 300B of FIG. 3B, the switches that are placed together are implemented as separate switches then the network 300B is the generalized folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with nine stages as disclosed in U.S. Provisional Patent Application Serial No. 60/940,389 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a two by four switch and a four by two switch. For example the switch input switch IS1 and output switch OS1 are placed together; so input switch IS1 is implemented as two by four switch with the

inlet links IL1 and IL2 being the inputs of the input switch IS1 and middle links ML(1,1) – ML(1,4) being the outputs of the input switch IS1; and output switch OS1 is implemented as four by two switch with the middle links ML(8,1), ML(8,2), ML(8,7) and ML(8,8) being the inputs of the output switch OS1 and outlet links OL1 – OL2 being the outputs of the output switch OS1. Similarly in this embodiment of network 300B all the switches that are placed together are implemented as separate switches.

Referring to layout 300C of FIG. 3C, in one embodiment, there are sixteen blocks namely Block 1_2, Block 3_4, Block 5_6, Block 7_8, Block 9_10, Block 11_12, Block 13_14, Block 15_16, Block 17_18, Block 19_20, Block 21_22, Block 23_24, Block 25_26, Block 27_28, Block 29_30, and Block 31_32. Each block implements all the switches in one row of the network 300B of FIG. 3B, one of the key aspects of the current invention. For example Block 1_2 implements the input switch IS1, output Switch OS1, middle switch MS(1,1), middle switch MS(7,1), middle switch MS(2,1), middle switch MS(6,1), middle switch MS(3,1), middle switch MS(5,1), and middle switch MS(4,1). For the simplification of illustration, Input switch IS1 and output switch OS1 together are denoted as switch 1; Middle switch MS(1,1) and middle switch MS(7,1) together are denoted by switch 2; Middle switch MS(2,1) and middle switch MS(6,1) together are denoted by switch 3; Middle switch MS(3,1) and middle switch MS(5,1) together are denoted by switch 4; And middle switch MS(4,1) is denoted by switch 5.

All the straight middle links are illustrated in layout 300C of FIG. 3C. For example in Block 1_2, inlet links IL1 – IL2, outlet links OL1 – OL2, middle link ML(1,1), middle link ML(1,2), middle link ML(8,1), middle link ML(8,2), middle link ML(2,1), middle link ML(2,2), middle link ML(7,1), middle link ML(7,2), middle link ML(3,1), middle link ML(3,2), middle link ML(6,1), middle link ML(6,2), middle link ML(4,1), middle link ML(4,2), middle link ML(5,1) and middle link ML(5,2) are illustrated in layout 300C of FIG. 3C.

Even though it is not illustrated in layout 300C of FIG. 3C, in each block, in addition to the switches there may be Configurable Logic Blocks (CLB) or any arbitrary digital circuit or sub-integrated circuit block depending on the applications in different embodiments. There are four quadrants in the layout 300C of FIG. 3C namely top-left,

bottom-left, top-right and bottom-right quadrants. Top-left quadrant implements Block 1_2, Block 3_4, Block 5_6, and Block 7_8. Bottom-left quadrant implements Block 9_10, Block 11_12, Block 13_14, and Block 15_16. Top-right quadrant implements Block 25_26, Block 27_28, Block 29_30, and Block 31_32. Bottom-right quadrant implements Block 17_18, Block 19_20, Block 21_22, and Block 23_24. There are two halves in layout 300C of FIG. 3C namely left-half and right-half. Left-half consists of top-left and bottom-left quadrants. Right-half consists of top-right and bottom-right quadrants.

Recursively in each quadrant there are four sub-quadrants. For example in top-left quadrant there are four sub-quadrants namely top-left sub-quadrant, bottom-left sub-quadrant, top-right sub-quadrant and bottom-right sub-quadrant. Top-left sub-quadrant of top-left quadrant implements Block 1_2. Bottom-left sub-quadrant of top-left quadrant implements Block 3_4. Top-right sub-quadrant of top-left quadrant implements Block 7_8. Finally bottom-right sub-quadrant of top-left quadrant implements Block 5_6. Similarly there are two sub-halves in each quadrant. For example in top-left quadrant there are two sub-halves namely left-sub-half and right-sub-half. Left-sub-half of top-left quadrant implements Block 1_2 and Block 3_4. Right-sub-half of top-left quadrant implements Block 7_8 and Block 5_6. Recursively in larger multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 > 32$, the layout in this embodiment in accordance with the current invention, will be such that the super-quadrants will also be arranged in a similar manner.

Layout 300D of FIG. 3D illustrates the inter-block links (in the layout 300C of FIG. 3C all the cross middle links are inter-block links) between switches 1 and 2 of each block. For example middle links ML(1,3), ML(1,4), ML(8,7), and ML(8,8) are connected between switch 1 of Block 1_2 and switch 2 of Block 3_4. Similarly middle links ML(1,7), ML(1,8), ML(8,3), and ML(8,4) are connected between switch 2 of Block 1_2 and switch 1 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 100D of FIG. 1D can be implemented as vertical tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(1,4) and ML(8,8) are implemented as two different tracks); or in an

alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(1,4) and ML(8,8) are implemented as a time division multiplexed single track).

Layout 300E of FIG. 3E illustrates the inter-block links between switches 2 and 3 of each block. For example middle links ML(2,3), ML(2,4), ML(7,11), and ML(7,12) are connected between switch 2 of Block 1_2 and switch 3 of Block 3_4. Similarly middle links ML(2,11), ML(2,12), ML(7,3), and ML(7,4) are connected between switch 3 of Block 1_2 and switch 2 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 300E of FIG. 3E can be implemented as diagonal tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(2,12) and ML(7,4) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(2,12) and ML(7,4) are implemented as a time division multiplexed single track).

Layout 300F of FIG. 3F illustrates the inter-block links between switches 3 and 4 of each block. For example middle links ML(3,3), ML(3,4), ML(6,19), and ML(6,20) are connected between switch 3 of Block 1_2 and switch 4 of Block 3_4. Similarly middle links ML(3,19), ML(3,20), ML(6,3), and ML(6,4) are connected between switch 4 of Block 1_2 and switch 3 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 300F of FIG. 3F can be implemented as vertical tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(3,4) and ML(6,20) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(3,4) and ML(6,20) are implemented as a time division multiplexed single track).

Layout 300G of FIG. 3G illustrates the inter-block links between switches 4 and 5 of each block. For example middle links ML(4,3), ML(4,4), ML(5,35), and ML(5,36) are connected between switch 4 of Block 1_2 and switch 5 of Block 3_4. Similarly middle links ML(4,35), ML(4,36), ML(5,3), and ML(5,4) are connected between switch 5 of Block 1_2 and switch 4 of Block 3_4. Applicant notes that the inter-block links illustrated

in layout 300G of FIG. 3G can be implemented as horizontal tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(4,4) and ML(5,36) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(4,4) and ML(5,36) are implemented as a time division multiplexed single track).

The complete layout for the network 300B of FIG. 3B is given by combining the links in layout diagrams of 300C, 300D, 300E, 300F, and 300G. Applicant notes that in the layout 300C of FIG. 3C, the inter-block links between switch 1 and switch 2 are vertical tracks as shown in layout 300D of FIG. 3D; the inter-block links between switch 2 and switch 3 are horizontal tracks as shown in layout 300E of FIG. 3E; the inter-block links between switch 3 and switch 4 are vertical tracks as shown in layout 300F of FIG. 3F; and finally the inter-block links between switch 4 and switch 5 are horizontal tracks as shown in layout 300G of FIG. 3G. The pattern is either vertical tracks, horizontal tracks or diagonal tracks. It continues recursively for larger networks of N > 32 as will be illustrated later.

Some of the key aspects of the current invention related to layout diagram 300C of IFG. 3C are noted. 1) All the switches in one row of the multi-stage network 300B are implemented in a single block. 2) The blocks are placed in such a way that all the inter-block links are either horizontal tracks, vertical tracks or diagonal tracks; 3) The length of the longest wire is about half of the width (or length) of the complete layout (For example middle link ML(4,4) is about half the width of the complete layout.);

The layout 300C in FIG. 3C can be recursively extended for any arbitrarily large generalized folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$. Referring to layout 300H of FIG. 3H, illustrates the extension of layout 300C for the network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 128$; $d = 2$; and $s = 2$. There are four super-quadrants in layout 300H namely top-left super-quadrant, bottom-left super-quadrant, top-right super-quadrant, bottom-right super-quadrant. Total number of blocks in the layout 300H is sixty four. Top-left super-quadrant implements the blocks from block 1_2

to block 31_32. Each block in all the super-quadrants has two more switches namely switch 6 and switch 7 in addition to the switches [1-5] illustrated in layout 300C of FIG. 3C. The inter-block link connection topology is the exactly the same between the switches 1 and 2; switches 2 and 3; switches 3 and 4; switches 4 and 5 as it is shown in the layouts of FIG. 3D, FIG. 3E, FIG. 3F, and FIG. 3G respectively.

Bottom-left super-quadrant implements the blocks from block 33_34 to block 63_64. Top-right super-quadrant implements the blocks from block 65_66 to block 95_96. And bottom-right super-quadrant implements the blocks from block 97_98 to block 127_128. In all these three super-quadrants also, the inter-block link connection topology is the exactly the same between the switches 1 and 2; switches 2 and 3; switches 3 and 4; switches 4 and 5 as that of the top-left super-quadrant.

Recursively in accordance with the current invention, the inter-block links connecting the switch 5 and switch 6 will be vertical tracks between the corresponding switches of top-left super-quadrant and bottom-left super-quadrant. And similarly the inter-block links connecting the switch 5 and switch 6 will be vertical tracks between the corresponding switches of top-right super-quadrant and bottom-right super-quadrant. The inter-block links connecting the switch 6 and switch 7 will be horizontal tracks between the corresponding switches of top-left super-quadrant and top-right super-quadrant. And similarly the inter-block links connecting the switch 6 and switch 7 will be horizontal tracks between the corresponding switches of bottom-left super-quadrant and bottom-right super-quadrant.

Ring Topology layout schemes:

Layout diagram 400C of FIG. 4C is another embodiment for the generalized folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ diagram 100B in FIG. 1B.

Referring to layout 400C of FIG. 4C, there are sixteen blocks namely Block 1_2, Block 3_4, Block 5_6, Block 7_8, Block 9_10, Block 11_12, Block 13_14, Block 15_16, Block 17_18, Block 19_20, Block 21_22, Block 23_24, Block 25_26, Block 27_28,

Block 29_30, and Block 31_32. Each block implements all the switches in one row of the network 100B of FIG. 1B, one of the key aspects of the current invention. For example Block 1_2 implements the input switch IS1, output Switch OS1, middle switch MS(1,1), middle switch MS(7,1), middle switch MS(2,1), middle switch MS(6,1), middle switch MS(3,1), middle switch MS(5,1), and middle switch MS(4,1). For the simplification of illustration, Input switch IS1 and output switch OS1 together are denoted as switch 1; Middle switch MS(1,1) and middle switch MS(7,1) together are denoted by switch 2; Middle switch MS(2,1) and middle switch MS(6,1) together are denoted by switch 3; Middle switch MS(3,1) and middle switch MS(5,1) together are denoted by switch 4; And middle switch MS(4,1) is denoted by switch 5.

All the straight middle links are illustrated in layout 400C of FIG. 4C. For example in Block 1_2, inlet links IL1 – IL2, outlet links OL1 – OL2, middle link ML(1,1), middle link ML(1,2), middle link ML(8,1), middle link ML(8,2), middle link ML(2,1), middle link ML(2,2), middle link ML(7,1), middle link ML(7,2), middle link ML(3,1), middle link ML(3,2), middle link ML(6,1), middle link ML(6,2), middle link ML(4,1), middle link ML(4,2), middle link ML(5,1) and middle link ML(5,2) are illustrated in layout 400C of FIG. 4C.

Even though it is not illustrated in layout 400C of FIG. 4C, in each block, in addition to the switches there may be Configurable Logic Blocks (CLB) or any arbitrary digital circuit or sub-integrated circuit block depending on the applications in different embodiments. The topology of the layout 400C in FIG. 4C is a ring. For each of the neighboring rows in diagram 100B of FIG. 1B the corresponding blocks are also physically neighbors in layout diagram 400C of FIG. 4C. In addition the topmost row is also logically considered as neighbor to the bottommost row. For example Block 1_2 (implementing the switches belonging to a row in diagram 100B of FIG. 1B) has Block 3_4 as neighbor since Block 3_4 implements the switches in its neighboring row. Similarly Block 1_2 also has Block 31_32 as neighbor since Block 1_2 implements topmost row of switches and Block 31_32 implements bottommost row of switches in diagram 100B of FIG. 1B. The ring layout scheme illustrated in 400C of FIG. 4C can be

generalized for a large multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 > 32$, in accordance with the current invention.

Layout 400B of FIG. 4B illustrates the inter-block links (in the layout 400A of FIG. 4A all the cross middle links are inter-block links) between switches 1 and 2 of each block. For example middle links ML(1,3), ML(1,4), ML(8,7), and ML(8,8) are connected between switch 1 of Block 1_2 and switch 2 of Block 3_4. Similarly middle links ML(1,7), ML(1,8), ML(8,3), and ML(8,4) are connected between switch 2 of Block 1_2 and switch 1 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 400B of FIG. 4B are implemented as vertical tracks or horizontal tracks or diagonal tracks. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(1,4) and ML(8,8) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(1,4) and ML(8,8) are implemented as a time division multiplexed single track).

Layout 400C of FIG. 4C illustrates the inter-block links between switches 2 and 3 of each block. For example middle links ML(2,3), ML(2,4), ML(7,11), and ML(7,12) are connected between switch 2 of Block 1_2 and switch 3 of Block 3_4. Similarly middle links ML(2,11), ML(2,12), ML(7,3), and ML(7,4) are connected between switch 3 of Block 1_2 and switch 2 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 400C of FIG. 4C are implemented as vertical tracks or horizontal tracks or diagonal tracks. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(2,12) and ML(7,4) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(2,12) and ML(7,4) are implemented as a time division multiplexed single track).

Layout 400D of FIG. 4D illustrates the inter-block links between switches 3 and 4 of each block. For example middle links ML(3,3), ML(3,4), ML(6,19), and ML(6,20) are connected between switch 3 of Block 1_2 and switch 4 of Block 3_4. Similarly middle links ML(3,19), ML(3,20), ML(6,3), and ML(6,4) are connected between switch 4 of Block 1_2 and switch 3 of Block 3_4. Applicant notes that the inter-block links illustrated

in layout 400D of FIG. 4D are implemented as vertical tracks or horizontal tracks or diagonal tracks. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(3,4) and ML(6,20) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(3,4) and ML(6,20) are implemented as a time division multiplexed single track).

Layout 400E of FIG. 4E illustrates the inter-block links between switches 4 and 5 of each block. For example middle links ML(4,3), ML(4,4), ML(5,35), and ML(5,36) are connected between switch 4 of Block 1_2 and switch 5 of Block 3_4. Similarly middle links ML(4,35), ML(4,36), ML(5,3), and ML(5,4) are connected between switch 5 of Block 1_2 and switch 4 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 400E of FIG. 4E are implemented as vertical tracks or horizontal tracks or diagonal tracks. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(4,4) and ML(5,36) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(4,4) and ML(5,36) are implemented as a time division multiplexed single track).

The complete layout for the network 100B of FIG. 1B is given by combining the links in layout diagrams of 400A, 400B, 400C, 400D, and 400E.

Some of the key aspects of the current invention related to layout diagram 400A of FIG. 4A are noted. 1) All the switches in one row of the multi-stage network 100B are implemented in a single block. 2) The blocks are placed in such a way that all the inter-block links are either horizontal tracks, vertical tracks or diagonal tracks; 3) Length of the different wires between the same two middle stages is not the same. However it gives an opportunity to implement the most connected circuits to place and route through the blocks which have shorter wires.

Layout diagram 400C1 of FIG. 4C1 is another embodiment for the generalized folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ diagram 100B in FIG. 1B. Referring to layout 400C1 of FIG. 4C1, there are sixteen blocks namely Block 1_2, Block

3_4, Block 5_6, Block 7_8, Block 9_10, Block 11_12, Block 13_14, Block 15_16, Block 17_18, Block 19_20, Block 21_22, Block 23_24, Block 25_26, Block 27_28, Block 29_30, and Block 31_32. Each block implements all the switches in one row of the network 100B of FIG. 1B, one of the key aspects of the current invention. For example Block 1_2 implements the input switch IS1, output Switch OS1, middle switch MS(1,1), middle switch MS(7,1), middle switch MS(2,1), middle switch MS(6,1), middle switch MS(3,1), middle switch MS(5,1), and middle switch MS(4,1). For the simplification of illustration, Input switch IS1 and output switch OS1 together are denoted as switch 1; Middle switch MS(1,1) and middle switch MS(7,1) together are denoted by switch 2; Middle switch MS(2,1) and middle switch MS(6,1) together are denoted by switch 3; Middle switch MS(3,1) and middle switch MS(5,1) together are denoted by switch 4; And middle switch MS(4,1) is denoted by switch 5.

All the straight middle links are illustrated in layout 400C1 of FIG. 4C1. For example in Block 1_2, inlet links IL1 – IL2, outlet links OL1 – OL2, middle link ML(1,1), middle link ML(1,2), middle link ML(8,1), middle link ML(8,2), middle link ML(2,1), middle link ML(2,2), middle link ML(7,1), middle link ML(7,2), middle link ML(3,1), middle link ML(3,2), middle link ML(6,1), middle link ML(6,2), middle link ML(4,1), middle link ML(4,2), middle link ML(5,1) and middle link ML(5,2) are illustrated in layout 400C1 of FIG. 4C1.

Even though it is not illustrated in layout 400C1 of FIG. 4C1, in each block, in addition to the switches there may be Configurable Logic Blocks (CLB) or any arbitrary digital circuit or sub-integrated circuit block depending on the applications in different embodiments. The topology of the layout 400C1 in FIG. 4C1 is another embodiment of ring layout topology. For each of the neighboring rows in diagram 100B of FIG. 1B the corresponding blocks are also physically neighbors in layout diagram 400C of FIG. 4C. In addition the topmost row is also logically considered as neighbor to the bottommost row. For example Block 1_2 (implementing the switches belonging to a row in diagram 100B of FIG. 1B) has Block 3_4 as neighbor since Block 3_4 implements the switches in its neighboring row. Similarly Block 1_2 also has Block 31_32 as neighbor since Block 1_2 implements topmost row of switches and Block 31_32 implements bottommost row

of switches in diagram 100B of FIG. 1B. The ring layout scheme illustrated in 400C of FIG. 4C can be generalized for a large multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 > 32$, in accordance with the current invention.

All the layout embodiments disclosed in the current invention are applicable to generalized multi-stage networks $V(N_1, N_2, d, s)$, generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$, generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$, generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$, and generalized hypercube networks $V_{hcube}(N_1, N_2, d, s)$ for s = 1,2,3 or any number in general, and for both $N_1 = N_2 = N$ .and $N_1 \neq N_2$, and d is any integer.

Conversely applicant makes another important observation that generalized hypercube networks $V_{hcube}(N_1, N_2, d, s)$ are implemented with the layout topology being the hypercube topology shown in layout 100C of FIG. 1C with large scale cross point reduction as any one of the networks described in the current invention namely: generalized multi-stage networks $V(N_1, N_2, d, s)$, generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$, generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$, generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$ for s = 1,2,3 or any number in general, and for both $N_1 = N_2 = N$ .and $N_1 \neq N_2$, and d is any integer.

Applications Embodiments:

All the embodiments disclosed in the current invention are useful in many varieties of applications. FIG. 5A1 illustrates the diagram of 500A1 which is a typical two by two switch with two inlet links namely IL1 and IL2, and two outlet links namely

OL1 and OL2. The two by two switch also implements four crosspoints namely CP(1,1), CP(1,2), CP(2,1) and CP(2,2) as illustrated in FIG. 5A1. For example the diagram of 500A1 may the implementation of middle switch MS(1,1) of the diagram 100K of FIG. 1K where inlet link IL1 of diagram 500A1 corresponds to middle link ML(1,1) of diagram 100K, inlet link IL2 of diagram 500A1 corresponds to middle link ML(1,7) of diagram 100K, outlet link OL1 of diagram 500A1 corresponds to middle link ML(2,1) of diagram 100K, outlet link OL2 of diagram 500A1 corresponds to middle link ML(2,3) of diagram 100K.

1) Programmable Integrated Circuit Embodiments:

All the embodiments disclosed in the current invention are useful in programmable integrated circuit applications. FIG. 5A2 illustrates the detailed diagram 500A2 for the implementation of the diagram 500A1 in programmable integrated circuit embodiments. Each crosspoint is implemented by a transistor coupled between the corresponding inlet link and outlet link, and a programmable cell in programmable integrated circuit embodiments. Specifically crosspoint CP(1,1) is implemented by transistor C(1,1) coupled between inlet link IL1 and outlet link OL1, and programmable cell P(1,1); crosspoint CP(1,2) is implemented by transistor C(1,2) coupled between inlet link IL1 and outlet link OL2, and programmable cell P(1,2); crosspoint CP(2,1) is implemented by transistor C(2,1) coupled between inlet link IL2 and outlet link OL1, and programmable cell P(2,1); and crosspoint CP(2,2) is implemented by transistor C(2,2) coupled between inlet link IL2 and outlet link OL2, and programmable cell P(2,2).

If the programmable cell is programmed ON, the corresponding transistor couples the corresponding inlet link and outlet link. If the programmable cell is programmed OFF, the corresponding inlet link and outlet link are not connected. For example if the programmable cell P(1,1) is programmed ON, the corresponding transistor C(1,1) couples the corresponding inlet link IL1 and outlet link OL1. If the programmable cell P(1,1) is programmed OFF, the corresponding inlet link IL1 and outlet link OL1 are not connected. In volatile programmable integrated circuit embodiments the programmable

cell may be an SRAM (Static Random Address Memory) cell. In non-volatile programmable integrated circuit embodiments the programmable cell may be a Flash memory cell. Also the programmable integrated circuit embodiments may implement field programmable logic arrays (FPGA) devices, or programmable Logic devices (PLD), or Application Specific Integrated Circuits (ASIC) embedded with programmable logic circuits or 3D-FPGAs.

FIG. 5A2 also illustrates a buffer B1 on inlet link IL2. The signals driven along inlet link IL2 are amplified by buffer B1. Buffer B1 can be inverting or non-inverting buffer. Buffers such as B1 are used to amplify the signal in links which are usually long.

2) One-time Programmable Integrated Circuit Embodiments:

All the embodiments disclosed in the current invention are useful in one-time programmable integrated circuit applications. FIG. 5A3 illustrates the detailed diagram 500A3 for the implementation of the diagram 500A1 in one-time programmable integrated circuit embodiments. Each crosspoint is implemented by a via coupled between the corresponding inlet link and outlet link in one-time programmable integrated circuit embodiments. Specifically crosspoint CP(1,1) is implemented by via V(1,1) coupled between inlet link IL1 and outlet link OL1; crosspoint CP(1,2) is implemented by via V(1,2) coupled between inlet link IL1 and outlet link OL2; crosspoint CP(2,1) is implemented by via V(2,1) coupled between inlet link IL2 and outlet link OL1; and crosspoint CP(2,2) is implemented by via V(2,2) coupled between inlet link IL2 and outlet link OL2.

If the via is programmed ON, the corresponding inlet link and outlet link are permanently connected which is denoted by thick circle at the intersection of inlet link and outlet link. If the via is programmed OFF, the corresponding inlet link and outlet link are not connected which is denoted by the absence of thick circle at the intersection of inlet link and outlet link. For example in the diagram 500A3 the via V(1,1) is programmed ON, and the corresponding inlet link IL1 and outlet link OL1 are connected as denoted by thick circle at the intersection of inlet link IL1 and outlet link OL1; the via V(2,2) is programmed ON, and the corresponding inlet link IL2 and outlet link OL2 are

connected as denoted by thick circle at the intersection of inlet link IL2 and outlet link OL2; the via V(1,2) is programmed OFF, and the corresponding inlet link IL1 and outlet link OL2 are not connected as denoted by the absence of thick circle at the intersection of inlet link IL1 and outlet link OL2; the via V(2,1) is programmed OFF, and the corresponding inlet link IL2 and outlet link OL1 are not connected as denoted by the absence of thick circle at the intersection of inlet link IL2 and outlet link OL1. One-time programmable integrated circuit embodiments may be anti-fuse based programmable integrated circuit devices or mask programmable structured ASIC devices.

3) Integrated Circuit Placement and Route Embodiments:

All the embodiments disclosed in the current invention are useful in Integrated Circuit Placement and Route applications, for example in ASIC backend Placement and Route tools. FIG. 5A4 illustrates the detailed diagram 500A4 for the implementation of the diagram 500A1 in Integrated Circuit Placement and Route embodiments. In an integrated circuit since the connections are known a-priori, the switch and crosspoints are actually virtual. However the concept of virtual switch and virtal crosspoint using the embodiments disclosed in the current invention reduces the number of required wires, wire length needed to connect the inputs and outputs of different netlists and the time required by the tool for placement and route of netlists in the integrated circuit.

Each virtual crosspoint is used to either to hardwire or provide no connectivity between the corresponding inlet link and outlet link. Specifically crosspoint CP(1,1) is implemented by direct connect point DCP(1,1) to hardwire (i.e., to permanently connect) inlet link IL1 and outlet link OL1 which is denoted by the thick circle at the intersection of inlet link IL1 and outlet link OL1; crosspoint CP(2,2) is implemented by direct connect point DCP(2,2) to hardwire inlet link IL2 and outlet link OL2 which is denoted by the thick circle at the intersection of inlet link IL2 and outlet link OL2. The diagram 500A4 does not show direct connect point DCP(1,2) and direct connect point DCP(1,3) since they are not needed and in the hardware implementation they are eliminated. Alternatively inlet link IL1 needs to be connected to outlet link OL1 and inlet link IL1 does not need to be connected to outlet link OL2. Also inlet link IL2 needs to be connected to outlet link OL2 and inlet link IL2 does not need to be connected to outlet

link OL1. Furthermore in the example of the diagram 500A4, there is no need to drive the signal of inlet link IL1 horizontally beyond outlet link OL1 and hence the inlet link IL1 is not even extended horizontally until the outlet link OL2. Also the absence of direct connect point DCP(2,1) illustrates there is no need to connect inlet link IL2 and outlet link OL1.

In summary in integrated circuit placement and route tools, the concept of virtual switches and virtual cross points is used during the implementation of the placement & routing algorithmically in software, however during the hardware implementation cross points in the cross state are implemented as hardwired connections between the corresponding inlet link and outlet link, and in the bar state are implemented as no connection between inlet link and outlet link.

3) More Application Embodiments:

All the embodiments disclosed in the current invention are also useful in the design of SoC interconnects, Field programmable interconnect chips, parallel computer systems and in time-space-time switches.

Numerous modifications and adaptations of the embodiments, implementations, and examples described herein will be apparent to the skilled artisan in view of the disclosure.

CLAIMS

What is claimed is:

1. An integrated circuit device comprising a plurality of sub-integrated circuit blocks and a routing network, and

Said each plurality of sub-integrated circuit blocks comprising a plurality of inlet links and a plurality of outlet links; and

Said routing network interconnects any one of said outlet link of one of said sub-integrated circuit block to one or more said inlet links of one or more of said sub-integrated circuit blocks; and

Said routing network comprising of a plurality of stages y, starting from the lowest stage to the highest stage; and

Said routing network comprising a plurality of switches of size $d \times d$, where $d \geq 2$, in each said stage and each said switch of size $d \times d$ having d inlet links and d outlet links; and

Said each sub-integrated circuit block comprising a plurality of said switches corresponding to each said stage; and

Said each sub-integrated circuit block comprising a plurality of forward connecting links connecting from switches in lower stage to switches in the immediate succeeding higher stage, and also comprising a plurality of backward connecting links connecting from switches in higher stage to switches in the immediate preceding lower stage; and

Said each sub-integrated circuit block comprising a plurality straight links in said forward connecting links from switches in lower stage to switches in the immediate succeeding higher stage and a plurality cross links in said forward connecting links from switches in lower stage to switches in the immediate succeeding higher stage, and further comprising a plurality of straight links in said backward connecting links from switches

in higher stage to switches in the immediate preceding lower stage and a plurality of cross links in said backward connecting links from switches in higher stage to switches in the immediate preceding lower stage.

2. The integrated circuit device of claim 1, wherein said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and

said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks.

3. The integrated circuit device of claim 2, wherein said plurality of sub-integrated circuit blocks arranged in a two-dimensional grid.

4. The integrated circuit device of claim 3, wherein said cross links in succeeding stages are connecting as alternative vertical and horizontal links between switches in said sub-integrated circuit blocks.

5. The integrated circuit device of claim 4, wherein said cross links from switches in a stage in one of said sub-integrated circuit blocks are connecting to switches in the succeeding stage in another of said sub-integrated circuit blocks so that said cross links are either vertical links or horizontal and vice versa, and hereinafter such cross links are "shuffle exchange links").

6. The integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are substantially of equal length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are substantially of equal length in the entire said integrated circuit device.

7. The integrated circuit device of claim 6, wherein the shortest horizontal shuffle exchange links are connecting at the lowest stage and between switches in two

nearest neighboring said sub-integrated circuit blocks, and length of the horizontal shuffle exchange links is doubled in each succeeding stage; and the shortest vertical shuffle exchange links are connecting at the lowest stage and between switches in two nearest neighboring said sub-integrated circuit blocks, and length of the vertical shuffle exchange links is doubled in each succeeding stage.

8. The integrated circuit device of claim 7, wherein $y \geq (\log_2 N)$ so that the length of the horizontal shuffle exchange links in the highest stage is equal to half the size of the horizontal size of said two dimensional grid of sub-integrated circuit blocks and the length of the vertical shuffle exchange links in the highest stage is equal to half the size of the vertical size of said two dimensional grid of sub-integrated circuit blocks.

9. The integrated circuit device of claim 8, wherein $d = 2$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast Benes network with full bandwidth.

10. The integrated circuit device of claim 8, wherein $d = 2$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast Benes network and rearrangeably nonblocking for arbitrary fan-out multicast Benes network with full bandwidth.

11. The integrated circuit device of claim 8, wherein $d = 2$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast Benes network with full bandwidth.

12. The integrated circuit device of claim 7, wherein $y \geq (\log_2 N)$ so that the length of the horizontal shuffle exchange links in the highest stage is equal to half the size of the horizontal size of said two dimensional grid of sub-integrated circuit blocks and the length of the vertical shuffle exchange links in the highest stage is equal to half the size of the vertical size of said two dimensional grid of sub-integrated circuit blocks, and

said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks.

13. The integrated circuit device of claim 12, wherein $d = 2$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast butterfly fat tree network with full bandwidth.

14. The integrated circuit device of claim 12, wherein $d = 2$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast butterfly fat tree network and rearrangeably nonblocking for arbitrary fan-out multicast butterfly fat tree network with full bandwidth.

15. The integrated circuit device of claim 12, wherein $d = 2$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast butterfly fat tree network with full bandwidth.

16. The integrated circuit device of claim 1, wherein said horizontal and vertical links are implemented on two or more metal layers.

17. The integrated circuit device of claim 1, wherein said switches comprising active and reprogrammable cross points and said each cross point is programmable by an SRAM cell or a Flash Cell.

18. The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks are of equal die size.

19. The integrated circuit device of claim 16, wherein said sub-integrated circuit blocks are Lookup Tables (hereinafter "LUTs") and said integrated circuit device is a field programmable gate array (FPGA) device or field programmable gate array (FPGA) block embedded in another integrated circuit device.

20. The integrated circuit device of claim 16, wherein said sub-integrated circuit blocks are AND or OR gates and said integrated circuit device is a programmable logic device (PLD).

21. The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks comprising any arbitrary hardware logic or memory circuits.

22. The integrated circuit device of claim 1, wherein said switches comprising active one-time programmable cross points and said integrated circuit device is a mask programmable gate array (MPGA) device or a structured ASIC device.

23. The integrated circuit device of claim 1, wherein said switches comprising passive cross points or just connection of two links or not and said integrated circuit device is a Application Specific Integrated Circuit (ASIC) device.

24. The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks further recursively comprise one or more super-sub-integrated circuit blocks and a sub-routing network.

25. The integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and $y \geq (\log_2 N)$.

26. The integrated circuit device of claim 25, wherein $d = 2$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized multi-stage network with full bandwidth.

27. The integrated circuit device of claim 25, wherein $d = 2$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized multi-stage network and rearrangeably nonblocking for arbitrary fan-out multicast generalized multi-stage network with full bandwidth.

28. The integrated circuit device of claim 25, wherein $d = 2$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized multi-stage network with full bandwidth.

29. The integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and $y \geq (\log_2 N)$, and

said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks.

30. The integrated circuit device of claim 29, wherein $d = 2$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized butterfly fat tree network with full bandwidth.

31. The integrated circuit device of claim 29, wherein $d = 2$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized butterfly fat tree Network and rearrangeably nonblocking for arbitrary fan-out multicast generalized butterfly fat tree network with full bandwidth.

32. The integrated circuit device of claim 29, wherein $d = 2$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized butterfly fat tree network with full bandwidth.

33. The integrated circuit device of claim 1, wherein said straight links connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and

said cross links are connecting as vertical or horizontal or diagonal links between two different said sub-integrated circuit blocks.

34. The integrated circuit device of claim 8, wherein $d = 4$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast multi-link Benes network with full bandwidth.

35. The integrated circuit device of claim 8, wherein $d = 4$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast multi-link Benes network and rearrangeably nonblocking for arbitrary fan-out multicast multi-link Benes network with full bandwidth.

36. The integrated circuit device of claim 8, wherein $d = 4$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast multi-link Benes network with full bandwidth.

37. The integrated circuit device of claim 12, wherein $d = 4$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast multi-link butterfly fat tree network with full bandwidth.

38. The integrated circuit device of claim 12, wherein $d = 4$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in

each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast multi-link butterfly fat tree network and rearrangeably nonblocking for arbitrary fan-out multicast multi-link butterfly fat tree network with full bandwidth.

39. The integrated circuit device of claim 12, wherein $d = 4$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast multi-link butterfly fat tree network with full bandwidth.

40. The integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and $y \geq (\log_2 N)$.

41. The integrated circuit device of claim 40, wherein $d = 4$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized multi-link multi-stage network with full bandwidth.

42. The integrated circuit device of claim 40, wherein $d = 4$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized multi-link multi-stage network and rearrangeably nonblocking for arbitrary fan-out multicast generalized multi-link multi-stage network with full bandwidth.

43. The integrated circuit device of claim 40, wherein $d = 4$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized multi-link multi-stage network with full bandwidth.

44. The integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and $y \geq (\log_2 N)$, and

said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks.

45. The integrated circuit device of claim 44, wherein $d = 4$ and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized multi-link butterfly fat tree network with full bandwidth.

46. The integrated circuit device of claim 44, wherein $d = 4$ and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized multi-link butterfly fat tree Network and rearrangeably nonblocking for arbitrary fan-out multicast generalized multi-link butterfly fat tree network with full bandwidth.

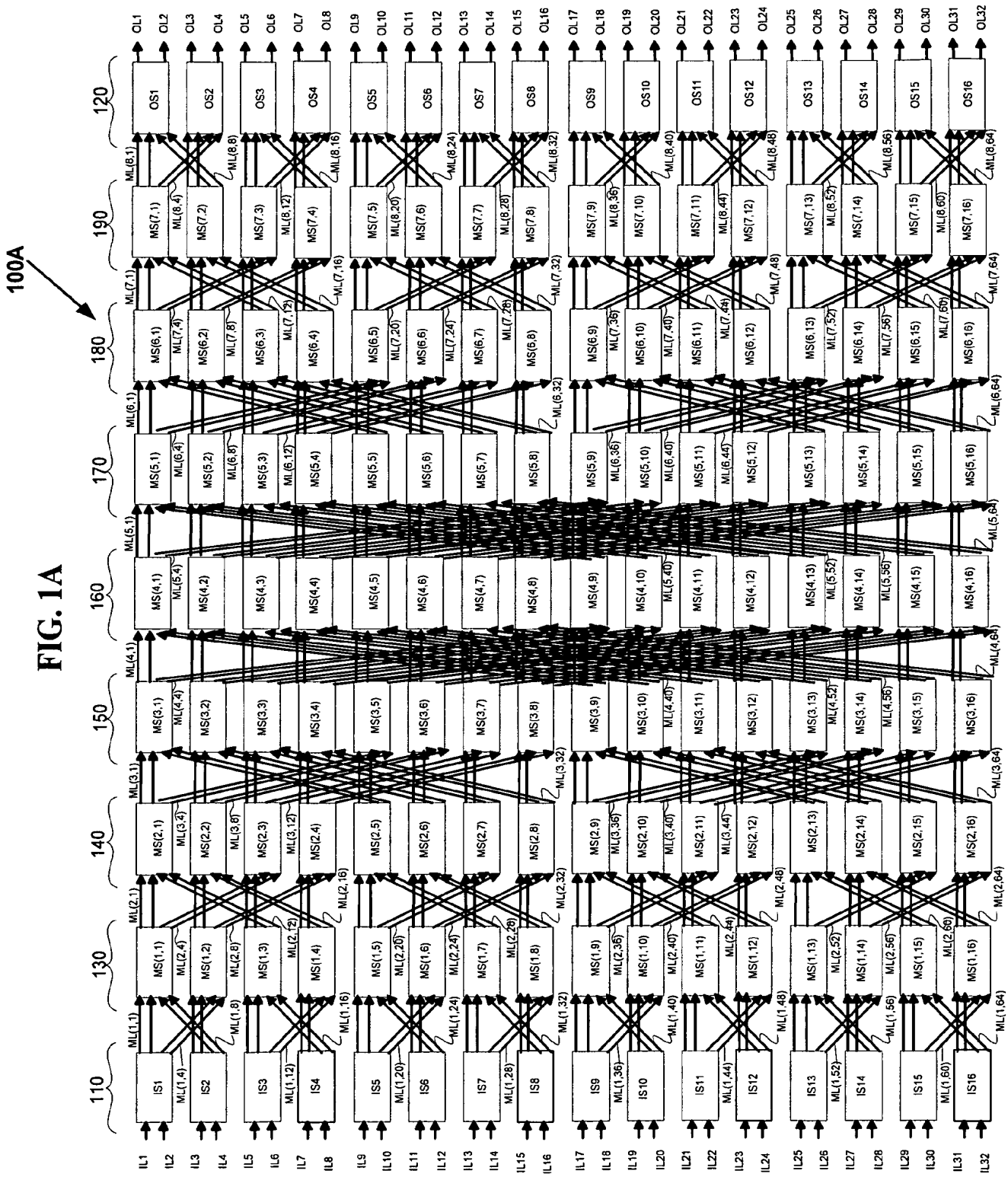
47. The integrated circuit device of claim 44, wherein $d = 4$ and there are at least three switches in each said stage in each said sub-integrated circuit block connecting

said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized multi-link butterfly fat tree network with full bandwidth.

48. The integrated circuit device of claim 1, wherein said plurality of forward connecting links use a plurality of buffers to amplify signals driven through them and said plurality of backward connecting links use a plurality of buffers to amplify signals driven through them; and said buffers can be inverting or non-inverting buffers.

49. The integrated circuit device of claim 1, wherein said wherein said all switches of size $d \times d$ are either fully populated or partially populated.

FIG. 1A


100A
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120
130
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IL1
IL2
IL3
IL4
IL5
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IL7
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OS2
OS3
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OS14
OS15
OS16

FIG. 1B

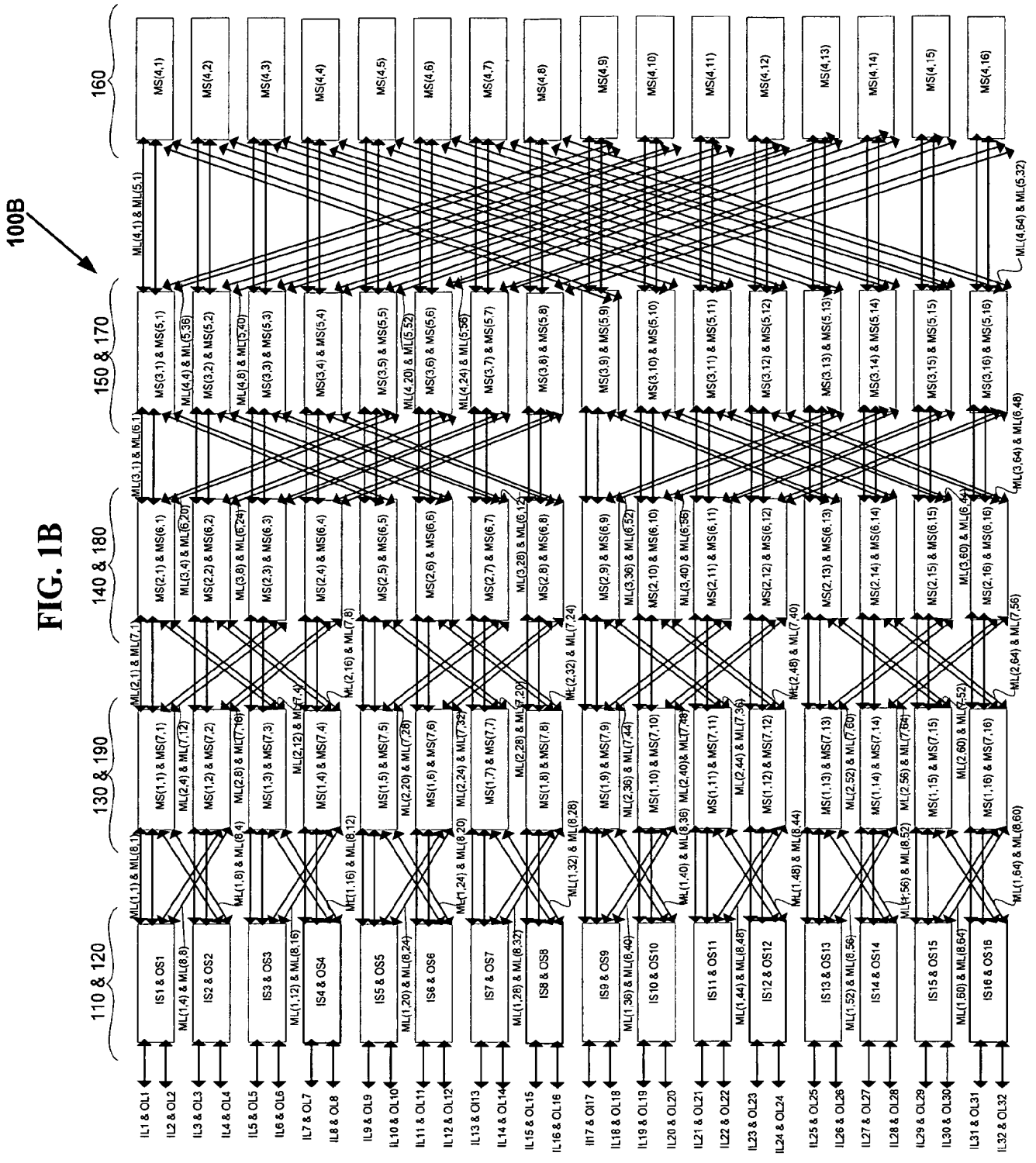

100B
110 & 120
130 & 190
140 & 180
150 & 170
160
IL1 & OL1
IL2 & OL2
IL3 & OL3
IL4 & OL4
IL5 & OL5
IL6 & OL6
IL7 & OL7
IL8 & OL8
IL9 & OL9
IL10 & OL10
IL11 & OL11
IL12 & OL12
IL13 & OI13
IL14 & OL14
IL15 & OL15
IL16 & OL16
II17 & OI17
IL18 & OL18
IL19 & OL19
IL20 & OL20
IL21 & OL21
IL22 & OL22
IL23 & OL23
IL24 & OL24
IL25 & OL25
IL26 & OL26
IL27 & OL27
IL28 & OL28
IL29 & OL29
IL30 & OL30
IL31 & OL31
IL32 & OL32
IS1 & OS1
IS2 & OS2
IS3 & OS3
IS4 & OS4
IS5 & OS5
IS6 & OS6
IS7 & OS7
IS8 & OS8
IS9 & OS9
IS10 & OS10
IS11 & OS11
IS12 & OS12
IS13 & OS13
IS14 & OS14
IS15 & OS15
IS16 & OS16
MS(1,1) & MS(7,1)
MS(1,2) & MS(7,2)
MS(1,3) & MS(7,3)
MS(1,4) & MS(7,4)
MS(1,5) & MS(7,5)
MS(1,6) & MS(7,6)
MS(1,7) & MS(7,7)
MS(1,8) & MS(7,8)
MS(1,9) & MS(7,9)
MS(1,10) & MS(7,10)
MS(1,11) & MS(7,11)
MS(1,12) & MS(7,12)
MS(1,13) & MS(7,13)
MS(1,14) & MS(7,14)
MS(1,15) & MS(7,15)
MS(1,16) & MS(7,16)
MS(2,1) & MS(6,1)
MS(2,2) & MS(6,2)
MS(2,3) & MS(6,3)
MS(2,4) & MS(6,4)
MS(2,5) & MS(6,5)
MS(2,6) & MS(6,6)
MS(2,7) & MS(6,7)
MS(2,8) & MS(6,8)
MS(2,9) & MS(6,9)
MS(2,10) & MS(6,10)
MS(2,11) & MS(6,11)
MS(2,12) & MS(6,12)
MS(2,13) & MS(6,13)
MS(2,14) & MS(6,14)
MS(2,15) & MS(6,15)
MS(2,16) & MS(6,16)
MS(3,1) & MS(5,1)
MS(3,2) & MS(5,2)
MS(3,3) & MS(5,3)
MS(3,4) & MS(5,4)
MS(3,5) & MS(5,5)
MS(3,6) & MS(5,6)
MS(3,7) & MS(5,7)
MS(3,8) & MS(5,8)
MS(3,9) & MS(5,9)
MS(3,10) & MS(5,10)
MS(3,11) & MS(5,11)
MS(3,12) & MS(5,12)
MS(3,13) & MS(5,13)
MS(3,14) & MS(5,14)
MS(3,15) & MS(5,15)
MS(3,16) & MS(5,16)
MS(4,1)
MS(4,2)
MS(4,3)
MS(4,4)
MS(4,5)
MS(4,6)
MS(4,7)
MS(4,8)
MS(4,9)
MS(4,10)
MS(4,11)
MS(4,12)
MS(4,13)
MS(4,14)
MS(4,15)
MS(4,16)

FIG. 1C

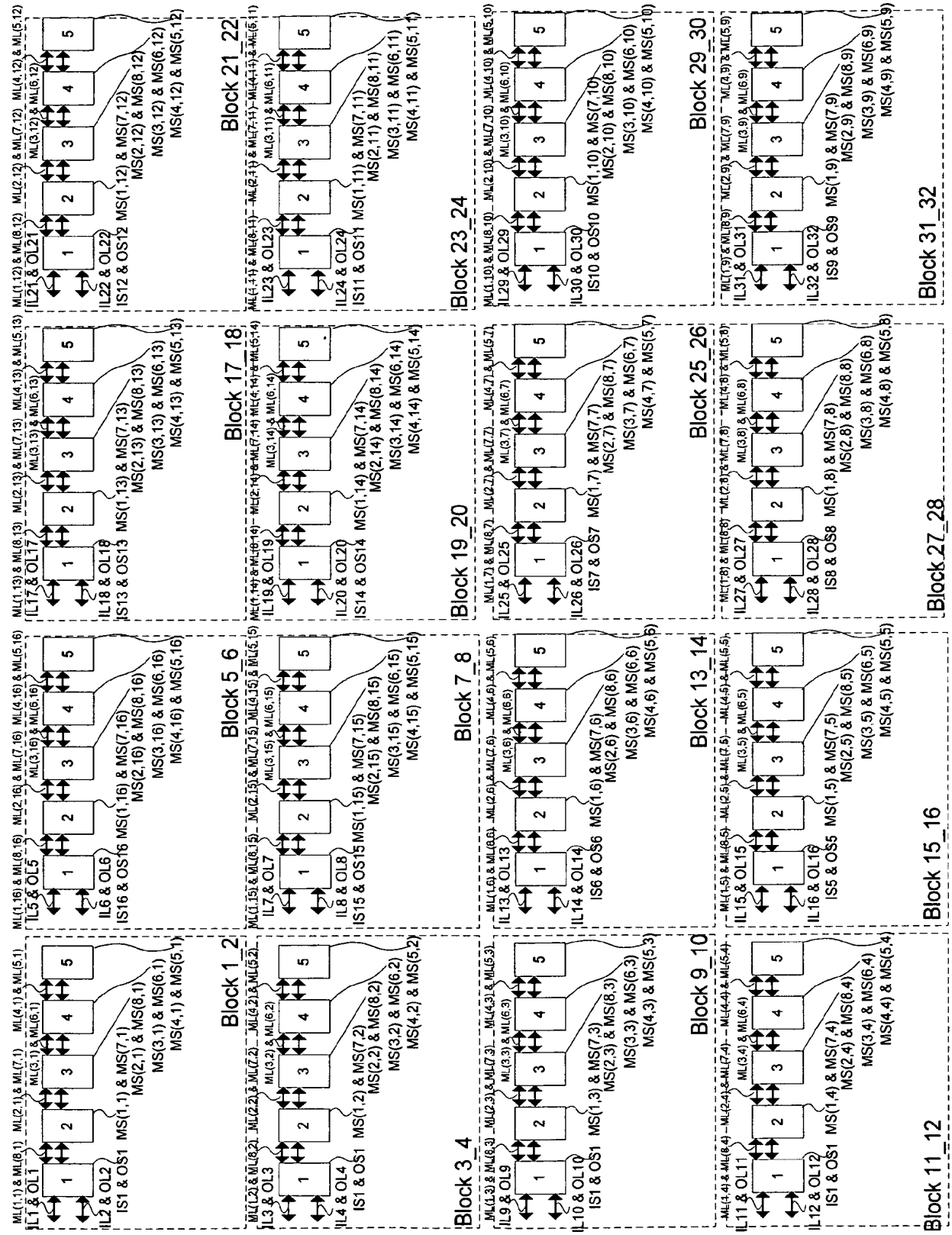

100C
Block 1_2
Block 3_4
Block 5_6
Block 7_8
Block 9_10
Block 11_12
Block 13_14
Block 15_16
Block 17_18
Block 19_20
Block 21_22
Block 23_24
Block 25_26
Block 27_28
Block 29_30
Block 31_32

FIG. 1D

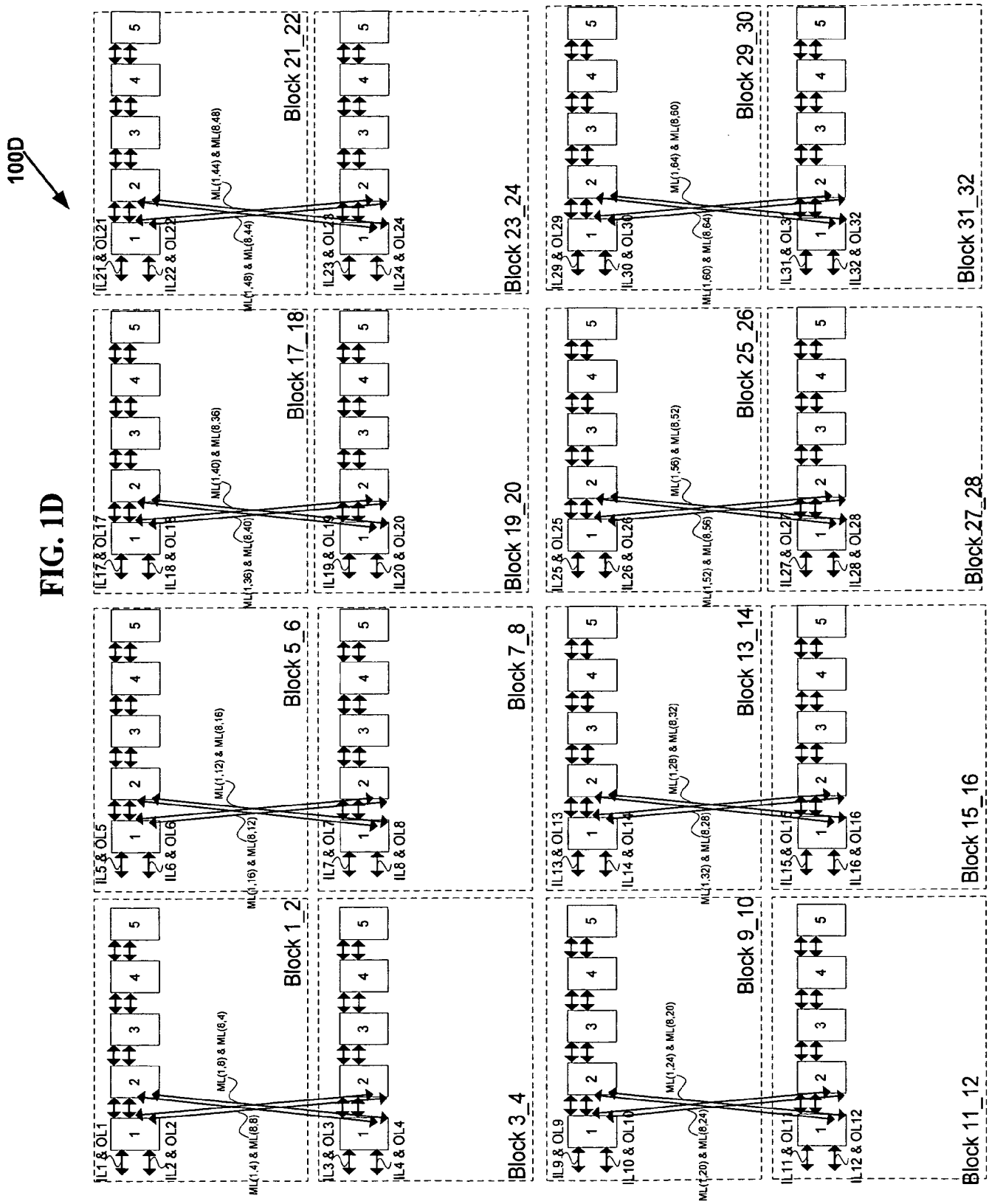

100D
Block 1_2
Block 3_4
Block 5_6
Block 7_8
Block 9_10
Block 11_12
Block 13_14
Block 15_16
Block 17_18
Block 19_20
Block 21_22
Block 23_24
Block 25_26
Block 27_28
Block 29_30
Block 31_32

FIG. 1E

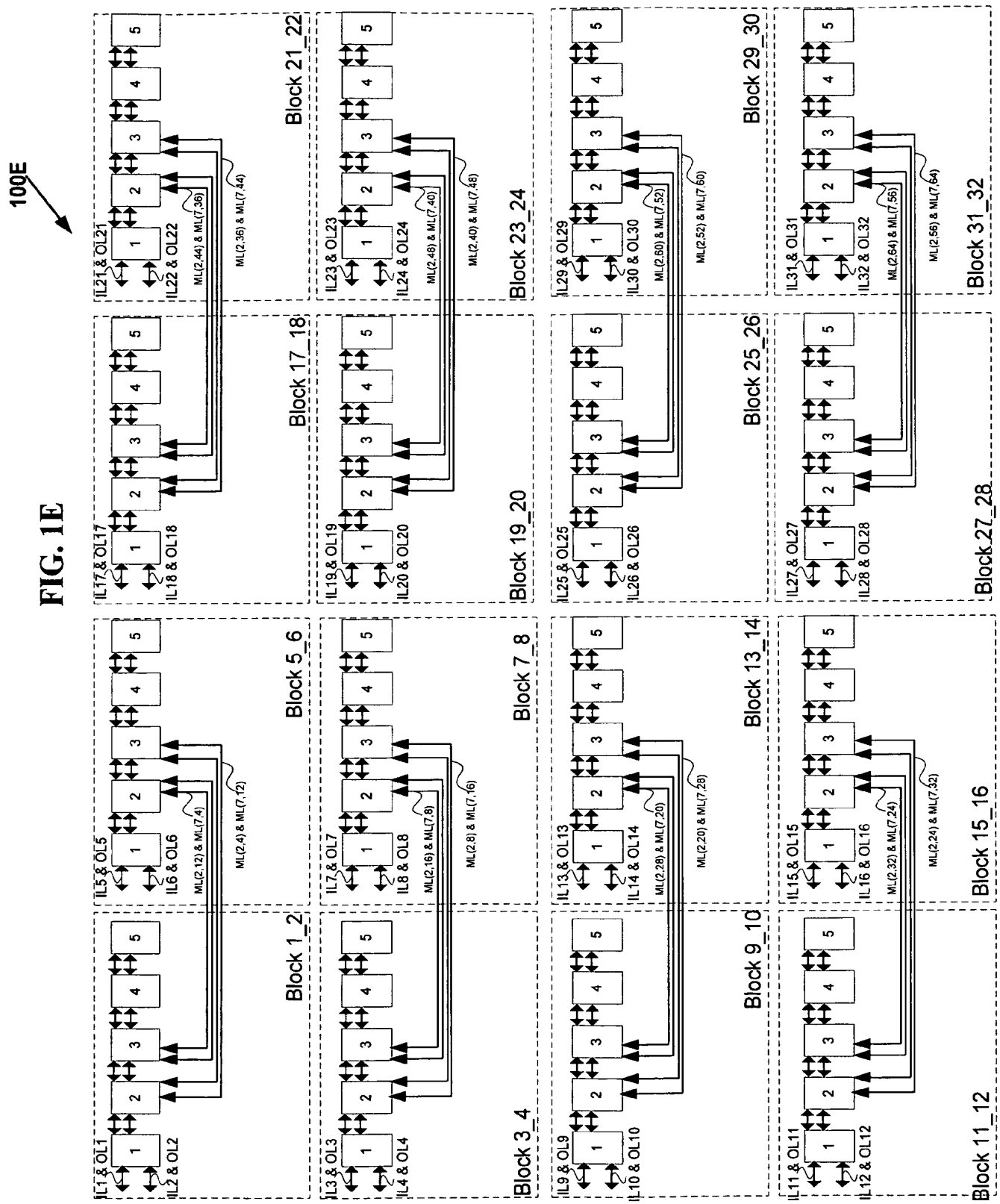

100E
Block 1_2
Block 3_4
Block 5_6
Block 7_8
Block 9_10
Block 11_12
Block 13_14
Block 15_16
Block 17_18
Block 19_20
Block 21_22
Block 23_24
Block 25_26
Block 27_28
Block 29_30
Block 31_32
IL1 & OL1
IL2 & OL2
IL3 & OL3
IL4 & OL4
IL5 & OL5
IL6 & OL6
IL7 & OL7
IL8 & OL8
IL9 & OL9
IL10 & OL10
IL11 & OL11
IL12 & OL12
IL13 & OL13
IL14 & OL14
IL15 & OL15
IL16 & OL16
IL17 & OL17
IL18 & OL18
IL19 & OL19
IL20 & OL20
IL21 & OL21
IL22 & OL22
IL23 & OL23
IL24 & OL24
IL25 & OL25
IL26 & OL26
IL27 & OL27
IL28 & OL28
IL29 & OL29
IL30 & OL30
IL31 & OL31
IL32 & OL32
ML(2,4) & ML(7,12)
ML(2,12) & ML(7,4)
ML(2,8) & ML(7,16)
ML(2,16) & ML(7,8)
ML(2,20) & ML(7,28)
ML(2,28) & ML(7,20)
ML(2,24) & ML(7,32)
ML(2,32) & ML(7,24)
ML(2,36) & ML(7,44)
ML(2,44) & ML(7,36)
ML(2,40) & ML(7,48)
ML(2,48) & ML(7,40)
ML(2,52) & ML(7,60)
ML(2,60) & ML(7,52)
ML(2,56) & ML(7,64)
ML(2,64) & ML(7,56)

FIG. 1F

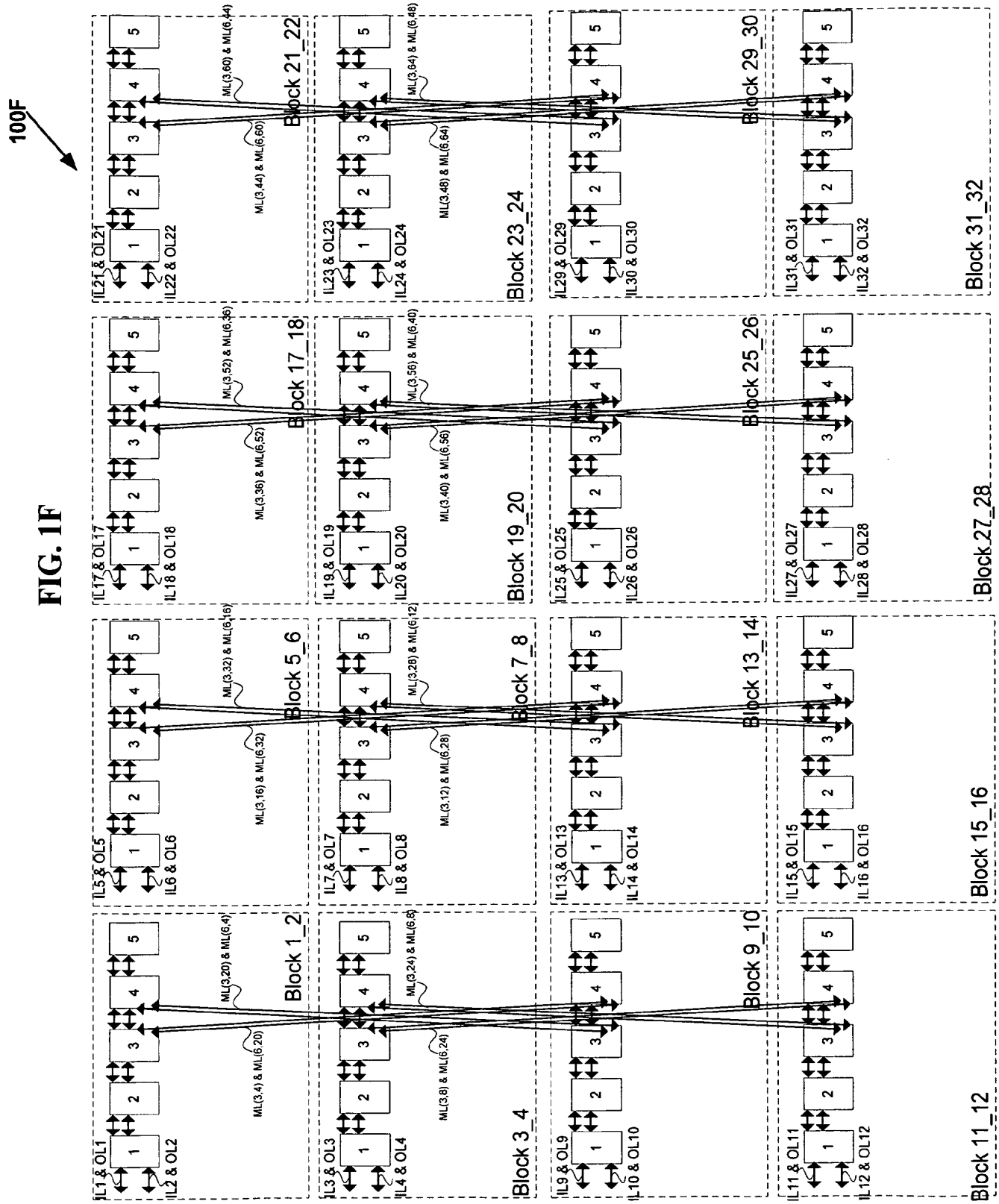

100F
Block 1_2
Block 3_4
Block 5_6
Block 7_8
Block 9_10
Block 11_12
Block 13_14
Block 15_16
Block 17_18
Block 19_20
Block 21_22
Block 23_24
Block 25_26
Block 27_28
Block 29_30
Block 31_32

FIG. 1G

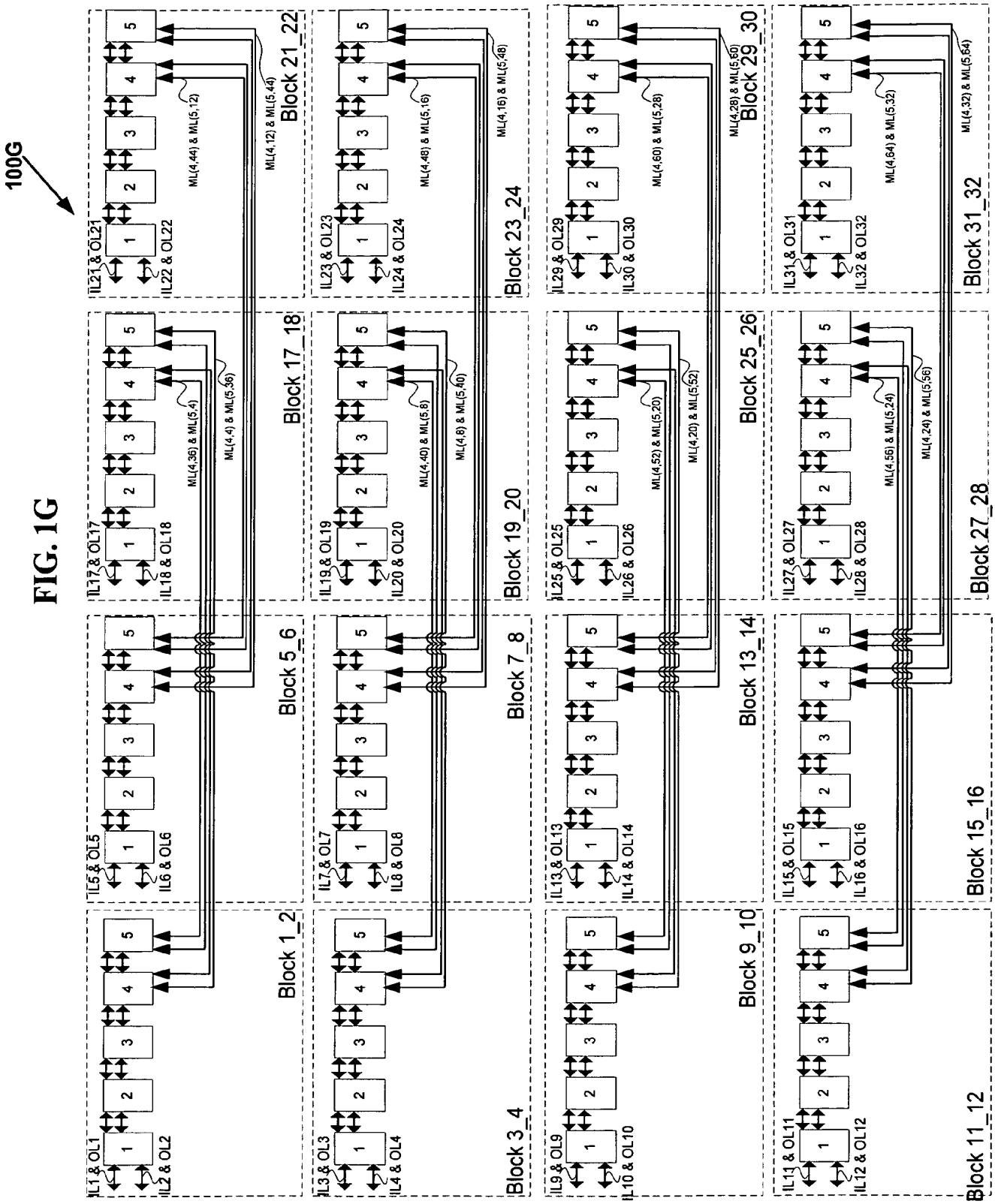

100G
Block 1_2
Block 3_4
Block 5_6
Block 7_8
Block 9_10
Block 11_12
Block 13_14
Block 15_16
Block 17_18
Block 19_20
Block 21_22
Block 23_24
Block 25_26
Block 27_28
Block 29_30
Block 31_32

FIG. 1H

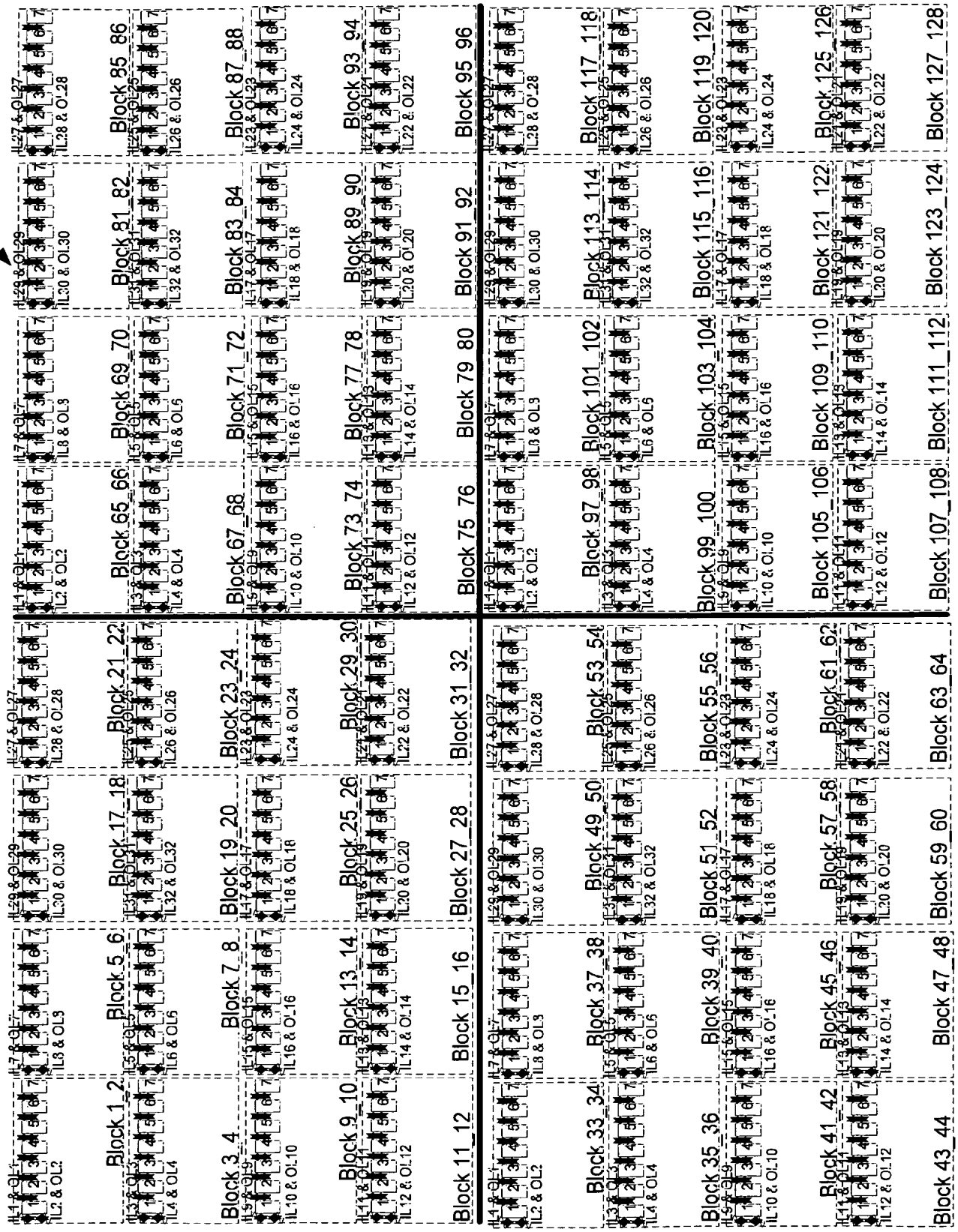
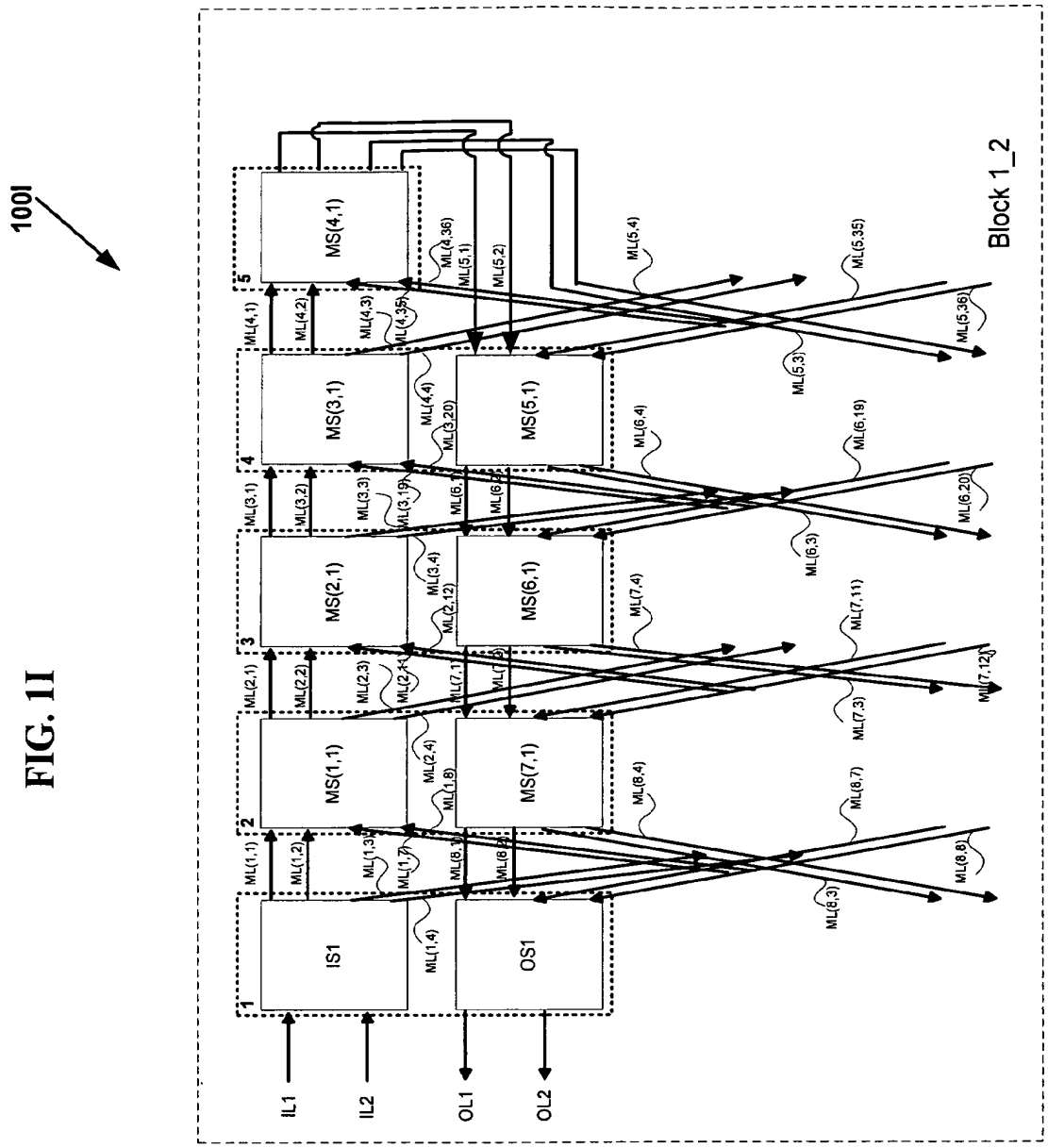

100H
Block 1_2
Block 3_4
Block 5_6
Block 7_8
Block 9_10
Block 11_12
Block 13_14
Block 15_16
Block 17_18
Block 19_20
Block 21_22
Block 23_24
Block 25_26
Block 27_28
Block 29_30
Block 31_32
Block 33_34
Block 35_36
Block 37_38
Block 39_40
Block 41_42
Block 43_44
Block 45_46
Block 47_48
Block 49_50
Block 51_52
Block 53_54
Block 55_56
Block 57_58
Block 59_60
Block 61_62
Block 63_64
Block 65_66
Block 67_68
Block 69_70
Block 71_72
Block 73_74
Block 75_76
Block 77_78
Block 79_80
Block 81_82
Block 83_84
Block 85_86
Block 87_88
Block 89_90
Block 91_92
Block 93_94
Block 95_96
Block 97_98
Block 99_100
Block 101_102
Block 103_104
Block 105_106
Block 107_108
Block 109_110
Block 111_112
Block 113_114
Block 115_116
Block 117_118
Block 119_120
Block 121_122
Block 123_124
Block 125_126
Block 127_128

FIG. 1I


100I
Block 1_2
IS1
OS1
MS(1,1)
MS(2,1)
MS(3,1)
MS(4,1)
MS(5,1)
MS(6,1)
MS(7,1)
IL1
IL2
OL1
OL2

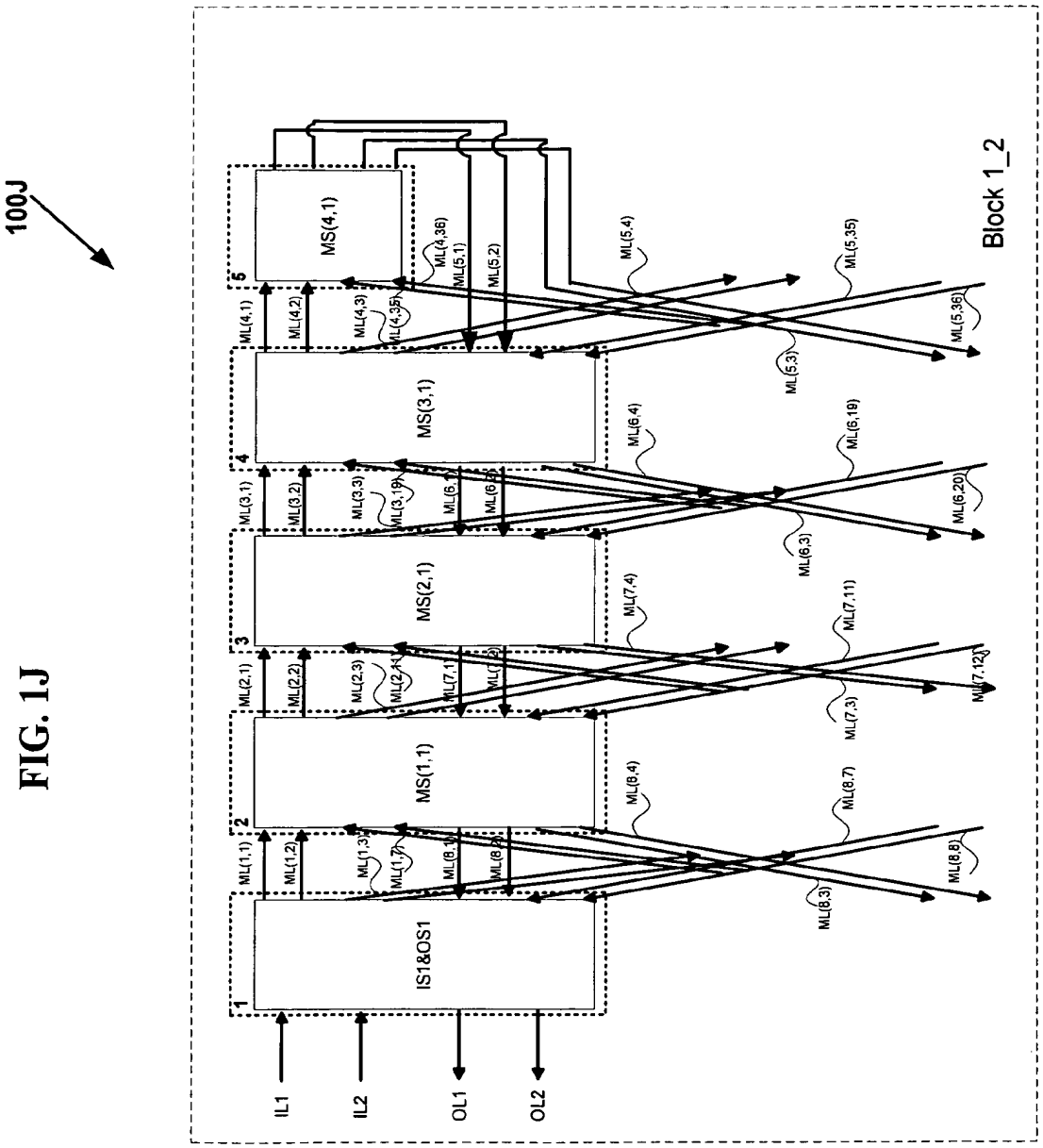


FIG. 1J

FIG. 1K

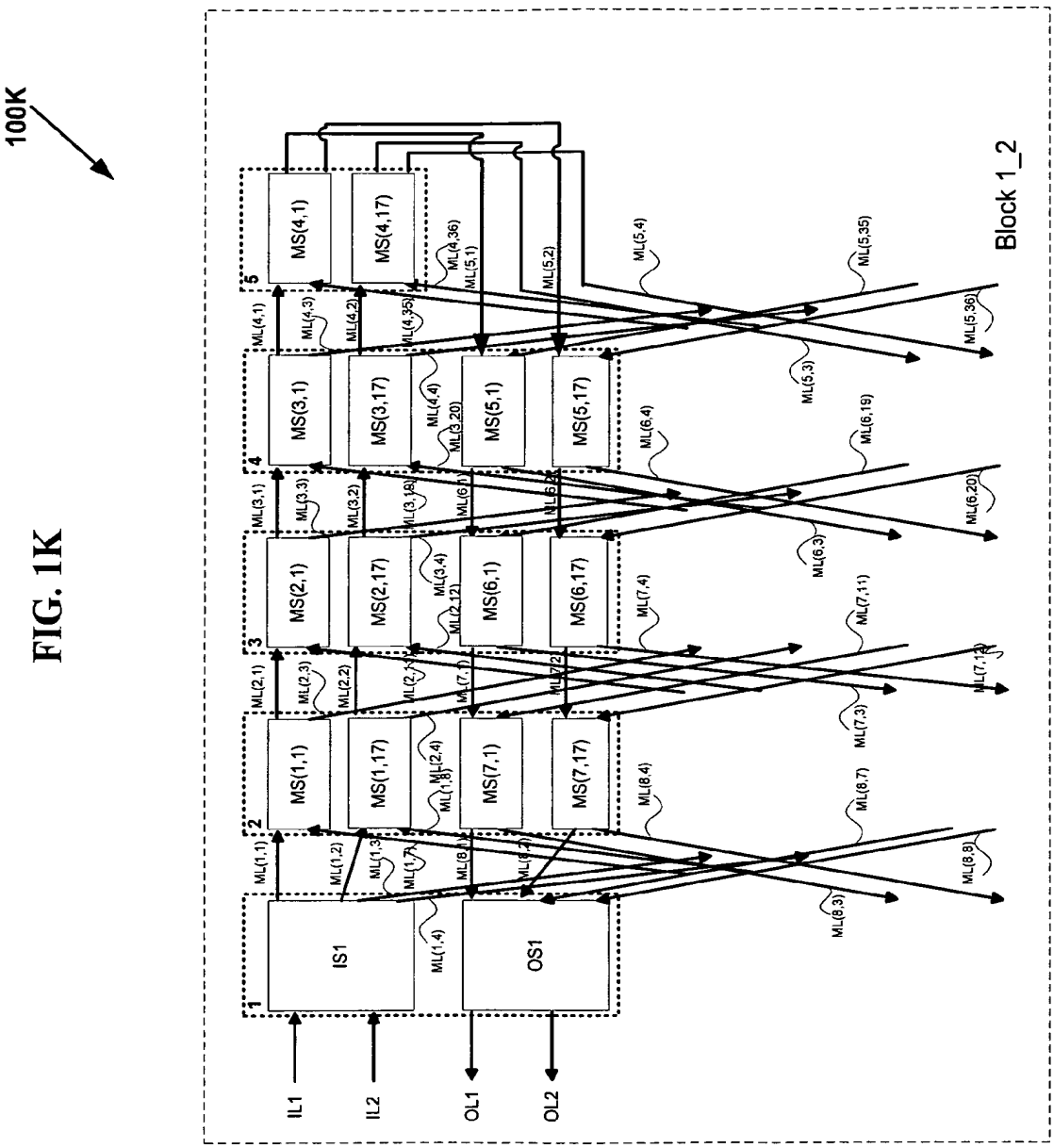
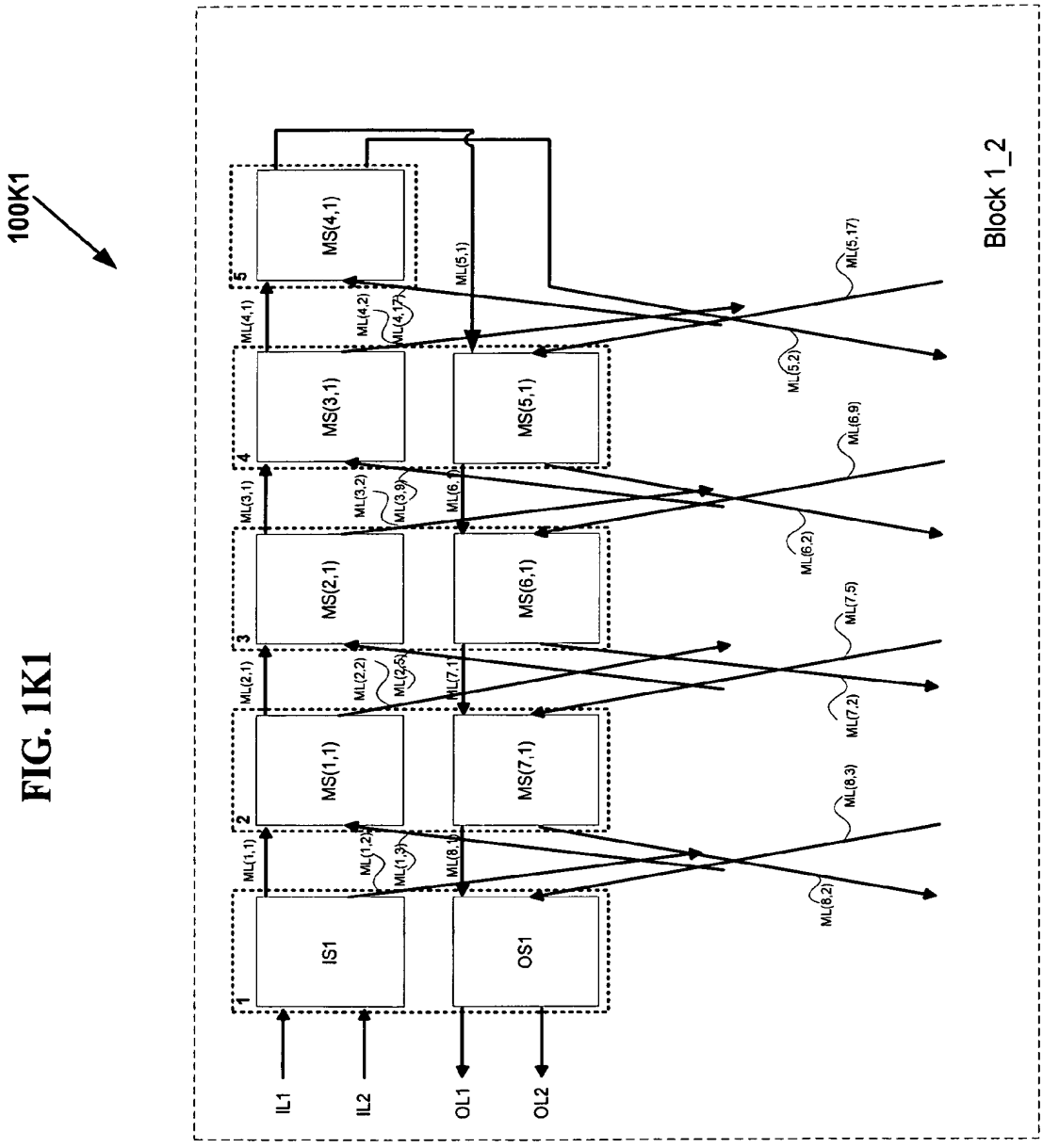

100K
Block 1_2
IL1
IL2
OL1
OL2
IS1
OS1
MS(1,1)
MS(1,17)
MS(2,1)
MS(2,17)
MS(3,1)
MS(3,17)
MS(4,1)
MS(4,17)
MS(5,1)
MS(5,17)
MS(6,1)
MS(6,17)
MS(7,1)
MS(7,17)

FIG. 1K1


100K1
Block 1_2
IS1
OS1
MS(1,1)
MS(7,1)
MS(2,1)
MS(6,1)
MS(3,1)
MS(5,1)
MS(4,1)
IL1
IL2
OL1
OL2
ML(1,1)
ML(1,2)
ML(1,3)
ML(8,1)
ML(2,1)
ML(2,2)
ML(2,5)
ML(7,1)
ML(3,1)
ML(3,2)
ML(3,9)
ML(6,1)
ML(4,1)
ML(4,2)
ML(4,17)
ML(5,1)
ML(5,17)
ML(5,2)
ML(6,9)
ML(6,2)
ML(7,5)
ML(7,2)
ML(8,3)
ML(8,2)

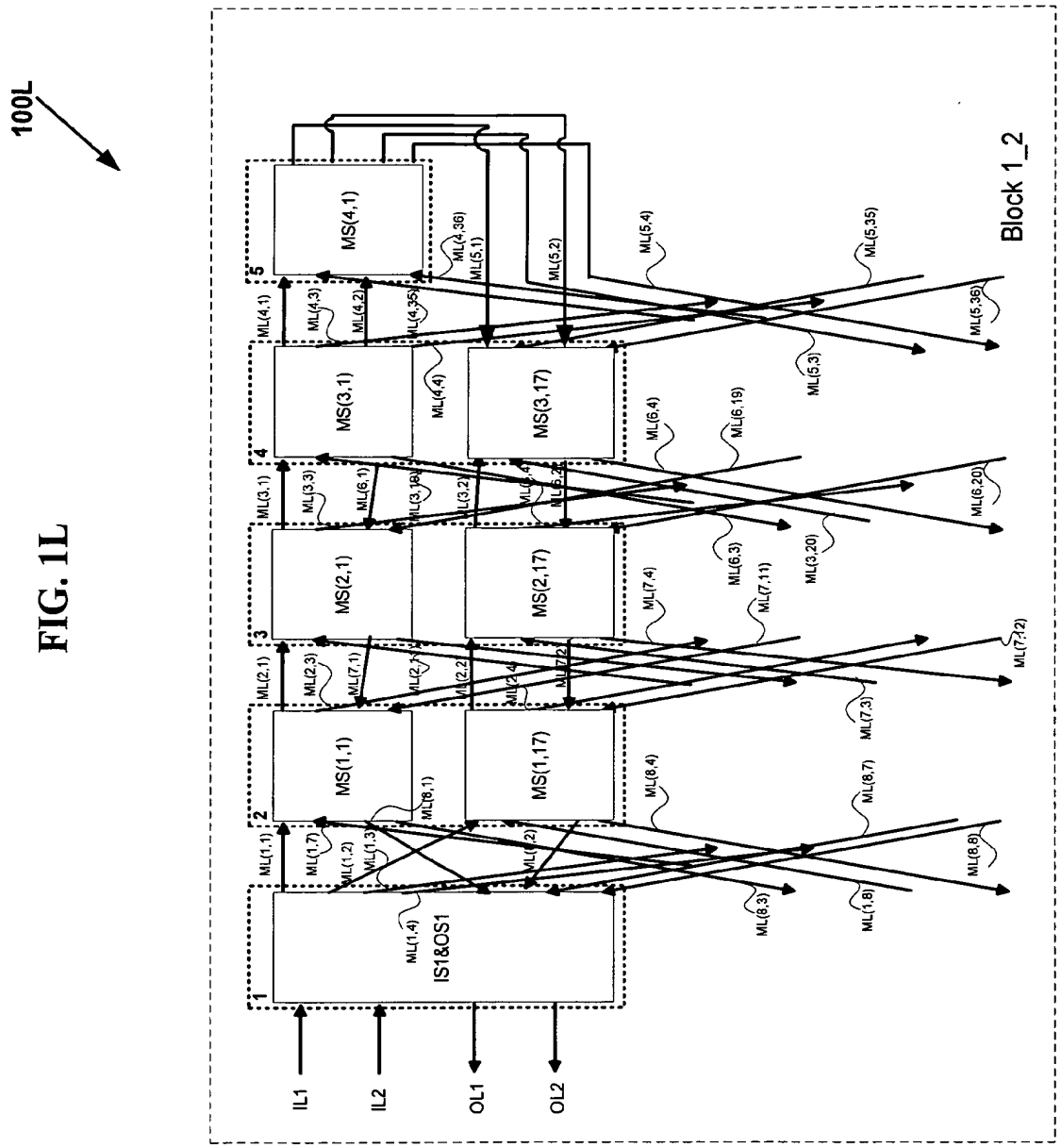

100L
Block 1_2
IS1&OS1
MS(1,1)
MS(1,17)
MS(2,1)
MS(2,17)
MS(3,1)
MS(3,17)
MS(4,1)
IL1
IL2
OL1
OL2

FIG. 1L

FIG. 1L1

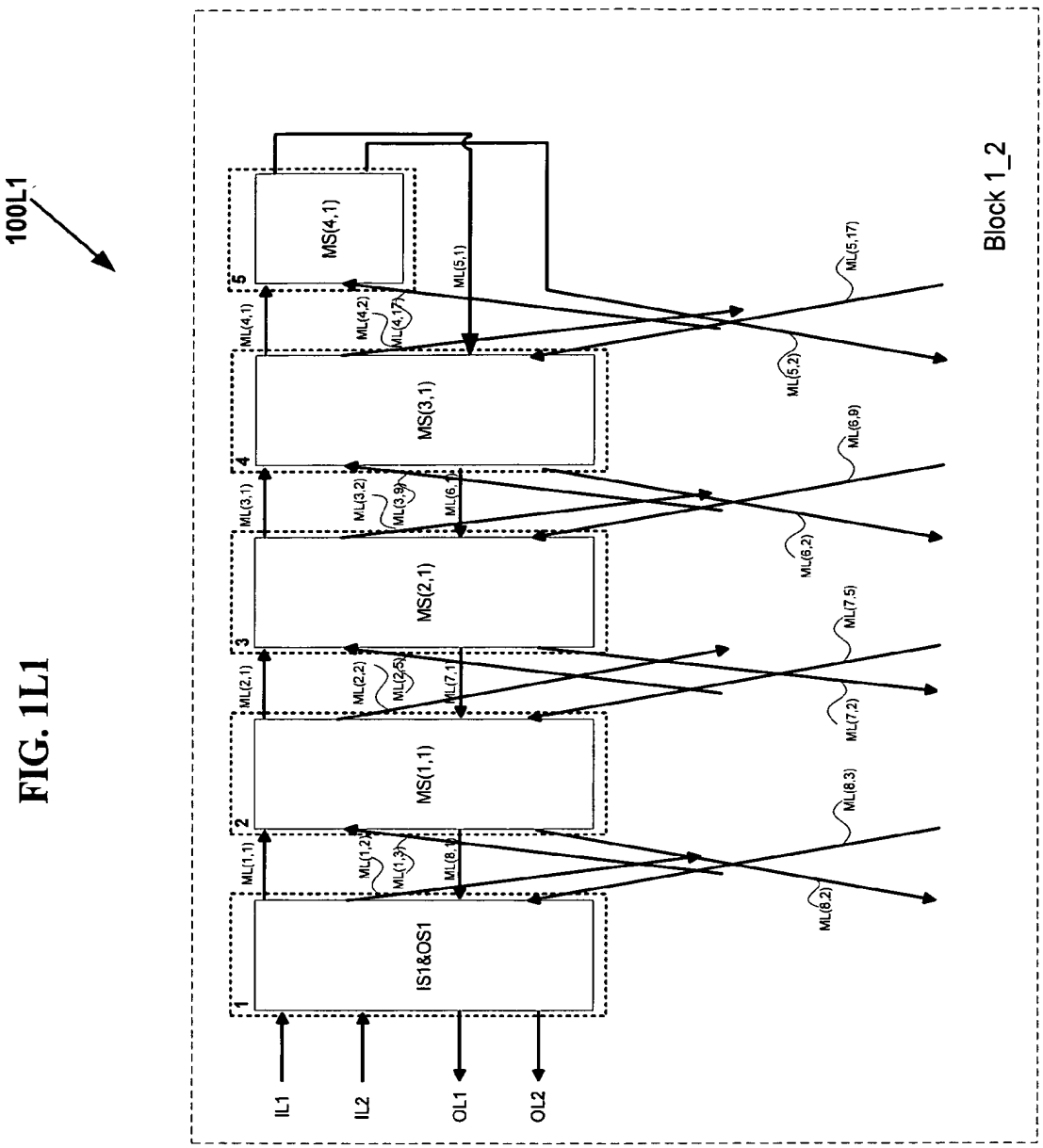

100L1
Block 1_2
IS1&OS1
MS(1,1)
MS(2,1)
MS(3,1)
MS(4,1)
IL1
IL2
OL1
OL2
ML(1,1)
ML(2,1)
ML(3,1)
ML(4,1)
ML(5,1)
ML(5,17)
ML(5,2)
ML(6,9)
ML(6,2)
ML(7,5)
ML(7,2)
ML(8,3)
ML(8,2)

FIG. 2A1

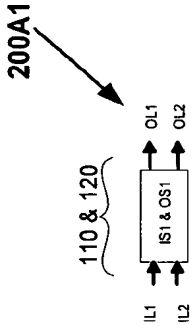


FIG. 2A2

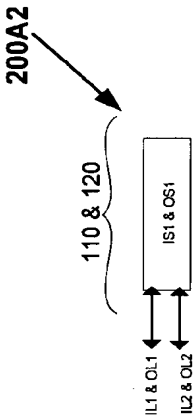


FIG. 2A3

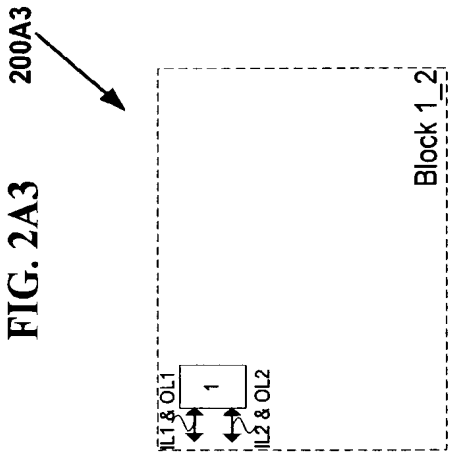


FIG. 2B1

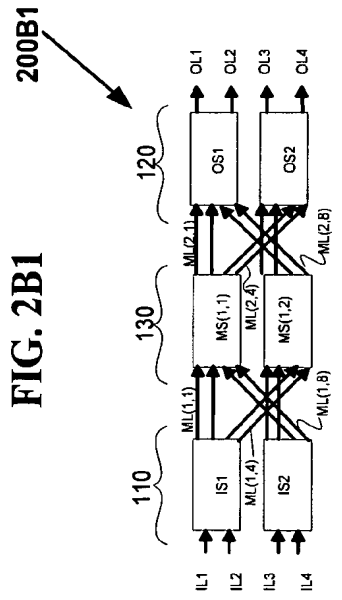


FIG. 2B2

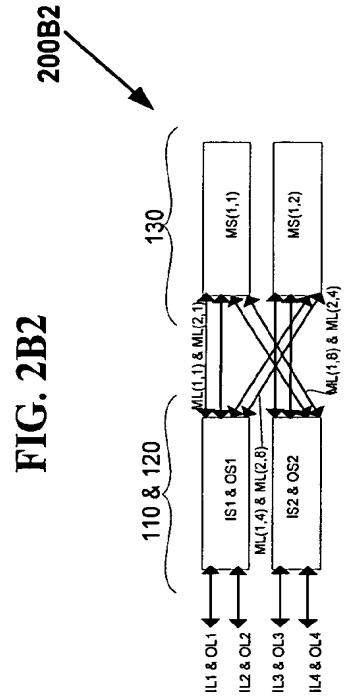


FIG. 2B3

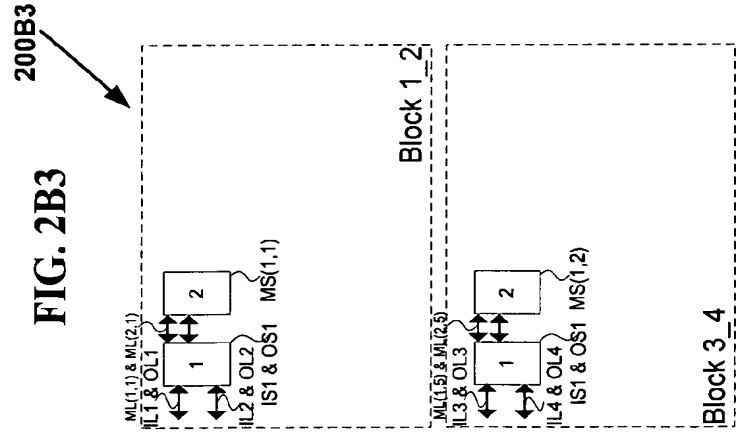


FIG. 2B4

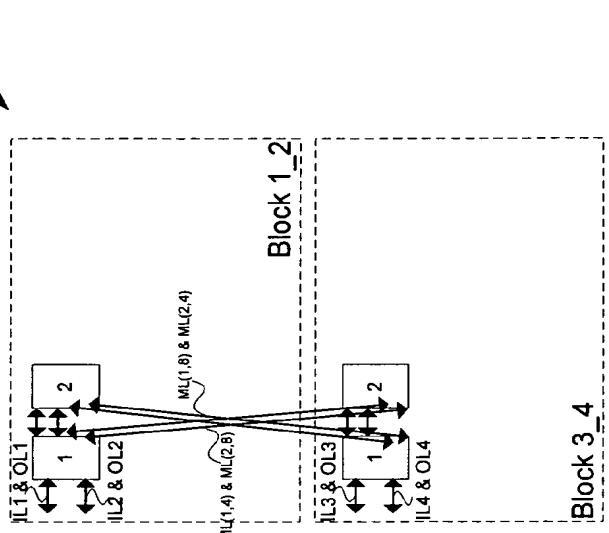


FIG. 2C11

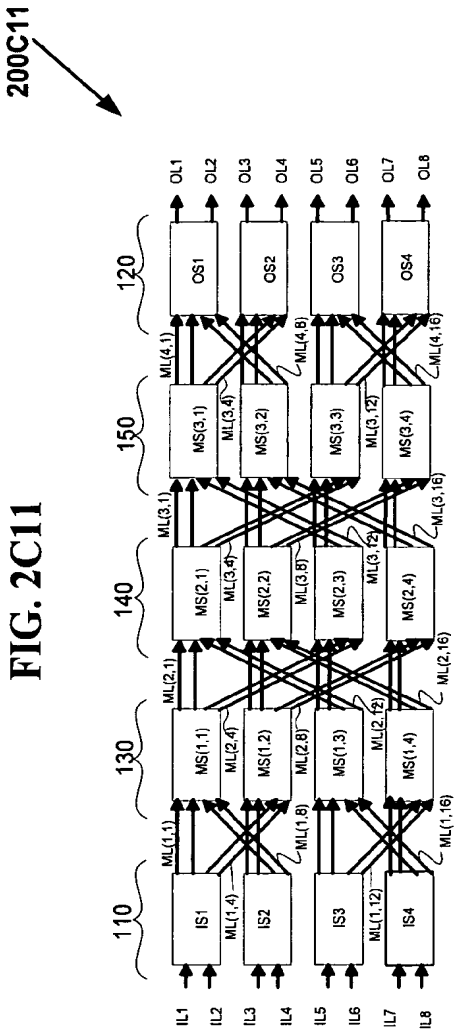


FIG. 2C12

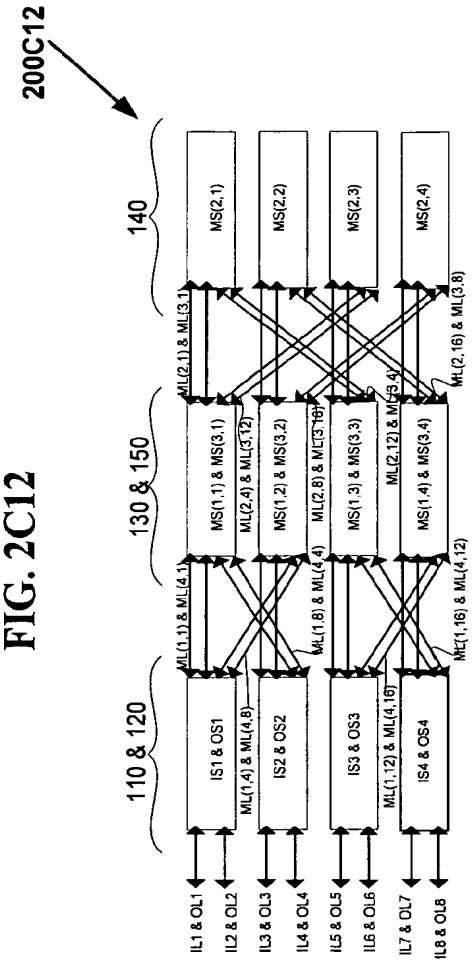


FIG. 2C21

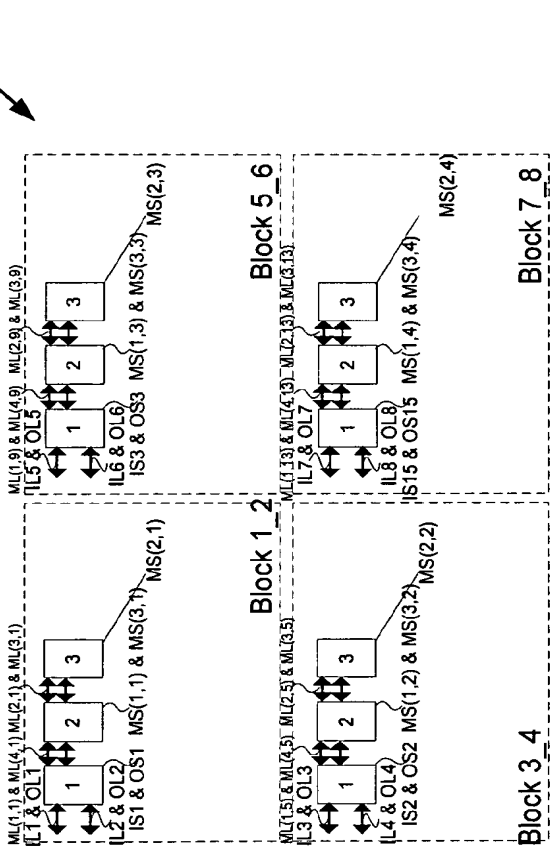


FIG. 2C22

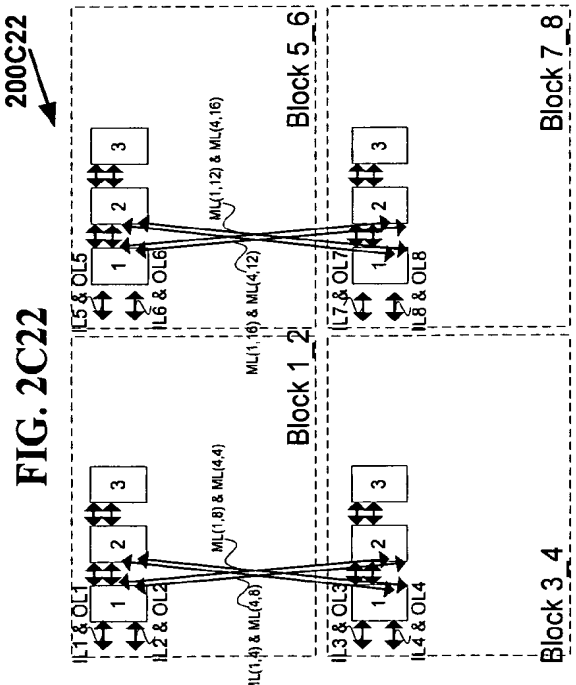


FIG. 2C23

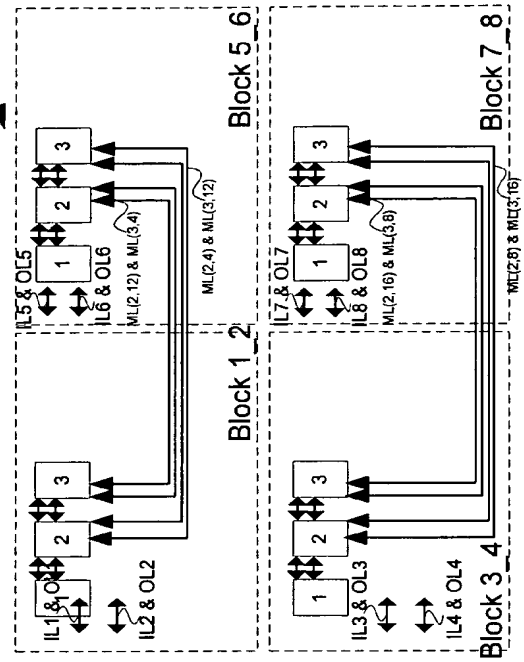
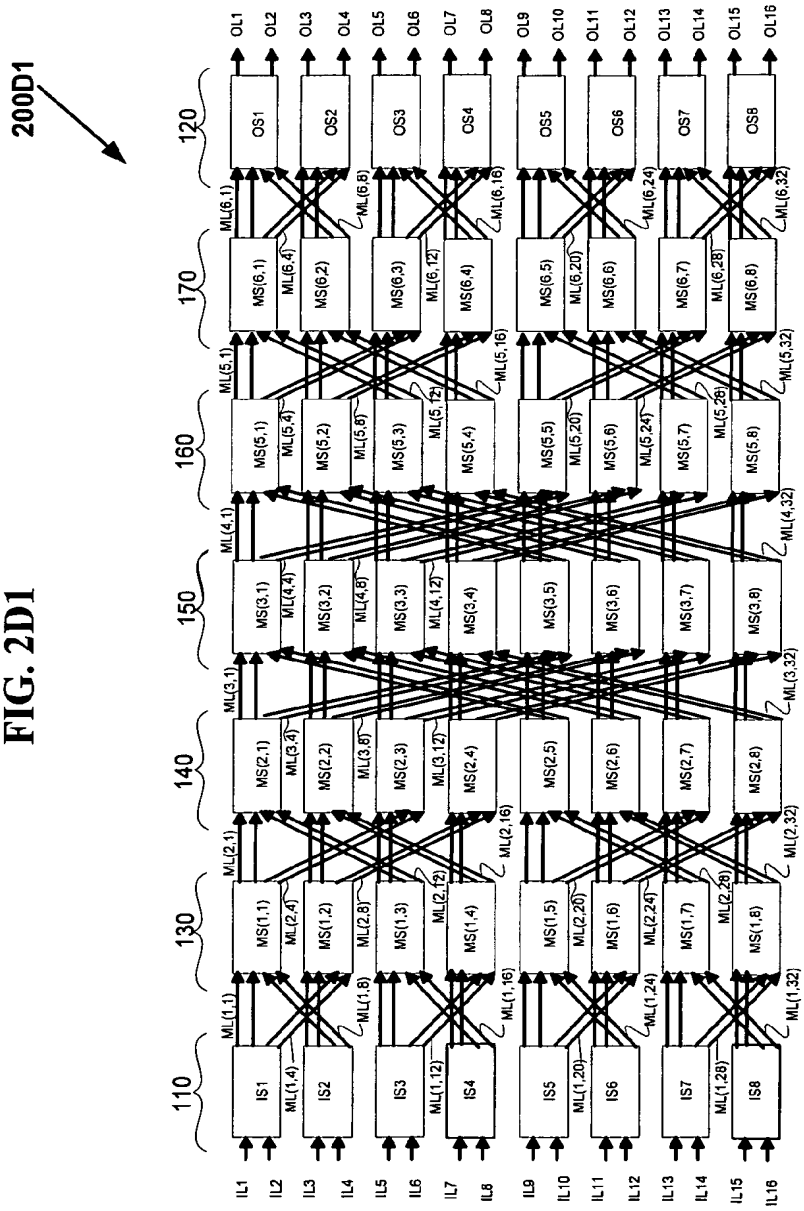


FIG. 2D1


200D1
110
120
130
140
150
160
170
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
IL9
IL10
IL11
IL12
IL13
IL14
IL15
IL16
IS1
IS2
IS3
IS4
IS5
IS6
IS7
IS8
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
OL9
OL10
OL11
OL12
OL13
OL14
OL15
OL16
OS1
OS2
OS3
OS4
OS5
OS6
OS7
OS8
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ML(1,4)
ML(1,8)
ML(1,12)
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ML(1,20)
ML(1,24)
ML(1,28)
ML(1,32)
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ML(2,4)
ML(2,8)
ML(2,12)
ML(2,16)
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ML(3,4)
ML(3,8)
ML(3,12)
ML(3,16)
ML(3,20)
ML(3,24)
ML(3,28)
ML(3,32)
ML(4,1)
ML(4,4)
ML(4,8)
ML(4,12)
ML(4,16)
ML(4,20)
ML(4,24)
ML(4,28)
ML(4,32)
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ML(5,4)
ML(5,8)
ML(5,12)
ML(5,16)
ML(5,20)
ML(5,24)
ML(5,28)
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ML(6,4)
ML(6,8)
ML(6,12)
ML(6,16)
ML(6,20)
ML(6,24)
ML(6,28)
ML(6,32)
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(1,5)
MS(1,6)
MS(1,7)
MS(1,8)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(2,5)
MS(2,6)
MS(2,7)
MS(2,8)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
MS(3,5)
MS(3,6)
MS(3,7)
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MS(5,2)
MS(5,3)
MS(5,4)
MS(5,5)
MS(5,6)
MS(5,7)
MS(5,8)
MS(6,1)
MS(6,2)
MS(6,3)
MS(6,4)
MS(6,5)
MS(6,6)
MS(6,7)
MS(6,8)

FIG. 2D2

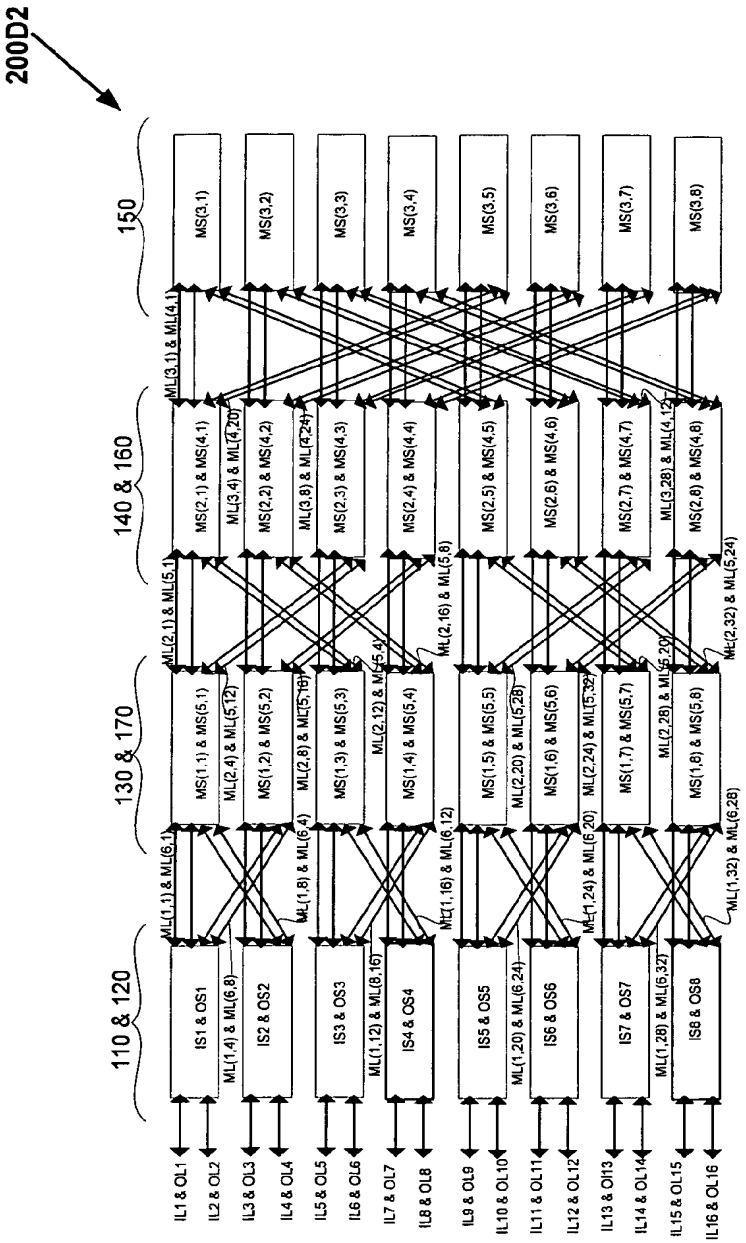

200D2
110 & 120
130 & 170
140 & 160
150
IL1 & OL1
IL2 & OL2
IL3 & OL3
IL4 & OL4
IL5 & OL5
IL6 & OL6
IL7 & OL7
IL8 & OL8
IL9 & OL9
IL10 & OL10
IL11 & OL11
IL12 & OL12
IL13 & OI13
IL14 & OL14
IL15 & OL15
IL16 & OL16
IS1 & OS1
IS2 & OS2
IS3 & OS3
IS4 & OS4
IS5 & OS5
IS6 & OS6
IS7 & OS7
IS8 & OS8
MS(1,1) & MS(6,1)
MS(1,2) & MS(5,2)
MS(1,3) & MS(5,3)
MS(1,4) & MS(5,4)
MS(1,5) & MS(6,5)
MS(1,6) & MS(5,6)
MS(1,7) & MS(5,7)
MS(1,8) & MS(5,8)
MS(2,1) & MS(4,1)
MS(2,2) & MS(4,2)
MS(2,3) & MS(4,3)
MS(2,4) & MS(4,4)
MS(2,5) & MS(4,5)
MS(2,6) & MS(4,6)
MS(2,7) & MS(4,7)
MS(2,8) & MS(4,8)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
MS(3,5)
MS(3,6)
MS(3,7)
MS(3,8)
ML(1,1) & ML(6,1)
ML(1,4) & ML(6,8)
ML(1,8) & ML(6,4)
ML(1,12) & ML(8,16)
ML(1,16) & ML(6,12)
ML(1,20) & ML(6,24)
ML(1,24) & ML(6,20)
ML(1,28) & ML(6,32)
ML(1,32) & ML(6,28)
ML(2,1) & ML(5,1)
ML(2,4) & ML(5,12)
ML(2,8) & ML(5,16)
ML(2,12) & ML(5,4)
ML(2,16) & ML(5,8)
ML(2,20) & ML(5,28)
ML(2,24) & ML(5,32)
ML(2,28) & ML(5,20)
ML(2,32) & ML(5,24)
ML(3,1) & ML(4,1)
ML(3,4) & ML(4,20)
ML(3,8) & ML(4,24)
ML(3,28) & ML(4,12)

FIG. 2D3

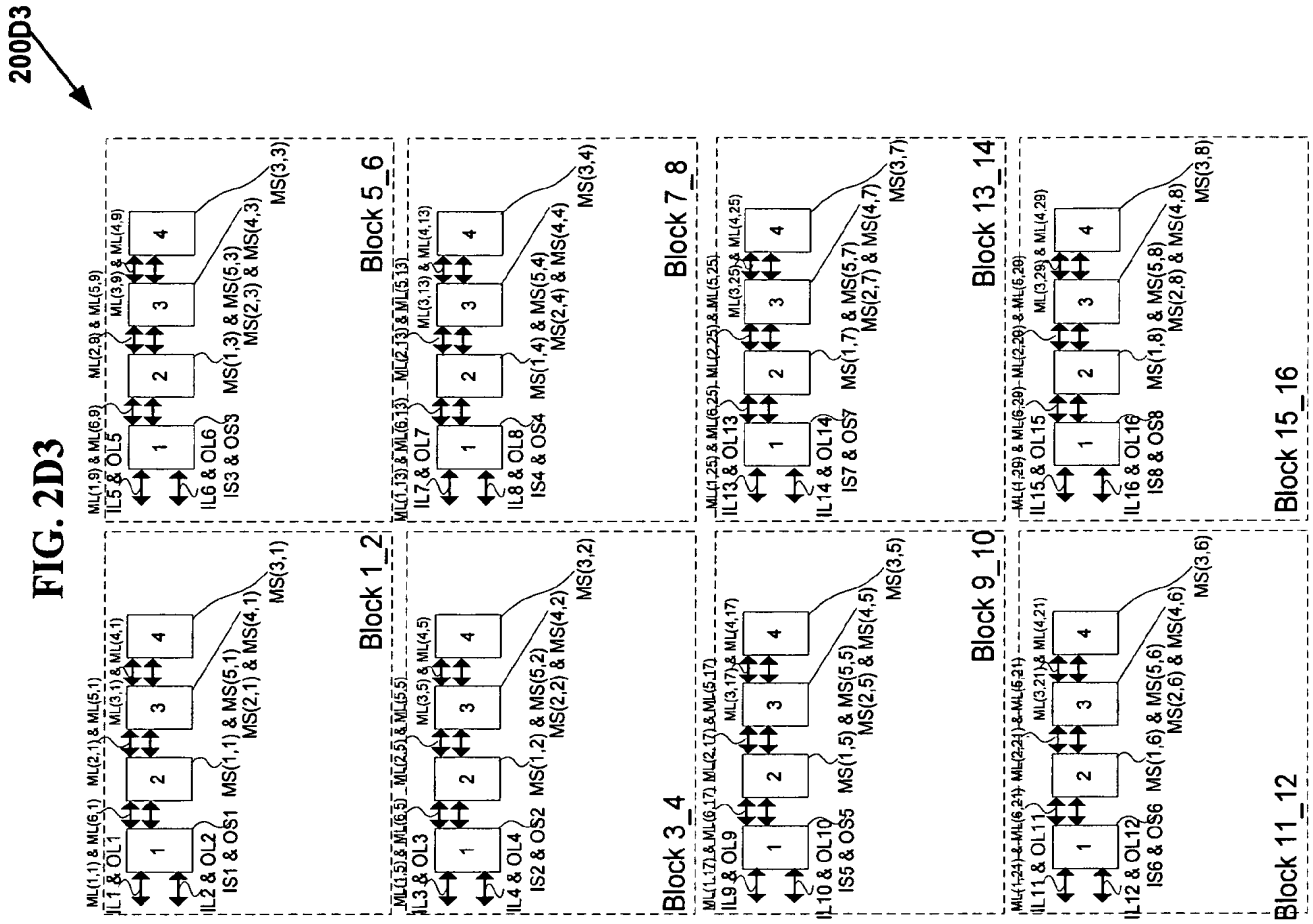

200D3
Block 1_2
Block 3_4
Block 5_6
Block 7_8
Block 9_10
Block 11_12
Block 13_14
Block 15_16
IL1 & OL1
IL2 & OL2
IS1 & OS1
IL3 & OL3
IL4 & OL4
IS2 & OS2
IL5 & OL5
IL6 & OL6
IS3 & OS3
IL7 & OL7
IL8 & OL8
IS4 & OS4
IL9 & OL9
IL10 & OL10
IS5 & OS5
IL11 & OL11
IL12 & OL12
IS6 & OS6
IL13 & OL13
IL14 & OL14
IS7 & OS7
IL15 & OL15
IL16 & OL16
IS8 & OS8
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
MS(3,5)
MS(3,6)
MS(3,7)
MS(3,8)

FIG. 2D4

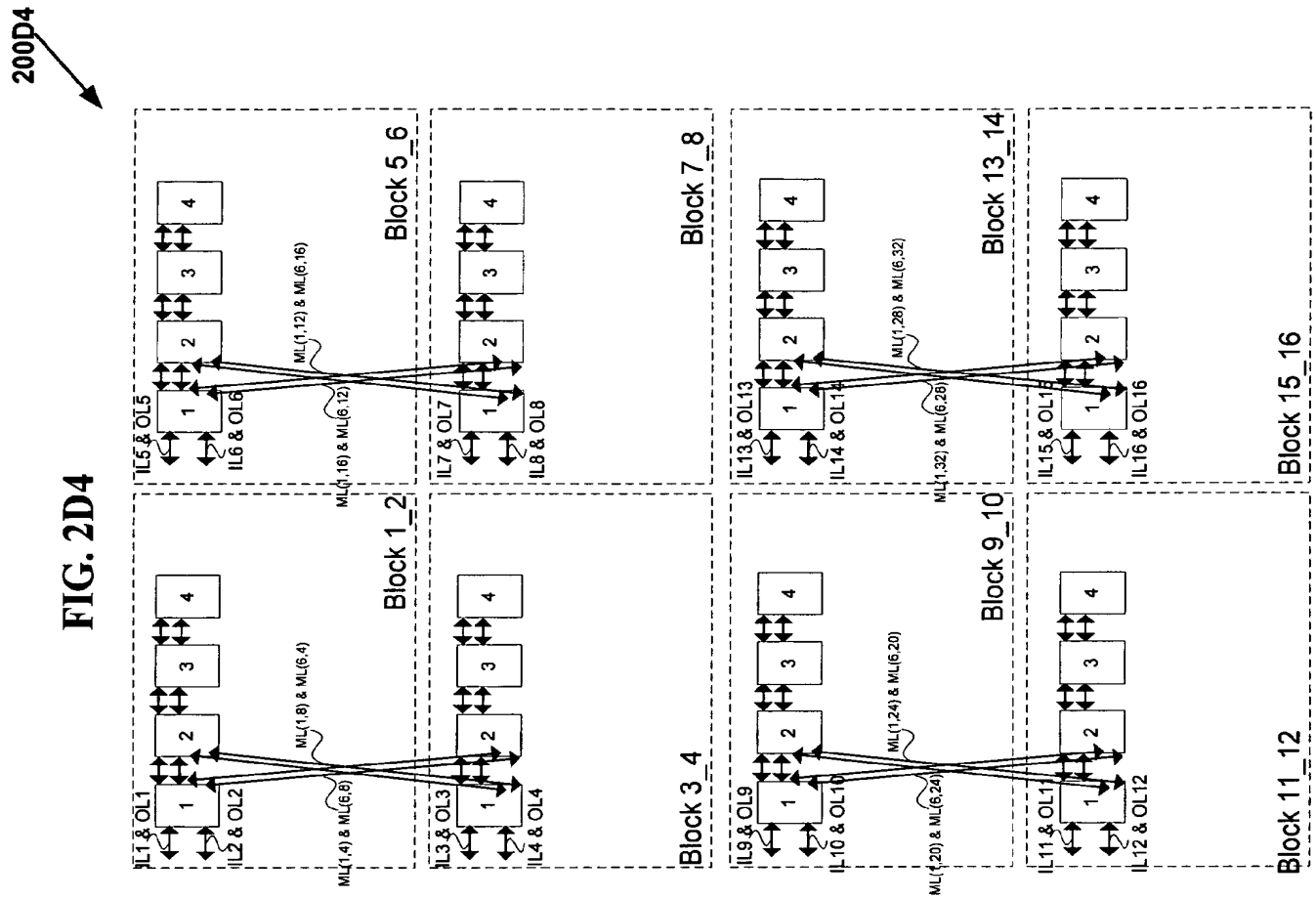

200D4
Block 1_2
Block 3_4
Block 5_6
Block 7_8
Block 9_10
Block 11_12
Block 13_14
Block 15_16
IL1 & OL1
IL2 & OL2
IL3 & OL3
IL4 & OL4
IL5 & OL5
IL6 & OL6
IL7 & OL7
IL8 & OL8
IL9 & OL9
IL10 & OL10
IL11 & OL11
IL12 & OL12
IL13 & OL13
IL14 & OL14
IL15 & OL15
IL16 & OL16
ML(1,8) & ML(6,4)
ML(1,4) & ML(6,8)
ML(1,12) & ML(6,16)
ML(1,16) & ML(6,12)
ML(1,24) & ML(6,20)
ML(1,20) & ML(6,24)
ML(1,28) & ML(6,32)
ML(1,32) & ML(6,28)

FIG. 2D5

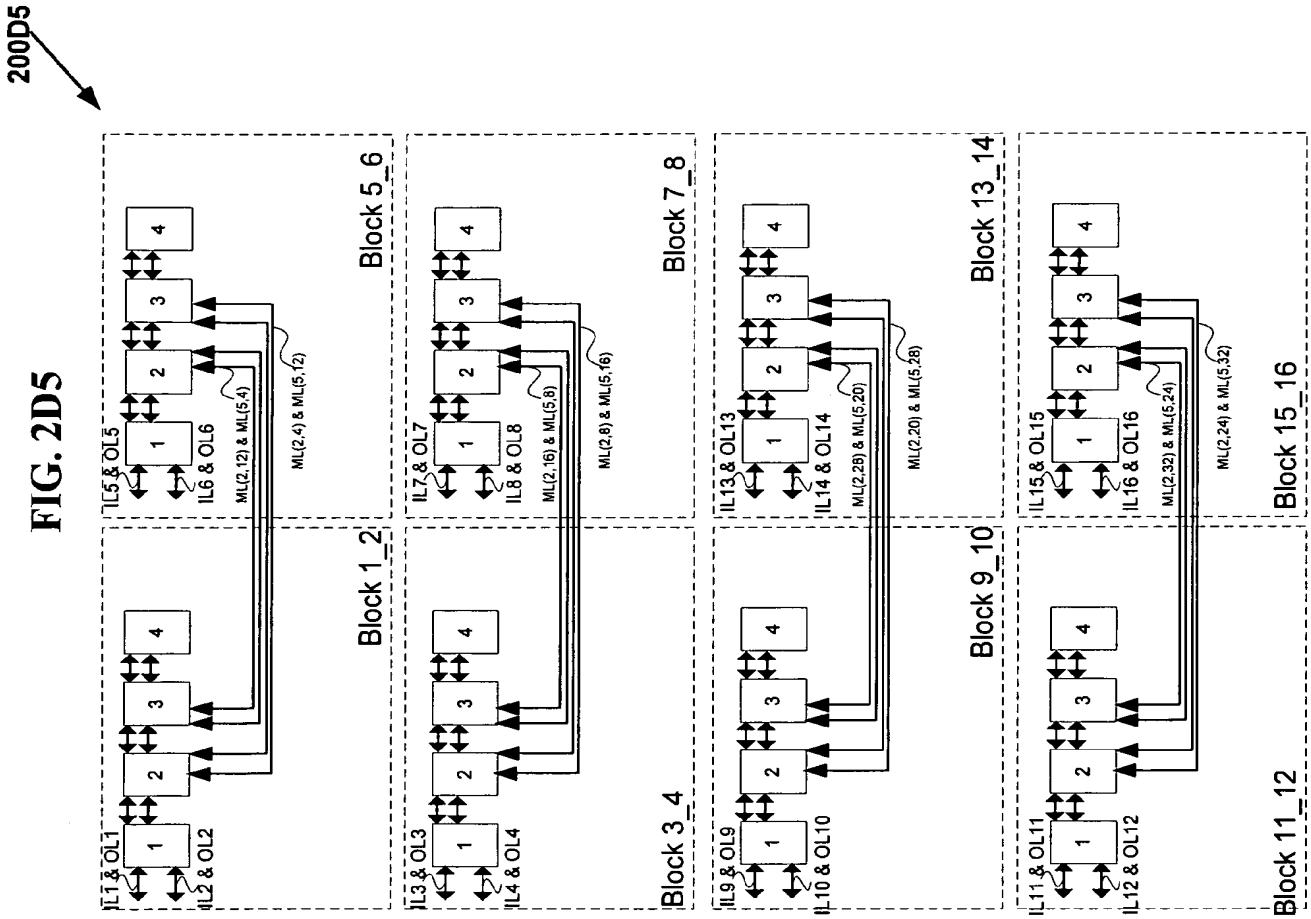

200D5
Block 1_2
Block 3_4
Block 5_6
Block 7_8
Block 9_10
Block 11_12
Block 13_14
Block 15_16
IL1 & OL1
IL2 & OL2
IL3 & OL3
IL4 & OL4
IL5 & OL5
IL6 & OL6
IL7 & OL7
IL8 & OL8
IL9 & OL9
IL10 & OL10
IL11 & OL11
IL12 & OL12
IL13 & OL13
IL14 & OL14
IL15 & OL15
IL16 & OL16
ML(2,4) & ML(5,12)
ML(2,12) & ML(5,4)
ML(2,8) & ML(5,16)
ML(2,16) & ML(5,8)
ML(2,20) & ML(5,28)
ML(2,28) & ML(5,20)
ML(2,24) & ML(5,32)
ML(2,32) & ML(5,24)

FIG. 2D6

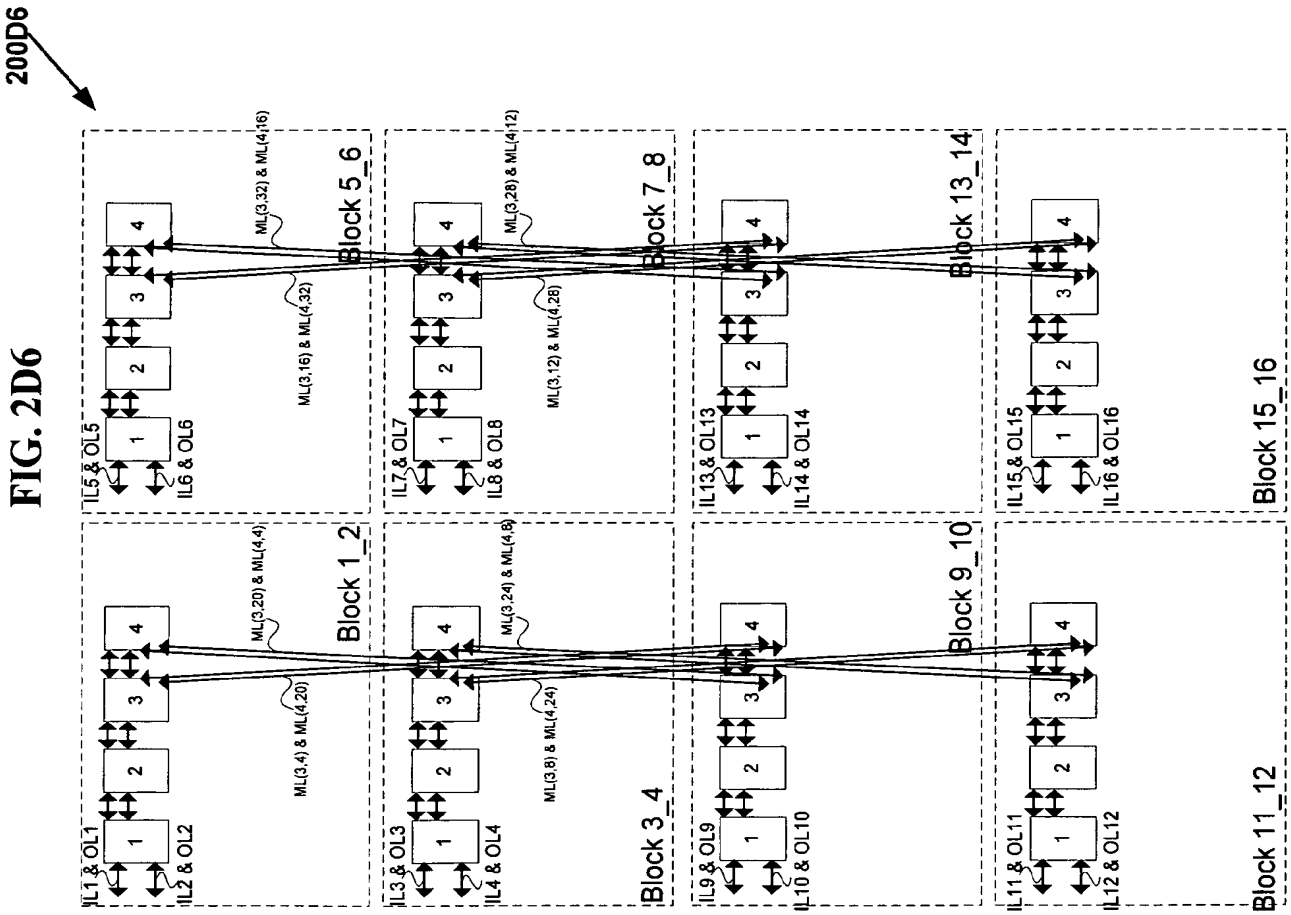

200D6
Block 1_2
Block 3_4
Block 5_6
Block 7_8
Block 9_10
Block 11_12
Block 13_14
Block 15_16
IL1 & OL1
IL2 & OL2
IL3 & OL3
IL4 & OL4
IL5 & OL5
IL6 & OL6
IL7 & OL7
IL8 & OL8
IL9 & OL9
IL10 & OL10
IL11 & OL11
IL12 & OL12
IL13 & OL13
IL14 & OL14
IL15 & OL15
IL16 & OL16
ML(3,20) & ML(4,4)
ML(3,4) & ML(4,20)
ML(3,24) & ML(4,8)
ML(3,8) & ML(4,24)
ML(3,32) & ML(4,16)
ML(3,16) & ML(4,32)
ML(3,28) & ML(4,12)
ML(3,12) & ML(4,28)

FIG. 3A

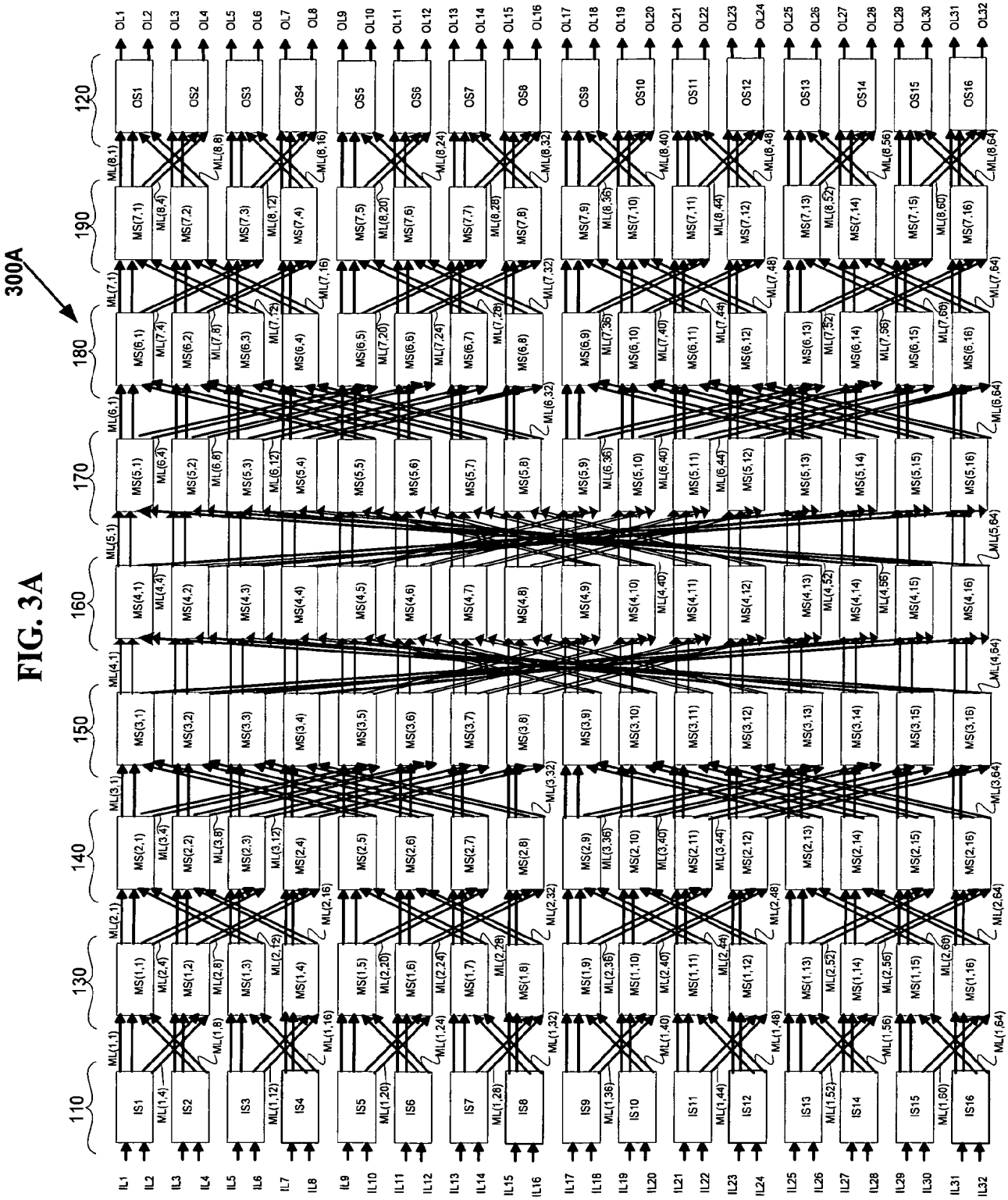

300A
110
130
140
150
160
170
180
190
120
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
IL9
IL10
IL11
IL12
IL13
IL14
IL15
IL16
IL17
IL18
IL19
IL20
IL21
IL22
IL23
IL24
IL25
IL26
IL27
IL28
IL29
IL30
IL31
IL32
IS1
IS2
IS3
IS4
IS5
IS6
IS7
IS8
IS9
IS10
IS11
IS12
IS13
IS14
IS15
IS16
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(1,5)
MS(1,6)
MS(1,7)
MS(1,8)
MS(1,9)
MS(1,10)
MS(1,11)
MS(1,12)
MS(1,13)
MS(1,14)
MS(1,15)
MS(1,16)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(2,5)
MS(2,6)
MS(2,7)
MS(2,8)
MS(2,9)
MS(2,10)
MS(2,11)
MS(2,12)
MS(2,13)
MS(2,14)
MS(2,15)
MS(2,16)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
MS(3,5)
MS(3,6)
MS(3,7)
MS(3,8)
MS(3,9)
MS(3,10)
MS(3,11)
MS(3,12)
MS(3,13)
MS(3,14)
MS(3,15)
MS(3,16)
MS(4,1)
MS(4,2)
MS(4,3)
MS(4,4)
MS(4,5)
MS(4,6)
MS(4,7)
MS(4,8)
MS(4,9)
MS(4,10)
MS(4,11)
MS(4,12)
MS(4,13)
MS(4,14)
MS(4,15)
MS(4,16)
MS(5,1)
MS(5,2)
MS(5,3)
MS(5,4)
MS(5,5)
MS(5,6)
MS(5,7)
MS(5,8)
MS(5,9)
MS(5,10)
MS(5,11)
MS(5,12)
MS(5,13)
MS(5,14)
MS(5,15)
MS(5,16)
MS(6,1)
MS(6,2)
MS(6,3)
MS(6,4)
MS(6,5)
MS(6,6)
MS(6,7)
MS(6,8)
MS(6,9)
MS(6,10)
MS(6,11)
MS(6,12)
MS(6,13)
MS(6,14)
MS(6,15)
MS(6,16)
MS(7,1)
MS(7,2)
MS(7,3)
MS(7,4)
MS(7,5)
MS(7,6)
MS(7,7)
MS(7,8)
MS(7,9)
MS(7,10)
MS(7,11)
MS(7,12)
MS(7,13)
MS(7,14)
MS(7,15)
MS(7,16)
OS1
OS2
OS3
OS4
OS5
OS6
OS7
OS8
OS9
OS10
OS11
OS12
OS13
OS14
OS15
OS16
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
OL9
OL10
OL11
OL12
OL13
OL14
OL15
OL16
OL17
OL18
OL19
OL20
OL21
OL22
OL23
OL24
OL25
OL26
OL27
OL28
OL29
OL30
OL31
OL32

FIG. 3B

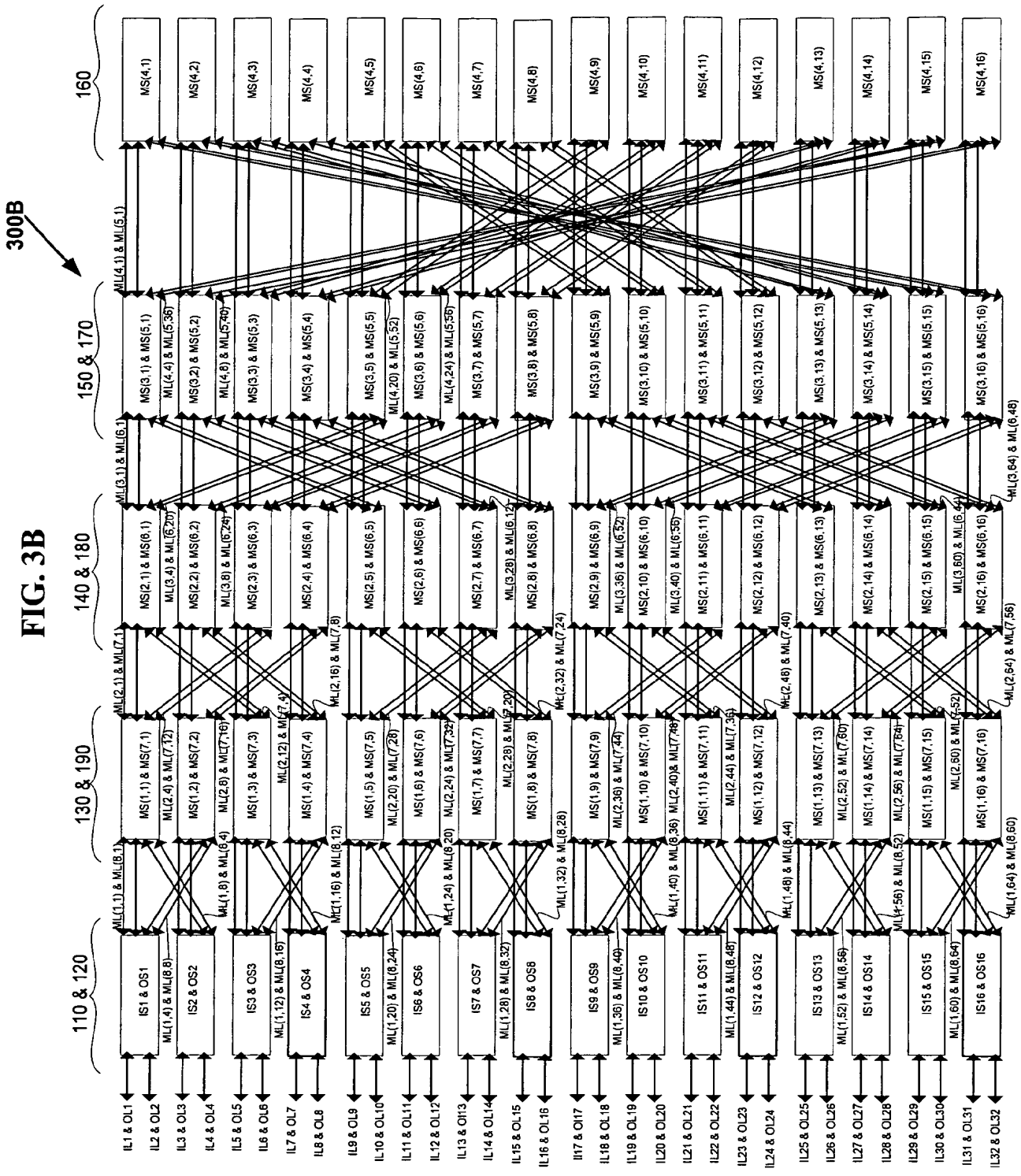

300B
110 & 120
130 & 190
140 & 180
150 & 170
160
IL1 & OL1
IL2 & OL2
IL3 & OL3
IL4 & OL4
IL5 & OL5
IL6 & OL6
IL7 & OL7
IL8 & OL8
IL9 & OL9
IL10 & OL10
IL11 & OL11
IL12 & OL12
IL13 & OI13
IL14 & OL14
IL15 & OL15
IL16 & OL16
II17 & OI17
IL18 & OL18
IL19 & OL19
IL20 & OL20
IL21 & OL21
IL22 & OL22
IL23 & OL23
IL24 & OL24
IL25 & OL25
IL26 & OL26
IL27 & OL27
IL28 & OL28
IL29 & OL29
IL30 & OL30
IL31 & OL31
IL32 & OL32
IS1 & OS1
IS2 & OS2
IS3 & OS3
IS4 & OS4
IS5 & OS5
IS6 & OS6
IS7 & OS7
IS8 & OS8
IS9 & OS9
IS10 & OS10
IS11 & OS11
IS12 & OS12
IS13 & OS13
IS14 & OS14
IS15 & OS15
IS16 & OS16
MS(4,1)
MS(4,2)
MS(4,3)
MS(4,4)
MS(4,5)
MS(4,6)
MS(4,7)
MS(4,8)
MS(4,9)
MS(4,10)
MS(4,11)
MS(4,12)
MS(4,13)
MS(4,14)
MS(4,15)
MS(4,16)

FIG. 3C

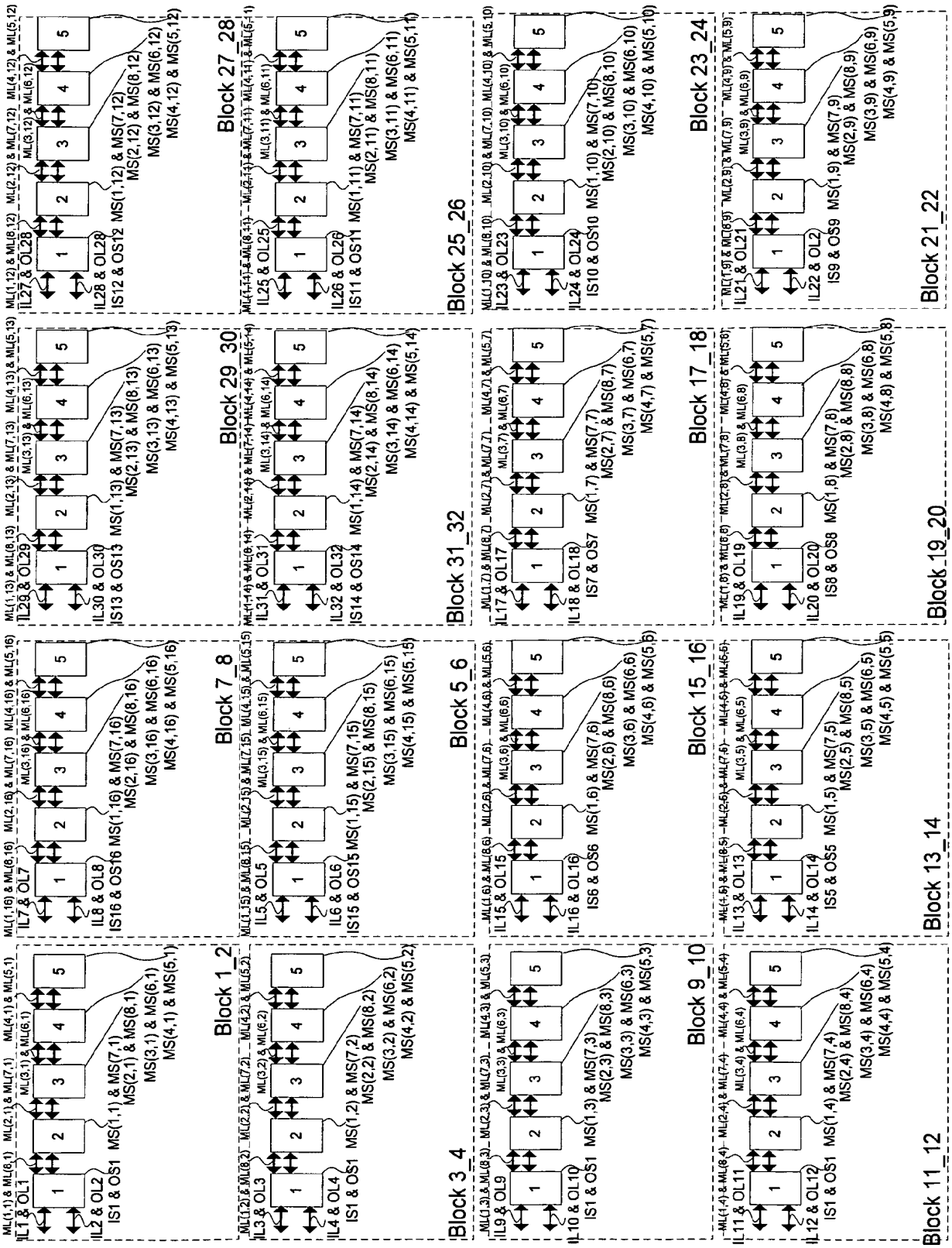

300C
Block 1_2
Block 3_4
Block 5_6
Block 7_8
Block 9_10
Block 11_12
Block 13_14
Block 15_16
Block 17_18
Block 19_20
Block 21_22
Block 23_24
Block 25_26
Block 27_28
Block 29_30
Block 31_32

FIG. 3D

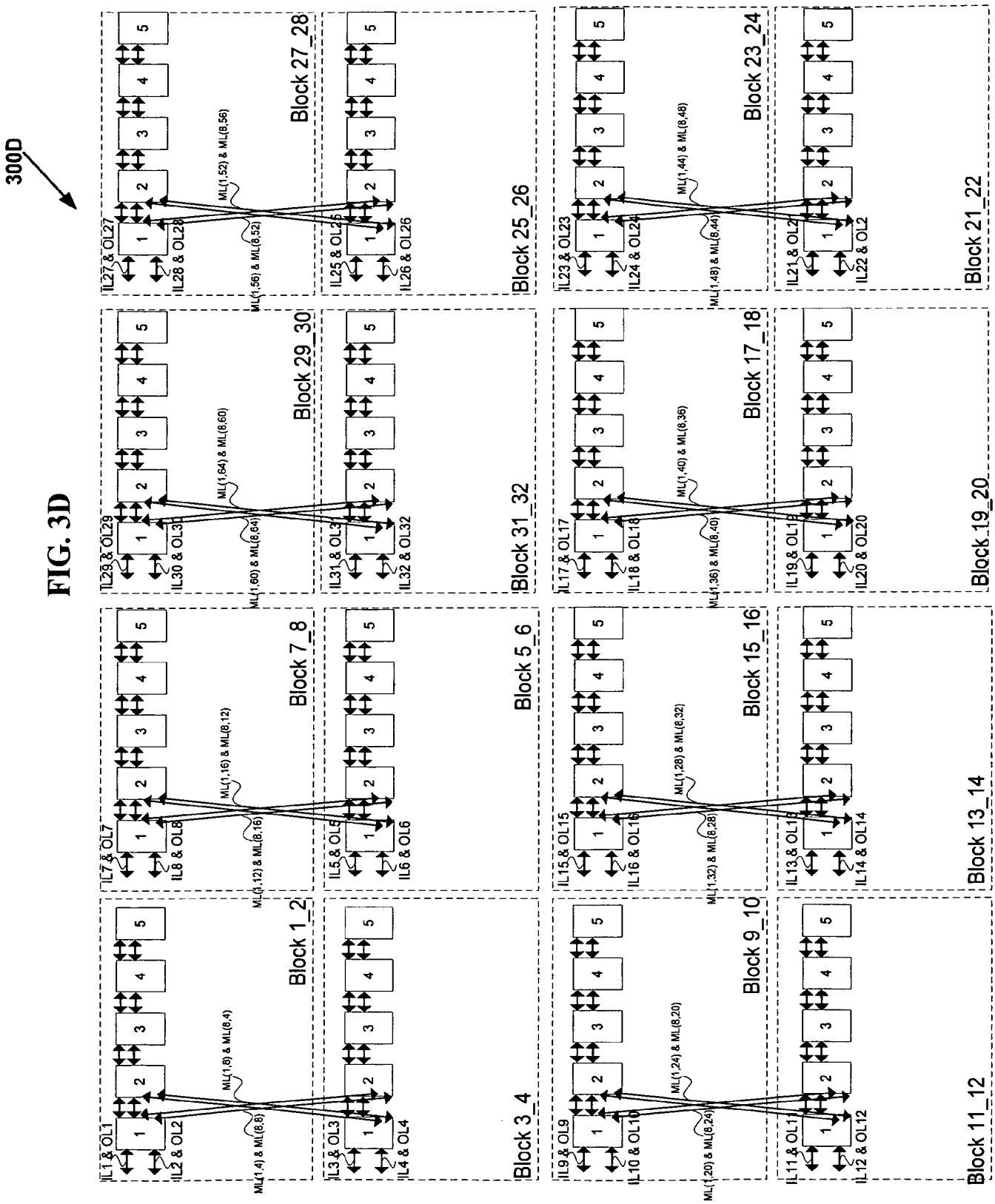

300D
Block 1_2
Block 3_4
Block 5_6
Block 7_8
Block 9_10
Block 11_12
Block 13_14
Block 15_16
Block 17_18
Block 19_20
Block 21_22
Block 23_24
Block 25_26
Block 27_28
Block 29_30
Block 31_32

FIG. 3E

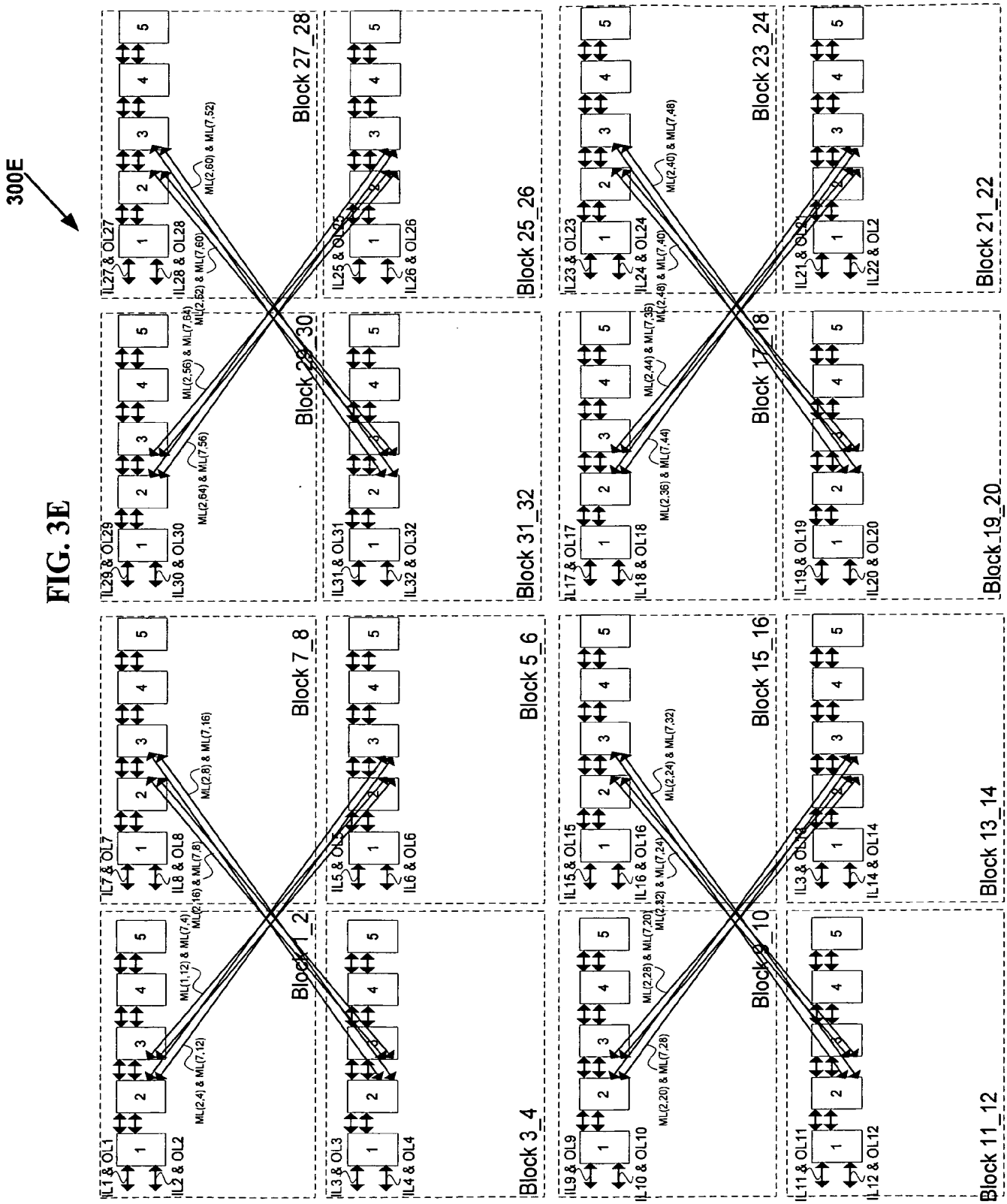

300E
Block 1_2
Block 3_4
Block 5_6
Block 7_8
Block 9_10
Block 11_12
Block 13_14
Block 15_16
Block 17_18
Block 19_20
Block 21_22
Block 23_24
Block 25_26
Block 27_28
Block 29_30
Block 31_32

FIG. 3F

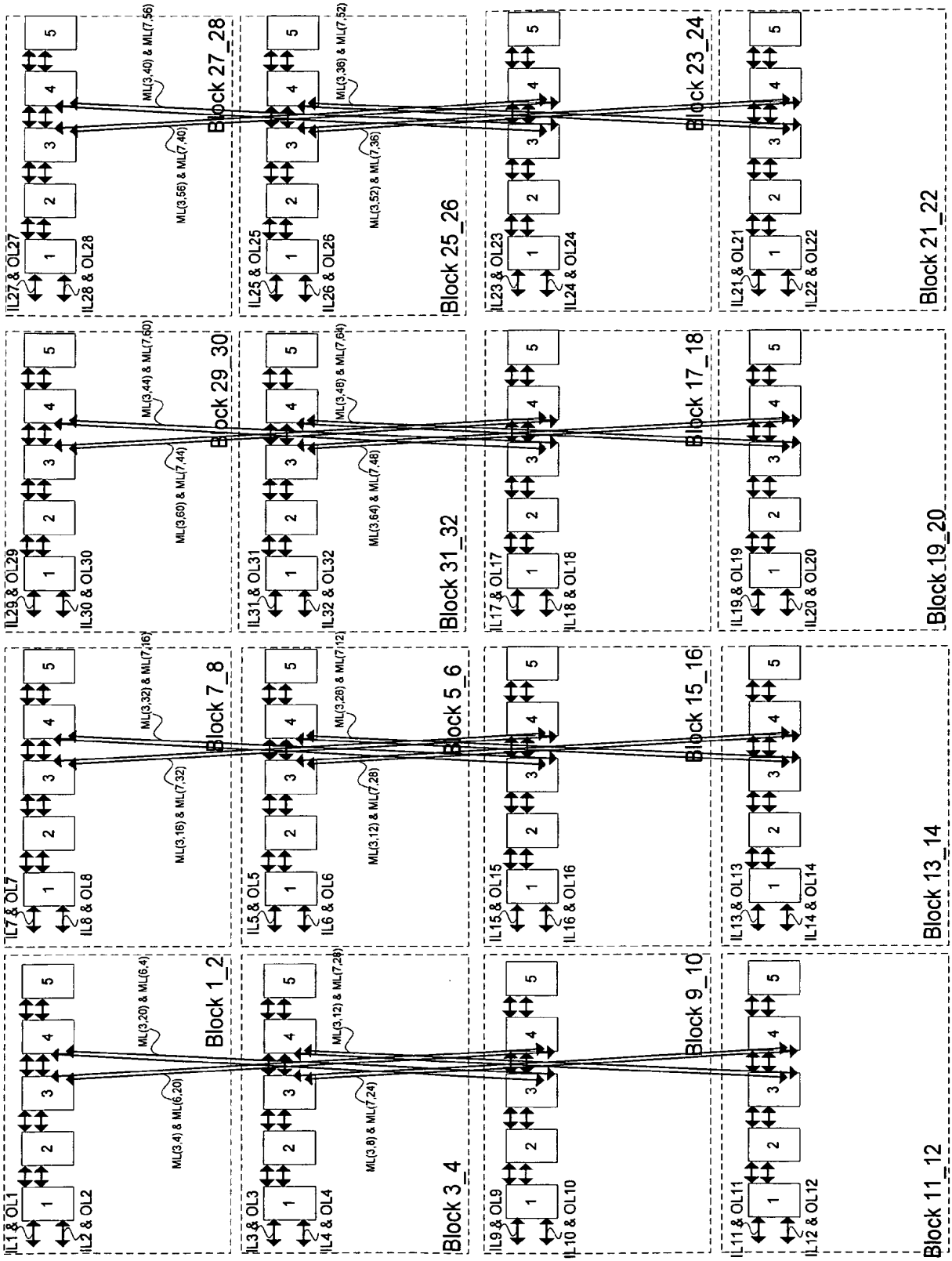

300F
Block 1_2
Block 3_4
Block 5_6
Block 7_8
Block 9_10
Block 11_12
Block 13_14
Block 15_16
Block 17_18
Block 19_20
Block 21_22
Block 23_24
Block 25_26
Block 27_28
Block 29_30
Block 31_32

FIG. 3G

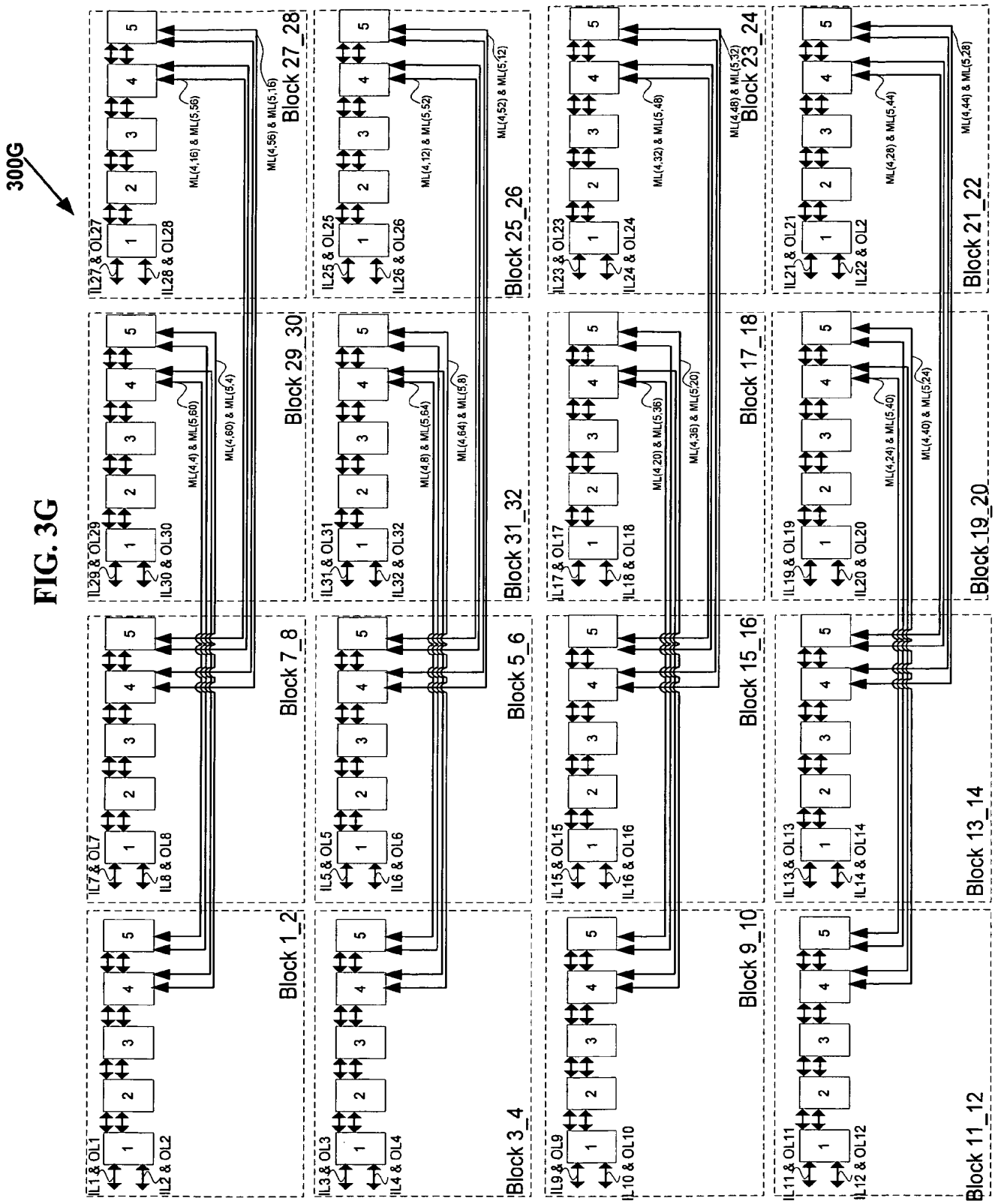

300G
Block 1_2
Block 3_4
Block 5_6
Block 7_8
Block 9_10
Block 11_12
Block 13_14
Block 15_16
Block 17_18
Block 19_20
Block 21_22
Block 23_24
Block 25_26
Block 27_28
Block 29_30
Block 31_32
IL1 & OL1
IL2 & OL2
IL3 & OL3
IL4 & OL4
IL5 & OL5
IL6 & OL6
IL7 & OL7
IL8 & OL8
IL9 & OL9
IL10 & OL10
IL11 & OL11
IL12 & OL12
IL13 & OL13
IL14 & OL14
IL15 & OL15
IL16 & OL16
IL17 & OL17
IL18 & OL18
IL19 & OL19
IL20 & OL20
IL21 & OL21
IL22 & OL2
IL23 & OL23
IL24 & OL24
IL25 & OL25
IL26 & OL26
IL27 & OL27
IL28 & OL28
IL29 & OL29
IL30 & OL30
IL31 & OL31
IL32 & OL32
ML(4,4) & ML(5,60)
ML(4,60) & ML(5,4)
ML(4,8) & ML(5,64)
ML(4,64) & ML(5,8)
ML(4,12) & ML(5,52)
ML(4,52) & ML(5,12)
ML(4,16) & ML(5,56)
ML(4,56) & ML(5,16)
ML(4,20) & ML(5,36)
ML(4,36) & ML(5,20)
ML(4,24) & ML(5,40)
ML(4,40) & ML(5,24)
ML(4,28) & ML(5,44)
ML(4,44) & ML(5,28)
ML(4,32) & ML(5,48)
ML(4,48) & ML(5,32)

FIG. 3H

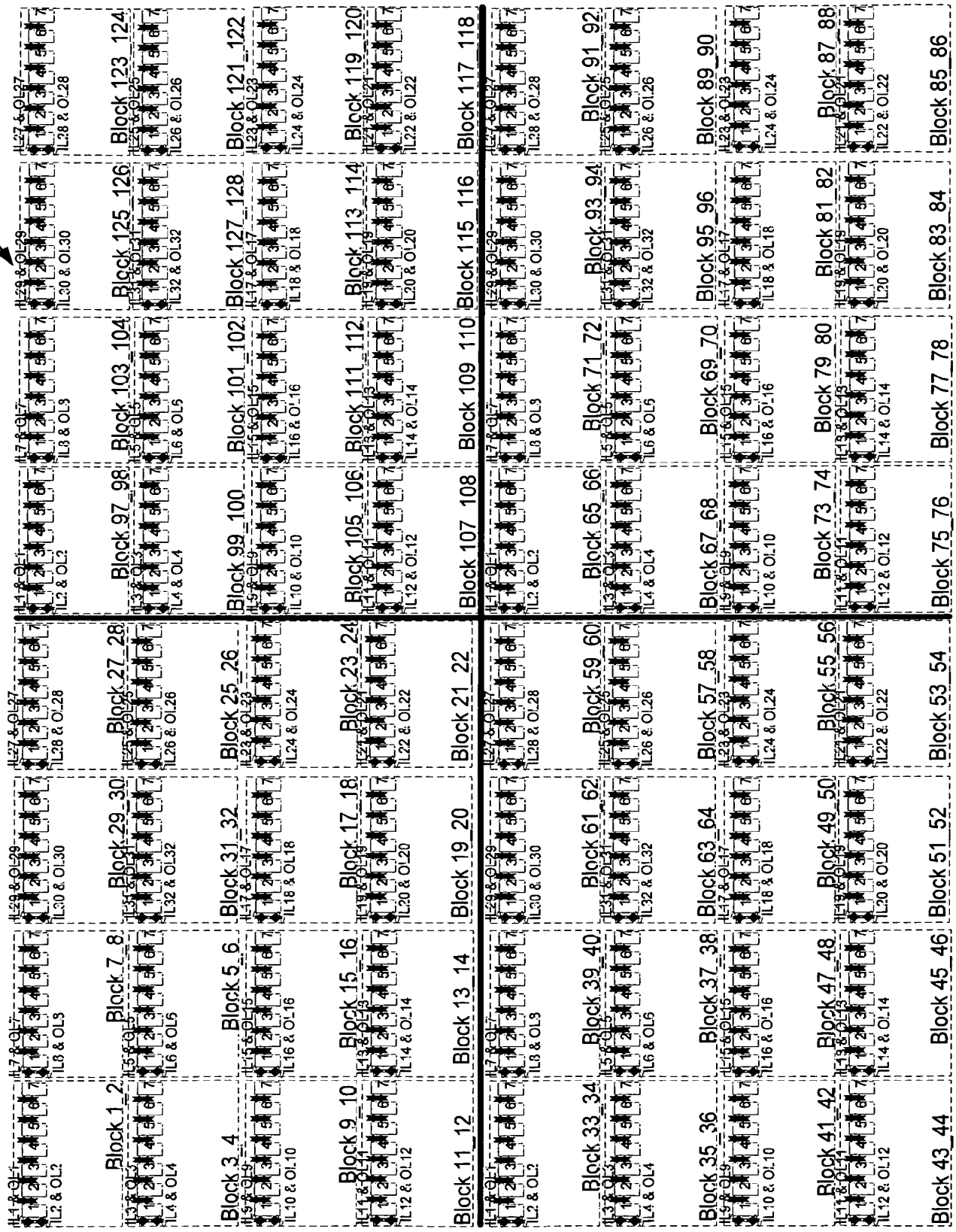

300H
Block 1_2
Block 3_4
Block 5_6
Block 7_8
Block 9_10
Block 11_12
Block 13_14
Block 15_16
Block 17_18
Block 19_20
Block 21_22
Block 23_24
Block 25_26
Block 27_28
Block 29_30
Block 31_32
Block 33_34
Block 35_36
Block 37_38
Block 39_40
Block 41_42
Block 43_44
Block 45_46
Block 47_48
Block 49_50
Block 51_52
Block 53_54
Block 55_56
Block 57_58
Block 59_60
Block 61_62
Block 63_64
Block 65_66
Block 67_68
Block 69_70
Block 71_72
Block 73_74
Block 75_76
Block 77_78
Block 79_80
Block 81_82
Block 83_84
Block 85_86
Block 87_88
Block 89_90
Block 91_92
Block 93_94
Block 95_96
Block 97_98
Block 99_100
Block 101_102
Block 103_104
Block 105_106
Block 107_108
Block 109_110
Block 111_112
Block 113_114
Block 115_116
Block 117_118
Block 119_120
Block 121_122
Block 123_124
Block 125_126
Block 127_128

FIG. 4A

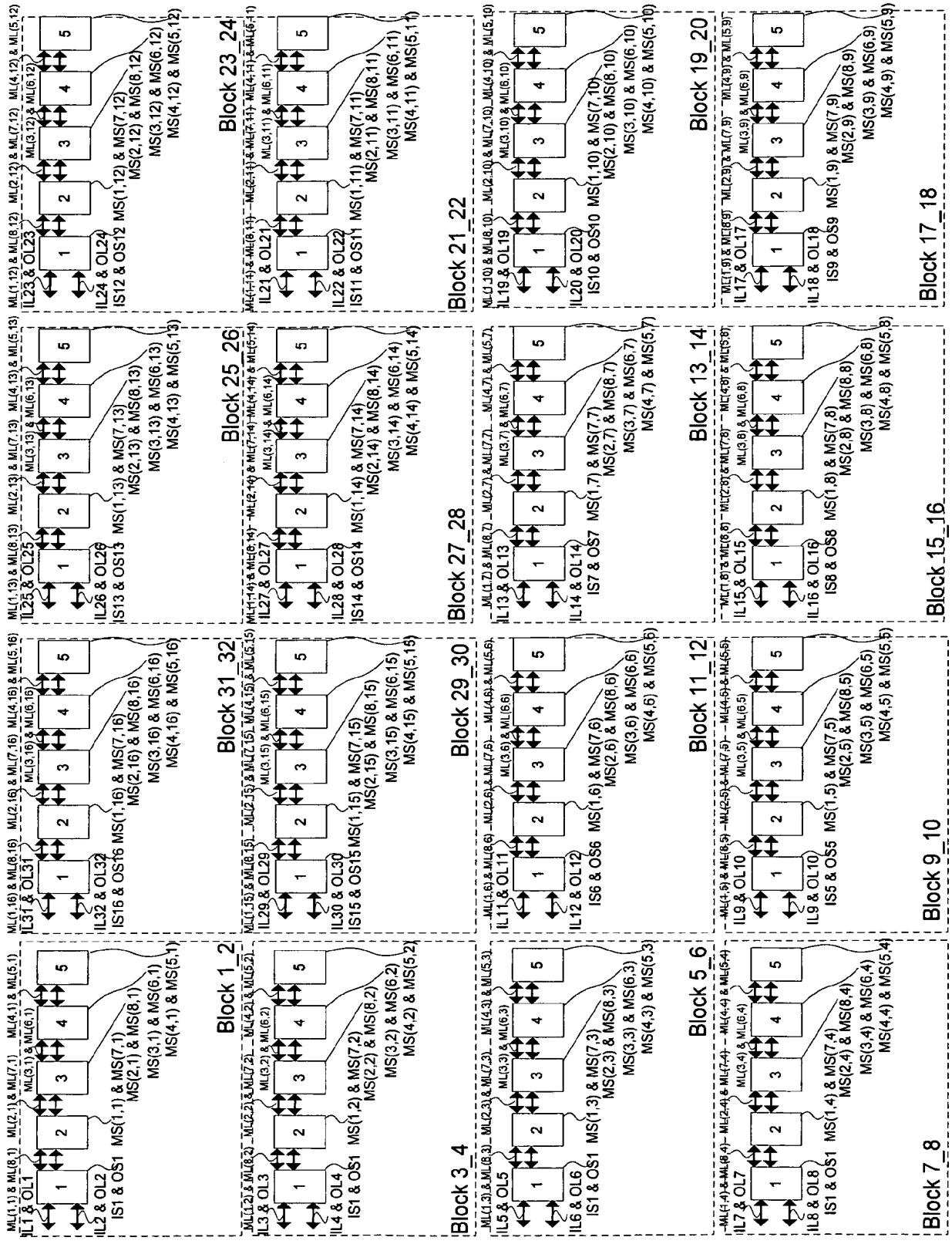

400A
Block 1_2
Block 3_4
Block 5_6
Block 7_8
Block 9_10
Block 11_12
Block 13_14
Block 15_16
Block 17_18
Block 19_20
Block 21_22
Block 23_24
Block 25_26
Block 27_28
Block 29_30
Block 31_32

FIG. 4B

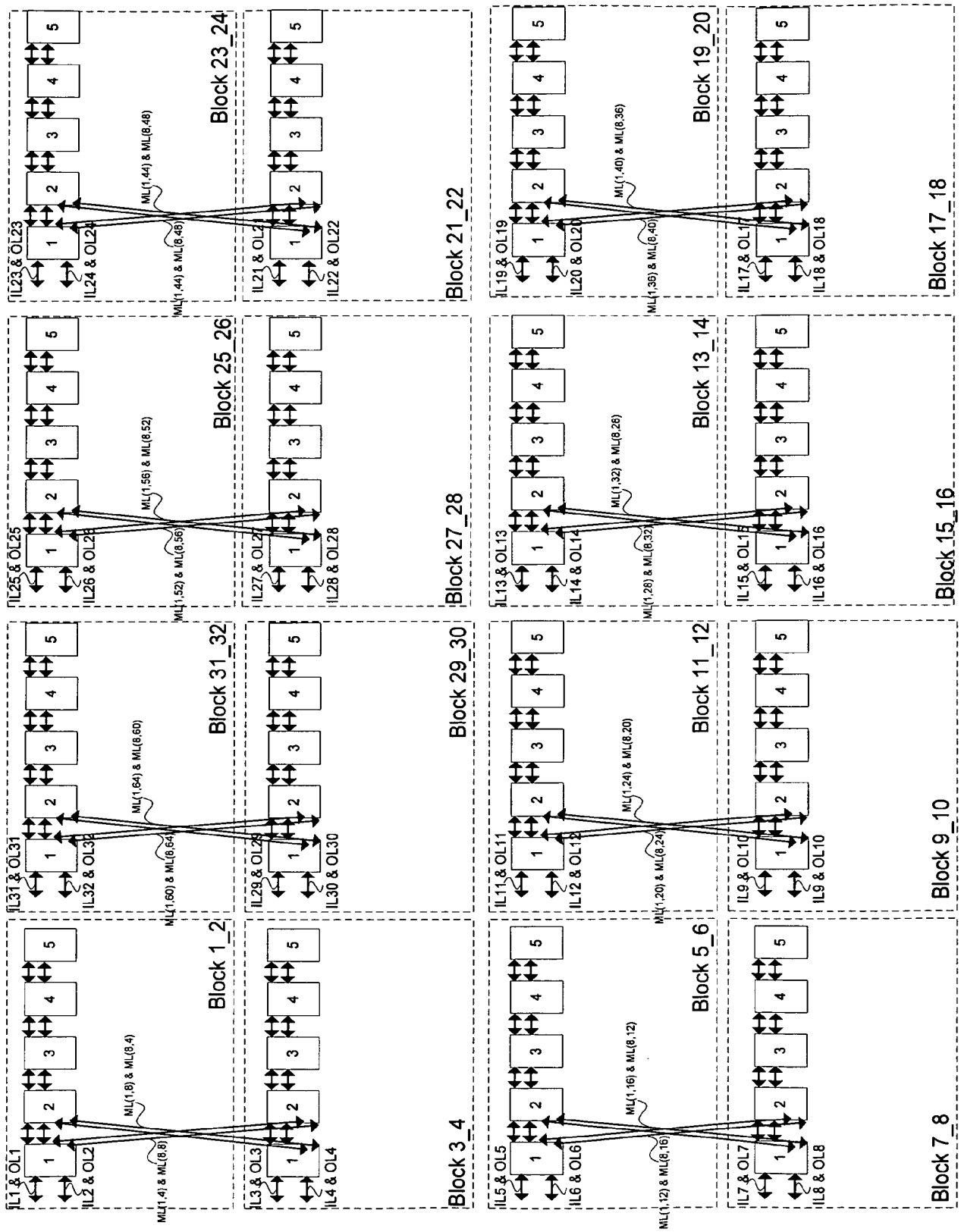

400B
Block 23_24
Block 21_22
Block 25_26
Block 27_28
Block 31_32
Block 29_30
Block 1_2
Block 3_4
Block 19_20
Block 17_18
Block 13_14
Block 15_16
Block 11_12
Block 9_10
Block 5_6
Block 7_8

FIG. 4C

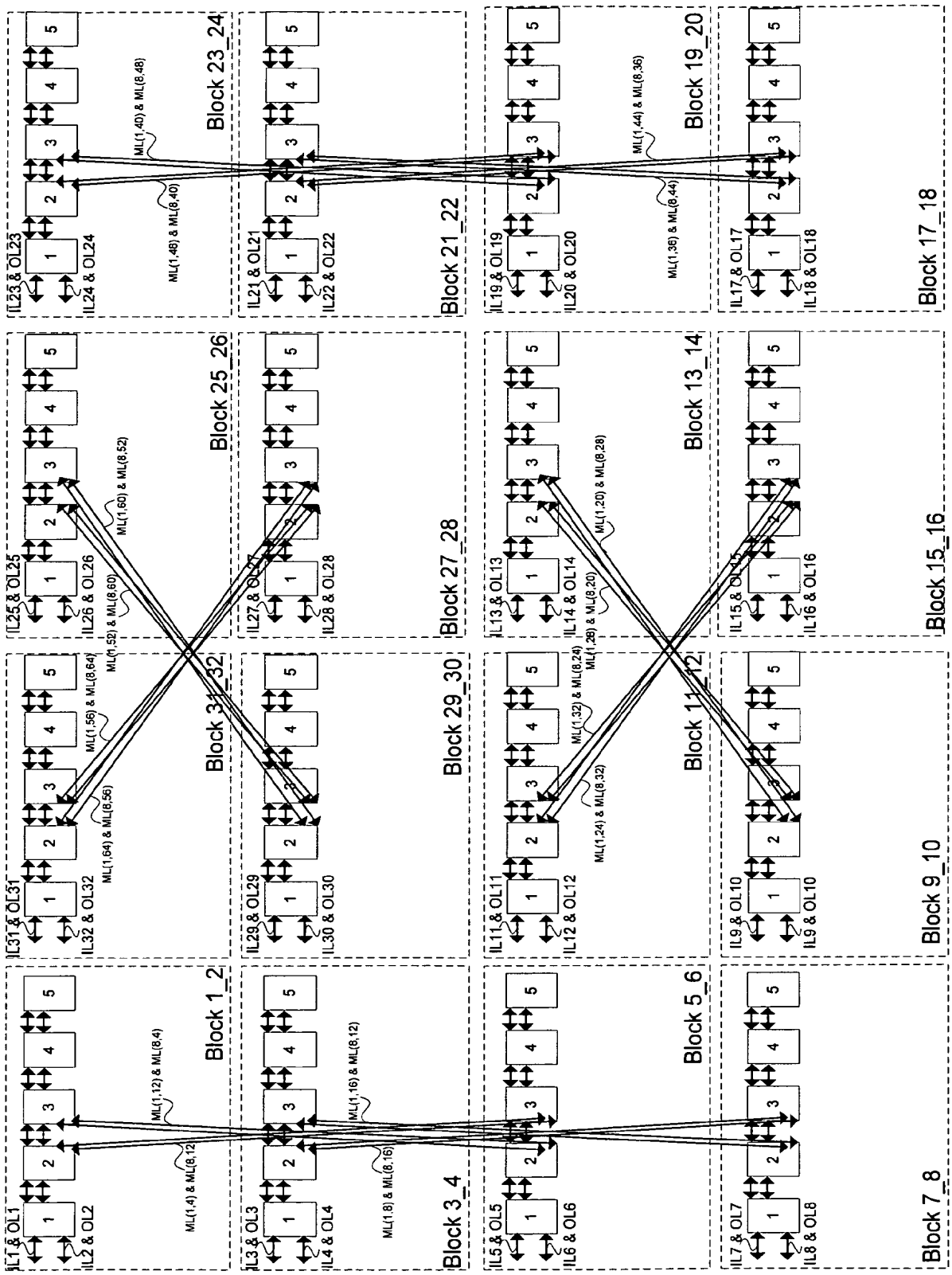

400C
Block 23_24
Block 21_22
Block 19_20
Block 17_18
Block 25_26
Block 27_28
Block 13_14
Block 15_16
Block 31_32
Block 29_30
Block 11_12
Block 9_10
Block 1_2
Block 3_4
Block 5_6
Block 7_8

FIG. 4D

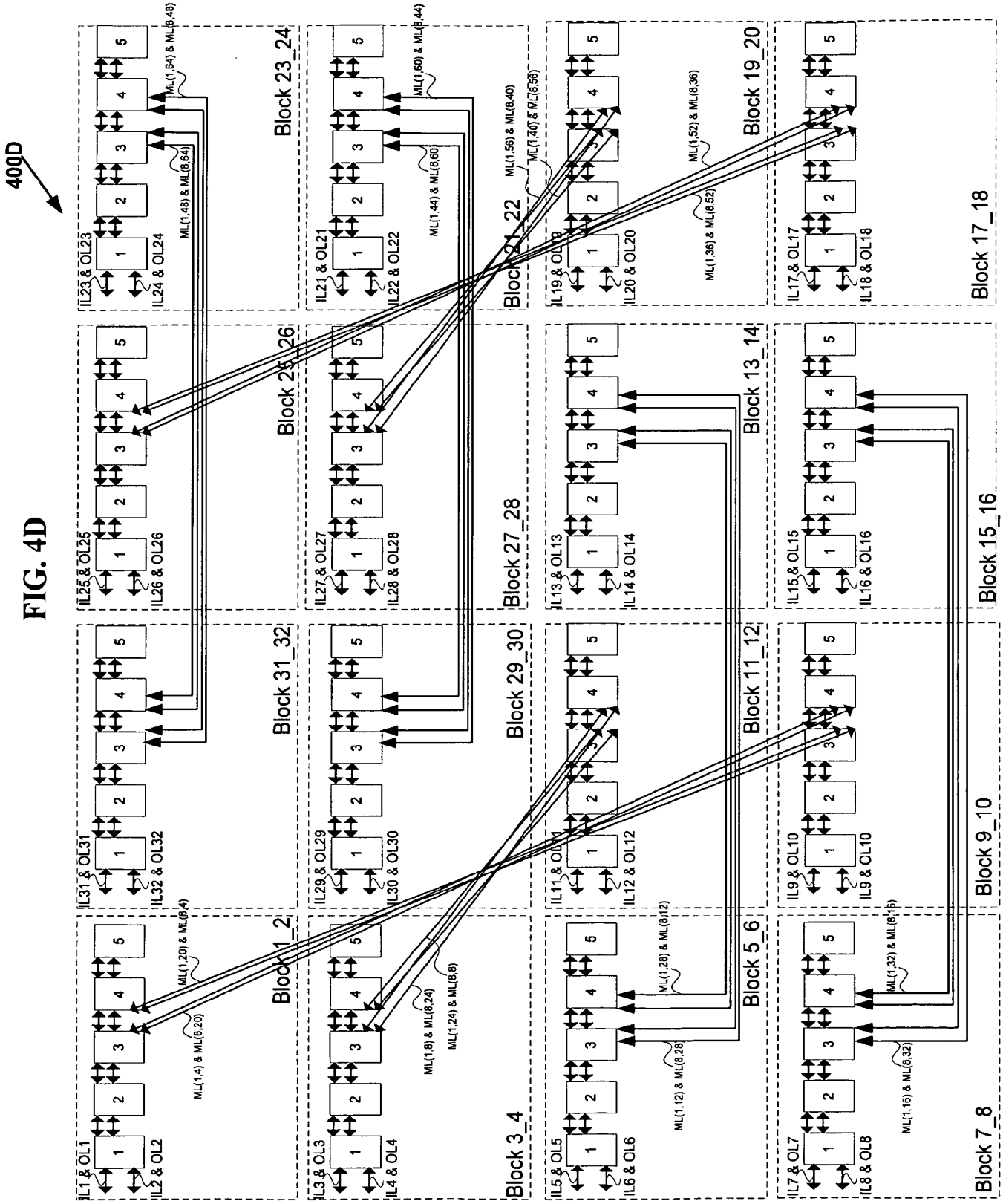
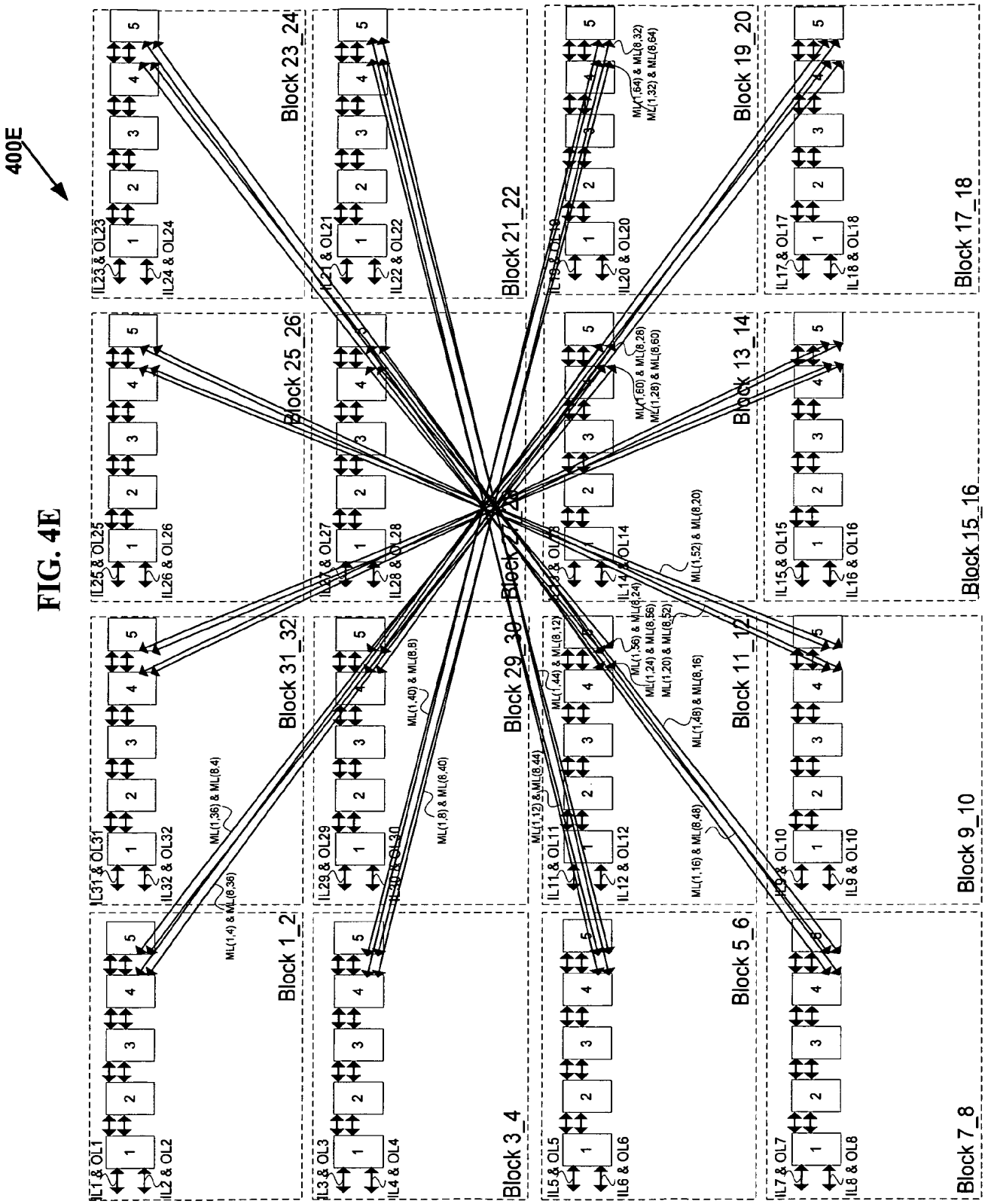

400D
Block 1_2
Block 3_4
Block 5_6
Block 7_8
Block 9_10
Block 11_12
Block 13_14
Block 15_16
Block 17_18
Block 19_20
Block 21_22
Block 23_24
Block 25_26
Block 27_28
Block 29_30
Block 31_32
IL1 & OL1
IL2 & OL2
IL3 & OL3
IL4 & OL4
IL5 & OL5
IL6 & OL6
IL7 & OL7
IL8 & OL8
IL9 & OL10
IL11 & OL11
IL12 & OL12
IL13 & OL13
IL14 & OL14
IL15 & OL15
IL16 & OL16
IL17 & OL17
IL18 & OL18
IL19 & OL19
IL20 & OL20
IL21 & OL21
IL22 & OL22
IL23 & OL23
IL24 & OL24
IL25 & OL25
IL26 & OL26
IL27 & OL27
IL28 & OL28
IL29 & OL29
IL30 & OL30
IL31 & OL31
IL32 & OL32
ML(1,4) & ML(8,20)
ML(1,20) & ML(8,4)
ML(1,8) & ML(8,24)
ML(1,24) & ML(8,8)
ML(1,12) & ML(8,28)
ML(1,28) & ML(8,12)
ML(1,16) & ML(8,32)
ML(1,32) & ML(8,16)
ML(1,36) & ML(8,52)
ML(1,52) & ML(8,36)
ML(1,40) & ML(8,56)
ML(1,56) & ML(8,40)
ML(1,44) & ML(8,60)
ML(1,60) & ML(8,44)
ML(1,48) & ML(8,64)
ML(1,64) & ML(8,48)

FIG. 4E


400E
Block 1_2
Block 3_4
Block 5_6
Block 7_8
Block 9_10
Block 11_12
Block 13_14
Block 15_16
Block 17_18
Block 19_20
Block 21_22
Block 23_24
Block 25_26
Block 27_28
Block 29_30
Block 31_32
IL1 & OL1
IL2 & OL2
IL3 & OL3
IL4 & OL4
IL5 & OL5
IL6 & OL6
IL7 & OL7
IL8 & OL8
IL9 & OL10
IL11 & OL11
IL12 & OL12
IL14 & OL14
IL15 & OL15
IL16 & OL16
IL17 & OL17
IL18 & OL18
IL20 & OL20
IL21 & OL21
IL22 & OL22
IL23 & OL23
IL24 & OL24
IL25 & OL25
IL26 & OL26
IL27 & OL27
IL28 & OL28
IL29 & OL29
IL32 & OL32
ML(1,4) & ML(8,36)
ML(1,36) & ML(8,4)
ML(1,8) & ML(8,40)
ML(1,40) & ML(8,8)
ML(1,12) & ML(8,44)
ML(1,44) & ML(8,12)
ML(1,16) & ML(8,48)
ML(1,48) & ML(8,16)
ML(1,20) & ML(8,52)
ML(1,24) & ML(8,56)
ML(1,28) & ML(8,60)
ML(1,60) & ML(8,28)
ML(1,32) & ML(8,64)
ML(1,64) & ML(8,32)
ML(1,52) & ML(8,20)

400C1

FIG. 4C1

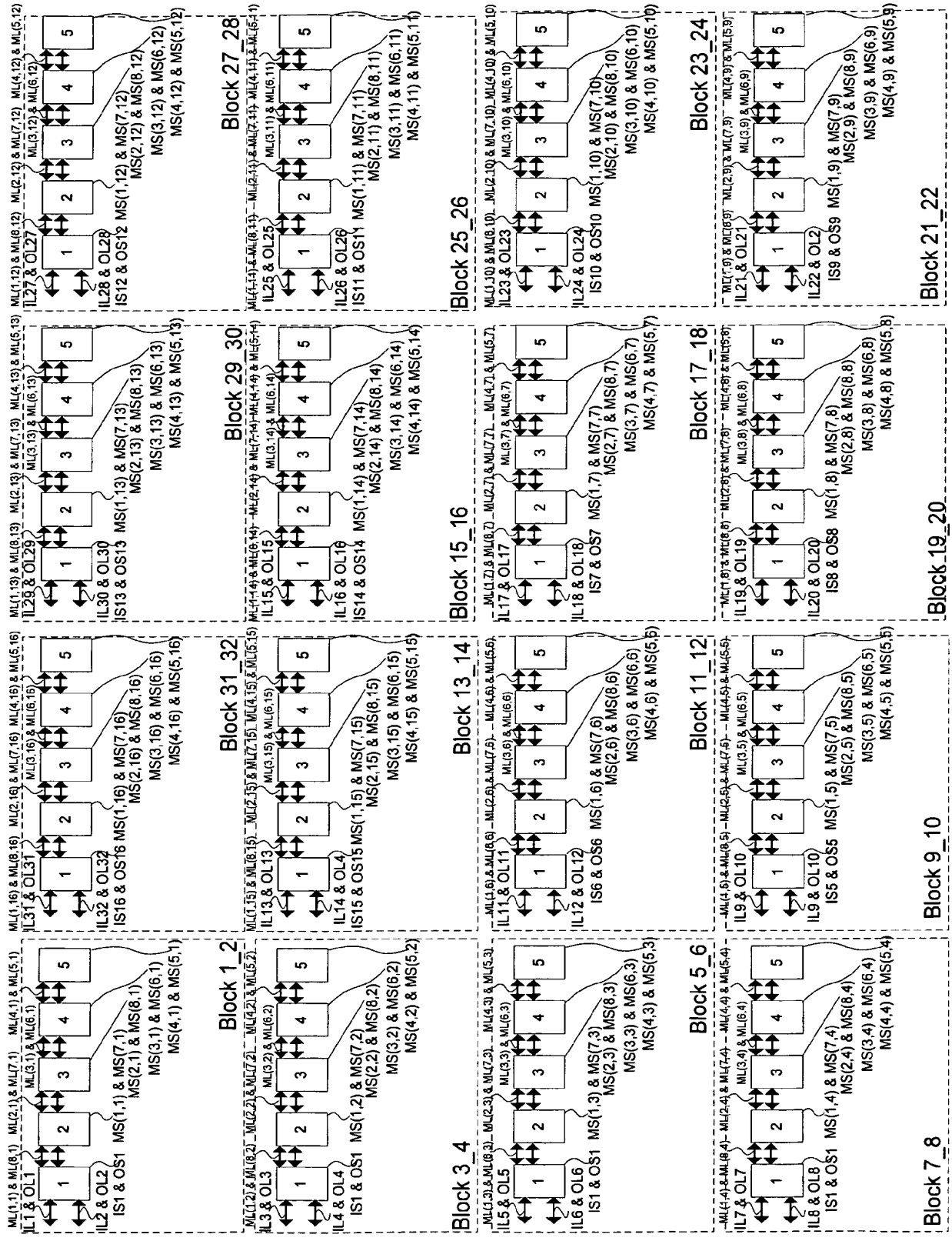


FIG. 5A

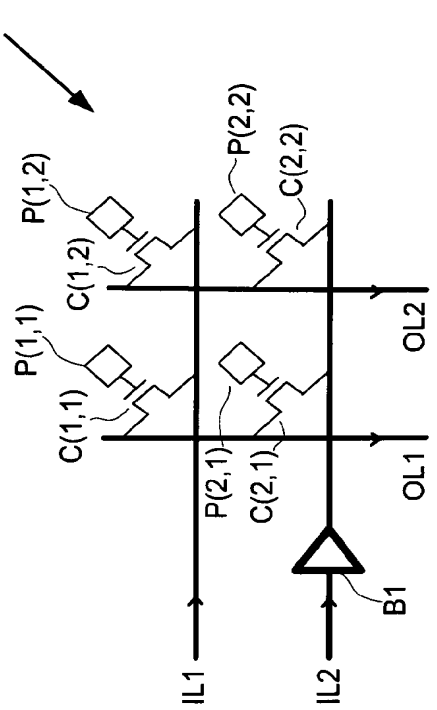


FIG. 5A2
(Prior Art)

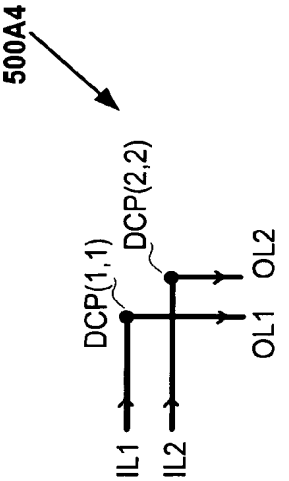


FIG. 5A4

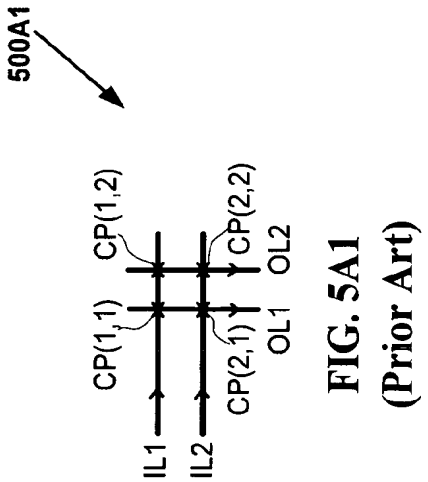


FIG. 5A1
(Prior Art)

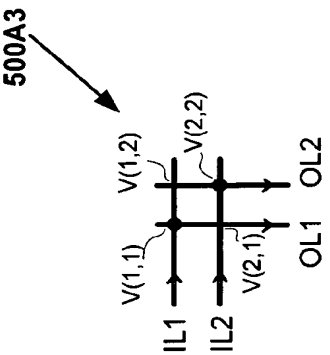


FIG. 5A3
(Prior Art)