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Paper 13
Entered: September 19, 2019

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

FLEX LOGIX TECHNOLOGIES INC.,
Petitioner,

v.

VENKAT KONDA,
Patent Owner.

Case PGR2019-00040
Patent 10,003,553 B2

Before PATRICK M. BOUCHER, CHARLES J. BOUDREAU, and NORMAN H. BEAMER, *Administrative Patent Judges*.

BOUCHER, *Administrative Patent Judge*.

DECISION
Denying Institution of Post-Grant Review
35 U.S.C. § 324

Flex Logix Technologies, Inc. ("Petitioner") filed a Petition (Paper 1, "Pet.") pursuant to 35 U.S.C. ¶¶ 321–329 to institute a post-grant review of claims 1–7, 9–15, and 17–19 of U.S. Patent No. 10,003,553 B2 ("the '553

patent"). Venkat Konda ("Patent Owner")[1] filed a Preliminary Response (Paper 5, "Prelim. Resp."). For the reasons set forth below, we exercise our discretion under 35 U.S.C. § 324 and deny the Petition.

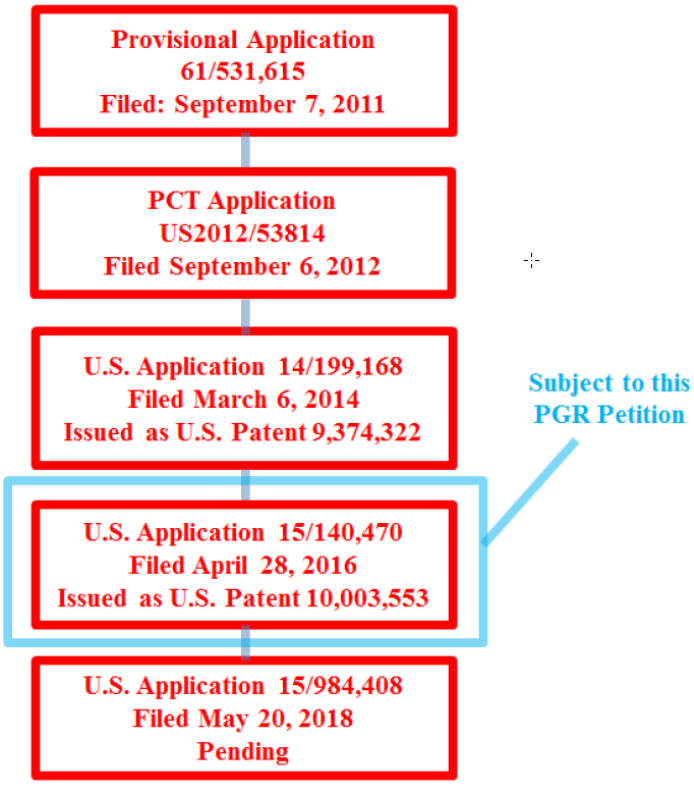
I. BACKGROUND

A. The '553 Patent

The '553 patent was filed on April 28, 2016, and claims the benefit of the following: (1) the March 6, 2014 filing date of U.S. Patent Appl. No. 14/199,168 (now issued as U.S. Patent No. 9,374,322 ("the '322 patent")); (2) the September 6, 2012 filing date of PCT/US12/53814 ("the '814 PCT application"); and (3) the September 7, 2011 filing date of Provisional Patent Appl. No. 61/531,615 ("the '615 provisional application"). Ex. 1001, 1:8–14; Ex. 1004, 1 (Certificate of Correction). A summary drawing provided by Petitioner is reproduced below. Pet. 4.

[1] The Petition identifies the owner of the '553 patent as Konda Technologies, Inc. Pet. 1. This appears to have been correct at the time the Petition was filed, on March 18, 2019. But on April 8, 2019, an assignment was recorded with the Office at reel/frame 048822/0867 assigning the '553 patent to Venkat Konda. This ownership is also reflected in Patent Owner's mandatory notices, filed on April 9, 2019. Paper 4.

PGR2019-00040
Patent 10,003,553



Petitioner's drawing summarizes certain claims to earlier filing dates, and is similar to a drawing provided by Patent Owner that is in substantial agreement. *See* Prelim. Resp. 7. Although the drawing also refers to U.S. Patent Appl. No. 15/984,408, that application is not relevant to this proceeding. In addition, the '553 patent recites that it incorporates the "entirety" of several additional patents and applications. *Id.* at 1:14–2:62.

The '553 patent relates to multi-stage interconnection networks that find utility in multiple applications. *Id.* at 2:66–3:1. According to the '553 patent, very large scale integration ("VLSI") layouts for integrated circuits with such networks can be "inefficient and complicated." *Id.* at 3:2–4. For example, prior-art networks of the type identified by the '553 patent "require large area to implement the switches on the chip, large number of wires, longer wires, with increased power consumption, increased latency of the

signals which [a]ffect the maximum clock speed of operation." *Id.* at 3:43–48.

Accordingly, the '553 patent discloses a number of configurations of multi-stage hierarchical networks. One example is illustrated in Figure 1A of the patent, reproduced below.

FIG. 1A

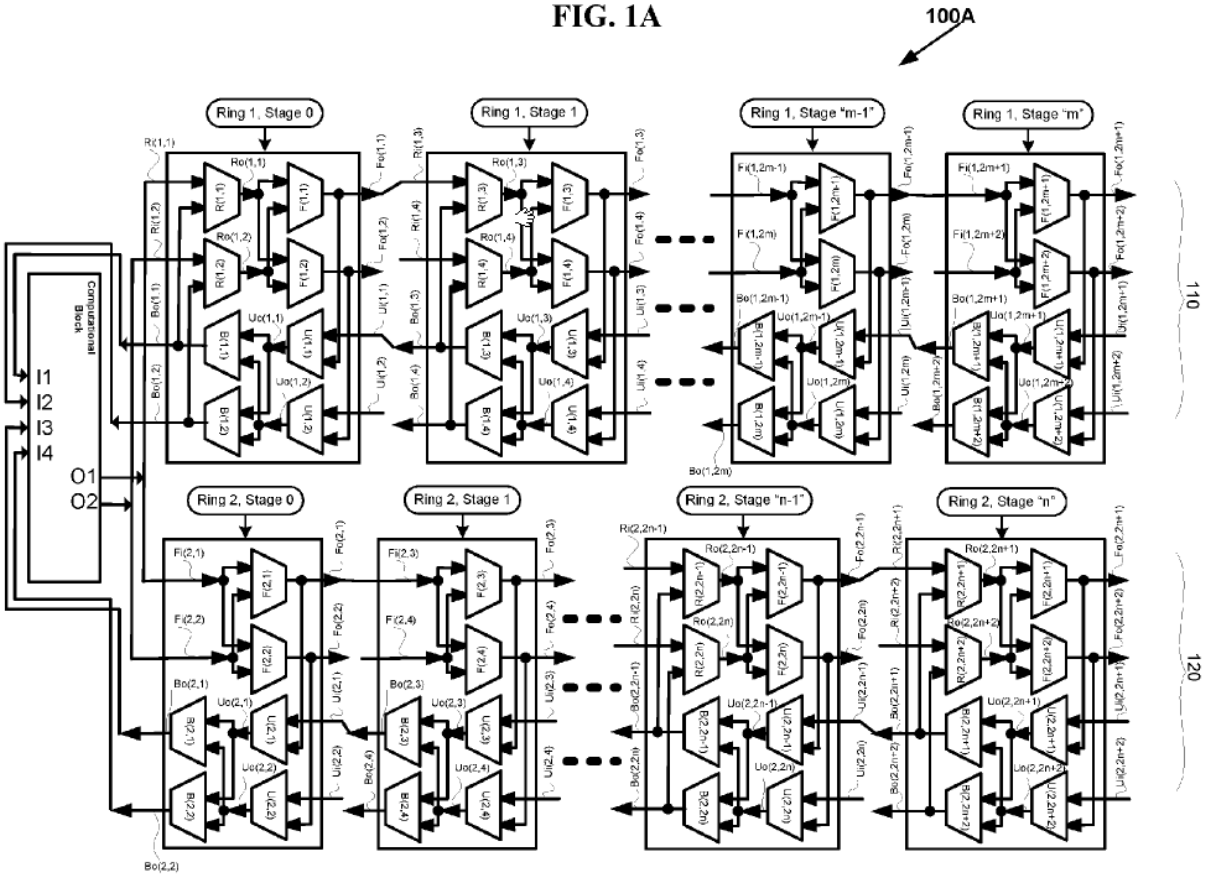


Figure 1A illustrates an exemplary partial multi-stage hierarchical network (or "block") in which each computational block has four inlet links I1, I2, I3, I4 and two outlet links O1, O2. *Id.* at 8:57–62. For each computational block, a corresponding partial multi-stage hierarchical network has two "rings" 110, 120. *Id.* at 8:62–9:3. Ring 110 has inlet links Ri(1,1), Ri(1,2) and outlet links Bo(1,1), Bo(1,2). *Id.* at 9:4–6. Ring 120 similarly has inlet

links Fi(2,1), Fi(2,2) and outlet links Bo(2,1), Bo(2,2). *Id.* at 9:5–6. The partial multi-stage hierarchical network thus has four inlet links and four outlet links corresponding to the two rings 110, 120. *Id.* at 9:6–9.

Several connections characterize the specific structure illustrated. First, outlet link O1 is connected to inlet link Ri(1,1) of ring 110 and also to inlet link Fi(2,1) of ring 120. *Id.* at 9:9–11. Second, outlet link O2 is connected to inlet link Ri(1,2) of ring 110 and also to inlet link Fi(2,2) of ring 120. *Id.* at 9:11–13. Third, outlet link Bo(1,1) of ring 110 is connected to inlet link I1. *Id.* at 9:14–15. Fourth, outlet link Bo(1,2) of ring 110 is connected to inlet link I2. *Id.* at 9:15–16. Fifth, outlet link Bo(2,1) of ring 120 is connected to inlet link I3. *Id.* at 9:17–18. Sixth, outlet link Bo(2,2) of ring 120 is connected to inlet link I4. *Id.* at 9:18–20. Because outlet link O1 is connected to both inlet link Ri(1,1) of ring 110 and inlet link Fi(2,1) of ring 120, and outlet link O2 is connected to both inlet link Ri(1,2) of ring 110 and inlet link Fi(2,2) of ring 120, the partial multi-stage hierarchical network has two inlet links and four outlet links. *Id.* at 9:20–26.

The drawing also illustrates multiple "stages." Ring 110 (i.e., ring 1) consists of m+1 stages, and ring 120 (i.e., ring 2) consists of n+1 stages. *Id.* at 8:65–9:1. For example, "ring 1, stage 0" has four inputs Ri(1,1), Ri(1,2), Ui(1,1), Ui(1,2) and four outputs Bo(1,1), Bo(1,2), Fo(1,1), Fo(1,2). *Id.* at 9:62–66. That stage also has eight 2:1 multiplexers R(1,1), R(1,2), F(1,1), F(1,2), U(1,1), U(1,2), B(1,1), B(1,2). *Id.* at 9:66–10:2. Multiplexer R(1,1) has two inputs Ri(1,1), Bo(1,1) and one output Ro(1,1). *Id.* at 10:2–3. Multiplexer R(1,2) has two inputs Ri(1,2), Bo(1,2) and one output Ro(1,2). *Id.* at 10:3–6. Multiplexer F(1,1) has two inputs Ro(1,1), Ro(1,2) and one

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