### Volume I Technical and Management Proposal

Title: Energy-Efficient Butterfly FPGA Hardware and Programming Tools

A proposal submitted to

Dr. William Harrod, DARPA/TCTO

in response to

**DARPA-BAA 10-78:** Omnipresent High Performance Computing (OHPC)

**Technical Area:** Energy Efficient Computing

**Lead Organization:** University of California, Los Angeles (UCLA)

Department of Electrical Engineering

Los Angeles, CA 90095-1594

**Type of Business:** Other Educational

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Total funds requested: \$2,374,111

Year 1: \$789,927 Year 2: \$792,100 Year 3: \$792,086

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### **Executive Summary**

UCLA offers to perform research on a revolutionary new FPGA technology consisting of FPGA hardware and supporting mapping tools. We will design, fabricate, and test hierarchical FPGA interconnect network to demonstrate FPGA technology that is 15x more energy-efficient than existing FPGAs. The new interconnect architecture allows for significant reduction in the number of switch points, buffers, and wire length in comparison to standard 2D-mesh architecture used by existing FPGAs. The proposed technology is a radical departure from 2D-mesh design, which for N logic blocks has complexity O(N²), incomplete and heuristic routing. The proposed technology has only O(N·log<sub>2</sub>N) complexity, complete and fully deterministic routing. The proposed technology has significant benefits: 15x lower power, 3x lower area, 2x higher performance compared to existing FPGA technology. The new FPGA technology will be used to demonstrate HPC benchmarks with a 15x higher power efficiency for DOD and commercial users. The PI has established interactions with industrial partners that will lead to the transition of ideas into the commercial space.



### **Section II - Technical Details**

### 2.1. PowerPoint Summary Chart

Performance (2x)

MC interface (160 pins/chip

With significant improvements:

Our FPGA chips

Power (15x)

Area (3x)

New FPGA hardware and mapping tools.

Expected Impact

N = 100 k

Z = 1 K

1 ≤ 10 B

9,97 k

1.66 M

6,200x 100x **Number of LUTs** 

2D-Mesh

Hierarchical

Savings factor

# For DOD and commercial apps. with 15x higher power efficiency. To demonstrate HPC benchmarks

### Objective: significantly improve energy efficiency of FPGAs Problem: Presently, FPGA chips use 2D-mesh architecture, which is very complex (over 75% of chip area is interconnect). Interconnect results in energy-inefficient computations. **Energy Efficiency** (MOPS/mW) 0.01 0.1 100 10 Technical Challenge and Objective Microprocessors • 4 σ 6 8 9 10 11 12 13 14 15 16 17 18 19 20 Chip Number 30-50x Purpose DSPs and FPGAs Dedicated magnitude! 3 orders of

### Connection Number of connections in 2D-Mesh and Hierarchical networks 2D-Mesh Network Switch-3x reduction in units, there is a the number of Even with just 4 processing connections $(24) \to (8)$

 Our hierarchical butterfly interconnect scheme significantly reduces interconnect complexity. **Key Innovations** 

Connection-

**Energy-Efficient Butterfly FPGA Hardware and Programming Tools** 

### Key proposed innovations: 2D-Mesh FPGA — Our FPGA

- Ideas verified on chip (3x reduction in interconnect area).
  - >2x performance improvement >2x overall chip area reduction >10x lower power
- Interconnect architecture optimization.
- Hardware demonstrations of area, power, and performance.
- Mapping tools for the new FPGA architecture.

Demonstrations of HPC benchmarks. PI: Dejan Markovic (UCLA)



**Butterfly Network** 

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