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Paper 22
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

FLEX LOGIX TECHNOLOGIES, INC.,
Petitioner,

v.

VENKAT KONDA,
Patent Owner.

IPR2020-00261
Patent 8,269,523 B2

Before SALLY C. MEDLEY, THOMAS L. GIANNETTI, and JO-ANNE M. KOKOSKI, *Administrative Patent Judges.*

KOKOSKI, *Administrative Patent Judge.*

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Flex Logic Technologies, Inc., ("Petitioner") filed a Petition to institute an *inter partes* review of claims 2–7 and 11 (the "challenged claims") of U.S. Patent No. 8,269,523 B2 ("the '523 patent," Ex. 1001). Paper 1 ("Pet."). Patent Owner Venkat Konda filed a Preliminary Response. Paper 9 ("Prelim. Resp."). With Board authorization, Petitioner filed a reply addressing certain issues raised in the Preliminary Response ("Reply," Paper 13), and Patent Owner filed a Sur-reply ("Sur-Reply," Paper 16). At the Board's direction (Paper 12), Petitioner filed a Notice explaining its reasons for filing multiple petitions challenging the claims of the '523 patent. Paper 15 ("Notice"). Patent Owner filed a Reply to Petitioner's Notice. Paper 18 ("Notice Reply").

Institution of an *inter partes* review is authorized by statute when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314 (2018); *see* 37 C.F.R. § 42.4 (2019). Upon consideration of the Petition, the Preliminary Response, the Reply, the Sur-Reply, the Notice, the Notice Reply, and the evidence of record, we determine that Petitioner has established a reasonable likelihood of prevailing with respect to the unpatentability of at least 1 claim of the '523 patent. Accordingly, for the reasons that follow, we institute an *inter partes* review of claims 2–7 and 11 of the '523 patent.

A. Related Proceedings

Petitioner identifies the following district court proceeding involving the '523 patent: *Konda Technologies Inc. v. Flex Logix Technologies, Inc.*, No. 5:18-cv-07581 (N.D. Cal.). Pet. 2.

The '523 patent is the subject of two other *inter partes* review proceedings filed by Petitioner: IPR2020-00260 ("260 IPR") and IPR2020-00262 ("262 IPR"). Prelim. Resp. 1, n.1. Also, two post grant proceedings brought by the Petitioner challenging a related patent are pending: PGR2019-00037, and PGR2019-00042. Pet. 2. A third petition for post grant review of that related patent (PGR2019-00040) was denied. *Id.*

Patent Owner additionally identifies a pending application to reissue the '523 patent: U.S. Patent Application No. 16/202,067, filed November 27, 2018 ("the '067 reissue application"). Paper 6, 2.

B. Real Parties-in-Interest

Petitioner identifies Flex Logix Technologies, Inc., as the real party-in-interest. Pet. 1. Patent Owner identifies himself, Venkat Konda, as the real party-in-interest. Paper 6, 1.

C. The '523 Patent

The '523 patent is titled "VLSI Layouts of Fully Connected Generalized Networks." Ex. 1001, code (54). The most commonly used VLSI (Very Large Scale Integration) layout in an integrated circuit is based on a two-dimensional grid model comprising only horizontal and vertical tracks. *Id.* at 2:40–42. The '523 patent describes VLSI layouts of generalized multi-stage networks for broadcast, unicast, and multicast connections using only horizontal and vertical links. *Id.* at 3:21–24. The

VLSI layouts employ shuffle exchange links, where outlet links of cross links from switches in a stage in one sub-integrated circuit block are connected to inlet links of switches in the succeeding stage in another sub-integrated circuit block. *Id.* at 3:24–28. The cross links are either vertical links or horizontal, and vice versa. *Id.* at 3:28–29.

In one embodiment, the sub-integrated circuit blocks are arranged in a hypercube arrangement in a two-dimensional plane. *Id.* at 3:29–31. The VLSI layouts exploit the benefits of significantly lower cross points, lower signal latency, lower power, and full connectivity with significantly fast compilation. *Id.* at 3:31–34.

D. Illustrative Claims

Petitioner challenges dependent claims 2–7 and 11 of the '523 patent. Pet. 1, 4. Claim 2 directly depends from claim 1, which is the only independent claim in the '523 patent. Claims 1 and 2 are reproduced below.

> 1. An integrated circuit device comprising a plurality of sub-integrated circuit blocks and a routing network, and
> Said each plurality of sub-integrated circuit blocks comprising a plurality of inlet links and a plurality of outlet links; and
>
> Said routing network comprising of a plurality of stages y, in each said sub-integrated circuit block, starting from the lowest stage of 1 to the highest stage of y, where y≧1; and
>
> Said routing network comprising a plurality of switches of size d×d, where d≧2, in each said stage and each said switch of size d×d having d inlet links and d outlet links; and
>
> Said plurality of outlet links of said each sub-integrated circuit block are directly connected to said inlet links of said switches of its corresponding said lowest stage of 1, and said plurality of inlet links of said each sub-integrated circuit block

are directly connected from said outlet links of said switches of its corresponding said lowest stage of 1; and

Said each sub-integrated circuit block comprising a plurality of forward connecting links connecting from switches in a lower stage to switches in its immediate succeeding higher stage, and also comprising a plurality of backward connecting links connecting from switches in a higher stage to switches in its immediate preceding lower stage; and

Said each sub-integrated circuit block comprising a plurality straight links in said forward connecting links from switches in said each lower stage to switches in its immediate succeeding higher stage and a plurality cross links in said forward connecting links from switches in said each lower stage to switches in its immediate succeeding higher stage, and further comprising a plurality of straight links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage and a plurality of cross links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage,

said plurality of sub-integrated circuit blocks arranged in a two-dimensional grid of rows and columns, and

said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks which are either placed vertically above or below, or placed horizontally to the left or to the right,

each said plurality of sub-integrated circuit blocks comprising same number of said stages and said switches in each said stage, regardless of the size of said two-dimensional grid so that each said plurality of sub-integrated circuit block with its

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