UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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FLEX LOGIX TECHNOLOGIES INC,

Petitioner

V.

VENKAT KONDA,

Patent Owner

_____

Case IPR2020-00261

Patent 8,269,523 B2

_____

DECLARATION OF VENKAT KONDA

I, Venkat Konda, make this declaration in connection with the proceedings

identified above.

1.　　I am the sole inventor of U.S. Patent No. 8,269,523 ("the '523

Patent"). I submit this declaration in support of Patent Owner's Preliminary

Response to the Petition for *Inter Partes* Review in Case IPR2020-00261 filed by

Petitioner Flex Logix Technologies Inc. ("Petitioner") challenging claims 2-7 and

11 (the "Challenged Claims") of the '523 Patent. Paper 1.

2.　　I earned a Bachelor of Technology in Electronics and

Communications Engineering from Nagarjuna University in Vijayawada, India

in1986, a Master of Technology in Electrical Engineering from the Indian Institute

of Technology in Kharagpur, India in 1988, and a Ph.D. in Computer Science and

Engineering from the University of Louisville, Kentucky in 1992.

3.　　I have over 25 years of Research and Development and Management

experience in various semiconductor integrated circuit and systems companies

with extensive experience in interconnection networks including nCube

Corporation from March 1992 to March 1995, Mitsubishi Electric Research Labs

and VSIS Inc. from April 1995 to July 1998, Infineon Technologies from July

1998 to December 2000, and Velio Communications from December 2000 to June

2001. I was the founder of Teak Networks Inc. in August 2001 and CEO from

August 2001 until March 2007. I was also co-founder of Teak Technologies Inc.

founded in February 2005 and CTO from February 2005 until April 2006.

4.   In 1994-95, I taught graduate courses related to **interconnection**

networks as an adjunct faculty member in the department of Computer Science

and Engineering, Santa Clara University, Santa Clara, CA.

5.   I founded Teak Networks Inc. after solving an approximately 60-year-

old research problem by inventing strictly and rearrangeably non-blocking multi-

cast solutions for Clos Networks. I have been granted several related patents for

that technology including U.S. Patents No. 6,885,669, 6,868,084, 7,424,010,

7,424,011 and 7,378,938 by the United States Patent and Trademark Office

("USPTO").

6.   I founded Konda Technologies, Inc. ("Konda Tech"), in 2007, after

solving approximately 30-year-old open research problems by inventing strictly

and rearrangeably non-blocking multi-cast solutions for Benes and Butterfly Fat

Tree Networks and the seminal 2D-layouts to implement those networks using

only vertical and horizontal wires. I am a pioneer in multi-stage based field-

programmable gate array ("FPGA") routing fabric and interconnection networks

technology. Konda Tech was founded to commercialize semiconductor integrated

circuits and system level interconnection technology solutions based on my work.

7.   Konda Tech licenses chip and system level interconnection

technology solutions to the commercial semiconductor industry. To date, Konda

Tech has eleven patents relating to the technology. Konda Tech has licensed

FPGA interconnection architecture patents to two FPGA chip vendors, the first of

which has made and sold three generations of chips using the 2D-layouts disclosed

in the '523 Patent.

8.   A selected list of some of my publications is attached in Appendix A.

I hereby declare under penalty of perjury under the laws of the United States of

America that all statements made herein of my own knowledge are true and that all

statements made herein on information and belief are believed to be true, and that

these statements were made with the knowledge that willful false statements and

the like so made are punishable by fine or imprisonment, or both, under Section

1001 of Title 18 of the United States Code.

Dated: May 6, 2020   Respectfully submitted,

                                                            /Venkat Konda/
                                                            Venkat Konda

PARTIAL LIST OF SOME SELECTED PUBLICATATIONS

1) **Rearrangeably nonblocking multicast multi-stage networks**
   - Priority Date: September 27, 2001
   - US Patent Application Number: 09/967,815
   - US Patent Number: US 6,885,669
   - Date of Patent: April 26, 2005

2) **Strictly nonblocking multicast multi-stage networks**
   - Priority Date: September 27, 2001
   - US Patent Application Number: 09/967,106
   - US Patent Number: US 6,868,084
   - Date of Patent: March 15, 2005

3) **Strictly non-blocking Multicast Multi-split Linear-time Multi-stage Networks**
   - Priority Date: September 6, 2003
   - US Patent Application Number: 10/933,900
   - US Patent Number: US 7,424,010
   - Date of Patent: September 9, 2008

4) **Rearrangeably nonblocking multicast multi-stage networks**
   - Priority Date: September 27, 2001
   - US Patent Application Number: 10/999,757
   - US Patent Number: US 7,424,011
   - Date of Patent: September 9, 2008

5) **Strictly nonblocking multicast multi-stage networks**
   - Priority Date: September 27, 2001
   - US Patent Application Number: 10/999,649
   - US Patent Number: US 7,378,938
   - Date of Patent: March 27, 2008

6) **Fully Connected Generalized Multi-stage Networks**
   - Priority Date: March 6, 2007
   - US Patent Application Number: 12/530,207
   - US Patent Number: US 8,270,400
   - Date of Patent: September 18, 2012

7) **Fully Connected Generalized Butterfly Fat Tree Networks**
   - Priority Date: March 25, 2007
   - US Patent Application Number: 12/601,273
   - US Patent Number: US 8,170,040

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