

[54] EDGE-SENSITIVE DYNAMIC SWITCH

[56]

References Cited

[75] Inventor: Thomas D. Fletcher, Orem, Utah

U.S. PATENT DOCUMENTS

4,039,858 8/1977 Stewart .

[73] Assignee: North American Philips Corporation,
Signetics Division, Sunnyvale, Calif.

FOREIGN PATENT DOCUMENTS

0242721 12/1985 Japan 307/576

[21] Appl. No.: 180,425

Primary Examiner—John Zazworsky
Attorney, Agent, or Firm—R. Meetin; D. Treacy; T.
Briody

[22] Filed: Apr. 8, 1988

[57]

ABSTRACT

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 934,753, Nov. 25,
1986, Pat. No. 4,740,717.

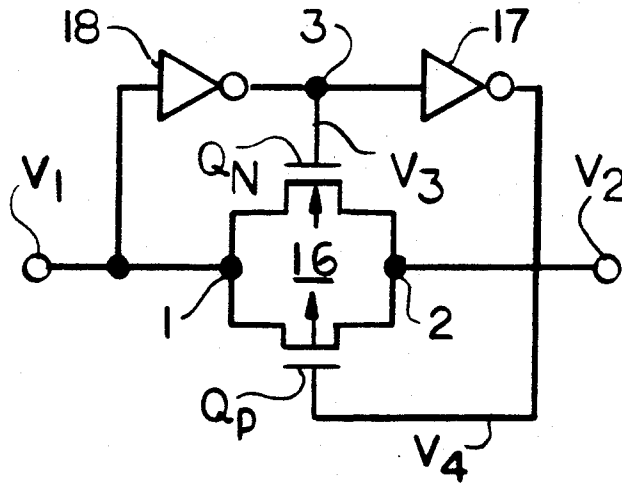
An edge-sensitive dynamic switch center around a transmission gate (16) formed with a pair of complementary FET's (Q_N and Q_P) coupled together in parallel between a pair of nodes (1 and 2). The signals at the two nodes vary between a low voltage level and a high voltage level. An inverter (17) is coupled between the gate electrodes of the FET's. A delay element (18) is coupled between one of the nodes and one of the gate electrodes. Due to the transmission delays through the delay element and the inverter, the switch turns off with a controlled delay.

[51] Int. Cl.⁴ H03K 5/153

[52] U.S. Cl. 307/605; 307/573;
307/576; 307/594; 307/517

[58] Field of Search 307/443, 573, 575, 576,
307/585, 597, 601, 605, 266, 261, 517, 518, 594,
273; 328/114

11 Claims, 5 Drawing Sheets



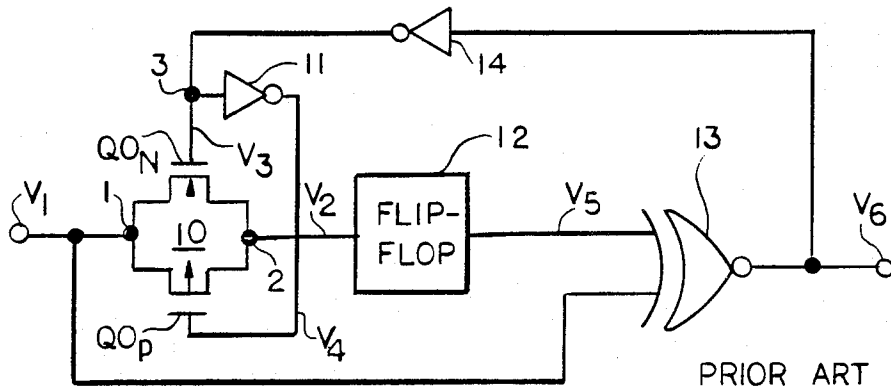


Fig. 1

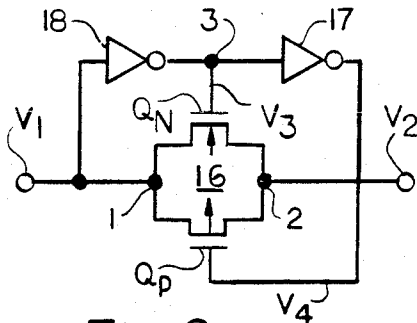


Fig. 2a

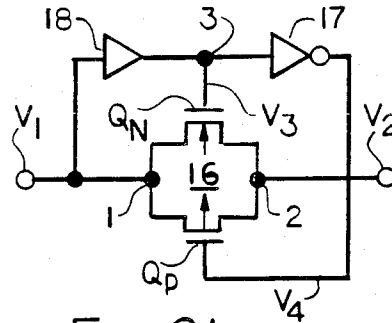


Fig. 2b

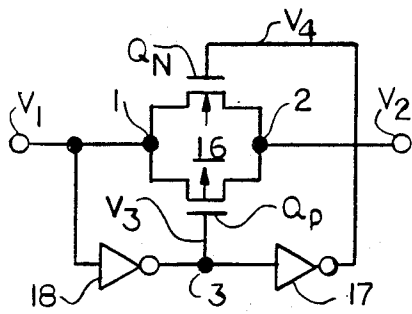


Fig. 2c

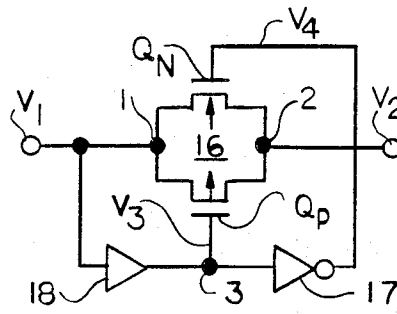
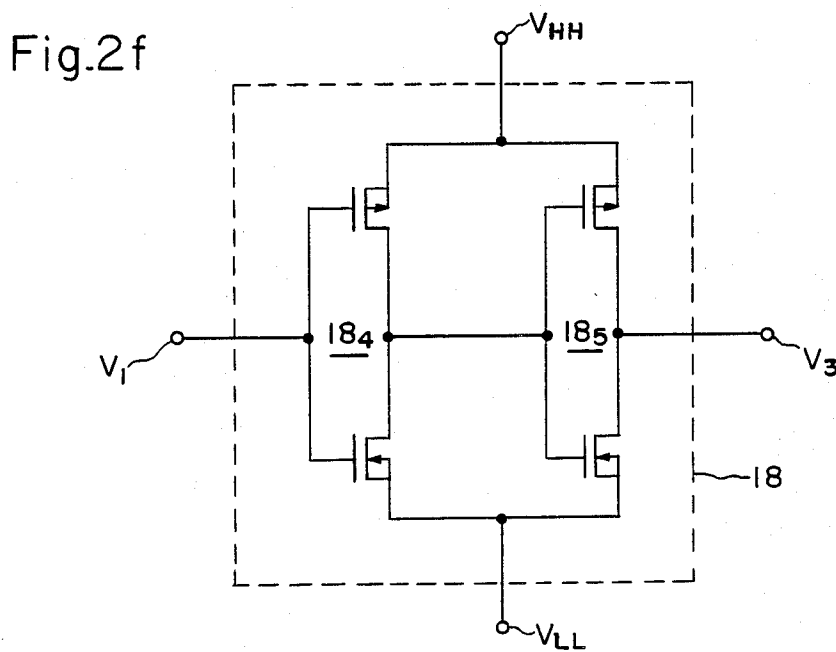
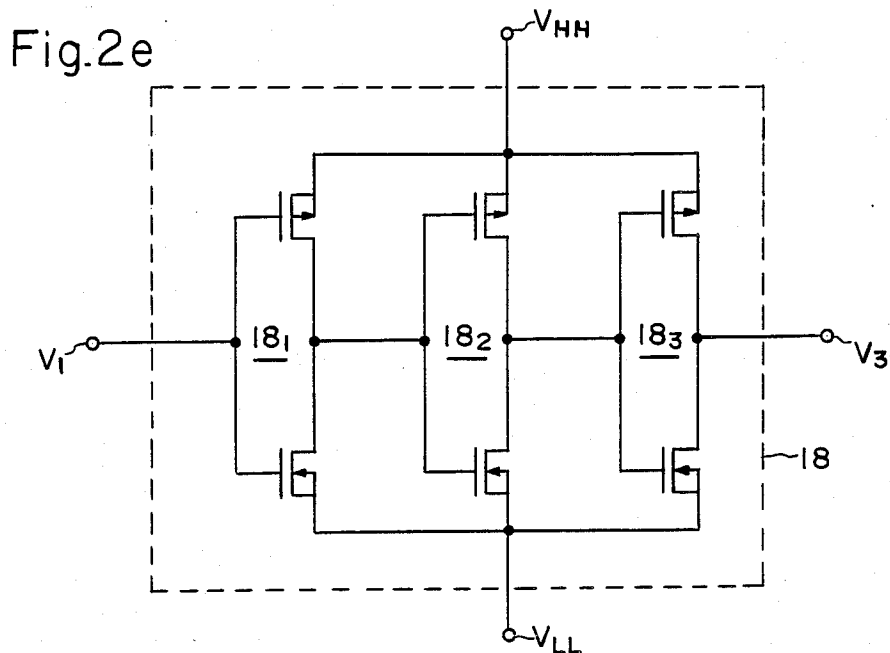


Fig. 2d



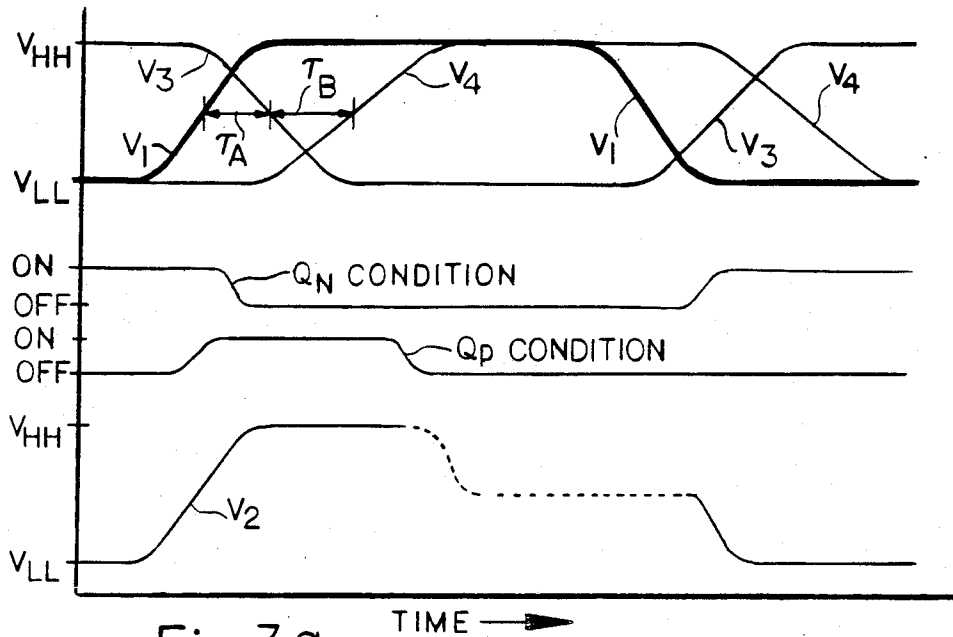


Fig. 3a

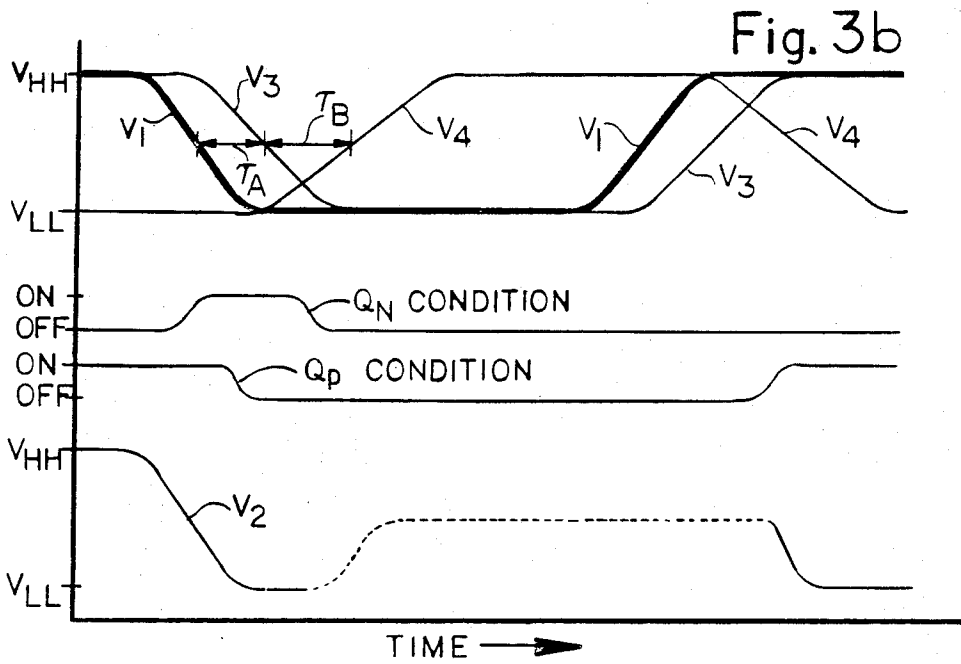
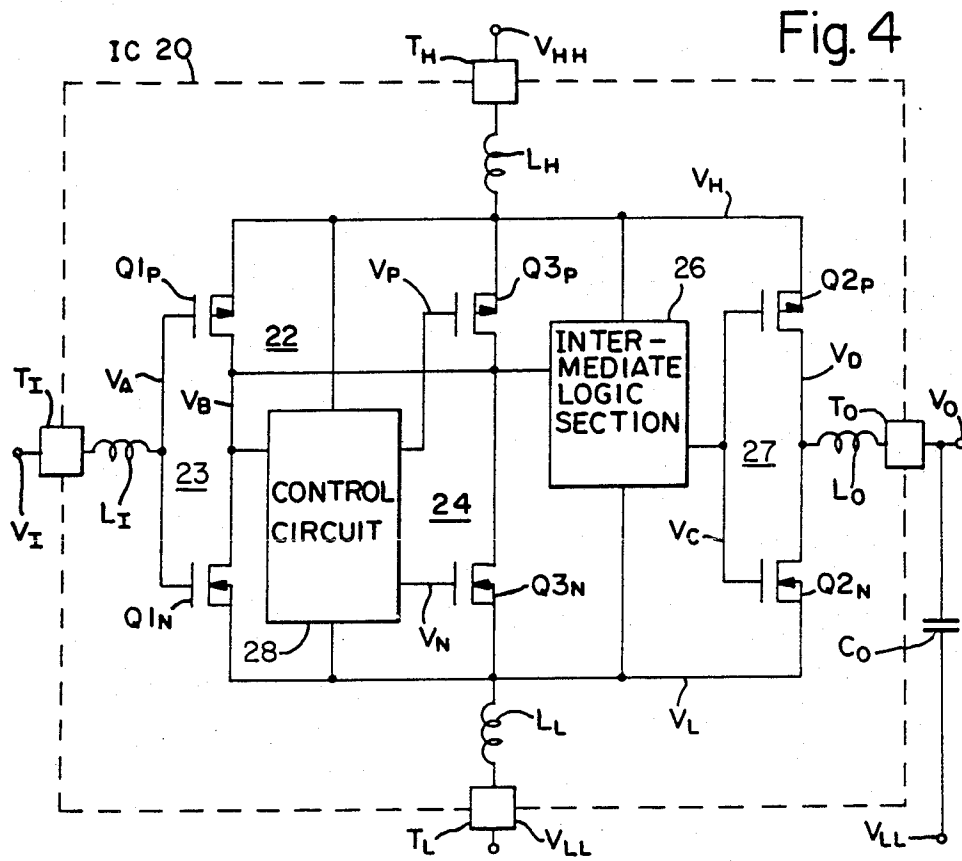


Fig. 3b



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