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Plaintiff *pro se*



**IN THE SUPERIOR COURT OF THE STATE OF CALIFORNIA**

**COUNTY OF SANTA CLARA**

**VENKAT KONDA, Ph.D., an individual,**

**Plaintiff,**

**v.**

**DEJAN MARKOVIC, Ph.D., an individual; CHENG C. WANG, Ph.D., an individual; FLEX LOGIX TECHNOLOGIES, INC., a Delaware Corporation; THE REGENTS OF THE UNIVERSITY OF CALIFORNIA; GEOFFREY TATE, an individual; PIERRE LAMOND, an individual; PETER HEBERT, an individual; LESLIE M. LACKMAN, Ph.D., an individual; and DOES 1-20, inclusive,**

**Defendants.**

**Case No. 19CV345846**

**Unlimited Civil Case**

**PLAINTIFF'S FOURTH AMENDED COMPLAINT FOR:**

1. **Unfair Business Practices**
2. **Unfair Competition - Passing off**
3. **Fraud: Intentional Misrepresentation**
4. **Fraud: Concealment**
5. **Conversion**
6. **Breach of Confidential Relationship**
7. **Intentional Interference With Prospective Economic Relations**
8. **Ongoing Conspiracy**

**Department: 2**
**Before: Honorable Drew C. Takaichi**

**Date Complaint Filed: April 3, 2019**
**Trial Date: None**

**DEMAND FOR JURY TRIAL**

Plaintiff Venkat Konda, Ph.D. (hereinafter referred to as "Dr. Konda" or "Plaintiff") alleges as follows in this Fourth Amended Complaint:

1. This case involves a surreptitious scheme by a professor, Dejan Markovic, Ph.D. (hereinafter referred to as "Defendant Markovic" or "Markovic") who recruited and conspired with one of the graduate students he advised, Cheng C. Wang, Ph.D. (hereinafter referred to as "Defendant Wang" or "Wang"), (hereinafter collectively referred to as "Defendants Markovic and Wang"), at the University of California Los Angeles (hereinafter referred to as "UCLA") which is part of the University of California system, to falsely claim innovation of certain technology by covertly implementing Dr. Konda's innovations, publishing technical papers as if it were their technology, and receiving illicit financial benefits, by passing off Dr. Konda's innovations pilfered from Dr. Konda and his Silicon Valley company, Konda Technologies, Inc. (hereinafter referred to as "Konda Tech") as their own. Through deception and manipulation (i.e., constantly trolling for and obtaining confidential business know-how, and product know-how for years starting in 2009 – 2014 by blatantly lying and brazenly concealing their misdeeds under the cloak of legitimacy afforded by their association with UCLA, which has knowingly benefitted from illicitly commercializing Dr. Konda's innovations. Defendants Markovic and Wang used Dr. Konda's confidential information disclosed by Dr. Konda to Defendant Markovic in confidence and additional documents including the text and diagrams published in Dr. Konda's published patent applications and patents without authorization or attribution to launch commercial products without the knowledge of Dr. Konda, through a now-dissolved California Corporation Hierlogix, Inc. formed by Defendants Markovic and Wang with funding by UCLA's Institute for Technology Advancement (hereinafter referred to as "UCLA/ITA") and its successor Defendant Flex Logix Technologies, Inc. (hereinafter referred to as "Flex Logix").

2. Dr. Konda's confidential business information and practices relates to Field Programmable Gate Arrays (hereinafter referred to as "FPGAs"). FPGAs are semiconductor devices that comprise a matrix of configurable logic blocks (CLBs) having one or more Lookup Tables connected via a programmable interconnection network. After being fabricated, FPGAs can be reprogrammed for a desired application or functionality requirements. They are used in many different applications from simple devices such as calculators to sophisticated artificial intelligence (AI) systems that require high-speed logic operations. FPGAs can perform these

operations faster than a software application running on a computer's central processing unit (CPU).

3. Defendant Markovic was introduced to Dr. Konda by Flavio Bonomi, Ph.D. (hereinafter referred to as "Dr. Bonomi"), who was a Cisco Fellow, Vice President and the Head of the Advanced Architecture and Research Organization at Cisco Systems, Inc. in San Jose, California (hereinafter referred to as "Cisco") in 2009. After funding was orally offered by the Cisco Angel Network (based on Dr. Konda's goodwill in the industry), but later rescinded, Defendant Markovic reached out to Dr. Konda to troll for information beginning in or around March, 2009 and continuing through at least March, 2014.

4. Unbeknownst to Dr. Konda, Defendant Markovic seized the opportunity by conspiring with Defendant Wang, then a Ph.D. candidate studying under Markovic and looking for a Ph.D. Dissertation topic, to immediately begin implementing integrated circuit devices based on the disclosures in the 2008 Konda Publications without authorization from Dr. Konda or Konda Tech.

5. On the pretense of obtaining funding for Konda Tech, Defendant Markovic arranged for a presentation by Dr. Konda to UCLA/ITA including Defendant Leslie M. Lackman, Ph.D. (hereinafter referred to as "Dr. Lackman") on October 12, 2009, obtaining proprietary and confidential materials from Dr. Konda five days prior to the presentation in confidence. However, funding was not forthcoming because, as Defendant Markovic knew beforehand but concealed from Dr. Konda, the prerequisite nexus of a relationship between UCLA and Dr. Konda or Konda Tech did not exist. Nevertheless, within less than two months after the presentation to UCLA/ITA, in December, 2009, unbeknownst to Dr. Konda at that time, Defendant Wang covertly implemented and fabricated FPGA devices comprising CLBs and interconnect using published information through the graduate program at UCLA under the guidance of Defendant Markovic without Plaintiff's authorization.

6. Finding a research topic for a doctoral dissertation is the single most challenging task for a Ph.D. student, such as Defendant Wang. A Ph.D. advisor's first task is to let his student know how to carefully conceive a novel topic. It is very common for a Ph.D. student to propose a

concept and later learn that it was already pursued by someone earlier. And, the Ph.D. student must then find another research topic. However, here, Defendant Markovic in concert with Defendant Wang knowingly, brazenly chose to implement Dr. Konda's innovations as his topic. As a result, Defendant Wang's Ph.D. dissertation is essentially a plagiarization of Dr. Konda's published patent applications and patents and additional confidential information obtained by Defendant Markovic from Dr. Konda through a confidential relationship.

7. Defendants Markovic and Wang fraudulently based Defendant Wang's Ph.D. dissertation on Dr. Konda's innovations and then proceeded to commercialize their surreptitious work as a business opportunity to make financial gains, refusing to acknowledge the ownership of Dr. Konda, and in the process damaging Konda Tech and Dr. Konda.

8. Without disclosing that Defendants Markovic and Wang had implemented FPGA devices based on Dr. Konda's publications, Markovic eight to nine months after Dr. Konda's confidential presentation to UCLA/ITA including Dr. Lackman, contacted Dr. Konda to solicit him to submit a confidential joint proposal to DARPA. When Dr. Konda learned that covert work had been carried out without his authorization at UCLA as described in the draft confidential DARPA proposal prepared by Defendant Markovic, Dr. Konda told Markovic that Markovic was not authorized to have done that work and to cease any further work at UCLA. However, again on the pretense of obtaining funding for Konda Tech, but in actuality to obtain funding for Markovic's and Wang's development of software tools to program FPGA devices they had covertly implemented, Dr. Konda agreed to the submission of the confidential DARPA proposal with Dr. Konda as the Principal Investigator, because Defendant Markovic promised Dr. Konda that if the confidential DARPA proposal were to be granted, Markovic would obtain a license to carry on any further work at UCLA; otherwise Markovic promised that he would cease any further implementation of Dr. Konda's innovations at UCLA **as an academic project only**.

9. Approximately five weeks later while the first confidential DARPA proposal was still pending, Defendant Markovic then solicited Dr. Konda to join in submitting a second confidential DARPA proposal, but with UCLA as the Principal Investigator. Defendant Markovic again promised Dr. Konda that if the second confidential DARPA proposal were to be

granted, he would agree to a license to carry out any further work at UCLA, and otherwise Markovic would cease all further implementation of Dr. Konda's innovations at UCLA **as an academic project only**.

10. Both of the confidential DARPA proposals were rejected in late 2010. At that point, Dr. Konda believed that all of the FPGA device work incorporating Dr. Konda's patent applications and patents and confidential information disclosed by Dr. Konda in connection with the confidential DARPA proposals at UCLA had ceased, **as an academic project only,** based on the prior representations of Defendant Markovic.

11. At or around that time, Dr. Konda contacted Defendant Markovic to inform him in confidence that Konda Tech had licensed a commercial FPGA supplier, QuickLogic Corporation (hereinafter referred to as "QuickLogic"), with whom Dr. Konda had worked between late September, 2010 and mid-January, 2011 to prove the value of Dr. Konda's innovations. Defendant Markovic seized that opportunity to troll for confidential information regarding Dr. Konda's work with QuickLogic. Dr. Konda informed Defendant Markovic in confidence regarding the licensee information and other confidential business information. Defendant Markovic was keenly interested in this information and further inquired what other FPGA suppliers Dr. Konda had contacted. At that time Markovic misrepresented to Dr. Konda that he and his students had stopped implementing Dr. Konda's innovations.

12. Unbeknownst to Dr. Konda, Defendants Markovic and Wang concealed that they had formed Hierlogix Inc. ("Hierlogix") on January 4, 2011 with its principal place of business at Defendant Wang's private residence. Hence, Defendants Markovic and Wang stopped the academic project of implementing the disclosures in the 2008 Konda Publications using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals which Dr. Konda had previously disclosed to Defendant Markovic in confidence and brazenly, but covertly started commercializing the results of their purported academic work without a license or authorization from Dr. Konda.

13. Unbeknownst to Dr. Konda, Defendants Markovic and Wang raised funding from UCLA/ITA for Hierlogix. Hierlogix is substantially based on confidential business knowledge and practices based on the confidential and propriety presentation given by Dr. Konda to UCLA/ITA on October 12, 2009 and the confidential DARPA proposals.

14. Unbeknownst to Dr. Konda at that time, Defendants Markovic and Wang also concealed that they had submitted a paper based on Dr. Konda's innovations in January 2011 to the VLSI Symposium without any authorization by or attribution to Dr. Konda. More particularly, the paper was based on Konda Tech's 2D BFT layouts which are the cornerstone for achieving area, power, and performance improvements in FPGAs. The paper was presented by Defendants Markovic and Wang as their own innovation at the VLSI Symposium in June 2011.

15. Also, unbeknownst to Dr. Konda, Defendant Wang was completing his Ph.D. program under the guidance of Defendant Markovic and submitted his dissertation based on the covert implementation of Dr. Konda's innovations without attribution to Dr. Konda, yet Wang was awarded his Ph.D. in June 2013 and recognized for having submitted a distinguished Ph.D. dissertation under the supervision of Defendant Markovic.

16. In April 2013, Defendant Markovic invited Dr. Konda by email to meet him at Stanford University while Markovic represented that he was a "Visiting Professor." When they met, Dr. Konda inquired to confirm whether Defendant Markovic and his students had indeed discontinued implementing Dr. Konda's innovations as part of the academic work at UCLA. Defendant Markovic falsely replied "yes." During the conversation, Defendant Markovic also asked Dr. Konda to inform him in confidence of the names of customers Dr. Konda was currently working with. Thus, Defendant Markovic repeatedly trolled for Dr. Konda's confidential business knowledge and practices which Dr. Konda disclosed in confidence believing that Defendant Markovic was helping to find funding and/or business opportunities for Dr. Konda, while all the time Markovic was misrepresenting and concealing facts as to Defendants Markovic's and Wang's activities.

17. In January, 2014, while Defendant Markovic represented himself to be a "Visiting Professor" at Stanford University, Dr. Konda and Defendants Markovic and Wang were invited

to a meeting with Dr. Bonomi at his residence. Dr. Bonomi had recently founded a startup company, Nebliolo Technologies, Inc. (hereinafter referred to as "Nebliolo") and was interested in obtaining a supplier of FPGAs based on Dr. Konda's innovations. He invited Defendants Markovic and Wang whom he understood had founded a semiconductor design company that he thought might be able to develop FPGAs based on Dr. Konda's innovations in an embedded FPGA block to supply to Nebliolo. At that meeting, Defendant Markovic mentioned that he was in the process of raising funding for a startup company. When Dr. Konda queried Markovic if the startup was in the area of wireless and digital signal processors (DSPs), Defendant Markovic said "yes," which was an intentional misrepresentation. Defendant Markovic concealed the facts that Hierlogix had been founded by Markovic and Wang three years earlier to commercialize FPGAs and that the technological focus of the startup for which he was seeking funding was to produce embedded FPGA blocks (hereinafter referred to as "eFPGAs") covertly implementing Dr. Konda's innovations without having a license.

18. Unbeknownst to Dr. Konda at that time, Defendants Markovic and Wang concealed the fact that they were involved in founding Defendant Flex Logix on February 26, 2014 as the successor to Hierlogix to continue the commercialization of eFPGA blocks implementing and passing off Dr. Konda's innovations as their own innovations.

19. In or about December, 2015 Dr. Konda arranged to meet with Professor Vaughn Betz, Ph.D. (hereinafter referred to as "Dr. Betz") in the Department of Electrical and Computer Engineering at the University of Toronto, Toronto, Canada, to discuss certain results Dr. Konda had achieved with the Versatile Place and Route (hereinafter referred to as "VPR") tool suite developed by Dr. Betz using VPR to implement Dr. Konda's innovations. Dr. Konda met with Dr. Betz in Toronto on or about December 18, 2015. During their meeting, Dr. Betz asked Dr. Konda if he had heard of Flex Logix. Dr. Konda responded that he was not aware of Flex Logix. Nor was Dr. Konda aware of any paper submitted by Defendants Markovic and Wang, Wang's Ph.D. dissertation, Hierlogix, or Flex Logix at the time of his meeting with Dr. Betz on December 18, 2015.

20. After returning to California after his meeting with Dr. Betz on December 18, 2015, Dr. Konda began to investigate to uncover facts regarding the activities of Defendants Markovic and Wang and to investigate Flex Logix. In his pursuit to uncover the facts, Dr. Konda prepared an email which he sent to Flex Logix and UCLA and others on March 27, 2016 requesting additional information from, and action by, those entities regarding possible wrongdoing that he first suspected had occurred on the part of Defendants Markovic and Wang when his investigation yielded information during the weekend of March 26-27, 2016, when he first formed a suspicion that Flex Logix appeared to be implementing eFPGAs based on Dr. Konda's innovations.

21. Due to the intentional misrepresentations and concealment of Defendants Markovic and Wang, Dr. Konda was unsuspecting until that time of the illicit activities of Markovic and Wang until he was able to piece together the facts included in his March 27, 2016 email. Until then, Dr. Konda was in disbelief that Defendant Markovic would have betrayed the confidences and trust of the relationship he believed he had with Dr. Markovic, who cloaked himself with and exploited the pretextual credibility of UCLA, heretofore promoted as a respected educational institution, but now exposed as a commonplace cutthroat competitor whose employees (*i.e.*, Defendant Markovic) deprive unsuspecting inventors of their innovations. In view of the intentional misrepresentations, concealment, and breach of the confidential relationship by Defendant Markovic and his co-conspirator Wang, the facts regarding their wrongdoing were concealed and thus not previously discoverable or known by Dr. Konda. At the time that he prepared his March 27, 2016 email, Dr. Konda realized for the first time that he has been harmed by the concealed, unauthorized commercialization of Dr. Konda's innovations by the Defendants.

22. Beginning March 27, 2016 until July 2018, Chief Executive Officer Geoffrey Tate (hereinafter referred to as "CEO Tate" or "Mr. Tate") of Flex Logix continuously dragged Dr. Konda into email interactions and face-to-face meetings under the pretense of continuous settlement negotiations, seeking more and more information from Dr. Konda.

23. Then, notwithstanding the continuing settlement negotiations, on July 13, 2018, Flex Logix filed a lawsuit in the Federal District Court against Konda Tech and Dr. Konda for unfair business practices.

24. Subsequently, after Dr. Konda and Konda Tech prepared counterclaims to be filed in the Federal District Court action, Flex Logix requested to extend settlement discussions to prevent Konda Tech and Dr. Konda from filing the counterclaims.

25. Later, on December 10, 2018, Flex Logix voluntarily dismissed the lawsuit after the Federal District Court ordered Konda Tech and Dr. Konda to answer the lawsuit filed by Flex Logix by December 10, 2018.

26. On December 17, 2018, Konda Tech filed a lawsuit against Flex Logix in the Federal District Court. After Flex Logix filed a motion to dismiss on January 24, 2019, Konda Tech filed a First Amended Complaint on February 21, 2019, with additional causes of action, including, fraud – intentional misrepresentation, and fraud – concealment. On March 18, 2019 Flex Logix filed another motion to dismiss.

27. On April 3, 2019, Dr. Konda filed his California state complaint and dismissed the District Court action, without prejudice.

28. On June 3, 2019, CEO Tate of Flex Logix threatened an eFPGA vendor at Design Automation Conference 2019 (hereinafter referred to as "DAC 2019"), Las Vegas that the vendor should not do business with Konda Tech or Dr. Konda.

29. As an unnecessary adjunct to the "Motion for Protective Order," counsel for the Defendants Markovic, Wang, and Flex Logix, Mr. Steven M. Perry (hereinafter referred to as "Mr. Perry"), publicly e-filed his declaration together with Dr. Konda's confidential Trade Secret List without notifying or obtaining authorization from Dr. Konda and without filing the Trade Secret List using the "Confidential" selection under the "Security and Optional Services" category on the e-filing system. Thus, Mr. Perry made Dr. Konda's confidential Trade Secret List public in furtherance of the ongoing conspiracy to deprive Dr. Konda of his trade secrets.

30. On January 15, 2020, Defendants Markovic, Wang, Flex Logix, The Regents of the University of California (hereinafter referred to as "UC Regents"), Mr. Tate, Mr. Pierre Lamond

(hereinafter referred to as "Mr. Lamond"), Mr. Peter Hebert (hereinafter referred to as "Mr. Hebert), and Leslie M. Lackman Ph.D. (hereinafter referred to as "Dr. Lackman") committed witness tampering by threatening a Professor at UC Davis (hereinafter referred to as "Prof. at UC Davis") who provided a declaration in support of the confidential trade secret document indeed containing confidential trade secrets and with particularity, which was provided by Dr. Konda during the meet and confer process to resolve a discovery dispute.

31. As a result, all Defendants have committed actionable acts and continued their ongoing conspiracy even after Dr. Konda's original complaint and First Amended Complaint were filed.

**PARTIES**

32. Plaintiff Venkat Konda, Ph.D. is and at all times herein mentioned was a resident of Santa Clara County, California. Konda Tech, a California Corporation, has assigned to Dr. Konda as the sole shareholder and owner of Konda Tech the right to bring this action in his individual capacity, as well as all right, title, and interest to recover damages and injunctive relief.

33. Plaintiff is informed and believes, and thereupon alleges, that Defendant Markovic is an individual who is a resident of California and conducts business in Santa Clara County, California.

34. Plaintiff is informed and believes, and thereupon alleges, that Defendant Wang is an individual who is a resident of California and conducts business in Santa Clara County, California.

35. Plaintiff is informed and believes that Defendant The Regents of the University of California have their principal office in California and conduct business in Santa Clara County, California.

36. Plaintiff is informed and believes that Flex Logix has its principal place of business and conducts business in Santa Clara County, California.

37. Plaintiff is informed and believes, and thereupon alleges, that Defendant Mr. Tate is an individual who is a resident of California and conducts business in Santa Clara County, California.

38. Plaintiff is informed and believes, and thereupon alleges, that Defendant Mr. Lamond is an individual who is a resident of California and conducts business in Santa Clara County, California.

39. Plaintiff is informed and believes, and thereupon alleges, that Defendant Mr. Hebert is an individual who is a resident of California and conducts business in Santa Clara County, California.

40. Plaintiff is informed and believes, and thereupon alleges, that Defendant Dr. Lackman is an individual who is a resident of California and conducts business in Santa Clara County, California.

41. Plaintiff is ignorant of the true names and capacities of Defendants sued herein as DOES 1 through 20, inclusive, and therefore sues these Defendants by such fictitious names. Plaintiff prays leave to amend this Fourth Amended Complaint to allege their true names and capacities when the same have been ascertained.

42. Plaintiff is informed and believes, and thereupon alleges, that each of the Defendants sued herein is responsible in some manner for the occurrences herein alleged, and that Plaintiff's damages were proximately caused by such Defendants.

43. Plaintiff is informed and believes, and thereupon alleges, that at all times herein mentioned, each of the Defendants, was and were, at all times, acting as principals or agents, employees, or representatives within the purpose and scope of such agency, employment, or representation as being responsible in some manner for the occurrences herein alleged.

## JURISDICTION AND VENUE

44. This Court has jurisdiction over this Fourth Amended Complaint pursuant to California Code of Civil Procedure Section 395(a) as the transactions, occurrences, and omissions to act giving rise to the liability on the part of the Defendants occurred in Santa Clara County,

California and/or they have directed their unlawful acts complained of herein in Santa Clara County, California.

45. This Court has personal jurisdiction over the Defendants for the additional reason that they have engaged in systematic and continuous contacts with Santa Clara County, California, *inter alia,* regularly conducting and soliciting business in Santa Clara County, and deriving substantial benefit from products and/or services provided to persons in Santa Clara County, California.

## FACTUAL BACKGROUND

46. Dr. Konda has a Ph.D. in Computer Science and Engineering from the University Of Louisville, Kentucky. Dr. Konda is a pioneer in FPGA routing fabric and interconnection networks technology. Dr. Konda has been granted more than fifteen patents in the technology as of today. Dr. Konda founded Konda Tech, a California corporation, in 2007. Konda Tech's business is based on Dr. Konda's work, and provides chip and system level interconnect technology solutions. Konda Tech has licensed FPGA interconnect architecture intellectual property rights to two FPGA chip vendors, the first of which has made and sold three generations of chips.

47. In 2008, four of Dr. Konda's patent applications were published, namely, WIPO WO 2008109756 A1 published on December 9, 2008 (*See,* Declaration of Vipin Chaudhary, Ph.D. ("Dr. Chaudhary Decl.") Exhibit A attached thereto), WIPO WO 2008147926 A1 published on December 4, 2008 (*See,* Dr. Chaudhary Decl. Exhibit C attached thereto), WIPO WO 2008147927 A1 published on December 4, 2008 (*See,* Dr. Chaudhary Decl. Exhibit E attached hereto), and WIPO WO 2008147928 A1 published on December 4, 2008 (*See,* Dr. Chaudhary Decl. Exhibit G attached thereto) (hereinafter referred to collectively as the "2008 Konda Publications").

48. In late 2008, on a plane from San Francisco to New Orleans, Dr. Bonomi met Defendant Markovic of the Department of Electrical Engineering, University of California at Los Angeles, California. Defendant Markovic told Dr. Bonomi that his research interest and expertise was in

digital circuits, Digital Signal Processors ("DSPs"), and wireless systems. Defendant Markovic had not conducted any research in FPGAs prior to the time that he met Dr. Bonomi.

49. In or around January 2009, Dr. Konda was introduced to Defendant Markovic by Dr. Bonomi. Defendant Markovic was and is a UCLA professor teaching technology courses in circuits and embedded systems (which technology overlaps and complements Dr. Konda's innovations in FPGA routing fabric, but does not involve FPGA design or interconnection networks for FPGAs). Defendant Markovic also has interactions with UCLA/ITA. Defendant Markovic was not focused on FPGA work until he learned of Dr. Konda. Konda Tech was one of six startups that received an oral offer for funding from Cisco, led by Dr. Bonomi. Defendant Markovic was aware of the oral offer to fund Konda Tech. (*See*, Exhibit 10 attached hereto.) The Cisco offer was later rescinded for all six startups so Cisco funding for Konda Tech did not materialize. Defendant Markovic became aware that Cisco's offer to Konda Tech had been rescinded, and that Konda Tech was still looking for funding. At that time Defendant Markovic began to troll Dr. Konda for confidential information. (*See*, Exhibit 11 attached hereto.)

50. Unbeknownst to Dr. Konda, Defendant Markovic seized the opportunity to involve Defendant Wang, then a Ph.D. candidate working under Markovic and looking for a Ph.D. Dissertation topic, immediately began implementing integrated circuit devices based on the disclosures in the 2008 Konda Publications without authorization from Dr. Konda or Konda Tech.

51. Defendant Markovic further seized the opportunity to contact Dr. Konda, misrepresenting that Konda Tech could receive funding through UCLA/ITA. (*See*, Exhibit 12 attached hereto.) Defendant Markovic concealed the fact from Dr. Konda that Markovic and Wang had already started implementing the disclosures in the 2008 Konda Publications as integrated devices in Markovic's lab at UCLA. Hence, Defendant Markovic, by presenting himself as an advisor to Dr. Konda and purporting to arrange funding for Konda Tech, obtained confidential information from Dr. Konda in confidence and thus entered into a confidential relationship with Dr. Konda. Defendant Markovic suggested that Dr. Konda make a presentation to UCLA/ITA. Dr. Konda provided Konda Tech's confidential Business Presentation to Defendant Markovic on October 7,

2009 in confidence. (*See*, Exhibit 13 attached hereto in a Confidential and sealed envelope.) However, after Dr. Konda arrived in Los Angeles on October 12, 2009 to present the confidential Konda Tech business plan to UCLA/ITA, Defendant Markovic for the first time told Dr. Konda that Dr. Konda should not expect UCLA/ITA to fund Konda Tech, because UCLA/ITA does not fund technologies innovated outside UCLA. Dr. Konda did not suspect any wrongdoing by Markovic at that time because Markovic was a professor at UCLA, a world renowned educational institution. Since the confidential Konda Tech Business Presentation was also sent to UCLA/ITA on October 7, 2009, Dr. Konda made a presentation on October 12, 2009 to UCLA/ITA in confidence. Defendant Markovic began the presentation by presenting the confidential Konda Tech Business Presentation to Defendant Dr. Lackman, Deputy Director, Institute for Technology Advancement, UCLA and the other UCLA/ITA Directors in attendance, including Winn Hong. Dr. Lackman stopped Defendant Markovic after one slide and questioned Defendant Markovic "Whose business plan is it?" or words to that effect. The confidential Konda Tech Business Presentation was clearly marked "Konda Tech confidential and proprietary" on all of the slides. Defendant Markovic replied "It is Dr. Konda's." Dr. Lackman then said "Let Dr. Konda present it."

52. Dr. Konda's confidential presentation on October 12, 2009 to UCLA/ITA was fruitless, confirming what Defendant Markovic told Dr. Konda just prior to Dr. Konda presenting to UCLA/ITA. UCLA/ITA rejected funding for Konda Tech on the basis that the complete Konda Tech Business Presentation involved innovations outside UCLA and had nothing to do with UCLA or Defendant Markovic.

53. After presenting to UCLA/ITA on October 12, 2009, Defendant Markovic asked Dr. Konda to give a seminar on the 2008 Konda's publications to Defendant Markovic's students. Dr. Konda obliged Defendant Markovic by presenting an overview to Defendant Markovic's students only with respect to disclosures of the 2008 Konda Publications. Among those in attendance at the October 12, 2009 seminar was Defendant Wang.

54. When Dr. Konda presented to Defendant Markovic's students on October 12, 2009, Dr. Konda clearly told those in attendance that what Dr. Konda was presenting to them was patent

pending technology by a commercial company, Konda Tech, and that the presented material was published as 2008 Konda Publications by then. So, no confidential material was presented by Dr. Konda to the students.

55. Defendant Markovic invited Dr. Konda to UCLA to gain access to the confidential Konda Tech Business Presentation and to give a seminar to Defendant Markovic's students including Defendant Wang. Defendant Markovic beginning at that time and continuing for the ensuing four years, trolled Dr. Konda to learn about all details of Dr. Konda's technology including not only the disclosures in Konda Tech's pending patent applications, but also confidential and proprietary implementation details, technical know-how, and business know-how, and the then customers and potential customers of Konda Tech and Konda Tech's interaction with them which Plaintiff disclosed to Defendant Markovic in confidence in the belief that Defendant Markovic would maintain the information confidential. As a result, Defendant Markovic insidiously learned about FPGA business models and the know-how of the FPGA industry with respect to interconnect technology and its evolution.

56. In June and July 2010, Defendant Markovic called Dr. Konda, and told him that he wanted to use Konda's confidential information in submitting two different confidential proposals for DARPA funding for Konda Tech. Dr. Konda advised that he did not then have the time to work with Defendant Markovic. However, both times, Defendant Markovic assured Dr. Konda that he would not have to spend any time on the confidential DARPA proposals, and that Markovic would incorporate the Konda's confidential information with the disclosures in the 2008 Konda Publications, as well as confidential and proprietary implementation details and technical know-how which Plaintiff had disclosed to Markovic in confidence, with the understanding that the DARPA proposals were confidential. But, Defendant Markovic deceived Dr. Konda by concealing that Konda Tech confidential proprietary information was revealed to Defendant Wang. Defendant Markovic assured Dr. Konda that he would secure a license from Konda Tech should a DARPA grant be approved for a DARPA project.

57. Attached hereto as Exhibits 14 and 15 are the June 23, 2010 and August 6, 2010 confidential DARPA funding proposals (hereinafter referred to as "Two Confidential DARPA Proposals") that followed those conversations between Dr. Konda and Defendant Markovic.

58. The Two Confidential DARPA Proposals make clear that Konda's confidential and proprietary information was at the heart of what Defendants Markovic and Wang were hoping to accomplish:

> Konda Technologies inventions with regular VLSI layouts for Benes/BFT based hierarchical networks are seminal and subsumes all the other known network topologies such as Clos networks, hypercube networks, cube-connected cycles and pyramid networks, which makes these networks implementable in a FPGA devices with regular structures both interconnect distribution-wise and layout-wise which is the key to exploit improved area, power, and performance of FPGA devices. The regularity of Konda hierarchical layout is also the key for its commercializability in System-on-Chip interconnect devices, FPIC devices as well.

Indeed, the Two Confidential DARPA Proposals state that they "will make use of hierarchically routed and proprietary Konda interconnect architecture." The first confidential DARPA Proposal further estimated that Dr. Konda and Konda Tech would complete 620 task hours of the estimated 1020 task hours for key personnel.

59. On October 8, 2010, Dr. Konda disclosed in confidence to Defendant Markovic by email that Konda Tech secured a license from QuickLogic, and Defendant Markovic acknowledged the receipt of that email on October 10, 2010. (*See*, Exhibit 17 attached hereto.) Accordingly, Defendant Markovic learned the commercial viability of Konda's confidential and proprietary information and the disclosures in the 2008 Konda Publications in FPGA products.

60. The Two Confidential DARPA Proposals, replete with references to Konda's confidential information and the disclosures in the 2008 Konda publications, were rejected. However, unbeknownst to Dr. Konda, Defendants Markovic and Wang were not dissuaded from continuing to work on implementation of Konda's confidential and proprietary information and disclosures in the 2008 Konda Publications without authorization from Dr. Konda. In 2010, Defendant Markovic told Dr. Konda over the phone that his students, including Defendant Wang, were implementing disclosures in the 2008 Konda Publications as an "academic project," specifically the 2D layout, on an FPGA chip. When Defendant Markovic told Dr. Konda that his students

had begun implementing Dr. Konda's technology, Dr. Konda told him to stop. Dr. Konda told Defendant Markovic that without a license from Konda Tech, Dr. Konda did not agree that he or UCLA had a right to implement Konda Tech's technology and to stop immediately. Defendant Markovic's answer was, as a university professor, he could "implement any publicly available technology including any technology disclosed in patents or patent applications," or words to that effect. However, Defendant Markovic intentionally misrepresented the fact that the confidential and proprietary information also obtained from Dr. Konda in confidence was being used in connection with the work performed by Defendants Markovic and Wang **solely for academic purposes at UCLA**.

61. By January 2011, Defendant Markovic had trolled Dr. Konda in confidence to obtain the following confidential information including knowledge about the FPGA industry, such information compiled by sweat of the brow and protectable by being maintained confidential by the compiler of the information and not published. including contemporary industry analytics and trend analyses, business practices, disadvantages of the competition, advantages vis-à-vis the competition, customer procurement, relationship building, and management, and business successes ("Konda Business Knowledge and Practices") of Dr. Konda by misrepresenting and concealing Markovic's intent as to use of the information :

a) Dr. Konda did not publish technical papers at technical conferences, and that the reviewers of technical papers are typically not knowledgeable about patents/patent publications such as Dr. Konda's patent publications, including the 2008 Konda Publications;

b) Dr. Konda did not attend generic integrated circuit conferences;

c) Dr. Konda attends only FPGA conferences;

d) Dr. Konda was not building an FPGA product company and had adopted a licensing model including the then Konda's patent publications and trade secret know-how.

62. Unbeknownst to Plaintiff, in defiance of Plaintiff's demand to Defendant Markovic to stop implementing disclosures in the 2008 Konda Publications, Defendants Markovic and Wang founded Hierlogix on January 4, 2011 to commercialize Konda's technology using the

confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, without authorization from Dr. Konda. (*See*, Exhibit 36 attached hereto.) Notably, Hierlogix was incorporated within approximately three months after the Two Confidential DARPA Proposals were rejected. Also, unbeknownst to Dr. Konda, on or about March 27, 2016, Hierlogix was funded by UCLA/ITA, of which Defendant Lackman is a board member and participated in the decision to fund Hierlogix. Hierlogix even today on the UCLA/ITA website at https://www.ita.ucla.edu/companies/ describes "Hierlogix provides Energy-Efficient Hierarchical FPGA and Programming Tools. By developing a revolutionary new interconnect architecture, Hierlogix can provide hardware and software tools that are capable of greatly reducing FPGA power and size requirements, while producing higher speeds and performance." The "revolutionary new interconnect architecture" is in fact proprietary to Dr. Konda as disclosed in the 2008 Konda Publications.

63. In or around January 11, 2011, Defendant Markovic called Plaintiff to engage in continued trolling of Konda Business Knowledge and Practices. During that call Dr. Konda again asked if Defendant Markovic and his students had stopped implementing the disclosures in the 2008 Konda Publications. Defendant Markovic intentionally misrepresented to Dr. Konda that he and his students had stopped doing any kind of FPGA work implementing the disclosures in the 2008 Konda Publications. Dr. Konda believed what Defendant Markovic said, because Markovic had never worked in FPGAs, let alone attended any FPGA specific conferences that Dr. Konda attends. For these reasons, Dr. Konda believed Defendant Markovic that he and his students had stopped implementing the disclosures in the 2008 Konda Publications prior to 2011.

64. During the same conversation in or around January 11, 2011, Defendant Markovic again congratulated Dr. Konda for securing a license from QuickLogic and suggested that he would speak to and would introduce Dr. Konda to another potential licensing customer, i.e., ST Microelectronics.

65. On the same day, Defendant Markovic introduced Dr. Konda to ST Microelectronics, and a conference call was scheduled for January 18, 2011. Defendant Markovic also joined the call

and obtained additional Konda Business Knowledge and Practices discussed with ST Microelectronics. (*See*, Exhibit 18 attached hereto.)

66. Unbeknownst to Dr. Konda at the time of the conference call with ST Microelectronics, Defendant Markovic concealed that he was working on a technical paper to submit to the 2011 Symposium on VLSI Circuits. The call for papers announcement for the 2011 Symposium on VLSI Circuits stated that the last day for a paper submission was 17:00 JST, January 24, 2011. (*See*, Exhibit 19 attached hereto.)

67. As noted earlier, Defendant Markovic learned in confidence from Dr. Konda that Dr. Konda did not publish at technical conferences or in journals. It is common knowledge that reviewers of technical conferences do not search patents or published patent applications for prior publication of subject matter. Defendants Markovic and Wang plagiarized the disclosures in the 2008 Konda Publications and at the 2011 Symposium on VLSI Circuits without authorization from or attribution to Dr. Konda. Accordingly, Defendants Markovic and Wang deceived the technical reviewers of 2011 Symposium on VLSI Circuits and passed off of Dr. Konda's innovations for interconnection networks for FPGAs as their innovations.

68. In June 2011, unbeknownst to Dr. Konda and without his authorization or attribution to Dr. Konda, Defendants Markovic and Wang presented a paper at the 2011 VLSI Circuits Symposium titled "A 1.1 GOPS/mQ FPGA Chip with Hierarchical Interconnect Fabric" (hereinafter referred to as "2011 VLSI Paper"), based on the disclosures in the 2008 Konda Publications as well as the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, as well as Konda Business Knowledge and Practices, which Dr. Konda had previously disclosed to Defendant Markovic in confidence. (*See*, Dr. Chaudhary Decl. at ¶¶ 16-19, ¶¶ 20-22 and ¶¶ 29-30.) Attached hereto as Exhibit 20 is the 2011 VLSI Paper in which Defendants Markovic and Wang falsely claim Dr. Konda's innovations as their innovations.

69. Dr. Konda now believes that Defendants Markovic and Wang conspired so that Dr. Markovic provided Defendant Wang with access to the confidential Konda Tech Business

Presentation to UCLA/ITA on October 12, 2009 which was clearly marked "Konda Tech confidential and proprietary." (*See*, Exhibit 13 attached hereto.)

70. Defendant Markovic breached his obligation of confidentiality by trolling for and using Konda Business Knowledge and Practices provided to him in confidence, and used his UCLA professorship as a ploy not only for his illicit implementation of the disclosures in the 2008 Konda Publications using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, without authorization from Dr. Konda, but also by using Konda Business Knowledge and Practices obtained in confidence to eliminate the industry learning and jump start his commercialization of the technology. Defendants Markovic and Wang covertly incorporated Hierlogix on January 4, 2011 to commercialize published as well as confidential and proprietary technical information, as well as Konda Business Knowledge and Practices received in confidence without the authorization of Plaintiff to compete with Dr. Konda. Defendants Markovic and Wang blatantly plagiarized the disclosures in the 2008 Konda Publications and shamelessly published the 2011 VLSI Paper in which they intentionally misrepresented that Dr. Konda's alternate vertical and horizontal layout of Benes/BFT layouts was their innovation in furtherance of their illicit scheme of violating Konda Business Knowledge and Practices received in confidence and obtained by trolling Dr. Konda and unfairly competing against Dr. Konda. (*See,* Dr. Chaudhary Decl. at ¶¶ 16-19, ¶¶ 20-22 and ¶¶ 29-30.)

71. Unbeknownst to Dr. Konda, UCLA/ITA funded Hierlogix pursuant to a decision made by Dr. Lackman, Deputy Director of UCLA/ITA. Dr. Lackman was fully aware of the confidential and proprietary Konda Technologies Business Presentation and yet funded Hierlogix which is based on the disclosures in the 2008 Konda Publications using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, as well as Konda Business Knowledge and Practices disclosed in confidence to Markovic.

72. Hierlogix even today on the UCLA/ITA the website at https://www.ita.ucla.edu/companies/ describes: "Hierlogix provides Energy-Efficient

Hierarchical FPGA and Programming Tools. By developing a revolutionary new interconnect architecture, Hierlogix can provide hardware and software tools that are capable of greatly reducing FPGA power and size requirements, while producing higher speeds and performance." The "revolutionary new interconnect architecture" is in fact Dr. Konda's innovation.

73. The WIPO WO 2011047368 A2 publication was published on April 21, 2011 (hereinafter referred to as the "2011 Konda Publication"). (*See*, Dr. Chaudhary Decl. Exhibit I attached thereto.)

74. Subsequently, Defendant Markovic invited Dr. Konda by email in April 2013 to meet him at Stanford University when he represented to Dr. Konda that he was a "Visiting Professor." (*See*, Exhibit 21 attached hereto.) Prior to this invitation from Defendant Markovic, Dr. Konda received a LinkedIn connection request from Dr. Lackman. Dr. Konda was surprised to receive LinkedIn connection request from Dr. Lackman. Dr. Konda did not accept the connection request from Dr. Lackman.

75. When Dr. Konda met Markovic at Stanford University, Dr. Konda inquired whether Defendant Markovic and his students had stopped implementing the disclosures in the 2008 Konda Publications using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals as part of academic work at UCLA. Defendant Markovic replied "yes," intentionally misrepresenting that he and his students, including Defendant Wang, were no longer working on implementing the disclosures in the 2008 Konda Publications using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals. During the conversation, Defendant Markovic trolled Dr. Konda to provide the names of customers he was working with to license to obtain additional Konda Business Knowledge and Practices, and Dr. Konda did so in confidence, because he was not aware that Dr. Markovic had betrayed him. During this meeting, Dr. Konda mentioned to Markovic that he received a LinkedIn connection request from Defendant Lackman, and Dr. Konda expressed

surprise why Dr. Lackman sent such a request. Defendant Markovic responded he did not know about the LinkedIn connection request from Defendant Lackman.

76. Dr. Konda a few days later tried to accept the LinkedIn connection request from Defendant Lackman, which was not active anymore (i.e., it must have been withdrawn). Dr. Konda did not pay any interest in it at that time. However Dr. Konda now suspects that Markovic talked to Dr. Lackman to withdraw Dr. Lackman's LinkedIn connection request to Dr. Konda. Dr. Konda now further believes that Dr. Lackman is fully aware that Hierlogix is founded based on stealing Konda Tech's FPGA interconnect technology and joined the ongoing conspiracy by Markovic and Wang.

77. Between 2011 and 2014, Defendant Markovic and Dr. Konda had occasional phone calls, during which they spoke about the progress of their respective work and Defendant Markovic trolled for further Konda Business Knowledge and Practices, but Defendant Markovic never disclosed that the disclosures in the 2008 Konda Publications using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals was the subject of Defendant Markovic's work or Defendant Wang's 2013 Ph.D. dissertation titled, "Building Efficient, Reconfigurable Hardware using Hierarchical Interconnects" (hereinafter referred to as "Wang's 2013 Ph.D. Dissertation"). Defendant Markovic also concealed that he and Defendant Wang had founded Hierlogix on January 4, 2011 to illicitly commercialize the disclosures in the 2008 Konda Publications using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, as well as Konda Business Knowledge and Practices disclosed in confidence to Markovic.

78. Dr. Konda was unaware of Wang's 2013 Ph.D. Dissertation until subsequent to December 18, 2015. Attached hereto as Exhibit 22 is a copy of Chapters II and III and portions of Chapters V and VI of Wang's 2013 Ph.D. Dissertation. The disclosure in Chapters II and III and portions of Chapters V and VI of Wang's 2013 Ph.D. dissertation brazenly copies the 2008 Konda Publications and 2011 Konda Publication, especially the figures and layouts, as shown by

the highlighted portions of Exhibit 22. (*See*, Dr. Chaudhary Decl. at ¶¶ 16-19, ¶¶ 23-25 and ¶¶ 29, 31-32.)

79. On January 28, 2014, Dr. Konda met with Defendants Markovic and Wang at the home of Dr. Bonomi. (*See*, Exhibit 23 attached hereto.) Dr. Bonomi, who was no longer at Cisco, had invited them to his home because he wanted to share that he was in the process of forming his own startup company, and wanted a supplier that would provide FPGAs under license from Dr. Konda and was looking for potential implementation help from Defendants Markovic and Wang. During the course of the discussions, Defendants Markovic and Wang stated that they were looking for funding for a separate startup, but when queried if their startup was in the field of wireless and DSP, Defendant Markovic replied "yes" which was an intentional misrepresentation and a concealment of the fact that Defendants Markovic and Wang had already started up Hierlogix three years earlier with funding by UCLA/ITA to commercialize FPGAs. During the meeting, Dr. Konda was requested to give an update of Dr. Konda's activities and details of Konda Business Knowledge and Practices. Defendant Markovic stated that he was potentially interested in working with Dr. Bonomi and cryptically stated that he "may need to license from Konda Tech". Dr. Konda replied that most of the Konda patents were published or granted and suggested that Defendant Markovic check them on the Web to see if a license was needed and if so, to contact Dr. Konda to obtain a license.

80. While Dr. Bonomi was trying to set up the meeting on January 28, 2014, Dr. Bonomi and Dr. Konda were not aware that Defendants Markovic and Wang had founded the FPGA startup Hierlogix three years earlier. Dr. Konda was not aware of the 2011 VLSI Paper and Wang's 2013 Ph.D. Dissertation was on FPGA interconnects. Defendants Markovic and Wang concealed from Dr. Bonomi and Dr. Konda that Wang's 2013 Ph.D. Dissertation was on FPGA interconnects. Defendants Markovic and Wang concealed from Dr. Bonomi and Dr. Konda that they had founded an FPGA company called Hierlogix and were in the process of founding its successor Flex Logix. Otherwise, Dr. Bonomi would not have set up the meeting at his home for Dr. Bonomi and Dr. Konda to meet with Defendants Markovic and Wang. (*See*, Dr. Bonomi's declaration attached hereto.)

81. A couple of weeks after the January 28, 2014 meeting with Dr. Bonomi, unbeknownst to Dr. Konda at the time, Defendants Markovic and Wang submitted a paper titled "A Multi-Granularity FPGA with Hierarchical Interconnects for Efficient and Flexible Mobile Computing" to the 2014 International Solid State Circuits Conference (hereinafter referred to as the "2014 ISSCC Paper"). The 2014 ISSCC Paper is attached hereto as Exhibit 24. The 2014 ISSCC Paper is based on the disclosures in the 2008 Konda Publications and 2011 Konda Publication using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals and 2011 Konda Publication. The 2014 ISSCC Paper describes and demonstrates technologies that were innovated by Dr. Konda, and monetized by Konda Tech and reveals the illicit scheme of Defendants Markovic and Wang of violating the disclosures in the 2008 Konda Publications and 2011 Konda Publication using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, as well as Konda Business Knowledge and Practices disclosed in confidence to Markovic, and unfairly competing against Konda Tech, as well as falsely passing off Dr. Konda's innovations as their innovations. (*See,* Dr. Chaudhary Decl. at ¶¶ 16-19, ¶¶ 26-28 and ¶ 29, ¶ 31, ¶ 33.)

82. While submitting papers to integrated circuit conferences, Defendants Markovic and Wang never attended or submitted any paper to the International Symposium on FPGAs held annually in Monterey, California. This is the primary FPGA conference, and one they know Dr. Konda attends every year based on Konda Business Knowledge and Practices obtained in confidence by Defendant Markovic.

83. Until on or around March 2014, Defendant Markovic was pursuing Dr. Bonomi to serve as a reference for him, as he was applying to move as a Professor to Stanford University, Stanford, California (hereinafter referred to as "Stanford") as well as California Institute of Technology, Pasadena, California (hereinafter referred to as "Cal Tech"). (*See*, Dr. Bonomi's declaration attached hereto.)

84. On February 18, 2014, Dr. Bonomi also set up a meeting for Dr. Konda and Defendants Markovic and Wang to meet with Sundar Iyer, Ph.D. (hereinafter referred to as "Dr. Iyer"), Co-founder and Chief Executive Officer of Memoir Technologies Inc. (hereinafter referred to as "Memoir") a company in the field of computer memory technologies. The objective of this meeting was for Dr. Iyer to share his experiences of building intellectual property companies with Dr. Konda, Dr. Markovic, and Dr. Wang. Notably, Defendants Markovic and Wang did not use either Hierlogix's or Flex Logix's email IDs in communicating to arrange the meeting with Dr. Iyer to conceal their involvement with those companies from Dr. Konda. (*See*, Exhibit 25 attached hereto.)

85. Dr. Konda and Defendants Markovic and Wang met Dr. Iyer at Memoir's offices on March 5, 2014. At that meeting, Defendants Markovic and Wang again concealed from Dr. Konda the fact that both Hierlogix and their new startup Flex Logix were building FPGA products based on the disclosures in the 2008 Konda Publications and 2011 Konda Publication using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals relating to the revolutionary interconnect architecture innovated by Dr. Konda. (*See*, Exhibit 25 attached hereto.)

86. While Dr. Bonomi was trying to set up the meeting with Dr. Iyer on March 5, 2014, Dr. Bonomi and Dr. Konda were not aware that Defendants Markovic and Wang had built the FPGA startup Hierlogix or recently founded Flex Logix. Dr. Konda was not aware of the 2011 VLSI Paper and 2014 ISSCC Paper, or that the topic of Wang's 2013 Ph.D. Dissertation was FPGA interconnects based on the disclosures in the 2008 Konda Publications and 2011 Konda Publication using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals. Defendants Markovic and Wang concealed from Dr. Bonomi and Dr. Konda that Wang's 2013 Ph.D. Dissertation was on FPGA interconnects. Defendants Markovic and Wang did not tell Dr. Bonomi and Dr. Konda about the 2011 VLSI Paper or the 2014 ISSCC Paper. Defendants Markovic and Wang did not tell Dr. Bonomi and Dr. Konda that

they had built an FPGA company called Hierlogix. While Dr. Bonomi was trying to set up the meeting with Dr. Iyer on March 5, 2014, Defendants Markovic and Wang did not tell Dr. Bonomi and Dr. Konda that they founded Flex Logix on February 26, 2014. Otherwise, Dr. Bonomi would not have set up the meeting with Dr. Iyer at Dr. Iyer's office for Dr. Konda and Defendants Markovic and Wang to meet with Dr. Iyer on March 5, 2014. And, Dr. Konda would not have attended the meeting on March 5, 2014 to avoid being trolled by Defendants Markovic and Wang for more Konda Business Knowledge and Practices.

87. Unbeknownst to Dr. Konda at the time of the meeting at Dr. Iyer's office, Defendants Markovic and Wang had already founded Flex Logix on February 26, 2014 as the successor to Hierlogix to illicitly compete against Konda Tech based on implementing the disclosures in the 2008 Konda Publications and 2011 Konda Publication using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals without authorization from Dr. Konda. (*See*, Exhibit 49 attached hereto.)

88. Dr. Konda's expertise is not circuit design, so Dr. Konda never attended integrated circuits conferences nor followed what is published at such conferences.

89. The 2011 VLSI Paper was published after Hierlogix was founded and the 2014 ISSCC Paper was published after Flex Logix was founded. Notably, the 2011 VLSI Paper and the 2014 ISSCC Paper list Defendants Markovic and Wang as affiliated with UCLA only to conceal from Dr. Konda that Defendants Markovic and Wang were associated in any way with those companies.

90. Dr. Konda was not aware of the 2011 VLSI Paper, Wang's 2013 Ph.D. Dissertation, and the 2014 ISSCC Paper, until subsequent to December 18, 2015 when Dr. Konda was told about Flex Logix by Dr. Betz during the visit to Dr. Betz's office. At that time, Dr. Konda first learned about Flex Logix and started investigating Flex Logix.

91. The conduct of Defendants Markovic and Wang makes clear that they employed subterfuge and deceit to gain access to confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to

prepare the Two Confidential DARPA Proposals, develop their fraudulent credibility in the FPGA technology through papers submitted to integrated circuits conferences based on the disclosures in the 2008 Konda Publications and 2011 Konda Publication using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, as well as Konda Business Knowledge and Practices disclosed in confidence to Markovic, to launch their own startup company Hierlogix with funding by UCLA/ITA and its successor Flex Logix in competition with Konda Tech, covertly usurping Konda Business Knowledge and Practices received in confidence from Dr. Konda as the cornerstone for establishing and operating those companies.

92. It must be noted that the 2008 Konda Publications and 2011 Konda Publication are the key reasons Markovic and Wang were able to implement FPGAs and to found Hierlogix and Flex Logix, combined with the Konda Business Knowledge and Practices Markovic and Wang learned in confidence from Dr. Konda that 1) Dr. Konda was not publishing technical papers in refereed conferences, 2) Konda Tech has a licensing business model, and 3) Dr. Konda does not attend circuits conferences.

93. Unbeknownst to Dr. Konda, Flex Logix was in stealth mode from its inception in February 2014 until on or about March 2015.

94. In the first part of December, 2015, Dr. Konda contacted Dr. Betz, and they agreed to meet on December 18, 2015 in Toronto, Canada. They met on December 18, 2015 from approximately 1:00 – 2:30 PM at Dr. Betz's office at the University of Toronto to discuss certain results Dr. Konda had achieved using the Versatile Place and Route tool suite (hereinafter referred to as "VPR") as part of Konda Business Knowledge and Practices. VPR was built by Dr. Betz and his students working for several years at the Department of Electrical and Computer Engineering at the University of Toronto, Toronto, Canada, and Dr. Betz was interested in discussing Dr. Konda's results.

95. Dr. Betz was aware of Dr. Konda's patents and published patent applications and Konda Business Knowledge and Practices received in confidence since last quarter of 2012 as both of them interacted regarding Konda Business Knowledge and Practices.

96. During the meeting, Dr. Betz asked Dr. Konda "Have you given a license to Flex Logix?" or words to that effect. Dr. Konda was shocked when Dr. Betz asked him that question. Then, Dr. Konda replied that he hadn't heard about Flex Logix and inquired of Dr. Betz about Flex Logix. Dr. Betz told Dr. Konda that Flex Logix is an FPGA startup co-founded by Defendant Markovic and his student Defendant Wang.

97. At the same meeting, Dr. Betz told Dr. Konda that he had immediately realized Flex Logix's purported interconnect technology is a knock-off of the disclosures in the 2008 Konda Publications and 2011 Konda Publication.

98. After his meeting with Dr. Betz on December 18, 2015, Dr. Konda immediately started investigating what Dr. Betz said to him by first visiting the website for Flex Logix (www.flex-logix.com). Dr. Konda discovered that Flex Logix's products purport to be eFPGA blocks and that Defendants Markovic and Wang had intentionally misrepresented to Dr. Konda at the January 28, 2014 meeting with Dr. Bonomi that they were involved with a startup company in the digital signal processor (DSP) field for communications applications. As Dr. Konda continued his investigation he thereafter discovered Wang's 2013 Ph.D. Dissertation and after analyzing the dissertation determined that it plagiarized the disclosure in the 2008 Konda Publications and 2011 Konda Publication. (*See*, Dr. Chaudhary Decl. at ¶¶ 16-19, ¶¶ 23-25 and ¶¶ 29, 31-32.) Dr. Konda later discovered for the first time the 2014 ISSCC Paper and determined that it described an implementation of the plagiarized the disclosures in the 2008 Konda Publications and 2011 Konda Publication. (*See*, Dr. Chaudhary Decl. at ¶¶ 16-19, ¶¶ 26-28 and ¶ 29, ¶ 31, ¶ 33.)

99. Notably, Flex Logix touts the 2014 ISSCC paper on its website as describing Flex Logix's "new, patented interconnect, XFLX™" misleading the public that Dr. Konda's innovations are instead the innovations of Flex Logix. *See*, http://www.flex-logix.com/fpga-tutorial/.

100. On or about the fourth week of December 2015, Dr. Konda texted Dr. Bonomi to meet, but Dr. Bonomi was in Italy at that time. On January 7, 2016, after Dr. Bonomi returned to California, Dr. Konda met Dr. Bonomi at his office in Milpitas, California. Dr. Konda informed him about the meeting with Dr. Betz on December 18, 2015 and that he had subsequently searched on the World Wide Web and only then discovered that Defendants Markovic and Wang had founded Flex Logix to manufacture eFPGAs apparently based on the disclosures in the 2008 Konda Publications and 2011 Konda Publication using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals and that Dr. Konda had been systematically trolled by Defendant Markovic over a period of years from 2009 – 2014 to obtain Konda Business Knowledge and Practices which Dr. Konda had disclosed in confidence. Dr. Konda asked if Dr. Bonomi knew that Wang's 2013 Ph.D. Dissertation was on FPGA multi-stage interconnects and if he knew about Hierlogix products or Flex Logix. Dr. Bonomi himself was shocked and said that was the first time he heard about these facts.

101. To the utmost shock of Dr. Konda, Defendants Markovic and Wang, beginning at the time he first met Dr. Markovic and continuing for years, learned about all details of Dr. Konda's technology including the disclosures in the 2008 Konda Publications and 2011 Konda Publication, confidential and proprietary implementation details, technical know-how, and business know-how and the then customers and potential customers of Konda Tech and Konda Tech's interaction with them and other Konda Business Knowledge and Practices. As a result, Defendants Markovic and Wang learned about FPGA business models and the know-how of the FPGA industry with respect to interconnect technology and its historical evolution and Dr. Konda's revolutionary interconnect architecture. This provided Defendants Markovic and Wang a significant unfair head start in implementing the disclosures in the 2008 Konda Publications and 2011 Konda Publication using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, as well as Konda Business Knowledge and Practices disclosed in confidence to Markovic, before launching Hierlogix and Flex Logix to

compete with Dr. Konda covertly using Konda Business Knowledge and Practices received from Dr. Konda in confidence as the cornerstone for commercial eFPGA products.

102. Defendant Markovic deceived Dr. Konda by presenting himself as an advisor to Dr. Konda. Dr. Konda believed that what he disclosed to Defendant Markovic was disclosed in confidence as evidenced, for example, by the Two Confidential DARPA Proposals, and believed that the intentions of Defendant Markovic were to help Konda Tech because he is a UCLA Professor and was not a competitor. Dr. Konda always expected Defendant Markovic as a professor at a premier educational and research institution like UCLA, who teaches students and conducts research, to conduct himself in a professional way. Dr. Konda was shocked to learn over the period of time up to March 27, 2016 what Defendant Markovic had done for years in such a deceitful manner without the knowledge of Dr. Konda.

103. More importantly Markovic and Wang, then a Ph.D. student, both had no knowledge of Konda Business Knowledge and Practices and the FPGA industry until they deceitfully trolled Dr. Konda.

104. Dr. Konda and Konda Tech marked the confidential and proprietary Konda Tech Business Presentation, implementation details and technical know-how, and Konda Business Knowledge and Practices ”confidential and proprietary.” Any such information was and is disclosed to customers of Konda Tech under non-disclosure agreements. All written disclosures to Defendant Markovic were marked “confidential and proprietary.” All such information which Dr. Konda verbally disclosed to Defendant Markovic likewise was considered to be in confidence and absolutely not intended to be used by Defendants Markovic and Wang to compete with Dr. Konda or Konda Tech.

105. Defendant Markovic implementing the disclosures in the 2008 Konda Publications and 2011 Konda Publication using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals for academic purposes at UCLA in 2010 was a testimonial to Dr. Konda’s innovations, and there was no economic damage to Dr. Konda in the implementations for academic purposes. Therefore, in 2010, Dr. Konda did not have any reason

to suspect that Defendant Markovic, a professor at UCLA, a world-renowned university would breach the confidence reposed in him regarding the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals.

106. Economic damage to Dr. Konda did not occur until Defendants Markovic and Wang began illicitly commercializing the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, about which Dr. Konda did not become aware until after December 18, 2015.

107. Defendants Markovic and Wang concealed that they were actually using the disclosures in the 2008 Konda Publications and 2011 Konda Publication and the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, as well as Konda Business Knowledge and Practices disclosed in confidence to Markovic, to secretly launch Flex Logix until after December 18, 2015.

108. Dr. Konda was not aware of the 2011 VLSI Paper, Wang's 2013 Ph.D. Dissertation, and the 2014 ISSCC Paper until subsequent to December 18, 2015 and had no reason that he should have become aware of those papers, particularly because Defendants Markovic and Wang concealed the existence of the papers and because Markovic intentionally misled Dr. Konda that Markovic and Wang were not even in the FPGA industry.

109. After nearly exhausting his search for additional facts about Defendants Markovic and Wang and Flex Logix and consulting with an attorney, Dr. Konda formed his suspicion that Flex Logix was manufacturing eFPGAs based on the disclosures in the 2008 Konda Publications and 2011 Konda Publication using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, as well as confidential Konda Business Knowledge and Practices obtained by Defendant Markovic trolling Dr. Konda for information

that Dr. Konda had communicated to Defendant Markovic and Defendant Wang in confidence, which had enabled Hierlogix and its successor Flex Logix to start up its business.

110. On March 27, 2016, Dr. Konda acted on his suspicion and prepared and sent an email with the subject "Flex-logix is Infringing Konda interconnect IP; Cheng Cheng Wang's UCLA PhD Dissertation is a blatant copy of Konda Technologies granted Patent(s)" to Mr. Tate, Mr. Peter Hebert, Co-founder/Managing Director of Lux Capital and board member of Flex Logix, and Mr. Shirish Sathaye, General Partner of Formation 8, Foundation Capital and board member of Flex Logix (hereinafter referred to as "Mr. Sathaye"), Dr. Gene David Block, Chancellor, UCLA, Dr. Jayathi Murthy, Dean of Henry Samuel School of Engineering and Applied Science, UCLA (hereinafter referred to as "Dr. Murthy"), Dr. Lackman, Deputy Director, Institute for Technology Advancement, UCLA, and Defendant Markovic with several of the facts Dr. Konda had discovered after he had visited Dr. Betz. (*See*, Exhibit 26 attached hereto.)

111. On March 28, 2016, Dr. Konda received a response from Mr. Tate saying that he would investigate the issue and get back to Dr. Konda in about a week. On March 28, 2016, Dr. Konda also received a response from Dr. Murthy saying that she would get back to him in a week. On April 7, 2016, Mr. Tate sent an email on the pretense that he needed additional information from Dr. Konda. (*See*, Exhibit 27 attached hereto.)

112. Dr. Konda did not receive any response from Dr. Lackman whom Dr. Konda met during his confidential Konda Tech Business Presentation to UCLA/ITA on October 12, 2009. On April 7, 2016, Dr. Konda sent a follow-up email to Dr. Lackman. (*See*, Exhibit 28 attached hereto.) Not until that time did Dr. Konda discover on the UCLA/ITA website a company named Hierlogix and inquired of Dr. Lackman whether that was an earlier name for Flex Logix. Dr. Konda pointed out that UCLA/ITA funding of Defendants Markovic and Wang for any work done at UCLA based on the disclosures in the 2008 Konda Publications and 2011 Konda Publication using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals needed to be investigated by UCLA/ITA immediately. Dr. Konda also asked Dr. Lackman: "What are your policies and how soon do you take action

against them?" Dr. Lackman has never responded to Dr. Konda's April 7, 2016 email leading to Dr. Konda's belief that UCLA/ITA was at that time and continues to be aware of the unauthorized use of the disclosures in the 2008 Konda Publications and 2011 Konda Publication using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals by Hierlogix and Flex Logix.

113. Defendant Wang received a distinguished dissertation award for Wang's 2013 Ph.D. Dissertation under the supervision of Defendant Markovic. Dr. Konda requested Defendants Wang and Markovic to explain how Wang's 2013 Ph.D. Dissertation is different from the disclosures in the 2008 Konda Publications and 2011 Konda Publication. Wang and Markovic have never responded in what way Wang's 2013 Ph.D. Dissertation differs from the disclosures in the 2008 Konda Publications and 2011 Konda Publication.

114. Defendants Markovic and Wang received the best paper award for the 2014 ISSCC Paper. Dr. Konda questioned Wang and Markovic how the 2014 ISSCC paper differs from the disclosures in the 2008 Konda Publications and 2011 Konda Publication. Defendants Wang and Markovic have never responded in what way the 2014 ISSCC Paper differs from the disclosures in the 2008 Konda Publications and 2011 Konda Publication.

115. Continuing with his investigation, it was not until on or about June 25, 2016 that Dr. Konda discovered the 2011 VLSI Paper which plagiarized the disclosures in the 2008 Konda Publications and 2011 Konda Publication using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals and additional Konda Business Knowledge and Practices disclosed by Dr. Konda to Defendant Markovic in confidence. Dr. Konda was not aware of 2011 VLSI Paper until on or about June 25, 2016. (*See,* Dr. Chaudhary Decl. at ¶¶ 16-19, ¶¶ 20-22 and ¶¶ 29-30.)

116. On April 4, 2016, Dr. Konda received a response from Ann R. Karagozian, Ph.D. (hereinafter referred to as "Dr. Karagozian"), Interim Vice Chancellor of Research at UCLA (and predecessor to Roger Wakimoto, Ph.D. (hereinafter referred to as "Dr. Wakimoto"), Vice

Chancellor of Research at UCLA), and Ann Pollack, Ph.D. (hereinafter referred to as "Dr. Pollack"), Assistant Vice Chancellor of Research that they would investigate the matter pursuant to UCLA Policies and Procedures. They categorized Dr. Konda's facts in Dr. Konda's March 27, 2016 email as research misconduct and patent infringement. Regarding the research misconduct, Dr. Konda subsequently communicated with them and provided several documents to them. On May 7, 2018, Dr. Konda submitted a formal complaint of research misconduct. On July 19, 2018, Dr. Konda received a response from Dr. Pollack that the Two Confidential DARPA Proposals were not plagiarized, which is not what Dr. Konda had complained about. (*See*, Exhibit 33 attached hereto.) Instead, Dr. Konda asserted that the Two Confidential DARPA Proposals were proof of the plagiarism by Defendants Markovic and Wang in their 2011 VLSI Paper, in Wang's 2013 Ph.D. Dissertation, and in their 2014 ISSCC Paper. Dr. Konda requested a face-to-face meeting several times with Dr. Pollack, but his requests were declined. On April 30, 2019, Dr. Konda responded to Dr. Pollack that she still had not responded to all the points he raised. Dr. Konda has received no further response from the Vice Chancellor of Research at UCLA. Essentially Dr. Pollack's response was that Dr. Konda should deal directly with Defendants Markovic and Wang on the complaints, and UCLA would not cooperate with Dr. Konda to further investigate the matter in utter disregard of UCLA Research Misconduct Policies.

117. Regarding patent infringement, Dr. Konda submitted claim charts to Mr. Steven Drown (hereinafter referred to as "Mr. Drown"), Senior Counsel, Educational Affairs, Office of the General Counsel, University of California and Mr. Swerdlow, Senior Counsel, UCLA on August 1, 2018. Dr. Konda has not received any response in utter disregard of UCLA's Patent Infringement Policies.

118. From March 30, 2016 until May 20, 2016, Mr. Tate engaged Dr. Konda in an email exchange and requested additional information from Dr. Konda by stating that he did not agree with Dr. Konda's analysis. Dr. Konda provided additional information to Mr. Tate in at least three emails. To all of them, Mr. Tate's response was: 1) We have reviewed your recent email, 2) We definitely do not agree with your analysis or your position(s), and 3) We will certainly

consider any additional facts and listen to any new analysis you wish to provide us. Clearly, Mr. Tate's behavior was a pretense that a resolution could be reached and was simply to wear Dr. Konda out by avoiding the issues with no interest in resolving the matter. (*See*, Exhibit 29 attached hereto.)

119. From on or about August, 2016 until on or about April, 2017, Dr. Konda and Flex Logix had settlement negotiations represented by their attorneys. However, no resolution was achieved.

120. On May 19, 2017, Dr. Konda called Mr. Tate and left a voicemail inquiring if he was willing to meet to discuss an amicable settlement. Mr. Tate called back Dr. Konda by saying "I doubt that we can reach a settlement. But I am willing to listen." (*See*, Exhibit 8 attached hereto.)

121. On May 30, 2017, Dr. Konda and Mr. Tate met at a Starbucks in Mountain View, California. (*See*, Exhibit 30 attached hereto.) Dr. Konda explained at length the plagiarism and trolling for Dr. Konda's Konda Business Knowledge and Practices and Dr. Konda's trade secrets by Defendants Markovic and Wang, and patent infringement by Flex Logix and requested Mr. Tate to act fairly and resolve these issues immediately. Mr. Tate then threatened Dr. Konda that: "One of the senior board members of Flex Logix [alluding to Mr. Lamond] will ruin your career if you or Konda Tech files a lawsuit against Flex Logix."

122. Dr. Konda and Mr. Tate again met at the same Starbucks on June 1, 2017. During the discussions Mr. Tate reiterated his threat to Dr. Konda that: "One of the senior board members of Flex Logix [alluding to Mr. Lamond] will ruin your career if you or Konda Tech files a lawsuit against Flex Logix."

123. From July 14, 2017 until July 17, 2017, Dr. Konda and Mr. Tate engaged in an extensive email exchange with Mr. Tate finally saying his Board did not agree with anything that had been discussed in that email exchange. (*See*, Exhibit 31 attached hereto.)

124. From March 21, 2018 until May 20, 2018, Dr. Konda and Flex Logix engaged in further settlement negotiations. (*See*, Exhibit 32 attached hereto.)

125. From July 5, 2018 until July 9, 2018, Dr. Konda had continued settlement negotiations with Mr. Tate. (S*ee*, Exhibit 34 attached hereto.)

126. From March 27, 2016 until July 13, 2018, Flex Logix board members Mr. Tate, Mr. Lamond, Mr. Hebert and Defendant Wang were involved in further settlement negotiations but continued 1) to threaten Dr. Konda that Mr. Lamond would ruin Dr. Konda's career if Dr. Konda or Konda Tech were to file a lawsuit against Flex Logix, 2) to drag out the discussions, and 3) to collect information from Dr. Konda.

127. On July 13, 2018, Flex Logix brazenly filed a lawsuit in the Federal District Court against Konda Tech and Dr. Konda. (*See*, Exhibit 37 attached hereto.) The complaint was served on Dr. Konda on August 3, 2018. Konda Tech and Dr. Konda requested a 30-day extension to file an answer, and the due date to file an answer was extended until September 18, 2018.

128. Konda Tech and Dr. Konda prepared counterclaims and proposed settlement negotiations between the parties represented by the respective counsel. All parties submitted a stipulation for extension of the answer date by Konda Tech and Dr. Konda. The Federal District Court extended the due date for Konda Tech and Dr. Konda to answer to December 10, 2018. (*See*, Exhibit 38 attached hereto.)

129. Konda Tech and Flex Logix met twice to continue the settlement negotiations, i.e., on October 24, 2018 and on November 30, 2018.

130. On December 4, 2018, Flex Logix proposed to Konda Tech and Dr. Konda to stipulate for a further extension of the answer date for Konda Tech and Dr. Konda. The Federal District Court denied the stipulation to extend the due date and ordered Konda Tech and Dr. Konda to file an answer by December 10, 2018. (*See*, Exhibit 39 attached hereto.)

131. On December 10, 2018, Konda Tech and Dr. Konda demanded Flex Logix to dismiss the lawsuit or else Konda Tech and Dr. Konda would file an answer and counterclaims.

132. In response, Flex Logix dismissed the lawsuit without prejudice. (*See*, Exhibit 40 attached hereto.) Konda Tech and Dr. Konda agreed to the condition that in future if Konda Tech were to file a lawsuit against Flex Logix on the same issues raised by the counterclaims, Konda Tech would give two business days' prior notice to Flex Logix. (*See*, Exhibit 41 attached hereto.)

133. Accordingly, Dr. Konda and Konda Tech gave a two-day notice to Flex Logix on December 13, 2018 that Dr. Konda and Konda Tech intended to file a lawsuit against Flex Logix. (*See*, Exhibit 42 attached hereto.) Flex Logix did not refile its lawsuit against Dr. Konda and Konda Tech.

134. Konda Tech filed a lawsuit against Flex Logix on December 17, 2018 in the Federal District Court. (*See*, Exhibit 43 attached hereto.) Flex Logix was served with the complaint on January 3, 2019 and filed a motion to dismiss on January 24, 2019. (*See*, Exhibit 44 attached hereto.)

135. Konda Tech filed an opposition to Flex Logix's motion to dismiss on February 21, 2019 and also filed a first amended complaint requesting leave from the Federal District Court to enter the first amended complaint.

136. Flex Logix requested to stipulate to enter the first amended complaint after withdrawing the motion to dismiss. (*See*, Exhibit 45 attached hereto.) All parties agreed to the stipulation, and the Federal District Court entered the first amended complaint. (*See*, Exhibit 46 attached hereto.)

137. Flex Logix then filed a motion to dismiss the first amended complaint on March 18, 2019. (*See*, Exhibit 47 attached hereto.) However on April 3, 2019, Dr. Konda filed his California state complaint and on the same day Konda Tech dismissed the first amended complaint in the Federal District Court, without prejudice. (*See*, Exhibit 48 attached hereto.)

138. Starting from December 18, 2015 when Dr. Betz first asked Dr. Konda if Flex Logix was licensed by Dr. Konda, until March 27, 2016, Dr. Konda investigated facts about Defendants. Markovic and Wang and Flex Logix until forming a suspicion that Flex Logix was manufacturing eFPGAs based not only on the disclosures in the 2008 Konda Publications and 2011 Konda Publication using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, as well as Konda Business Knowledge and Practices disclosed in confidence to Markovic, which enabled Hierlogix and its successor Flex Logix to start up its business. At that point, Dr. Konda sent an email on March 27, 2016 in an

effort to obtain needed information and reach a resolution by way of settlement. (*See*, Exhibit 26 attached hereto.) For example, between March 27, 2016 and July 13, 2018 (the day Flex Logix filed a lawsuit against Konda Tech and Dr. Konda), Dr. Konda engaged in extensive efforts with the Defendants to settle out of the court in good faith.

139. Furthermore Dr. Konda continued the settlement negotiations with Flex Logix until December 17, 2018 when Konda Tech filed a lawsuit against Flex Logix. In fact, settlement negotiations between Konda Tech and Flex Logix continued between December 10, 2018 to August 6, 2019 at 6:48 PM PDT, and **accordingly the statute of limitations did not run during that period**.

140. Ever since Dr. Konda formed his suspicion about all the torts committed by Defendants Markovic and Wang, i.e., from March 27, 2016 afterwards, Dr. Konda was engaged in good faith settlement negotiations with UCLA and Flex Logix until at least August 6, 2019.

141. In October 2018, Dr. Konda for the first time submitted technical papers to the 2019 ACM/SIGDA International Symposium on Field Programmable Gate Arrays. The technical papers were reviewed double- blinded, i.e., both the author's name and author's affiliation were blinded to or hidden from all the reviewers. In response to the technical paper Dr. Konda submitted in November 2018, which was titled "Hierarchical FPGA Fabrics using 2D-Benes-BFT-Pyramid Network Layouts with Optimizations", one of the reviewers pointed to Wang's 2013 Ph.D. Dissertation, and a second reviewer pointed to the 2014 ISSCC Paper stating that the subject matter was already described in Wang's 2013 Ph.D. Dissertation and 2014 ISSCC Paper. (*See*, Exhibit 35 attached hereto.) Clearly, those two reviewers mistakenly believed that Defendants Markovic and Wang were the innovators of the disclosures in the 2008 Konda Publications and 2011 Konda Publication using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals and the 2011 Konda Publication. (*See*, Dr. Chaudhary Decl. at ¶¶ 16-19, ¶¶ 23-28 and ¶¶ 29, 31-33.)

142. During the DAC 2019 conference held at the Las Vegas Convention Center, Las Vegas, Nevada from June 2 - 6, 2019, on June 3, 2019, Dr. Konda met with an executive of an FPGA

manufacturer at the Center's food court regarding Konda FPGA interconnect technology from approximately 9 – 10 AM. Later on the same day while the executive was at his company's booth in the Las Vegas Convention Center, Mr. Tate, the Chief Executive Officer of Flex Logix which also had a booth at DAC 2019 consistent with his previous threats to Dr. Konda on May 30, 2017 and June 1, 2017, approached the executive of his competitor and said to him: "Can you provide me with the contact information of your lawyers, I think they shall talk together." At this, the executive replied to Mr. Tate: "Geoff, we are grown up men, if you have something to tell me, tell me now." Mr. Tate said he saw Dr. Konda talking to him earlier in the day. Mr. Tate further threatened the executive that: "I wanted to tell you that what we have is something totally different from Konda claims. I hope you are not helping him in any way."

143. During the period from September 25, 2019 at 2:43PM PDT to October 1, 2019 11:28 PM PDT, Dr. Konda engaged in long meet and confer sessions with Mr. Steven M. Perry (hereinafter referred to as "Mr. Perry") and Mr. Gregory P. Stone (hereinafter referred to as "Mr. Stone") regarding discovery. By that time both the parties agreed that any information marked as confidential would be treated as such under any protective order entered into in this case. Subsequently, Mr. Stone in his email to Dr. Konda on October 13, 2019 at 9:54AM PDT requested Dr. Konda to identify his trade secrets with particularity. (*See*, Exhibit 51 at p. 1, attached hereto.) Mr. Stone clearly wrote: "You may want to turn your attention to remedying that deficiency because, until you do, discovery cannot proceed." In response Dr. Konda sent an email to Mr. Perry and Mr. Stone on October 15, 2019 at 11:28 PM PDT. Dr. Konda stated that he was not interested in obtaining discovery of any of Defendants' trade secrets and that they should sign his Standard Protective Order, which Dr. Konda sent on September 20, 2019. Dr. Konda then sent his confidential list of trade secrets as a 5-page document marked "Venkat Konda Ph.D. Confidential" on each of the pages. Dr. Konda demanded that Defendants Markovic and Wang should respond to his discovery requests, now that Dr. Konda's trade secrets were identified with reasonable particularity.

144. Furthermore, Mr. Perry admitted in his declaration that Dr. Konda stated to him that Dr. Konda was not waiving his claim to the confidentiality of his confidential Trade Secret List

during a meet and confer call at 4:30 PM PDT on October 18, 2019. Knowing that his stance on the issue of the "reasonable particularity" of the identity of Dr. Konda's trade secrets based on Dr. Konda's confidential Trade Secret List was unsupportable, and that Dr. Konda would be entitled to discovery, on October 21, 2019, the day before responses from Defendants Markovic and Wang to Dr. Konda's discovery requests were due, Mr. Perry filed a misnamed "Motion for Protective Order" which was in reality a motion for a stay of discovery on the pretense that California's trade secret statute stayed the entire case based on his own disingenuous non-expert declaration that Dr. Konda had not identified his trade secrets with reasonable particularity. Notably, Mr. Perry is an attorney and has no technical background.

145. As an unnecessary adjunct to the "Motion for Protective Order," Mr. Perry publicly e-filed his declaration together with Dr. Konda's confidential Trade Secret List without notifying or obtaining authorization from Dr. Konda and without filing the Trade Secret List using the "Confidential" selection under the "Security and Optional Services" category on the e-filing system. Notably, the public filing of Dr. Konda's confidential Trade Secret List was not material to the "Motion for Protective Order," but was instead an abuse of process by Perry with malicious intent to disclose Dr. Konda's trade secrets with the ulterior purpose of defeasing Dr. Konda of his trade secrets.

146. Consistent with Mr. Tate's previous threats to Dr. Konda to ruin Dr. Konda's career, Flex Logix board members Mr. Tate, Mr. Lamond, Mr. Hebert, Wang and Markovic willfully and maliciously made Dr. Konda's confidential Trade Secret List public in an ongoing conspiracy.

147. The hearing for Motion for Protective Order was calendared for January 28, 2020. Dr. Konda's opposition was due on January 15, 2020.

148. Dr. Konda e-filed his opposition at 3:06 PM PST on January 15, 2020. Dr. Konda was in Springfield, MA and Glastonbury, CT on that day. In his opposition Dr. Konda also submitted a declaration by Prof. at UC Davis that the confidential Trade Secret List indeed lists Dr. Konda's trade secrets with adequate particularity. Dr. Konda filed the declaration by Prof. at UC Davis as confidential and under Court Seal. Prof. at UC Davis has been assisting Dr. Konda regarding the torts committed by Defendants Markovic and Wang since June 2016. On August 1, 2018 (See,

Exhibit 33 attached hereto), Dr. Konda informed UCLA that Prof. at Davis had been assisting Dr. Konda in support of Dr. Konda on the misappropriation of trade secrets by Markovic and Wang.

149. At 3:39 PM PST, Mr. Perry sent an email to Dr. Konda requesting permission to provide the declaration of Prof. at UC Davis to his clients, namely, Defendants Markovic and Wang and Mr. Tate. (*See*, Exhibit 52 attached hereto.) In an email exchange between Mr. Perry and Dr. Konda from 3:39 PM PST until 4:17 PM PST, Dr. Konda did not give permission to provide the declaration of Prof. at UC Davis to Defendants Markovic and Wang and Mr. Tate. (*See*, Exhibit 52 attached hereto.)

150. At 6:48 PM PST on January 15, 2020, Prof. at UC Davis phoned Dr. Konda and stated that he had been threatened by UC Regents' persons and requested to withdraw his declaration, and otherwise his 25+ year career would be in jeopardy. Prof. at UC Davis said he was calling from Salt Lake City and about to catch a flight to Phoenix. Dr. Konda and Prof. at UC Davis had 5 phone calls from 6:48 PM PST on January 15, 2020 until the next morning at 6:24 AM PST. The total duration of the 5 calls is 51 minutes based on Dr. Konda's phone billing statement. (*See,* Exhibit 53 attached hereto.)

151. Prof. at UC Davis sent an email to Dr. Konda on the same night, i.e., January 15, 2020, as dictated by the one of the UC Regents' persons who called him to demand he withdraw his declaration. (*See,* Exhibit 54, attached hereto.)

152. During the five calls, Dr. Konda informed Prof. at Davis about the email interaction between Mr. Perry and him from 3:39 PM – 4:17 PM PST and Dr. Konda's Opposition to Motion for Protective Order that was served only on the attorneys for the Defendants.

153. Notably, Prof. at UC Davis's declaration that the confidential Trade Secret List indeed lists Dr. Konda's trade secrets with adequate particularity was damaging to the Defendants and especially to the declaration filed by Mr. Perry in support of the "Motion for Protective Order."

154. Defendants' attorneys were in concert with the board members of Flex Logix, including Defendant Wang, and Dr. Lackman implemented a plan to threaten Prof. at UC Davis by UC

Regents' persons who have authority to exert control over the actions of Prof. at UC Davis through intimidation.

155. Dr. Konda asked Prof. at Davis not to withdraw his declaration. In response, Prof. at Davis reiterated that he was threatened and he had no option but to withdraw his declaration.

156. Prof. at UC Davis also told Dr. Konda that Defendants' plan was to use against Dr. Konda the fact that Dr. Konda has the audacity to name UC, which is a public institution, a Defendant in this case. Dr. Konda responded to Prof. at UC Davis that is ridiculous and that Dr. Konda never stated in his emails to UCLA nor initially intended to seek monetary damages from the UC Regents until discovering that the UC Regents is covering-up for Defendants Markovic and Wang, instead of cleaning up UCLA, and is financially benefitting from their unfairly competing with Dr. Konda as a result of Flex Logix commercializing eFPGAs based on the disclosures in the 2008 Konda Publications and 2011 Konda Publication using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, as well as Konda Business Knowledge and Practices disclosed in confidence to Markovic, through funding provided by UCLA/ITA to Hierlogix even though Dr. Lackman knew and continues to be aware of the passing off of eFPGA products by Flex Logix as being innovations of Defendants Markovic and Wang instead of the true innovator Dr. Konda.

157. Dr. Konda then suggested to Prof. at UC Davis, if withdrawal of his declaration was imperative, to withdraw based on conflict of interest. Prof. at UC Davis then stated he was threatened to withdraw by stating that "upon further thoughts I do not feel confident about the validity of the statements in the declaration." (See, Exhibit 54 attached hereto.) Thus, Defendants and their counsel intimidated Prof. at UC Davis to change the testimony in his declaration through their threats to Prof. at UC Davis.

158. Subsequently, Dr. Konda filed an ex parte application for hearing on January 22, 2020 to withdraw the Prof. at UC Davis' declaration and served counsel for the Defendants on January 21, 2020 at 9:36AM.

159. On February 4, 2020, Dr. Konda e-filed the Declaration of Professor Vipin Chaudhary, Ph.D., State University of New York Buffalo (hereinafter referred to as "Dr. Chaudhary") that Dr. Konda's confidential Trade Secret List indeed identified his trade secrets with reasonable particularity. Dr. Konda filed Dr. Chaudhary's declaration as confidential and under Court Seal.

160. Consistent with Mr. Tate's previous threats to Dr. Konda to ruin Dr. Konda's career, Defendants Markovic, Wang, Flex Logix, Mr. Tate, Mr. Lamond, Mr. Hebert, and Dr. Lackman acted in concert either directly or indirectly through other persons to engage in witness tampering by threatening Prof. at UC Davis to demand that he withdraw his declaration and intimidating him to change his sworn testimony.

161. Consistent with Mr. Tate's previous threats to Dr. Konda to ruin Dr. Konda's career, Defendants Markovic, Wang, Flex Logix, Mr. Tate, Mr. Lamond, Mr. Hebert, and Dr. Lackman deprived Dr. Konda of the support of Prof. at UC Davis who has assisted Dr. Konda on this case from June 2016.

162. During licensing negotiations with potential licensees, the potential licensees, for example, Achronix Semiconductor Corporation, an FPGA Company, have stated that the materials published on Flex Logix's website, including the 2011 VLSI Paper, indicate that Defendants Markovic, Wang and Flex Logix are the innovators of the technology attempted to be licensed by Dr. Konda, whereas the technology is in fact based on the disclosures in the 2008 Konda Publications and 2011 Konda Publication using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, as well as Konda Business Knowledge and Practices disclosed in confidence to Markovic. Thus, potential licensees of Dr. Konda are being misled as to the true innovator of the technology.

163. Because they are being misled, Dr. Konda's potential licensees are questioning why they should obtain a license when Flex Logix is commercializing eFPGAs without a license from Dr. Konda. This has resulted in a substantial loss of revenue to Dr. Konda.

164. Dr. Konda was not aware of Defendants Markovic's and Wang's covert scheme to misappropriate Dr. Konda's trade secrets and the confidential and proprietary implementation

details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals and the Business Knowledge and Practices disclosed in confidence to Markovic. Here, the California discovery rule prevented the statute of limitations from running during the period of Defendants Markovic's and Wang's concealment and intentional misrepresentations to Dr. Konda that delayed any suspicion of Defendants' scheme. Dr. Konda was alerted by Dr. Betz on December 18, 2015 only that Defendants Markovic and Wang had founded an FPGA company. Dr. Konda responded by trying to reach Dr. Bonomi and by launching his investigation to ferret out information about Flex Logix, finally culminating in gathering enough information to form a suspicion of wrongdoing by Markovic and Wang memorialized in an email to Flex Logix and Markovic's employer UC Regents on March 27, 2016. Flex Logix then responded by initiating continuous settlement negotiations which extended over the period of a year-and-a-half, including a lawsuit filed by Flex Logix against Dr. Konda and Konda Tech during the ongoing settlement negotiations. After Flex Logix dismissed its lawsuit, Dr. Konda filed a lawsuit against Flex Logix in the Federal District Court on December 17, 2018, within three years of his visit with Dr. Betz. Dr. Konda dismissed his lawsuit in the Federal District Court on April 3, 2019, without prejudice, and filed the present action in this court on the same day. Notably, the settlement discussions with Flex Logix spanned the filing of the lawsuits and continued through at least August 6, 2019. **Thus, the period of the statute of limitations did not run.**

165. Dr. Konda notes that **the core nucleus of this complaint** is not patent infringement nor misappropriation of trade secrets listed on Dr. Konda's Confidential Trade Secret List. Rather, this complaint is directed to the following causes of action.

## FIRST CAUSE OF ACTION
**(Unfair Business Practices)**

Defendants: Markovic, Wang, Flex Logix, Mr. Tate, UC Regents, and Dr. Lackman

166. Dr. Konda incorporates by reference every allegation contained in each and every one of the above paragraphs, as though set forth fully herein.

167. Defendants Markovic and Wang did not have Dr. Konda's authorization to implement the disclosures in the 2008 Konda Publications and 2011 Konda Publication or use the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals.

168. Neither did Defendants Markovic and Wang have Dr. Konda's authorization to publish technical papers or Wang's 2013 Ph.D. Dissertation plagiarizing and incorporating substantial portions of the disclosures in the 2008 Konda Publications and 2011 Konda Publication and the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, including plagiarizing substantial portions of text and drawings of the 2008 Konda Publications and 2011 Konda Publication, never citing to Dr. Konda's proprietary layouts in their technical papers or in Wang's 2013 Ph.D. Dissertation, without attribution to Dr. Konda or Konda Tech. (*See,* Chaudhary Decl. at ¶¶ 16-19, ¶¶ 20-28 and ¶¶ 29-33.)

169. Defendant Wang fraudulently received a distinguished dissertation award (his dissertation advisor being Defendant Markovic), which dissertation plagiarized the disclosures in the 2008 Konda Publications and 2011 Konda Publication and the confidential and included proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, without authorization from or attribution to Dr. Konda or Konda Tech. Defendants Markovic and Wang also published the 2011 VLSI Paper, which plagiarized the disclosures in the 2008 Konda Publications and incorporated the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, without authorization from or attribution to Dr. Konda or Konda Tech. (*See,* Id.)

170. Additionally, Defendants Markovic and Wang won the best paper award at the 2014 ISSCC Conference for the 2014 ISSCC Paper, which plagiarized the disclosures in the 2008 Konda Publications and 2011 Konda Publication and contained confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant

Markovic in confidence to prepare the Two Confidential DARPA Proposals, without authorization from or attribution to Dr. Konda or Konda Tech. (*See*, Id.)

171. By doing so, Defendants Markovic and Wang usurped credit for the breakthrough technology developed by Dr. Konda.

172. Notably, Flex Logix touts the 2014 ISSCC paper on its website as describing Flex Logix's "new, patented interconnect, XFLX™", misleading the public that Dr. Konda's innovations are instead innovations by Flex Logix. *See*, http://www.flex-logix.com/fpga-tutorial/.

173. Furthermore, Defendant Markovic's bio on the Flex Logix website touts that he supervised Wang's 2013 PhD Dissertation that won the distinguished dissertation award, notwithstanding that Wang's 2013 PhD Dissertation plagiarizes the texts and drawings of the disclosures in the 2008 Konda Publications and 2011 Konda Publication and includes confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, misleading the public that Dr. Konda's innovations are instead innovations of Flex Logix. (*See*, Chaudhary Decl. at ¶¶ 16-19, ¶¶ 23-25 and ¶¶ 29, 31-32.)

174. Moreover, Defendant Wang's bio on the Flex Logix website touts Wang's 2013 PhD Dissertation winning the distinguished dissertation award, which is a plagiarization of the texts and drawings of the disclosures in the 2008 Konda Publications and 2011 Konda Publication and incorporates confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, misleading the public that Dr. Konda's innovations are instead innovations of Flex Logix. (*See*, Chaudhary Decl. at ¶¶ 16-19, ¶¶ 23-5 and ¶¶ 29, 31-32.)

175. As a result, Defendants have misrepresented to the public, including potential customers of Dr. Konda and Konda Tech, that they are the innovators and owners of the innovations disclosed in the 2008 Konda Publications and 2011 Konda Publication and the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals. Hence,

Defendants are liable for unfair business practices under California Business and Professions Code Sections 17200, *et seq*.

176. Defendants have also substantially harmed Dr. Konda by usurping the innovations disclosed in the 2008 Konda Publications and 2011 Konda Publication and the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals and misrepresenting to the public that Defendants are the innovators instead of Dr. Konda.

177. Defendants Markovic, Wang, and Flex Logix have intentionally confused customers and potential customers for FPGA technology by misleading them to believe that Defendants were the innovators of the FPGA interconnect that the marketplace associates with Dr. Konda, or by misleading potential customers that Defendants are licensed by Dr. Konda. Dr. Konda has been deprived of customer licensees and revenue by Defendants Markovic's and Wang's co-founding of Hierlogix and Flex Logix in competition with Dr. Konda and Konda Tech using the disclosures in the 2008 Konda Publications and 2011 Konda Publication and the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals to compete against Dr. Konda without a license from or the authorization of Dr. Konda. Defendants Markovic and Wang and the companies they co-founded, Hierlogix with funding by UCLA/ITA and its successor Flex Logix, have caused severe harm in terms of Dr. Konda's loss of business opportunities and taking credit for the breakthroughs in technology that Dr. Konda made, but which are falsely claimed by Defendants, which has deprived Dr. Konda's ability to secure licenses from potential customers.

178. Additionally, Mr. Tate, CEO of Flex Logix, has made threats, both directly to Dr. Konda, as well as to the executive of a competitor of Flex Logix to intimidate the competitor to prevent it from doing any business with Dr. Konda or Konda Tech, with the intent to destroy Konda Tech and Dr. Konda.

179. Defendants Markovic, Wang, and Flex Logix intentionally and substantially interfered with Dr. Konda and Konda Tech by falsely representing that the innovations described in the

2011 VLSI Paper, Wang's 2013 Ph.D. Dissertation, and the 2014 ISSCC Paper are innovations of Defendants. (*See*, Chaudhary Decl. at ¶¶ 16-19, ¶¶ 20-28 and ¶¶ 29-33.)

180. Dr. Lackman, a director of UCLA/ITA, rejected to fund Konda Tech in 2009 stating that Konda technology (which has FPGA interconnect as the core innovation) was built outside UCLA.

181. Dr. Lackman knew that Defendants Markovic and Wang were building Hierlogix in the field of FPGAs using FPGA interconnect as the core differentiation.

182. UCLA/ITA funded Hierlogix, which is substantially based on the 2009 Konda Tech presentation disclosed in confidence by Dr. Konda to Dr. Lackman, UCLA/ITA on October 12, 2009.

183. Hierlogix was funded by UCLA/ITA, of which Defendant Lackman is a board member and participated in the decision to fund Hierlogix. Hierlogix even today on the UCLA/ITA website at https://www.ita.ucla.edu/companies/ describes "Hierlogix provides Energy-Efficient Hierarchical FPGA and Programming Tools. By developing a revolutionary new interconnect architecture, Hierlogix can provide hardware and software tools that are capable of greatly reducing FPGA power and size requirements, while producing higher speeds and performance." However, the "revolutionary new interconnect architecture" is in fact proprietary to Dr. Konda as disclosed in the 2008 Konda Publications and 2011 Konda Publication.

184. Before funding Hierlogix, Dr. Lackman should have asked Defendants Markovic and Wang about the competitive landscape. Particularly, Dr. Lackman should have asked how Hierlogix's purported FPGA interconnect is different from the disclosure in the Konda Tech Business Presentation to UCLA/ITA on October 12, 2009 and the disclosures in the 2008 Konda Publications and 2011 Konda Publication and the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals.

185. Dr. Lackman sent a LinkedIn connection request to Dr. Konda in 2013 and then withdrew the request after Defendant Markovic talked to Dr. Lackman. Dr. Lackman knowingly funded Hierlogix in spite of being founded based on the Konda Tech Business Presentation to

UCLA/ITA on October 12, 2009 and the disclosures in the 2008 Konda Publications and 2011 Konda Publication and the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals. Therefore, Dr. Lackman was and is fully aware that Hierlogix was founded based on stealing Konda Tech's FPGA interconnect technology and thereby joined the ongoing conspiracy by Markovic and Wang.

186. Dr. Lackman did not respond to Dr. Konda's email sent to him on March 27, 2016. Dr. Lackman has never responded to Dr. Konda's April 7, 2016 email. UCLA/ITA was at that time and continues to be aware of the unauthorized use by Hierlogix and Flex Logix of the disclosures in the 2008 Konda Publications and 2011 Konda Publication and using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals.

187. The UCLA/ITA website even today refers to the funding of Hierlogix. Flex Logix is the successor in interest to Hierlogix. UC Regents is believed to have a financial interest in Flex Logix and knowingly benefits from the false claim by Flex Logix to be the innovator of the FPGA interconnect technology incorporated into Flex Logix's FPGA products.

188. The false claim of innovation on the part of Flex Logix misleads the public, including potential customers and customers of Dr. Konda and Konda Tech.

189. The misleading unlawful acts of Flex Logix, as described above, constitute unfair and unlawful business practices pursuant to Business & Professions Code Section 17200, *et seq.*

190. Due to the unlawful conduct described herein, Dr. Konda has been and continues to be deprived of granting licenses, resulting in economic harm to Dr. Konda.

191. Konda Tech has duly assigned the right to prosecute this action to Dr. Konda, who is the sole shareholder and owner of Konda Tech, by Board Action by Written Consent of the Shareholders on March 31, 2019 before this action was filed. (*See*, Exhibit 9 attached hereto.) Therefore, Dr. Konda has standing to bring this cause of action for unfair and unlawful business practices pursuant to Business & Professions Code Section 17200, *et seq.*

192. As a direct and proximate result of their acts mentioned herein, Defendants have received and continue to receive ill-gotten gains belonging to Dr. Konda.

193. Dr. Konda is entitled to restitution for losses and has been damaged in an amount in excess of $300,000 and to be established at trial.

194. Because the conduct alleged herein is ongoing, and there is no indication that Defendants will cease their unlawful conduct described herein, Dr. Konda requests that this Court enjoin Defendants from further violations of California's laws.

## SECOND CAUSE OF ACTION

**Unfair Competition (Passing off)**

Defendants: Markovic, Wang, UC Regents, Dr. Lackman, and Flex Logix

195. Dr. Konda incorporates by reference every allegation contained in each and every one of the above paragraphs, as though set forth fully herein.

196. Defendants Markovic and Wang knew that they did not have Dr. Konda's authorization to implement the disclosures in the 2008 Konda Publications and 2011 Konda Publication and use the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals to do so, or to publish technical papers plagiarizing and incorporating substantial portions of the disclosures in the 2008 Konda Publications and 2011 Konda Publication and the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, in view of Konda Business Knowledge and Practices, or to plagiarize substantial portions of text and drawings of the 2008 Konda Publications and 2011 Konda Publication, never citing to Dr. Konda's proprietary layouts in their technical papers or in Wang's 2013 Ph.D. Dissertation, without the authorization of Dr. Konda and without attribution to Dr. Konda or Konda Tech. (*See*, Chaudhary Decl. at ¶¶ 16-19, ¶¶ 20-28 and ¶¶ 29-33.)

197. Dr. Konda's innovations have acquired a reputation as a revolutionary breakthrough technology in the field of FPGA interconnect and have generated substantial goodwill in the marketplace for significant area, power, and performance improvements in FPGA interconnect.

198. QuickLogic purchased a non-exclusive license based on the reputation and goodwill established by Dr. Konda and Konda Tech in the FPGA industry.

199. Defendants Markovic, Wang, and Flex Logix have intentionally confused customers and potential customers for FPGA products by selling products that the marketplace associates with Dr. Konda and Konda Tech by misleading potential customers to believe that Defendants are licensed by Dr. Konda and Konda Tech, thereby passing off Flex Logix's products as products produced under license or authorization by Dr. Konda or Konda Tech.

200. During licensing negotiations with potential licensees, the potential licensees, for example, Achronix Semiconductor Corporation, an FPGA Company, have stated to Dr. Konda that the materials published on Flex Logix's website, including the 2011 VLSI Paper, indicate that Defendants Markovic, Wang, and Flex Logix are the innovators of the technology attempted to be licensed by Dr. Konda, whereas the technology is in fact based on the disclosures in the 2008 Konda Publications and 2011 Konda Publication using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals Thus, potential licensees of Dr. Konda are being misled as to the true innovator of the technology.

201. Dr. Lackman knew that Defendants Markovic and Wang were founding Hierlogix in the field of FPGAs using FPGA interconnect as the core differentiation. Dr. Lackman led the UCLA/ITA funding of Hierlogix, which is substantially based on the confidential 2009 Konda Tech Business Presentation given by Dr. Konda to Dr. Lackman, UCLA/ITA on October 12, 2009 in confidence.

202. Hierlogix was funded by UCLA/ITA, of which Defendant Lackman is a board member, who joined in the decision to fund Hierlogix. Hierlogix even today on the UCLA/ITA website at https://www.ita.ucla.edu/companies/ describes: "Hierlogix provides Energy-Efficient

Hierarchical FPGA and Programming Tools. By developing a revolutionary new interconnect architecture, Hierlogix can provide hardware and software tools that are capable of greatly reducing FPGA power and size requirements, while producing higher speeds and performance." The "revolutionary new interconnect architecture" is in fact proprietary to Dr. Konda as disclosed in the 2008 Konda Publications and 2011 Konda Publication.

203. Dr. Konda has received questions from customers and potential customers whether Flex Logix is a licensee of Dr. Konda and Konda Tech and whether Dr. Konda is in actuality the true innovator. The goodwill of Dr. Konda and Konda Tech has been diminished by Flex Logix passing off its products without a license from Dr. Konda and Konda Tech.

204. Dr. Konda has suffered and is suffering damages because Defendants have confused customers that Defendants' FPGA products are authentic FPGA interconnect products based on Dr. Konda's innovations.

205. As a result, Dr. Konda and Konda Tech have lost goodwill with customers and have experienced difficulty in licensing potential customers.

206. Dr. Konda is entitled to damages for losses suffered and has been damaged in an amount in excess of $300,000 and to be established at trial.

207. Dr. Konda is also entitled to punitive damages.

## THIRD CAUSE OF ACTION

(**Fraud – Intentional Misrepresentation**)

Defendants: Markovic and Wang

208. Dr. Konda incorporates by reference every allegation contained in each and every one of the above paragraphs, as though set forth fully herein.

209. Defendant Markovic intentionally made false representations that harmed Dr. Konda by covering up the Defendants' scheme to commercialize FPGA products based on Dr. Konda's innovations without a license or authorization from Dr. Konda.

210. Defendant Markovic represented to Dr. Konda that he would assist Konda Tech to secure funding for Konda Tech to bring products based on the disclosures in the 2008 Konda

Publications and 2011 Konda Publication and the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals to the market. Defendant Markovic's representation was false.

211. Defendant Markovic knew that his representation was false when he made it, because he knew that UCLA/ITA only funds technologies developed within UCLA. Neither Dr. Konda nor Konda Tech have any nexus to UCLA and therefore did not qualify for funding by UCLA/ITA.

212. Dr. Konda did not become aware that funding by UCLA/ITA was not available until after he provided Konda Tech's confidential and proprietary business plan provided in confidence to Defendant Markovic prior to the scheduled presentation by Dr. Konda to UCLA/ITA. Had Dr. Konda been informed that UCLA/ITA does not fund technologies built outside UCLA, he would not have disclosed any confidential and proprietary information to Defendant Markovic.

213. Thereafter, Defendant Markovic contacted Dr. Konda pretending that he would help build Konda Tech by implementing the 2008 Konda Publications and the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals by submitting the Two Confidential DARPA Proposals with the promise that 1) if the Two Confidential DARPA proposals were granted, he would obtain a license from Konda Tech; and 2) otherwise if the proposals were rejected by DARPA, he would have his student Defendant Wang cease the chip implementations and any previous implementations would be used for academic purposes only.

214. Defendant Markovic intentionally made false representations to Dr. Konda that the chip implementations by him and his students, including Defendant Wang, would be used for academic purposes when in fact the work by Defendants Markovic and Wang implementing the 2008 Konda Publications and 2011 Konda Publication using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals were intended to

form the groundwork and head start for Defendants Markovic and Wang obtaining funding from UCLA/ITA to start up Hierlogix and its successor Flex Logix in competition with Konda Tech.

215. Additionally, Defendant Markovic intentionally made false representations to Dr. Konda in April 2013 when he invited Dr. Konda to meet at Stanford University while Defendant Markovic represented he was a Visiting Professor. When they met, Dr. Konda inquired whether Defendant Markovic and his students had discontinued implementing Konda's publications as part of the academic work at UCLA. Defendant Markovic falsely replied "yes." During the conversation, Defendant Markovic also asked Dr. Konda to inform him of the names of customers he was currently working with to license innovations disclosed in the 2008 Konda Publications and 2011 Konda Publication and the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, which Dr. Konda provided in confidence to Defendant Markovic in the belief that he was still trying to help Konda Tech when in fact, unbeknownst to Dr. Konda, Defendants Markovic and Wang had previously founded Hierlogix to commercially compete with Konda Tech.

216. Also, in January, 2014, while Defendant Markovic represented he was a Visiting Professor at Stanford University, Dr. Konda and Defendants Markovic and Wang met with Dr. Bonomi at his residence. When Dr. Konda queried if Defendants Markovic's and Wang's startup (i.e., Hierlogix) was in the area of wireless and digital signal processors (DSPs), Defendant Markovic falsely said "yes," which was an intentional misrepresentation because Defendants Markovic and Wang had previously founded Hierlogix with funding from UCLA/ITA to commercialize embedded FPGA blocks by covertly implementing the disclosures in the 2008 Konda Publications and 2011 Konda Publication using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals without having a license or authorization from Konda Tech.

217. Defendant Markovic intended that Dr. Konda rely on his telling Dr. Konda that he was helping Konda Tech so that Konda Tech would provide him with information in confidence over

a period of years based on his intentionally misrepresenting his intentions of helping Konda Tech when in truth he was extracting technical and business information from Dr. Konda for his own purposes in learning about the FPGA industry to launch a commercial venture with Defendant Wang and exploit the information fraudulently extracted from Dr. Konda and using the disclosures in the 2008 Konda Publications and 2011 Konda Publication and the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals and the Konda Business Knowledge and Practices disclosed to Defendant Markovic in confidence as the basis for Defendants commercial venture.

218. Defendants used the proprietary and confidential information provided by Dr. Konda and Konda Tech to develop FPGA chips which later became the basis for Defendants Markovic and Wang to found Hierlogix and its successor Flex Logix.

219. By Defendants Markovic and Wang using the 2008 Konda Publications and 2011 Konda Publication and the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals in view of Konda Business Knowledge and Practices for the benefit of their later founded commercial ventures, Defendants have deprived Konda Tech of revenue it would otherwise have received.

220. Defendant Markovic intended that Dr. Konda and Konda Tech rely on his intentional misrepresentations in providing confidential and proprietary information to Defendant Markovic.

221. But for that reliance, Dr. Konda and Konda Tech would not have disclosed any confidential and proprietary information to Defendant Markovic.

222. But for that reliance Dr. Konda would not have disclosed to Defendant Markovic the confidential information that a) Dr. Konda did not publish technical papers at technical conferences, and that the reviewers of technical papers are typically not knowledgeable about patents/patent publications such as Dr. Konda's patent publications, including the 2008 Konda Publications; b) Dr. Konda did not attend generic integrated circuit conferences; c) Dr. Konda

attends only FPGA conferences; d) Dr. Konda was not building an FPGA product company and had adopted a licensing model for Dr. Konda's innovations.

223. Dr. Konda's reliance on the intentional misrepresentations by Defendant Markovic that he was helping Konda Tech was a substantial factor in the harm to Dr. Konda and Konda Tech.

224. The unlawful conduct described herein has resulted in economic harm to Dr. Konda.

225. As a direct and proximate result of their acts of intentional misrepresentation mentioned herein, Defendants have received and continue to receive ill-gotten gains belonging to Dr. Konda and have unjustly enriched themselves at the expense of Dr. Konda.

226. Monetary damages are not sufficient to compensate Dr. Konda for the intentional misrepresentations that enabled Defendants to found Hierlogix and its successor Flex Logix and illicitly receive equity in those companies. Dr. Konda was damaged by being excluded as a founder notwithstanding the fact that the unauthorized use by Defendants Markovic and Wang of the disclosures in the 2008 Konda Publications and 2011 Konda Publication and the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals was instrumental to Defendants being founders of Hierlogix and its successor Flex Logix. Without such unauthorized use of the disclosures in the 2008 Konda Publications and 2011 Konda Publication and the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, Defendants Markovic and Wang would not have received the amount of founders shares they received in either of these companies. Dr. Konda is entitled to equitable damages in an amount of Defendant Markovic's and Defendant Wang's shares of Hierlogix and its successor Flex Logix that should have been issued to Dr. Konda to recognize the unauthorized and uncompensated use by Defendants Markovic and Wang of the disclosures in the 2008 Konda Publications and 2011 Konda Publication and the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals in view of Konda Business Knowledge and Practices, because they were unjustly enriched. Therefore, Defendants

Markovic and Wang should disgorge to Dr. Konda an amount of their founders' shares in Hierlogix and its successor Flex Logix to be determined at trial.

227. Dr. Konda is also entitled to punitive damages.

**FOURTH CAUSE OF ACTION**
**(Fraud – Concealment)**
Defendants: Markovic and Wang

228. Dr. Konda incorporates by reference every allegation contained in each and every one of the above paragraphs, as though set forth fully herein.

229. Defendants Markovic and Wang prevented Dr. Konda and Konda Tech from discovering certain facts, and intended to deceive Dr. Konda and Konda Tech by concealing facts. Defendant Markovic intentionally concealed the fact that his students had started to implement FPGA chips based on the 2008 Konda Publications and 2011 Konda Publication and the confidential and proprietary implementation details without authorization from Dr. Konda and Konda Tech. Defendants Markovic and Wang published papers and received awards for those papers without acknowledging that their work was essentially based on the work by Dr. Konda and the disclosures in the 2008 Konda Publications and 2011 Konda Publication and the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals.

230. Defendant Markovic intentionally concealed the facts that his then student Defendant Wang intended to obtain a Ph.D. and that Defendants Markovic and Wang wanted to publish technical papers and then eventually co-found Hierlogix and its successor Flex Logix based on the disclosures in the 2008 Konda Publications and 2011 Konda Publication and the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals.

231. Dr. Konda was not aware of Defendant Wang's Ph.D. Dissertation and technical paper publications by Defendants Markovic and Wang and eventual co-founding of Hierlogix and its

successor Flex Logix. These facts were concealed from Dr. Konda when Defendant Markovic and Dr. Konda communicated occasionally over the period of October, 2009 through March, 2014. Dr. Konda did not discover that Defendants concealed facts until after December 18, 2015.

232. Defendant Markovic intentionally deceived Dr. Konda. Defendants Markovic and Wang used the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals and to learn about FPGA business models and the FPGA industry with respect to interconnect technology and its evolution. However, Defendant Markovic deceived Dr. Konda by concealing how he was using the information that he obtained in confidence from Dr. Konda. Had Defendant Markovic told Dr. Konda that his intention, along with Defendant Wang, of how they were going to use the information they obtained from Dr. Konda, Dr. Konda would have immediately stopped communicating with Defendants Markovic and Wang.

233. In January, 2014, while Defendant Markovic was purportedly a Visiting Professor at Stanford University, Dr. Konda and Defendants Markovic and Wang met with Dr. Bonomi at his residence. During that meeting, Defendants Markovic and Wang concealed the fact that they had previously founded Hierlogix with funding from UCLA/ITA and were on the verge of founding its successor Flex Logix to commercialize embedded FPGA blocks based on covertly implementing the disclosures in the 2008 Konda Publications and 2011 Konda Publication using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, without having a license or authorization from Dr. Konda.

234. Subsequently, Dr. Konda and Defendants Markovic and Wang met Dr. Iyer at Memoir's offices on March 5, 2014. At that meeting Defendants Markovic and Wang again concealed from Dr. Konda the fact that both Hierlogix and their new startup Flex Logix were building FPGA products based on the disclosures in the 2008 Konda Publications and 2011 Konda Publication using the confidential and proprietary implementation details and technical know-

how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals relating to a revolutionary interconnect architecture.

235. As a result of the concealment of their use of the disclosures in the 2008 Konda Publications and 2011 Konda Publication and the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, Defendants have caused severe harm in terms of Dr. Konda's and Konda Tech's loss of business opportunities and taking credit for the breakthroughs in technology that Dr. Konda has made, which has negatively impacted Dr. Konda's and Konda Tech's ability to secure licenses from potential customers.

236. Defendants also concealed that they started a company, Hierlogix, and subsequently Flex Logix, based on the disclosures in the 2008 Konda Publications and 2011 Konda Publication and the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, without disclosing these facts to Dr. Konda.

237. Defendants Markovic and Wang concealed that their aim was to build their own company by implementing and commercializing FPGAs based on the disclosures in the 2008 Konda Publications and 2011 Konda Publication using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals on the pretense of helping to obtain funding for Konda Tech.

238. Plaintiff did not become aware of the concealed facts until after December 18, 2015.

239. Had the omitted facts been disclosed to Dr. Konda, Dr. Konda reasonably would have behaved differently.

240. Dr. Konda was harmed by the deprivation to Konda Tech of revenue it would otherwise have received as a result of the facts concealed by Defendants.

241. Defendants' concealment was a substantial factor in causing harm to Dr. Konda.

242. Monetary damages are not sufficient to compensate Dr. Konda for the intentional misrepresentations that enabled Defendants to found Hierlogix and its successor Flex Logix and

illicitly receive equity in those companies. Dr. Konda was damaged by being excluded as a founder notwithstanding the fact that the unauthorized use by Defendants Markovic and Wang of the disclosures in the 2008 Konda Publications and 2011 Konda Publication and the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals was instrumental to Defendants being founders of Hierlogix and its successor Flex Logix. Without such unauthorized use of the disclosures in the 2008 Konda Publications and 2011 Konda Publication and the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, Defendants Markovic and Wang would not have received the amount of founders shares they received in either of these companies. Dr. Konda is entitled to equitable damages in an amount of Defendant Markovic's and Defendant Wang's shares of Hierlogix and its successor Flex Logix that should have been issued to Dr. Konda to recognize the unauthorized and uncompensated use by Defendants Markovic and Wang of the disclosures in the 2008 Konda Publications and 2011 Konda Publication and the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals in view of Konda Business Knowledge and Practices, because they were unjustly enriched. Therefore, Defendants Markovic and Wang should disgorge to Dr. Konda an amount of their founders' shares in Hierlogix and its successor Flex Logix to be determined at trial.

243. Dr. Konda is also entitled to punitive damages

**FIFTH CAUSE OF ACTION**

**(Conversion)**

Defendants: Markovic, Wang, and Flex Logix

244. Plaintiff incorporates by reference every allegation contained in each and every one of the above paragraphs, as though set forth fully herein.

245. Defendant Markovic had trolled Dr. Konda in confidence to obtain the confidential information that a) Dr. Konda did not publish technical papers at technical conferences, and that the reviewers of technical papers are typically not knowledgeable about patents/patent publications such as Dr. Konda's patent publications, including the 2008 Konda Publications; b) Dr. Konda did not attend generic integrated circuit conferences; c) Dr. Konda attends only FPGA conferences; d) Dr. Konda was not building an FPGA product company and had adopted a licensing model including Konda's patent publications and the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals.

246. Without Dr. Konda's authorization or attribution to Dr. Konda, Defendants Markovic and Wang presented the 2011 VLSI Paper, based on the disclosures in the 2008 Konda Publications as well as the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, as well as Konda Business Knowledge and Practices which Dr. Konda had previously disclosed to Defendant Markovic in confidence. (*See*, Dr. Chaudhary Decl. at ¶¶ 16-19, ¶¶ 20-22 and ¶¶ 29-30.)

247. Defendants Markovic and Wang blatantly plagiarized the disclosures in the 2008 Konda Publications and shamelessly published the 2011 VLSI Paper in which they intentionally misrepresented that Dr. Konda's alternate vertical and horizontal layout of Benes/BFT layouts was their innovation in furtherance of their illicit scheme of depriving Dr. Konda of his innovations. (*See*, Id.)

248. Without his authorization or attribution to Dr. Konda, Wang's 2013 Ph.D. dissertation brazenly copies the 2008 Konda Publications and 2011 Konda Publication, especially the figures and layouts, as shown by the highlighted portions of Exhibit 22. (*See*, Dr. Chaudhary Decl. at ¶¶ 16-19, ¶¶ 23-25 and ¶¶ 29, 31-32.)

249. Defendants Markovic and Wang blatantly plagiarized the disclosures in the 2008 Konda Publications and shamelessly published the 2014 ISSCC Paper. (*See*, Dr. Chaudhary Decl. at ¶¶ 16-19, ¶¶ 26-28 and ¶ 29, ¶ 31, ¶ 33.)

250. In October 2018, Dr. Konda for the first time submitted technical papers to the 2019 ACM/SIGDA International Symposium on Field Programmable Gate Arrays, where the technical papers were reviewed double- blinded, i.e., both the author's name and author's affiliation were blinded from all the reviewers. In response to the technical paper Dr. Konda submitted in November 2018, which was titled "Hierarchical FPGA Fabrics using 2D-Benes-BFT-Pyramid Network Layouts with Optimizations", one of the reviewers pointed to Wang's 2013 Ph.D. Dissertation, and a second reviewer pointed to the 2014 ISSCC Paper stating that the subject matter was already described in Wang's 2013 Ph.D. Dissertation and 2014 ISSCC Paper. (*See*, Exhibit 35 attached hereto.) Clearly, those two reviewers mistakenly believed that Defendants Markovic and Wang were the innovators of the disclosures in the 2008 Konda Publications and 2011 Konda Publication using the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals and the 2011 Konda Publication. (*See*, Dr. Chaudhary Decl. at ¶¶ 16-19, ¶¶ 23-28 and ¶¶ 29, 31-33.)

251. Dr. Konda claims that Defendants Markovic and Wang have wrested away, usurped, and wrongfully exercised control over Dr. Konda's innovations disclosed in the 2008 Konda Publications and 2011 Konda Publication, and the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals in view of the Konda Business Knowledge and Practices disclosed by Dr. Konda to Defendant Markovic in confidence.

252. Konda Tech owned the right to possess Konda's confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, as well as the 2008 Konda Publications and 2011 Konda Publication innovated by Dr. Konda.

253. Defendants Markovic and Wang intentionally and substantially interfered with Konda's innovations by falsely representing their innovations as their innovation in the 2011 VLSI Paper, Wang's 2013 Ph.D. Dissertation, and the 2014 ISSCC Paper.

254. Defendants Markovic and Wang intentionally and substantially interfered with Konda's innovations based on confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, as well as the 2008 Konda Publications and 2011 Konda Publication, refusing to acknowledge Dr. Konda as the true innovator after Dr. Konda demanded then to do so.

255. Dr. Konda did not consent to Defendants' possession of Konda's confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals, as well as the 2008 Konda Publications and 2011 Konda Publication for their use.

256. Dr. Konda has been and continues to be harmed by Defendants' actions.

257. Defendants Markovic's and Wang's, and Flex Logix's conduct was a substantial factor in causing Dr. Konda's harm.

258. Dr. Konda is entitled to restitution for losses and has been damaged in an amount in excess of $300,000 and to be established at trial.

259. Dr. Konda is also entitled to punitive damages.

**SIXTH CAUSE OF ACTION**

**(Breach of Confidential Relationship)**

Defendants: Markovic and Wang

260. Plaintiff incorporates by reference every allegation contained in each and every one of the above paragraphs, as though set forth fully herein.

261. One who discloses or uses another's confidential information, without a privilege to do so, is liable to the other if his disclosure or use constitutes a breach of confidence reposed in him by the other in disclosing the confidential information to him.

262. Defendant Markovic by presenting himself as an advisor to Dr. Konda and a fund raiser for Konda Tech and obtaining confidential from Dr. Konda entered into a confidential relationship with Dr. Konda.

263. Dr. Konda provided Konda Tech's confidential Business Presentation to Defendant Markovic on October 7, 2009 in confidence. (*See*, Exhibit 13 attached hereto in a Confidential and sealed envelope.)

264. On the pretense of being an advisor and fund raiser over a period of years (i.e., from 2009 – 2014), Defendant Markovic gained access to the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals and the Konda Business Knowledge and Practices which Dr. Konda disclosed to Markovic in confidence.

265. Defendant Markovic disclosed the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals to Defendant Wang.

266. Defendant Wang knew that the confidential and proprietary implementation details and technical know-how and the Konda Business Knowledge and Practices disclosed to him by Defendant Markovic is the confidential information Dr. Konda disclosed in confidence to Defendant Markovic.

267. Defendants Markovic and Wang also disclosed the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals and the Konda Business Knowledge and Practices, which Dr. Konda had disclosed in confidence to Defendant Markovic, to Defendant Dr. Lackman.

268. Defendant Dr. Lackman knew the confidential and proprietary implementation details and technical know-how and the Konda Business Knowledge and Practices disclosed to him by Defendants Markovic and Wang was confidential information Dr. Konda disclosed in confidence to Defendant Markovic.

269. Defendants Markovic and Wang also disclosed the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals and the Konda

Business Knowledge and Practices, which Dr. Konda had disclosed in confidence to Defendant Markovic, to Defendant Flex Logix.

270. Defendant Flex Logix knew the confidential and proprietary implementation details and technical know-how which Dr. Konda had disclosed to Defendant Markovic in confidence to prepare the Two Confidential DARPA Proposals and the Konda Business Knowledge and Practices disclosed to by Defendants Markovic and Wang is the confidential information Dr. Konda disclosed in confidence to Defendant Markovic.

271. Defendant Markovic was Dr. Konda's confidant as Dr. Konda's advisor and fund raiser for Konda Tech.

272. Defendant Markovic had information relating to Dr. Konda and Konda Tech that Defendant Markovic knew or should have known was confidential.

273. Defendant Markovic disclosed and used Dr. Konda's confidential information for Defendant Markovic's own benefit.

274. Defendant Markovic communicated Dr. Konda's confidential information to Defendants Wang, Dr. Lackman, Hierlogix, and Flex Logix.

275. Dr. Konda did not give authorization for Markovic's conduct.

276. The confidential information disclosed by Dr. Konda to Defendant Markovic was not a matter of general knowledge.

277. One who discloses or uses another's confidential information, without a privilege to do so, is liable to the other if his disclosure or use constitutes a breach of confidence reposed in him by the other in disclosing the confidential information to him.

278. Dr. Konda claims that he was harmed by Defendant Markovic's breach of the confidential relationship with Dr. Konda.

279. Dr. Konda was harmed.

280. Defendant Markovic's conduct was a substantial factor in causing Dr. Konda's harm.

281. Dr. Konda is entitled to restitution for losses and has been damaged in an amount in excess of $300,000 and to be established at trial.

282. Dr. Konda is also entitled to punitive damages.

**SEVENTH CAUSE OF ACTION**

**(Intentional Interference With Prospective Economic Relations)**

Defendants: Mr. Tate and Flex Logix

283. Dr. Konda incorporates by reference every allegation contained in each and every one of the above paragraphs, as though set forth fully herein.

284. On May 30, 2017, Mr. Tate threatened Dr. Konda that: "One of the senior board members of Flex Logix [alluding to Mr. Lamond] will ruin your career if you or Konda Tech files a lawsuit against Flex Logix."

285. On June 1, 2017, Mr. Tate reiterated his threat to Dr. Konda that: "One of the senior board members of Flex Logix [alluding to Mr. Lamond] will ruin your career if you or Konda Tech files a lawsuit against Flex Logix."

286. Consistent with his previous threats to Dr. Konda on May 30, 2017 and June 1, 2017, on June 3, 2019, Mr. Tate approached the executive of his competitor, an eFPGA vendor, and said to him: "Can you provide me with the contact information of your lawyers, I think they shall talk together." At this, the executive replied to Mr. Tate: "Geoff, we are grown up men, if you have something to tell me, tell me now." Mr. Tate said he saw Dr. Konda talking to him earlier in the day. Mr. Tate further threatened the executive that: "I wanted to tell you that what we have is something totally different from Konda claims. I hope you are not helping him in any way."

287. In so doing, Mr. Tate intentionally interfered with prospective economic relations between Dr. Konda and the eFPGA vendor with whom Dr. Konda was currently in negotiations that would have resulted in an economic benefit to Dr. Konda.

288. Mr. Tate observed Dr. Konda meeting with the eFPGA vendor and knew of the relationship between Dr. Konda and the eFPGA vendor.

289. Mr. Tate, consistent with his previous threats to Dr. Konda on May 30, 2017 and June 1, 2017, on June 3, 2019, engaged in intentional interference to disrupt the relationship between Dr. Konda and the eFPGA vendor.

290. By engaging in this conduct, Mr. Tate intended to disrupt the relationship between Dr. Konda and eFPGA vendor, or knew that disruption of the relationship was certain, or substantially certain to occur.

291. The relationship between Dr. Konda and eFPGA vendor was disrupted.

292. Dr. Konda was harmed and deprived of a potential license opportunity with the eFPGA vendor.

293. Mr. Tate's conduct was a substantial factor in causing Dr. Konda's harm.

294. Dr. Konda is entitled to restitution for losses and has been damaged in an amount in excess of $300,000 and to be established at trial.

295. Dr. Konda is also entitled to punitive damages.

**EIGHTH CAUSE OF ACTION**

**(Ongoing Conspiracy)**

Defendants: Flex Logix, UC Regents, Markovic, Wang, Mr. Tate, Mr. Lamond, Mr. Hebert, and Dr. Lackman

296. Dr. Konda incorporates by reference every allegation contained in each and every one of the above paragraphs, as though set forth fully herein.

297. Dr. Lackman, when he authorized funding of Hierlogix, was fully aware that Hierlogix was founded based on Dr. Konda's FPGA interconnect technology and joined the ongoing conspiracy of Defendants Markovic and Wang.

298. The Regents of The University of California joined the conspiracy to commit all the causes of action perpetrated by Defendants when UCLA/ITA funded Hierlogix.

299. Flex Logix is the successor to Hierlogix and has committed additional wrongdoing constituting unfair business practices, unfair competition, and intentional interference with prospective economic relations as a result of the actions by Defendants Markovic, Wang, and Mr. Tate, the CEO of Flex Logix.

300. The Regents of the University of California, under California Civil Code Section 815.2, subdivision (a) and Flex Logix are responsible for all acts done as part of the conspiracy, and the other named Defendants are all responsible whether the acts occurred before or after The Regents of the University of California and Flex Logix joined the conspiracy.

301. Defendants Mr. Tate, Mr. Lamond, Mr. Hebert, and Dr. Lackman joined the conspiracy as shown by their acts, directly or indirectly, through other persons.

302. Consistent with Mr. Tate's threats in 2017 - 2019 to Dr. Konda to ruin Dr. Konda's career, Flex Logix board members Mr. Tate, Mr. Lamond, Mr. Hebert, Wang and Markovic willfully and maliciously made Dr. Konda's confidential Trade Secret List public in an ongoing conspiracy.

303. All Defendants have committed actionable acts and continued their ongoing conspiracy even after Dr. Konda's original complaint and First Amended Complaint were filed.

304. Dr. Konda is entitled to damages for losses and has been damaged in an amount to be established at trial.

305. Dr. Konda is also entitled to punitive damages from Defendants with the exception of The Regents of The University of California.

## PRAYER AND RELIEF REQUESTED

WHEREFORE, Plaintiff respectfully prays for relief as follows:

A. For judgment in Dr. Konda's favor and against all Defendants as to each of the above causes of action;

B. For damages in the amount to be determined at trial;

C. An award to Dr. Konda for all damages legally and/or proximately caused by Defendants and equitable relief as set forth above, including costs and prejudgment interest and punitive damages as appropriate;

D. An injunction to enjoin further unfair business practices and passing off as described above;

E. An award to Dr. Konda of such other or additional relief as the Court deems just and proper.

DATED this 22nd day of March, 2021.

Respectfully submitted

By: /Venkat Konda/

Venkat Konda Ph.D.

**VERIFICATION**

I, VENKAT KONDA, Ph.D. declare:

I have read the forgoing Fourth Amended Complaint and know the contents thereof; that the same is true of my own knowledge, except as to the matters which are therein stated on my information and belief, and to those matters I believe it to be true.

I declare under penalty of perjury under the laws of the State of California that the forgoing is true and correct.

Executed on this 22nd day of March 2021, at San Jose, California.

/Venkat Konda/

Venkat Konda Ph.D.

# EXHIBITS 1-7 Reserved

# EXHIBIT 8

Gmail

Venkat Konda <venkat@kondatech.com>

## Your voicemail

1 message

**geoff tate Flex Logix** <geoff@flex-logix.com> Fri, Ma
To: Venkat Konda <venkat@kondatech.com>
Cc: geoff tate <geoff@flex-logix.com>

Hello Venkat,

I received your voicemail.

I doubt that we can reach a settlement.

But I am willing to listen.

I am out of town next week.

Let's meet Tuesday 30th May at 230pm at Starbucks, 750 Castro Street, Mountain View.

Thanks,

Geoff Tate, CEO

flexlogix Technologies, Inc.

www.flex-logix.com
2465 Latham Street, Suite 100
Mountain View, California 94040, USA

AT&T Unified Messaging℠

The attached message was recently left in your AT&T Unified Messaging℠ mailbox. We are sending you this email because you have asked for your messages to be forwarded to this address.
Voicemail transcription

> H oh hi jeff this is Venkat Konda. I am ... wondering if we can meet toreach a settlement. My phone number is (408) 472-3273. Please letme know if that is possible. I just want to reach out to you if there is away that we can settle by talking. Thank you.

# EXHIBIT 9

**ACTION BY WRITTEN CONSENT**
**OF THE SHAREHOLDERS OF**
**KONDA TECHNOLOGIES, INC.**

**MARCH 31, 2019**

In accordance with Section 307(b) of the California Corporations Code, it is deemed desirable and in the best interests of Konda Technologies, Inc., a California Corporation (the "Company"), California Corporation Number C2948645, that the following actions be taken by the Shareholders of this Company pursuant to this Written Consent.

**NOW, THEREFORE, BE IT RESOLVED** that the undersigned Shareholders of this Company hereby consent to, approve, and adopt the following:

**BOARD OF DIRECTORS**

**WHEREAS,** it is in the best interests of this Company to designate the number of directors as one (1); and

**WHEREAS,** Venkat Konda, Ph.D. is nominated as the sole director;

**NOW, THEREFORE, BE IT RESOLVED,** that Venkat Konda, Ph.D. be appointed sole director of the Company; and

**BE IT FURTHER RESOLVED**, that the Company assigns, and hereby does assign, to Venkat Konda, Ph.D. in his individual capacity, all rights, title, and interest in and to all choses in action and to file and prosecute said action against Dejan Markovic and Cheng C. Wang and all other persons responsible in some manner for the occurrences alleged therein.

**RESOLVED FURTHER**, that each of the officers of the Company is hereby authorized and directed to take such actions and to execute and file, or cause to be executed and filed, such modifications and other documents as are necessary or appropriate for such compliance with the laws of the State of California.

**THIS WRITTEN CONSENT OF SHAREHOLDERS** may be executed in one or more counterparts, each of which shall be the original and all of which together shall be one and the same instrument. This Unanimous Written Consent shall be filed in the Minute Book of the Company and become a part of the records of this Company.

**COMMON STOCK**

Dated: March 31, 2019

By: Venkat Konda

Venkat Konda, Ph.D. 10,000,000 shares

**MINUTES OF THE MEETING**

**OF THE BOARD OF DIRECTORS**

**KONDA TECHNOLOGIES, INC.**

**MARCH 31, 2019**

The duly noticed and duly scheduled Meeting of the Board of Directors of the above-referenced California Corporation (the "Company"), pursuant to the California Corporations Code, was convened on March 31, 2019.

1. ATTENDANCE. All of the members of the Board of Directors were in attendance.
2. CALL TO ORDER. Venkat Konda, Ph.D. called the meeting to order. Venkat Konda, Ph.D. was elected as Secretary of the Meeting. Venkat Konda, Ph.D. was also elected as Chairman of the Meeting.
3. ASSIGNMENT OF RIGHTS TO PURSUE LAWSUIT.

RESOLVED, that it is in the best interests of the Company to assign to Venkat Konda, Ph.D. in his individual capacity, all rights, title, and interest in and to all choses in action and to file and prosecute said action against Dejan Markovic and Cheng C. Wang and all other persons responsible in some manner for the occurrences alleged therein.

RESOLVED FURTHER, that the officers of this corporation are, and each acting alone is, hereby authorized to do and perform any and all such acts, including execution of any and all documents and certificates, as said officers shall deem necessary or advisable, to carry out the purposes of the foregoing resolution.

RESOLVED FURTHER, that any actions taken by such officers prior to the date of the foregoing resolution adopted hereby that are within the authority conferred thereby are hereby ratified, confirmed, and approved as the acts and deeds of this Company.

4. ADJOURNMENT. All applicable business having come before the Board and all relevant resolutions having been entered, the organizational meeting of the Board of Directors was adjourned until the next meeting to be called.

Signed: Venkat Konda

Dated as of March 31, 2019

Venkat Konda, Ph.D.

Secretary of the Meeting

Witness: Kimberly Louie

Kimberly Heller Louie

# EXHIBIT 10

[redacted]

Gmail

**Venkat Konda <venkat@kondatech.com>**

## Great News!

**Venkat Konda** <venkat@kondatech.com> Fri, Mar 20, 2009 at 11:49 AM
To: Dejan Markovic <dejan@ee.ucla.edu>
Cc: Venkat Konda <venkat@kondatech.com>

Dejan,

Great News!

Flavio told me verbally that the due diligence is complete! And they are going to fund Konda Technologies!

Since Cisco Angel Network funding is just starting out, the process is still evolving. [Also Cisco Angel Network is going to fund a few other startups].

It might take a couple of more weeks to get the paperwork and the other logistics in place.

[redacted]

I will get back in touch once we reach the paperwork stage.

Keep you posted.

Regards,

Venkat

---

From: dejan.ucla@gmail.com [mailto:dejan.ucla@gmail.com] On Behalf Of Dejan Markovic
Sent: Monday, February 16, 2009 6:16 PM
To: Venkat Konda
Cc: flavio
Subject: Re: Nice meeting you on WED 2/11 in Mountanview

Venkat,

[redacted]

[redacted]

[redacted]

# EXHIBIT 11

Gmail

**Venkat Konda <venkat@kondatech.com>**

## Checking in...

**Dejan Markovic** <dejan@ee.ucla.edu> Sun, Apr 26, 2009 at 8:46 PM
To: Venkat Konda <venkat@kondatech.com>

Hi Venkat,

I wanted to check in how are things progressing... I've heard last week that Flavio has been moved within Cisco (?), so not sure how/if this is going to affect you. Btw, what do you think of these guys: http://www.achronix.com/

Best regards,
Dejan

# EXHIBIT 12

Gmail

**Venkat Konda <venkat@kondatech.com>**

# RE: ITA info -- meeting / FPGA technology [Konda Technologies Business Presentation]

**Les Lackman** <LLACKMAN@support.ucla.edu> Thu, Oct 8, 2009 at 9:18 AM
To: Venkat Konda <venkat@kondatech.com>, whong@ita.ucla.edu
Cc: Dejan Markovic <dejan@ee.ucla.edu>

It is a go..Les

Les Lackman , PhD
Director Industrial Relations
Deputy Director ITA & Adjunct Professor
Henry Samueli School of Engineering and Applied Science
7268-B Boelter Hall
Office 310-794-5444
Fax 310- 825-3966

---

**From:** Venkat Konda [mailto:venkat@kondatech.com]
**Sent:** Wednesday, October 07, 2009 6:54 PM
**To:** Les Lackman; whong@ita.ucla.edu
**Cc:** 'Dejan Markovic'; 'Venkat Konda'
**Subject:** RE: ITA info -- meeting / FPGA technology [Konda Technologies Business Presentation]

[redacted]

---

**From:** Venkat Konda [mailto:venkat@kondatech.com]
**Sent:** Wednesday, October 07, 2009 6:52 PM
**To:** 'LLACKMAN@support.ucla.edu'; 'whong@ita.ucla.edu'
**Cc:** 'Dejan Markovic'; 'Venkat Konda'
**Subject:** RE: ITA info -- meeting / FPGA technology [Konda Technologies Business Presentation]

Hi Les, Winn:

It is my pleasure to get an opportunity to present Konda Technologies Business Presentation to ITA @ UCLA on the recommendation of Dejan.

Please find the attached presentation.

We have a tremendous opportunity to bring a revolutionary interconnect technology to commercialization with wide target applications. The primary focus currently being FPGA device.

With the other opportunities being ASIC Placement and routing Tools, Hardware emulations systems, MP-SoC interconnects etc.

I strongly believe this is multi-billion dollar opportunity.

Please let me know for further questions.

Best Regards,

Venkat

---

Venkat Konda, Founder/CEO
Konda Technologies, Inc

6278 Grand Oak Way, San Jose, CA 95135
Email: venkat@kondatech.com
Ph: 408-238-2478 Cell: 408-472-3273

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From: **Winnhong** <winnhong@yahoo.com>
Date: Wed, Oct 7, 2009 at 1:22 PM
Subject: Re: ITA info -- meeting / FPGA technology
To: Dejan Markovic <dejan@ee.ucla.edu>
Cc: "whong@ita.ucla.edu" <whong@ita.ucla.edu>, Les Lackman <LLACKMAN@support.ucla.edu>, Venkat Konda <vkonda@gmail.com>, Dejan Markovic <dejan@ee.ucla.edu>

Hi Dejan

Pleasure meeting as well and thanks for the info. 4:15 is fine for me, but I wil let Les confirm the time

Les, what say you?

Winn Hong
Sr Strategist
ITA at UCLA

On Oct 7, 2009, at 12:51 PM, Dejan Markovic <dejan@ee.ucla.edu> wrote:

Winn,

Thank you for the meeting today. I look forward to continuing discussion tomorrow with you and Les. I am also bringing Venkat into the loop -- we could have him on the phone tomorrow as well and/or have him visit on Friday. Meanwhile, we'll send some material about the technology.

I look forward to talking to you tomorrow. Let's make it 4:15pm to play it safe (my talk ends at 3:55pm and agenda for review meetings can shift). Shall we meet in my office?

Thanks,
Dejan

On Wed, Oct 7, 2009 at 9:55 AM, Winn Hong <whong@ita.ucla.edu> wrote:
Look forward to talking with you.

Winn

--- On Wed, 10/7/09, Dejan Markovic <dejan@ee.ucla.edu> wrote:

From: Dejan Markovic <dejan@ee.ucla.edu>
Subject: Re: ITA info -- meeting / FPGA technology
To: whong@ita.ucla.edu
Cc: "Les Lackman" <LLACKMAN@support.ucla.edu>
Date: Wednesday, October 7, 2009, 9:48 AM
Hi Winn,

Great -- let's talk at 11am. I will call you as soon as I am done
with my meeting. Thu anytime after 4pm works well for me (I finish
WIN review presentation at 3:55pm).

My cell is: 510-612-2998

Thanks,
Dejan

On Wed, Oct 7, 2009 at 9:33 AM, Winn Hong <whong@ita.ucla.edu> wrote:
Hi Dejan,

I'd be happy to meet with you at 11am to discuss. As for the meeting with Les, can we set up a meeting tomorrow, Thursday, after 3pm? Below is my cell number, feel free to call me.

Thanks,

Winn

626-641-9561 cell

--- On Wed, 10/7/09, Dejan Markovic <dejan@ee.ucla.edu> wrote:

From: Dejan Markovic <dejan@ee.ucla.edu>
Subject: Re: ITA info -- meeting / FPGA technology
To: "Les Lackman" <LLACKMAN@support.ucla.edu>
Cc: whong@ita.ucla.edu
Date: Wednesday, October 7, 2009, 9:15 AM
Les,

This is significantly different from Prof. He's work -- we are talking about 10x better than Xilinx and Altera. It's a patented idea that we are building around, Xilinx and Altera acknowledged it, CISCO too, and are trying to get Venkat out of their claws (he has been running on his own savings for over 3 years and is running out) -- we need to act promptly (matter of days). He is willing to come for a visit on Friday if you have time.

This is more than 5x better than current startups and has many more benefits (I can discuss details). It's a $4B market. DARPA is in to make a program around this idea, but it will take up to 1 year and that's the time where we need Angel fund to get Venkat paid. My students are getting geared to do chip design for Dec 1 tapeout, so we need to start pretty quickly.

Winn, can we talk between 11am and noon today? Then we can follow up with Les and Dean on Friday if we can get everyone on the calendar.

Thanks,
Dejan

On Wed, Oct 7, 2009 at 8:55 AM, Les Lackman <LLACKMAN@support.ucla.edu>
wrote:
Hi Dejan ; We are already discussing this
area with
Prof He....I am tied
up the next two day, but you can work with
Winn Hong
of the ITA to get
your idea into the hopper...Les

Les Lackman , PhD
Director Industrial Relations
Deputy Director ITA & Adjunct Professor
Henry Samueli School of Engineering and
Applied
Science
7268-B Boelter Hall
Office 310-794-5444
Fax 310- 825-3966

-----Original Message-----
From: dejan.ucla@gmail.com
[mailto:dejan.ucla@gmail.com]
On Behalf Of
Dejan Markovic
Sent: Wednesday, October 07, 2009 12:47 AM
To: Les Lackman
Cc: Dejan Markovic
Subject: ITA info -- meeting / FPGA
technology

Dear Les,

This is Dejan Markovic from EE Dept. I just
talked
to Dean Dhir today
and he suggested I get in touch with you
about an idea
I'd like to
push forward. Would you be available for a
phone
call or meeting
tomorrow? The best time for me would be
between 11am
and noon.

Best regards,
Dejan

Dejan Markovic
Assistant Professor, UCLA EE Dept.
56-147E Eng-IV Bldg, 420 Westwood Plz.
Los Angeles, CA 90095-1594
Tel: (310) 825-8656
Fax: (310) 206-8495
Email: dejan@ee.ucla.edu
URL: www.ee.ucla.edu/~dejan


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# EXHIBIT 14

**Proprietary**
*Regular-Geometry Micro-Cells and Design Tools for Butterfly FPGA*
Proposal Number: D102-0003-0305, Topic Number: SB102-003 (DARPA)

## 1. Identification and Significance of the Problem or Opportunity

**1.1 Objective:** In this project, we plan to prepare a Phase I feasibility study of integrated circuit micro-cells based on regular geometry for use in our proprietary **hierarchical FPGA interconnect architecture**. The objective of the overall 3-phase FPGA project is to substantially reduce energy and cost of low-volume digital signal processing by using hierarchically routed interconnect, **regular-geometry micro-cells**, and associated tool-flow for routing and hardware mapping. Figure 1 illustrates our overall vision for the project. While the FPGA architecture and associated tool-flow for design and algorithm mapping reduces cost in design time and chip metrics (the focus of Phases II and III), enforcing regular layout geometries at the cell level provides additional reduction in the manufacturing cost, particularly in advanced technology nodes such as 32nm and below. This proposal will thus evaluate the design of regular layout cells for FPGA design and compare their circuit and cost metrics to standard-cell based CMOS design. Our team is formed from an industrial innovator (Dr. Venkat Konda) who has strong patent portfolio in routing networks (Phase II work), and academic leaders in the areas of regular geometry circuit design (Prof. Puneet Gupta), and energy-efficient architecture design and associated tool-flows (Prof. Dejan Markovic). Our objective is to develop **low-cost digital signal processing hardware and tool-flows** for emerging markets such as wireless and sensor applications where cost and power consumption are key concerns.

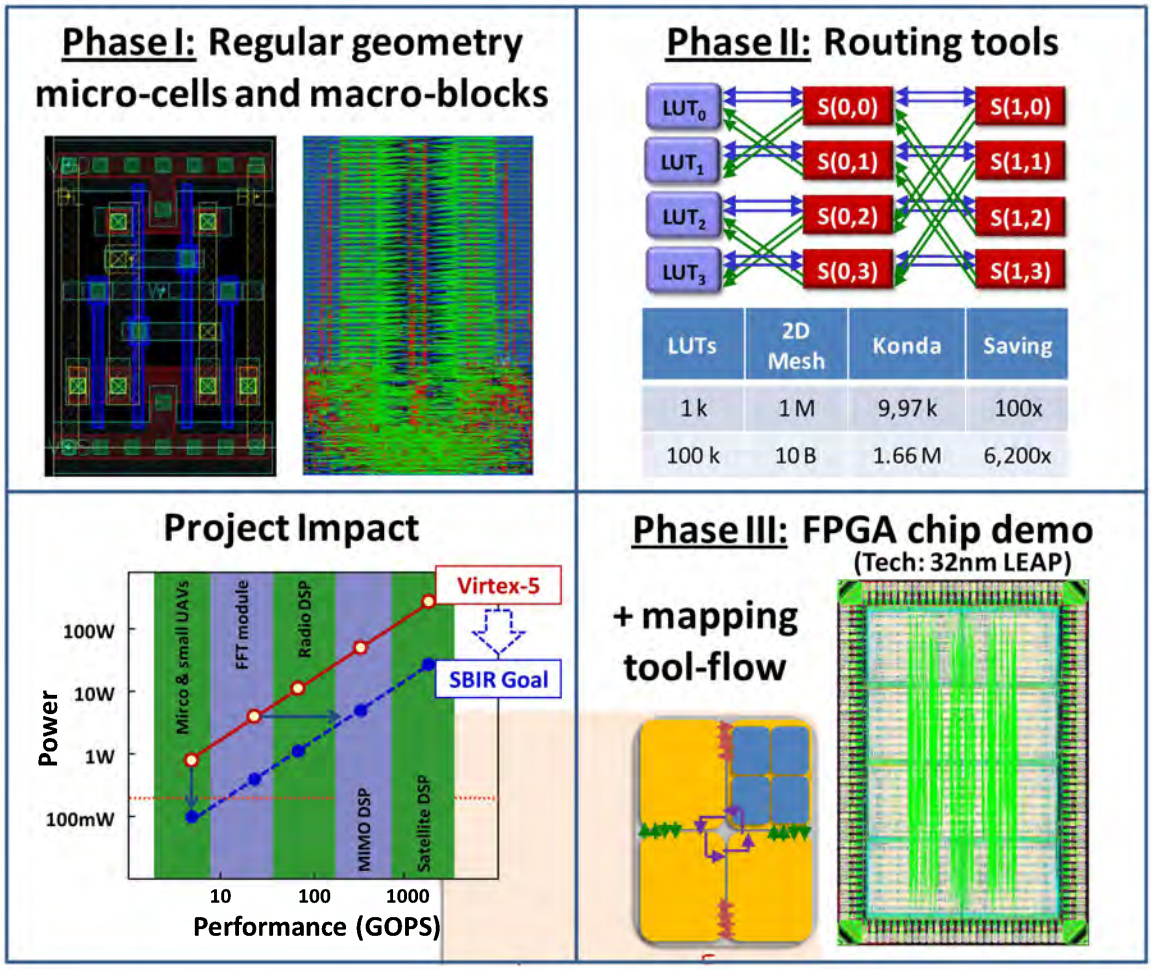


**Figure 1:** Regular-fabric micro-cells and blocks (output of Phase I) will be used to route Konda's hierarchical interconnect architecture (output of Phase II) and further integrated on a demo FPGA chip with supporting mapping tool-flow (output of Phase III) to demonstrate significant improvements in chip size, performance, power, and also manufacturing cost.

**1.2 Problem Addressed:** With increasing cost of semiconductor design and manufacturing, enforcing regularity at all layers from device technology to hardware architecture is essential for future low-power and low-cost digital signal processing hardware. At the architecture level, FPGA-like regularity is becoming an attractive solution particularly for low-volume applications, but the adoption of FPGAs will be greatly challenged with their excess power, area, and performance due to the massive FPGA interconnect. The complexity of the FPGA interconnect is a quadratic function, $O(N^2)$, of the number of processing elements, N. To mitigate the interconnect challenge, we will make use of hierarchically routed and proprietary Konda interconnect architecture which has greatly reduced complexity, $O(N \cdot \log_2 N)$, which results in improved area, power, and performance of FPGA chips. Additionally, we must face unique challenges of scaled technology and enforce regularity in the layout cells (micro-cells). With the slow development of Extreme Ultra Violet (EUV) lithography, double patterning technology (DPT) appears as the most viable lithography solution for 32nm and later technology nodes [1]. DPT allows for more compact and better-yielding layout using mask decomposition to effectively increase pitch size. To find best DPT decompositions as applicable to FPGA micro-cells and building blocks, we propose to investigate micro-cell routing algorithms and characterize the cells in energy-area-performance space as compared to their standard-cell based CMOS counterparts.

**1.3 Proposed Solution:** Our approach will consist of:

(a) Research the state-of-the-art regular layout geometries and routing algorithms for micro-cells,
(b) Innovate and provide unique solutions to overcome challenges at the cell layout, circuit, and architecture levels,
(c) Develop modeling and simulation framework that will guide the final selection of regular-geometry micro-cells to be used in FPGA macro-blocks such as lookup tables (LUTs), DSP slices, block RAM (BRAM) modules, switch matrix (SM) elements that include switch boxes (SBs) and configuration memory, and
(d) Perform **energy, area, performance, yield, and variability evaluation** of the propose micro-cell and macro-block structures for use in hierarchical FPGA interconnect architecture.

As a quantitative measure of our Phase I study, we plan to provide an extensive list of circuit metrics as listed in Table 1. The metrics include area, energy, performance, variability, and yield estimates for standard-cell and proposed regular-geometry cells (both at the micro and macro levels). The outcome of Phase I will be to populate Table 1 with quantitative measures of functional-block metrics, and to provide associated solutions for layout cells. The layout cells from Phase I will be subsequently used in hierarchical FPGA interconnect architecture (Phase II), FPGA chip and hardware mapping tool-flow (Phase III) to provide over 10x improvement in power compared to the state-of-the-art FPGAs.

**Table I:** Feasibility study of quantitative figures of merit of layout cells for FPGA application.

| Metric / Functional Block | Energy (fJ) | | Delay (ps) | | Variability (%) | | Yield (%) | |
|---|---|---|---|---|---|---|---|---|
| | Std-cell | Regular geometry | Std-cell | Regular geometry | Std-cell | Regular geometry | Std-cell | Regular geometry |
| NAND gate | | | | | | | | |
| Flip-flop | | | | | | | | |
| AOI gate | | | | | | | | |
| Full adder | | | | | | | | |
| 4-input LUT | | | | | | | | |
| DSP slice | | | | | | | | |
| Switch box | | | | | | | | |
| Switch matrix | | | | | | | | |

**1.4 Proposal Strength:** The main strength of the proposed work is the multi-disciplinary approach that spans technology, circuits, architectures, and algorithms for exploiting regularity multiple hierarchical layers in the design of digital signal processing hardware. The combined effort in the aforementioned areas will lead to the development of low-cost FPGA platform based on regular-geometry layout cells, hierarchically routed interconnect architecture, and tool-flow for area-efficient hardware mapping of digital signal processing algorithms. Our strength in all aspects from layout to algorithms will allow for (a) layout cell development, (b) accurate development of device and circuit specifications, (c) allow for extensive analysis to predict yield, power consumption, chip area, and performance, (d) provide full hardware/software demonstration at the end of the 3-phase program. Furthermore, our team has extensive experience in energy-efficient integrated circuits and architectures, CAD algorithms and layout cells, as well as network architectures and supporting routing algorithms.

**1.5 Market Opportunity:** We see a great market potential in broad area of digital signal processing hardware where the cost and power consumption are key challenges. Our final goal is to develop a simple and low-cost FPGA hardware/software technology based on regular layout cells, regular hierarchical interconnect architecture, and tools for block routing and hardware mapping. The potential markets include both commercial and defense segments. With greatly reduced power consumption and cost, the technology will particularly impact energy-starved applications such as embedded electronics and distributed sensors. The technology will also provide a solution to rapid prototyping and emulation for a variety of communications and imaging applications. To reduce design cost and ensure **scalability**, our approach will deliver **hierarchical methodology** from micro-cell layout to final chip architecture and supporting tool-flows.

**1.6 Company Profile:** Konda Technologies, Inc. is a startup company based in San Jose, CA. The company was founded in 2007 to develop & commercialize interconnect IP applicable for various products including FPGA routing interconnect, System-on-Chip interconnects and warehouse-scale datacenter switch networks. Our main customer today is Tier Logic Inc, a 3D-FPGA startup. The company has been engaged with vendors such as Xilinx Corporation, Altera Corporation and Cisco Systems.

## 2. Phase I Technical Objectives

**2.1 Objective 1: Development of reusable infrastructure of regularity evaluation at cell-level**
We will develop a tool infrastructure to allow for evaluation and exploration of regular layout styles. This would include fast estimation-based methods as well as layout generation and simulation based methods.

**2.2 Objective 2: Analysis of regularity tradeoffs at different layers and identification of layout styles suitable for the FPGA architecture**
Using the regularity evaluation framework developed above, we will identify the optimal choice of regular layout styles on front-end layers (poly, active, M1, M2, contact). This will be applied to varying levels of design complexity ranging from standard cells to entire FPGA functional macros.

**2.3 Objective 3: Develop a comprehensive plan for Phase II**
The outcome of Phase I will be a comprehensive study of micro-cells and macro-blocks that will be used in Phase II to implement hierarchical interconnect architecture. The objective is to significantly improve energy, area, and performance of the FPGA hardware. The output of Phase I will be guided by the metrics outlined in Table 1. Phase I solutions will be developed with tight interaction between architecture, circuit, and process parameters to ensure globally optimal solutions. We will propose an IP library and associated tools to reduce design cost and facilitate commercial adoption of our technology.

# 3. Phase I Work Plan

## 3.1 Introduction and Prior Art

Generally, regularity makes patterning easier. Inserting dummy features to ensure uniform density or to "isolate" standard cells from surroundings has been commonly followed approach. For more regularity, set of layout constraints or restrictive design rules [2], can be enforced to guarantee a lithography-friendly regular layout. As an example, a unidirectional fixed-pitch poly layer is enforced in Intel's 45nm process. Because of the success of such gridded design rules in enhancing printability and reducing variations [4], such rules might be adopted to pattern other patterning layers such as metal and contacts/vias. This principle of restricting the layout is pushed to the extreme in [5] where layout is constructed out of pre-characterized regular fabrics (as opposed to design rules). A regular layout approach can be excessively conservative especially for layouts where patterning imperfections would otherwise be tolerable [2]. Nevertheless, increasing degree of regularity is expected to make patterning even feasible in the near term.

Another important point is that regularity need not imply 1D gratings. The basic "template" for regularity could be something else while still ensuring good, low-cost printability (e.g., see [6]). The template printability can be optimized, for example, using source-mask optimization (SMO) or using character projection in maskless E-beam direct-write. Part of our work will also investigate if regularity other than gratings can be useful.

## 3.2 Our Approach

Our approach within this proposal, and in line with the SBIR call, is to examine routing tools for regular-geometry layout cells. The goal in Phase I will be to develop routing tools and layout cells for FPGA building blocks. The layout cells will vary in granularity from simple logic gates to complex blocks such as look-up tables, logic slices, switch boxes, and memory components. The regular cells will be characterized for density (area), yield, energy, and performance and compared to regular standard-cell based approach. The regular cells will be used in Phase II for interconnect architecture routing. The cells and routing tools will be made available as IP to facilitate rapid commercialization.

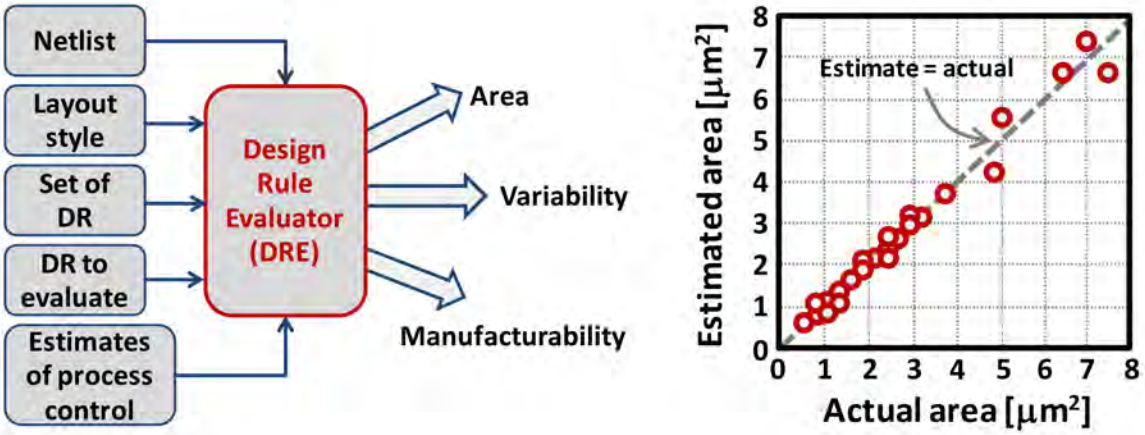


**Figure 2:** Regularity evaluation framework (left), DRE results on 45nm Nangate open-cell library (right).

Regularity is a continuum of possibilities and it has significant impact on area, delay, power as well as expected manufacturing yield. It therefore is very important to co-optimize design rules, regular layout styles as well as cell architectures. We have developed a Design Rule Evaluator (DRE) framework (see **Error! Reference source not found.**) which predicts the impact of layout style and design rule changes on important circuit metrics for standard cells as well as small custom blocks. DRE can run through a 100+ cell 45nm cell library in a few minutes with less than 2% average estimation error (see **Error! Reference source not found.**) making it perfectly suited for design space exploration of layout

regularity, design rules and design styles. As an example preliminary study using DRE, consider increasing regularity on the polysilicon layer (see Figure **1**). We compare the cases of unrestricted 2D layout to 1D layout with arbitrary pitches and restricted 1D fixed pitch (i.e., grating-like) layout styles for a 45nm sequential benchmark design.

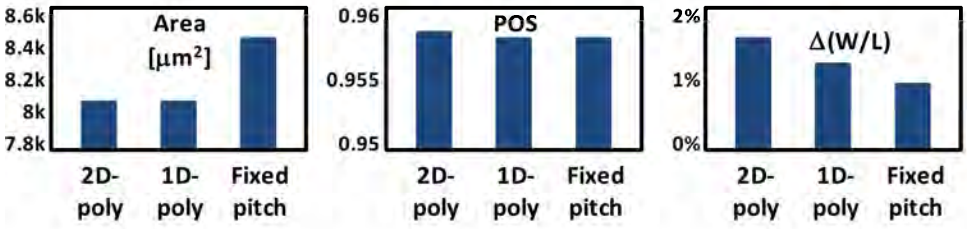


**Figure 1:** Comparing layout restrictions for a benchmark design on polysilicon layer in terms of area, catastrophic yield (POS or probability of survival) and current variability (change in W/L).

We will extend DRE to full-chip (FPGA) evaluation including local, intermediate and global metal/via layers. This will allow us to arrive at a principled choice of regularity and a layout style to enforce it for the FPGA interconnect fabric. The first phase will use DRE coupled with some layout design and simulation to identify optimal choice of regularity for basic building blocks of the FPGA.

### 3.3 Task 1: Identification of candidate layout styles for regularity evaluations

For different candidate patterning technologies at 32nm, 22nm, 16nm nodes, we will identify what forms of regularity and on what layers will help the most. This set may be a large one, especially, for the 22nm and 16nm nodes where lithographic patterning choices are still unclear (double patterning, self-aligned double patterning, e-beam direct write, interference-assisted lithography, etc).

### 3.4 Task 2: DRE-based exploration of regularity tradeoffs in FPGA building blocks

We will extend DRE framework to allow us to evaluate delay-power-yield-area-variability tradeoffs for regularity on polysilicon, contact, M1, M2 layers. The result will be a principled narrowing down of layout style choices with clear understanding of the tradeoffs.

### 3.5 Task 3: Generation of layout, simulation, and comparison

Using the optimized design rules and regular layout stules derived above, we will draw layouts of FPGA micro-cells. These will then be analyzed for delay/power/variability/manufacturability using explicit lithography simulation using a projected 32nm lithography setup coupled with non-rectangular transistor models. This will allow us for a close-to-silicon comparison of different layout styles (e.g., irregular, 2D standard cells vs. regular layouts).

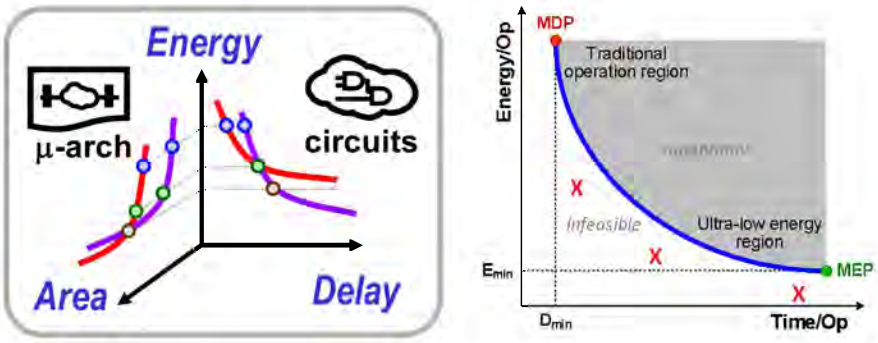


**Figure 4:** (left) Area-Energy-Delay space for comparing multiple circuit and micro-architectural options. (right) Energy-delay tradeoff in CMOS (solid line) indicating minimum-delay (MDP) and minimum-energy (MEP) points. Regular-geometry based designs marked in (X) are expected to provide better energy-delay tradeoff than standard-cell based CMOS.

We will use our methodology for area-energy-delay optimization of CMOS circuits and architectures [7, 8]. The methodology is based on pareto curve analysis for various circuit and architecture realizations as indicated in Fig. 4(a). Each tradeoff curve is a result of optimization program that minimizes energy subject to a delay constraint for circuits. The optimal tradeoff for the circuit-level energy and delay is illustrated in solid line in Fig. 4(b) by tuning gate size, supply, and threshold voltage. The line is bounded by minimum-delay (MDP) and minimum-energy (MEP) points. All points above the line are suboptimal, all points below the line are infeasible.

The goal of regular-geometry explorations is to achieve better energy-delay tradeoff than regular standard-cell based CMOS approach as indicated by the (X) markers in Fig. 4(b). Points below MEP are the most desirable and it is expected that the micro-cell development will go mainly in this direction. Points above MEP but still below E-D plot of CMOS are also very desirable. We will use compact circuit models to formulate optimization problems, perform simulations and to populate the metrics in Table 1. This includes various FPGA datapath and storage functions.

### 3.6 Task 4: A comprehensive Phase II development plan

Towards the end of Phase I, as outlined in Table 2, and based on the outcome of Phase I, we will create a comprehensive Phase II development plan. We aim to integrate hierarchical interconnect architecture in Phase II based on the micro-cells and macro-blocks from Phase I. Details of the proprietary hierarchical interconnect architecture will be available in our proposal at the conclusion of Phase I.

### 3.7 Timeline

**Table II:** Phase I project schedule

| Month | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| Task 1 | | | | | | |
| Task 2 | | | | | | |
| Task 3 | | | | | | |
| Task 4 | | | | | | |

### 3.8 Task Work Breakdown

**Table III:** Estimated task hours for key Personnel

| Task/Person | V. Konda (PI, Konda Tech) | Scientist (Konda Tech) | D. Markovic (UCLA) | P. Gupta (UCLA) |
|---|---|---|---|---|
| Task 1 | 100 | 140 | 20 | 80 |
| Task 2 | 80 | 100 | 30 | 70 |
| Task 3 | 60 | 60 | 50 | 30 |
| Task 4 | 40 | 40 | 100 | 20 |
| **TOTAL** | **280** | **340** | **200** | **200** |

## 4. Related Work

We have worked extensively on design-patterning interactions. We have developed methods for evaluation of regular layout styles through layout generation and simulation (DAC 2004) as well as through estimation and modeling (ICCAD 2009). Prof. Gupta has worked extensively on electrical modeling (SPIE'06, SPIE JM3'10, VLSID'10, ASPDAC'08, etc) and mitigation (TCAD'07, SPIE JM3'09, etc) of lithographic imperfections. Prof. Markovic has a strong track record in energy-efficient ASICs for digital signal processing.

**Relevant Business Relationships:** Since its founding in 2007, the company has attracted strong interest from a variety of companies. The company has been engaged with vendors such as Xilinx Corporation, Altera Corporation and Cisco Systems. Our main customer today is Tier Logic Inc, a 3D-FPGA startup.

**Related Work by Others:** Regular layouts have been under investigation to various extents in academia and industry for past few years. Commercial foundries enforce regularity to varying degrees using design rules (e.g., unidirectional, gridded poly is likely to be widely required at 32nm node). The origins of the approach lie in early work done by IBM on restricted design rules to be used for Alternating PSM patterning. Most cell libraries at 32nm node will use regular layouts, at least for the polysilicon layer. More regularity on other layers (contact, M1) has also been investigated in somewhat limited fashion by companies (e.g., PDBrix from PDF solutions and AreaTrim by Tela Innovations) but extensive tradeoff analyses between extent of regularity, area and yield is still an open problem.

## 5. Relationship with Future Research or Research and Development

### 5.1 Phase I Results

The goal of Phase I is to develop a tool infrastructure to allow for evaluation and exploration of regular layout styles. This would include fast estimation-based methods as well as layout generation and simulation based methods. Using the regularity evaluation framework developed above, we will identify the optimal choice of regular layout styles on front-end layers (poly, active, M1, M2, contact). Our approach in Phase I will also focus the demonstration of library IP and the use of software to reduce cost and facilitate rapid commercialization. We will also study preliminary routing strategies for regular interconnect architecture for Phase II.

### 5.2 Relationship to Phase II and its Objectives

The regularity layout cells will be extended to FPGA architecture. The FPGA devices have regularly placed LUTs (Look-up tables) in a 2D-plane on a silicon die. So far 2D-Mesh networks have been used in FPGA devices due to their regular structure, i.e., both interconnect distribution-wise as well as the horizontal and vertical routing tracks layout-wise. However the switch complexity of the 2D-Mesh based FPGA interconnect is a quadratic function, $O(N^2)$, of the number of processing elements, N. Even though Benes/Butterfly Fat Tree networks with switch complexity of $O(N \cdot \log_2 N)$, which results in improved area, power, and performance of FPGA chips, they are not implementable due to the lack of known regular VLSI layouts, till today. Konda Technologies inventions with regular VLSI layouts for Benes/BFT based hierarchical networks are seminal and subsumes all the other known network topologies such as Clos networks, hypercube networks, cube-connected cycles and pyramid networks, which makes these networks implementable in a FPGA devices with regular structures both interconnect distribution-wise and layout-wise which is the key to exploit improved area, power, and performance of FPGA devices. The regularity of Konda hierarchical layout is also the key for its commercializability in System-on-Chip interconnect devices, FPIC devices as well.

## 6. Commercialization Strategy

We believe that our fundamental intellectual property would help us to commercialize out IP by technology and tools licensing. We have already been successful with our current engagement with Tier Logic to incorporate our interconnect IP into Teir Logic's 3D-FPGA devices.

### 6.1 General Commercial and Technology Landscape

In the regular layout cells space, there have several undertakings in both academia and industry. Commercial foundries also enforce regularity to varying degrees using design rules (for example, unidirectional, gridded poly is likely to be widely required at 32nm node). The origins of the approach lie in early work done by IBM on restricted design rules to be used for Alternating PSM patterning.

Most cell libraries at 32nm node will use regular layouts, at least for the polysilicon layer. More regularity on other layers (contact, M1) has also been investigated in somewhat limited fashion by companies (e.g., PDBrix from PDF solutions and AreaTrim by Tela Innovations) but extensive tradeoff analyses between extent of regularity, area and yield is still an open problem. Our advantage is system-wide visibility and consideration of regularity that starts from micro-cell level and goes up to our proprietary interconnect architecture.

### 6.2 Market Opportunity

Our initial market focus will be in electronics for portable applications where energy consumption is limited and where cost is a key concern such that scalability can be achieved. The approach described in this proposal is to create library cells for programmable integrated circuits in advanced technology nodes such as 32nm and beyond. We expect this technology to complement existing patent portfolio at Konda Technologies, Inc. in the area of network routing algorithms for a variety of markets.

Commercialization of the technology is foreseen to be developed with close consultation with large semiconductor companies such as Qualcomm, Broadcom, ST Microelectronics, Novelics, Xilinx, and Altera where strategic partnerships have already been established. In addition, we expect large interest from defense companies such as Boeing and Northrop Grumman. We will certainly take inputs from both the civil and DoD companies to best tailor the technology platform to each market segment.

We foresee the opportunity to use the technology in application-specific integrated circuit (ASIC) markets as well as FPGA market. ASICs used in wireless devices are power-limited yet require large amounts of flexibility for multiple operation modes. FPGAs can provide the flexibility, but at a prohibitive cost in power and area. Our technology provides solution to both of these problems as we offer flexible yet low power FPGA technology. Our micro-cells and routing tools can be used as IP by communication and FPGA companies alike. In 2010, FPGA market is expected at $4B, with projections of steady growth up to $6B in 2015 [9]. The ASIC market, $18B in 2009, is projected to exceed $22B by 2010 [10].

We plan to expand our patent portfolio and issue soft IP (micro-cells and routing algorithms) on a non-exclusive license basis to ASIC and FPGA companies such as Qualcomm, Broadcom, Samsung, Xilinx, Altera, and Cisco.

## 7. Key Personnel

### 7.1 Company Background

Based on a breakthrough and patent-pending layout for Benes/Butterfly Fat Tree network using horizontal and vertical tracks and with commercial potential for wide target applications such as FPGA devices, FPIC devices, logic emulation systems, Konda Technologies was founded in 2007 to commercialize the intellectual property into these markets. Our initial focus has been to commercialize interconnect IP into FPGA devices.

### 7.2 Dr. Venkat Konda, Principal Investigator & CEO, Konda Technologies, Inc.

Venkat Konda is an inventor, experienced entrepreneur and the CEO of Konda Technologies which he founded in 2007 based on a breakthrough layout using only horizontal and vertical tracks for Benes/BFT hierarchical networks, seminal rearrangeably and strictly non-blocking multicast routing algorithms with an architecture optimum with switch cost, power and performance. Venkat is currently in the process of commercializing the IP in FPGA interconnects, System-on-Chip interconnects and warehouse-scale datacenter switches. Prior to it, Venkat invented seminal algorithms for rearrangeably and strictly non-blocking multicast routing algorithms for Clos Networks and founded a startup Teak Networks, to commercialize into packet switch fabrics which are also applicable to design cheaper optical cross connects. Venkat received PhD degree in Computer Science & Engg

from University of Lousiville, KY in 1992, and M.S in Electrical Engineering from Indian Institute of Technology, Kharagpur in 1988. Key patents/applications include:

[1] Venkat Konda, "Fully connected generalized multi-stage networks", USPTO App# 12/530,207.
[2] Venkat Konda, "Fully connected generalized Butterfly Fat Tree networks", USPTO App# 12/601,273.
[3] Venkat Konda, "VLSI Layouts of Fully connected generalized networks", USPTO App# 12/601,275.
[4] Venkat Konda, "Rearrangeably nonblocking multicast multi-stage networks **",** US Patent # 6,885,669.
[5] Venkat Konda, "Strictly nonblocking multicast multi-stage networks ", US Patent # 6,868,084.

**7.2 Prof. Dejan Markovic, UCLA, Electrical Engineering (Sub-contractor)**

Dejan Markovic is an Assistant Professor of Electrical Engineering at UCLA. He completed the Ph.D. degree in 2006 at the University of California, Berkeley. In recognition of the impact of his Ph.D. work, he was awarded 2007 David J. Sakrison Memorial Prize at UC Berkeley. His current research is focused on integrated circuits for emerging radio and healthcare systems, design with post-CMOS devices, optimization methods and CAD flows. He will be contributing to the design and circuit demonstration tasks in this project. His responsibilities will include layout cell characterization, design and optimization of FPGA building blocks. Some relevant publications include:

[1] D. Marković, C. C. Wang, L. Alarcon, T.-T. Liu, and J. M. Rabaey, "Ultralow-Power Design in Near-Threshold Region," Proceedings of the IEEE, vol. 98, no. 2, pp. 237-252, Feb. 2010.
[2] R. Nanda, C.-H. Yang, and D. Marković, "DSP Architecture Optimization in Matlab/Simulink Environment," in Proc. Int. Symp. on VLSI Circuits (VLSI'08), June 2008, pp. 192-193.
[3] D. Marković, B. Nikolić, and R.W. Brodersen, "Power and Area Minimization for Multidimensional Signal Processing," IEEE J. Solid-State Circuits, vol. 42, no. 4, pp. 922-934, April 2007.
[4] D. Marković, R.W. Brodersen, and B. Nikolić, "A 70GOPS 34mW Multi-Carrier MIMO Chip in 3.5mm2," in Proc. Int. Symp. on VLSI Circuits (VLSI'06), June 2006, pp. 196-197.
[5] D. Marković, V. Stojanović, B. Nikolić, M.A. Horowitz, and R.W. Brodersen, "Methods for True Energy-Performance Optimization," IEEE J. Solid-State Circuits, vol. 39, no. 8, pp. 1282-1293, Aug. 2004.

**7.3 Prof. Puneet Gupta, UCLA, Electrical Engineering (Sub-contractor)**

Puneet Gupta (http://nanocad.ee.ucla.edu) is currently an Assistant Professor of Electrical Engineering at UCLA. He received the B.Tech degree in Electrical Engineering from Indian Institute of Technology, Delhi in 2000 and Ph.D. in 2007 from University of California, San Diego. He co-founded Blaze DFM Inc. (acquired by Tela Inc.) in 2004 and served as its product architect till 2007. He is a recipient of NSF CAREER award, ACM/SIGDA Outstanding New Faculty Award, IBM Ph.D. fellowship and European Design Automation Association Outstanding Dissertation Award. Dr. Gupta's research has focused on building high-value bridges between physical design and semiconductor manufacturing for lowered cost, increased yield and improved predictability of integrated circuits. He will be contributing to the design and circuit demonstration tasks in this project. His responsibilities will include optimization of regular layout styles, layout generation and characterization. Key relevant publications include:

[1] P. Gupta, A. B. Kahng, D. Sylvester, and J. Yang, ``Toward a Methodology for Manufacturability Driven Design Rule Exploration," in Proc. DAC, June 2004.
[2] R. S. Ghaida and P. Gupta, ``A Framework for Early and Systematic Evaluation of Design Rules," in IEEE/ACM ICCAD, November 2009.
[3] P. Gupta, A. B. Kahng, P. Sharma, and D. Sylvester, ``Gate-Length Biasing for Runtime Leakage Control," IEEE Transactions on CAD, June 2006.
[4] T.-B. Chan, R. S. Ghaida, and P. Gupta, ``Electrical Modeling of Lithographic Imperfections," in Proc. IEEE/ACM VLSI Design Conference, 2010.
[5] R. S. Ghaida and P. Gupta, ``Within-Layer Overlay Impact for Design in Metal Double Patterning," to appear in IEEE Transactions on Semiconductor Manufacturing, 2010.

## 8. Facilities/Equipment

During Phase I of this project, no special facilities or equipment will be required to complete the proposed plan. Konda Technologies will only require the services of Profs. Gupta and Markovic from

Electrical Engineering at UCLA to provide design, modeling, and simulation capabilities. No equipment purchase will be necessary.

**8.1 Government Equipment and Facilities**

No government facilities or equipment will be used during this project.

## 9. Subcontractors/Consultants

**Subcontractors: Profs. Dejan Markovic and Puneet Gupta, UCLA Electrical Engineering**

UNIVERSITY OF CALIFORNIA, LOS ANGELES — UCLA

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Henry Samueli School of Engineering and Applied Science
Electrical Engineering Department
Engineering IV Building, 420 Westwood Plaza
Los Angeles, California 90095-1594

June 22, 2010

**To:** Dr. Venkat Konda
Konda Technologies, Inc.
6278 Grand Oak Way
San Jose, CA 95135

Dear Dr. Konda:

We would like to express our interest in working with Konda Technologies, Inc. in support of the DoD SBIR project solicitation topic SB102-003 "Design Tools for Highly Regular Circuit Geometries." Our groups at UCLA would be willing to provide collaboration in accordance with the following statement of work:

Phase I tasks:

1. Expoloration of candidate layout styles for regular-geometry circuit building blocks.
2. Design rule evaluator (DRE) based evaluation of selected regular layout styles.
3. Layout generation, simulation, and characterization of energy, area, delay, variation, and yield metrics.

UCLA Budget Phase I: $32,000

We understand that the start date will be mid-late 2010 and the total duration will be six months.

Sincerely,

Dejan Marković, Assistant Professor
UCLA Electrical Engineering Department
56-147E Eng-IV Bldg, 420 Westwood Plz
Los Angeles, CA 90095-1594
Tel: (310) 825-8656, Email: dejan@ee.ucla.edu
URL: http://www.ee.ucla.edu/~dejan

Puneet Gupta, Assistant Professor
UCLA Electrical Engineering Department
6730C Boelter Hall, 420 Westwood Plaza
Los Angeles, CA 90095-1594
Tel: (310) 825-1376, Email: puneet@ee.ucla.edu
URL: http://www.ee.ucla.edu/~puneet

## 10. Prior, Current, or Pending Support of Similar Proposals or Awards

None.

## 11. References

[1] G. E. Bailey, A. Tritchkov, J.-W. Park, L. Hong, V. Wiaux, E. Hendrickx, S. Verhaegen, P. Xie, and J. Versluijs, “Double pattern EDA solutions for 32nm HP and beyond,” In Proc. SPIE 6521, 2007.
[2] M. Lavin, F. Heng and G. Northrop, “Backend CAD flows for “restrictive design rules”, in Proc. IEEE/ACM Intl. Conf. on Computer Aided Design, pp. 739-746, 2004.
[3] R. S. Ghaida and P. Gupta, ``A Framework for Early and Systematic Evaluation of Design Rules," in IEEE/ACM ICCAD, November 2009.
[4] M. C. Smayling, H. Liu, and L. Cai, “Low k1 logic design using gridded design rules,” Proc. SPIE, p. 69250B, 2008.
[5] T. Jhaveri, V. Rovner, L. Liebmann, L. Pileggi, A. J.Strojwas, J.D. Hibbeler, “Co-optimization of circuits, layout and lithography for predictive technology scaling beyond gratings,”, IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 29, no. 4, pp. 509-527, 2010.
[6] R. S. Ghaida, G. Torres, and P. Gupta, ``Single-Mask Double-Patterning Lithography," in SPIE/BACUS Photomask Technology, September 2009.
[7] D. Marković, C. C. Wang, L. Alarcon, T.-T. Liu, and J. M. Rabaey, "Ultralow-Power Design in Near-Threshold Region," Proceedings of the IEEE, vol. 98, no. 2, pp. 237-252, Feb. 2010.
[8] D. Marković, V. Stojanović, B. Nikolić, M.A. Horowitz, and R.W. Brodersen, "Methods for True Energy-Performance Optimization," IEEE J. Solid-State Circuits, vol. 39, no. 8, pp. 1282-1293, Aug. 2004.
[9] Electronics Weekly, [Online] Available: http://www.electronicsweekly.com/Articles/2010/05/19/48677/fpga-market-soaring-to-4bn-in-2010-says-gavrielov.htm
[10] BCC Research, “The Global Market for ASICs,” Report Code: SMC067A, Published: June 2009 [Online] Available: http://www.bccresearch.com/report/SMC067A.html

# EXHIBIT 15

**Volume I**
**Technical and Management Proposal**

**Title:** Energy-Efficient Butterfly FPGA Hardware and Programming Tools

A proposal submitted to
**Dr. William Harrod, DARPA/TCTO**
in response to

| | |
|---|---|
| **DARPA-BAA 10-78:** | Omnipresent High Performance Computing (OHPC) |
| **Technical Area:** | Energy Efficient Computing |
| **Lead Organization:** | University of California, Los Angeles (UCLA)<br>Department of Electrical Engineering<br>Los Angeles, CA 90095-1594 |
| **Type of Business:** | Other Educational |
| **Team Members:** | Dejan Markovic (PI)<br>Venkat Konda (Consultant) |

**Technical Point of Contact:**

Dr. Dejan Markovic, PI
UCLA Associate Professor
Electrical Engineering Department
56-147D Engineering IV Building
420 Westwood Plaza
Los Angeles, CA 90095-1594

Tel: (310) 825-8656
Fax: (310) 206-8495
Email: dejan@ee.ucla.edu

**Administrative Point of Contact:**

Ms. Julia Zhu
UCLA Senior Grant Analyst
Office of Contract and Grant Administration
11000 Kinross Ave, Suite 102
Los Angeles, CA 90095-1406

Tel: (310) 794-0155
Fax: (310) 943-1658
Email: ocga5@research.ucla.edu

| | |
|---|---|
| **Total funds requested:** | **$2,374,111** |
| **Year 1:** | **$789,927** |
| **Year 2:** | **$792,100** |
| **Year 3:** | **$792,086** |

UCLA

**Date of proposal:** August 4, 2010

**UNIVERSITY OF CALIFORNIA, LOS ANGELES** **UCLA**

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OFFICE OF CONTRACT AND GRANT ADMINISTRATION
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LOS ANGELES, CALIFORNIA 90095-1406

PHONE: (310) 794-0102
FAX: (310) 794-0631

www.research.ucla.edu/ocga

August 5, 2010

DARPA/TCTO
ATTN: DARPA-BAA-10-78
3701 N. Fairfax Drive
Arlington, VA 22203-1714

The Regents of the University of California, Los Angeles, is pleased to submit the following proposal in response to solicitation DARPA-BAA-10-78.

Title: "Energy-Efficient Butterfly FPGA Hardware and Programming Tools."

Requested Period of Performance: September 15, 2010 – September 14, 2013

Amount Requested: $2,374,111

Principal Investigator: Dr. Dejan Markovic
Department of Electrical Engineering
dejan@ee.ucla.edu
310-825-8656

This application is being submitted in contemplation of an agreement containing mutually agreeable terms and conditions applicable to educational institutions conducting unclassified fundamental research.

Since UCLA is a public/State institution, open dissemination of research results and information, commitment to students, accessibility for research purposes, and legal integrity and consistency are part of the University's Principles/Policy. The University does not discriminate and impose restrictions on any individual as a result of their nationalities.

If an award is made, please be advised that if it is funded by budget category 6.3(Advanced Research) and is considered Non-fundamental research, we will not be able to accept the award due to publication restrictions.

Your favorable consideration of this proposal would be appreciated. Technical questions should be directed to Dr. Markovic. Administrative and contractual questions, should be directed to me at (310) 794-0155 or via email at jzhu@research.ucla.edu.

Sincerely,

Julia Zhu

Julia Zhu
Senior Grant Analyst

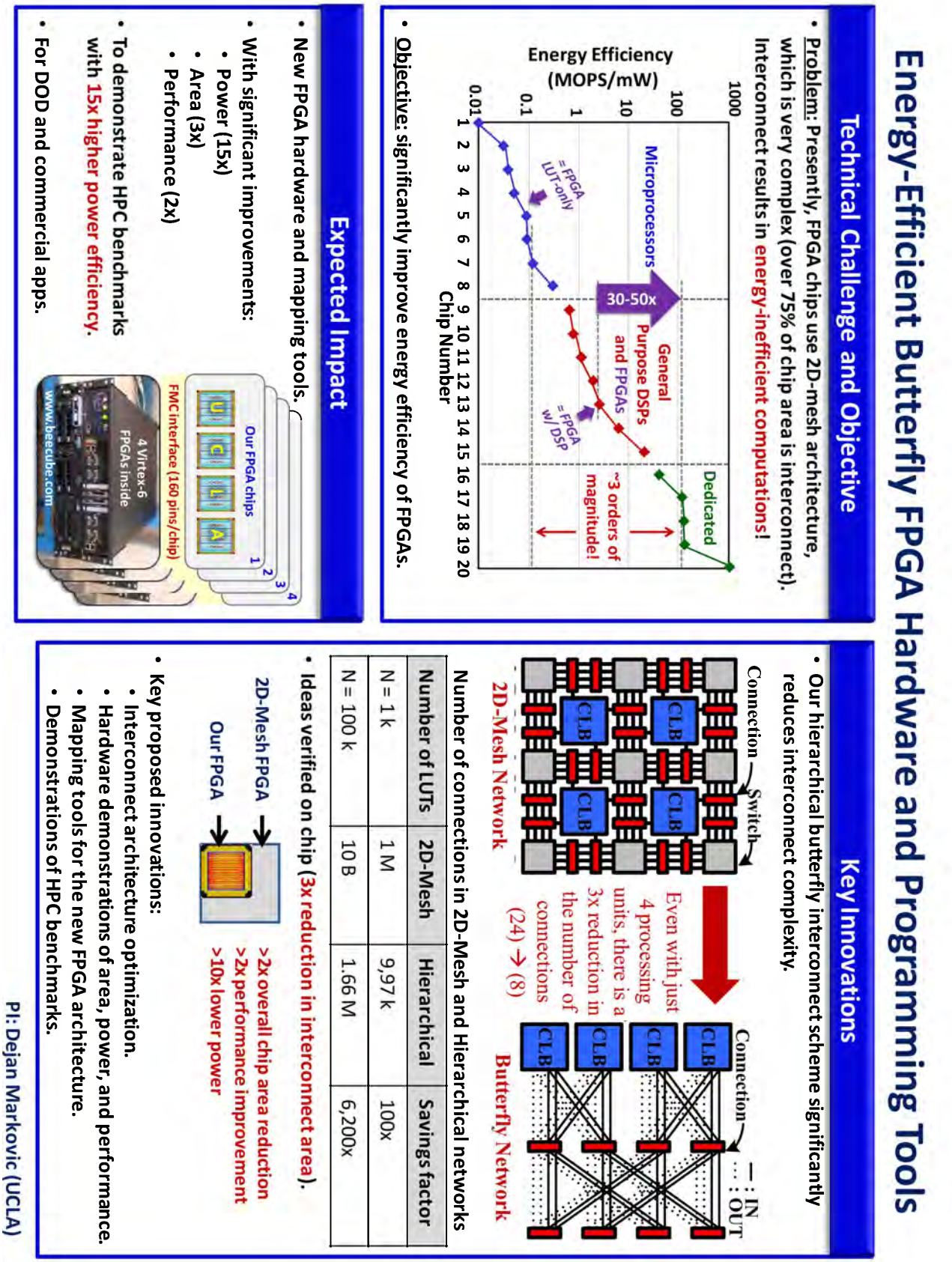
**Table of Contents**

**Executive Summary**

UCLA offers to perform research on a revolutionary new FPGA technology consisting of FPGA hardware and supporting mapping tools. We will design, fabricate, and test hierarchical FPGA interconnect network to demonstrate FPGA technology that is 15x more energy-efficient than existing FPGAs. The new interconnect architecture allows for significant reduction in the number of switch points, buffers, and wire length in comparison to standard 2D-mesh architecture used by existing FPGAs. The proposed technology is a radical departure from 2D-mesh design, which for N logic blocks has complexity $O(N^2)$, incomplete and heuristic routing. The proposed technology has only $O(N \cdot \log_2 N)$ complexity, complete and fully deterministic routing. The proposed technology has significant benefits: 15x lower power, 3x lower area, 2x higher performance compared to existing FPGA technology. The new FPGA technology will be used to demonstrate HPC benchmarks with a 15x higher power efficiency for DOD and commercial users. The PI has established interactions with industrial partners that will lead to the transition of ideas into the commercial space.

## Section II - Technical Details

### 2.1. PowerPoint Summary Chart



## 2.2. Innovative Claims for the Proposed Research

### Problem Description

Today's programmable FPGA devices are expensive in size, power, performance, scalability and flexibility. All of this is due to a fundamental problem in 2D-mesh interconnect architecture: it is large in size, has long latency, consumes lots of power, and is not scalable. Interconnect takes more than 75% of the FPGA chip area. Large number of inactive transistors also results in significant leakage power (about 50% of the total FPGA power). Due to inefficient interconnect architecture, there is a 30-50x energy-efficiency gap between FPGA and dedicated chips (Fig. 1).

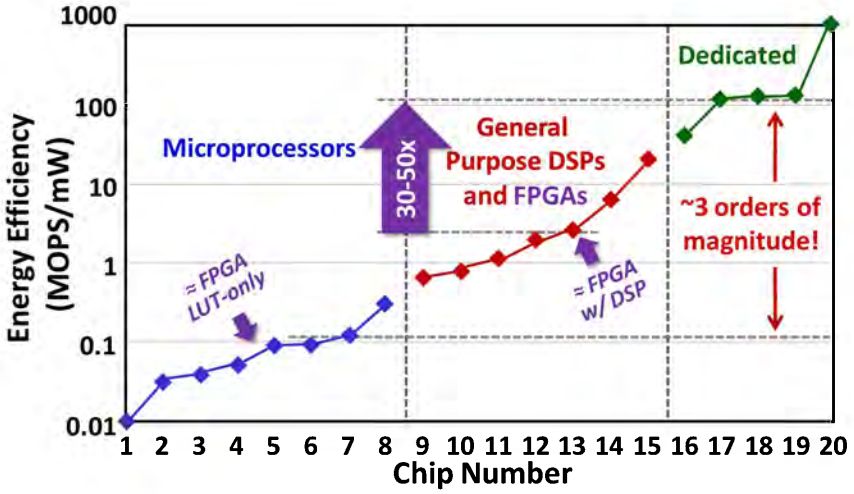



**Figure 1:** Energy efficiency for various computing architectures: microprocessors, general purpose DSPs, FPGAs, and dedicated chips. The study is based on chips from the ISSCC conference (normalized to the same technology). FPGAs with DSP cores are 30-50x less energy efficient than dedicated chips.

### Research Goals

We will integrate hierarchical interconnect network to demonstrate significant improvements in speed, power, and area as compared to existing FGPAs technology. The hierarchical interconnect architecture requires at least 3x smaller number of active network elements, switch points and drivers. This is illustrated in Fig. 2 for a very simple 2x2 example.

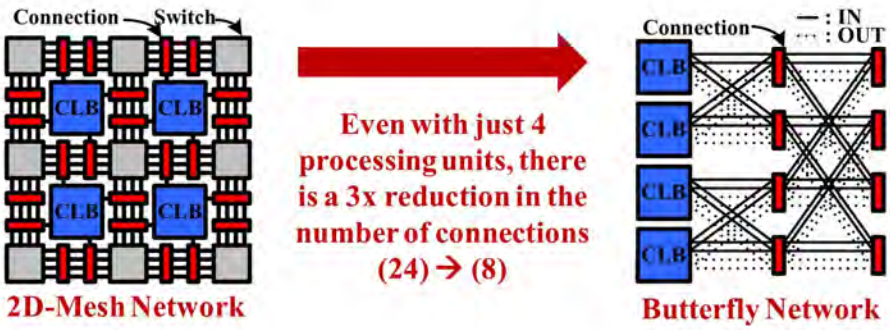



**Figure 2:** 2D-Mesh and Konda networks for a design consisting of 4 CLB blocks.

For larger number *N* of configurable logic elements, the benefits of hierarchical network will be even more pronounced (Table 1). Such large cost of the 2D-mesh architecture forces designers to employ heuristics to reduce the number of switch points, which results in insufficient connectivity. The hierarchical network provides complete and deterministic routing.

**Table 1:** Number of connections in 2D-Mesh and Konda networks.

| Number of LUTs | 2D-Mesh | Konda butterfly | Savings factor |
|---|---|---|---|
| 1 k | 1 M | 9.97 k | 100x |
| 100 k | 10 B | 1.66 M | 6,200x |

**Expected Impact**

The new FPGA platform will provide significant savings in power compared to today's FPGAs as shown in Fig. 3. Our FPGA technology, which includes hardware and supporting mapping tools, will provide an estimated 15x power reduction as compared to conventional FPGAs.

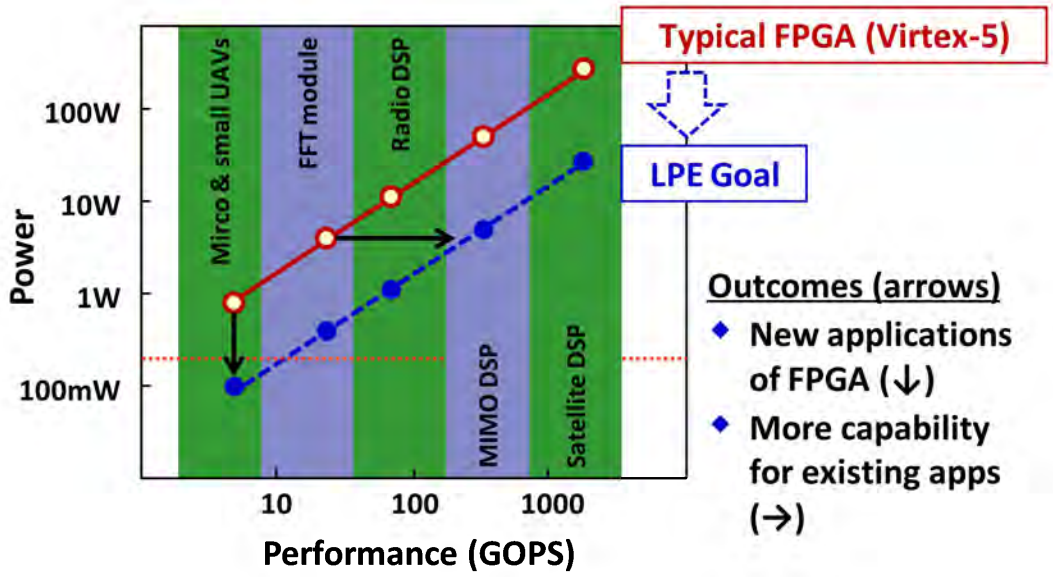



**Figure 3:** Power consumption for a range of applications. New FPGA will provide significant power reduction compared to typical Virtex-5 FPGA (normalized to the same technology).

We will provide new FPGA technology consisting of hardware and mapping tools. The hardware and mapping tools will provide significant impacts: 15x lower power, 3x lower area, 2x higher performance compared to existing FPGA technology. The new FPGA technology will be used to demonstrate HPC benchmarks with a 15x higher power efficiency for DOD and commercial users. Equivalently, our FPGA technology can provide >10x higher throughput for the same amount of power (as shown in Fig. 3). This technology will be of use for HPC applications and many other DOD applications which use FPGA technology.

### 2.3. Proposal Roadmap

**Main goals of the proposed research:** The main goal of the program is to develop energy-efficient programmable hardware and supporting software mapping tools. The hardware is based on hierarchical interconnect architecture that provides significant reduction in interconnect complexity as compared to today's FPGA hardware. With a combination of new interconnect architecture and supporting toolflow, we project over a 15x improvement in energy efficiency while also considerably reducing chip area and improving performance. The proposed work builds on patent-protected network architecture and successful chip demonstrations. The work proposed here focuses on the investigation of needed level of connectivity for large-sale designs, and supporting mapping tools to make the technology accessible to end users.

**Tangible benefits to end users:** Over a 15x improvement in energy-efficiency, considerable reduction in chip area (3-4x), and considerable improvement in performance (> 2x) compared to today's FPGA chips. Mapping tools will be developed to automatically map algorithms into hardware and abstract away hardware-specific details from end users.

**Critical technical barriers:** Hierarchical interconnect networks have been known to the academic and industrial community for a long time, but physical realization of these networks precluded their successful deployment. **The critical difficulty associated with the hierarchical networks is routing congestion during chip synthesis.** Leopard Logic, Inc, is one example of a company that failed to deploy hierarchical interconnect architecture. FPGA startups today, most notably Abound Logic, Tier Logic, Blue Chip Designs, and Achronix, provide customized solutions for increased logic density or speed, but they still don't solve the problem of power inefficiency associated with FPGA chip interconnects.

**Main elements of the proposed technical approach:** Our approach is based on alternating vertical and horizontal routing. LUTs (or any other processing elements) are partitioned in a 2-D floorplan with switch-boxes placed to allow full routability. An $N$-LUT design requires $\log_2(N)$ levels of switch-boxes. Simple example of $N = 4$ is shown below to illustrate the concept.

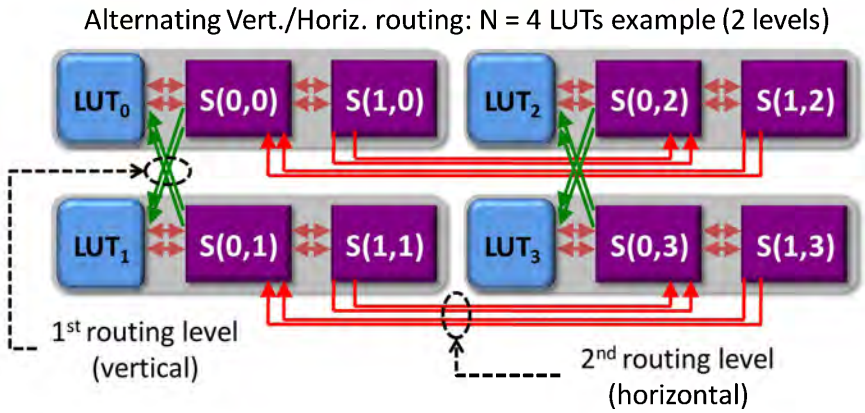



**Figure 4:** Hierarchical Konda interconnect architecture. $O(N \cdot \log_2 N)$ interconnect switches are required for full connectivity. Routing is fully deterministic.

In the case shown in Fig. 4, 2 levels of switch-boxes are required for $N = 4$ LUTs. LUTs with indices from 0 $N/2 - 1$ are placed on the left, the remaining LUTs are placed on the right. Switch-boxes are placed next to the LUT columns. Routing between elements with adjacent index is provided as a vertical connection (1st level routing); routing between elements with 2 indices apart is provided with a horizontal connection (2nd level routing). The routing continues in vertical/horizontal fashion for larger $N$.

**Basis of confidence:** Konda network architecture is a patent-protected technology that is recognized by many semiconductor companies including Cisco, Xilinx, Altera, and LSI Logic. To demonstrate the network in hardware, UCLA team has taped out 3 chips and successfully implemented variants of Konda network and also variants of processor-block features.

*Chip 1* (*90nm, LUT-slice FPGA, concept demo*)*:* A 1024-LUT FPGA was made in 90nm 9SF technology (Dec 2009 run). Our synthesis estimates predict a 250 mW of power and a 600 MHz maximum performance. The chip occupies 2.6 x 2.5 $mm^2$ in 90nm. *Status:* lab testing.

*Chip 2* (*65nm, LUT and DSP slices, small scale*): A 256-LUT 240-DSP 8-BRAM FPGA was made in 65nm technology (June 2010 run). The chip is aimed to show asymmetric network and heterogeneous computing blocks. The chip occupies 2.1 x 3.1 $mm^2$ in 65nm. *Status*: taped out.

*Chip 3 (45nm, DSP-slice FPGA, small scale):* A 512-DSP slice FPGA is made in IBM 45 nm SOI technology (June 2010 LEAP run). We expect power consumption below 500 mW. This design will be applicable to small-scale applications such as micro UAVs. *Status:* taped out.

**Nature and description of end results to be delivered to DARPA:** We will provide several deliverables to DARPA and DOD community as listed below.

- Interconnect architecture and routing tools (software).
- Hardware library in 32nm IBM SOI process (compatible with Cadence software).
- Routing software for the new interconnect architecture and hardware library (software).
- Chip demos of varying scale to demonstrate algorithms of interest to DOD (hardware).
- Tool flow for mapping algorithms onto FPGA chips (software).
- Demonstrations of HPC benchmarks using commercial technology.

The first three items in the list are intermediate steps towards the final hardware demonstration that also includes user-friendly mapping tool interface.

**Cost and schedule of the proposed effort:** $2,374,111 over 3 years.

### 2.4. Technical Approach

**Problem Description:** FPGAs are used in many signal processing and computing applications. DOD mission capability or computing performance can be greatly improved with more energy efficient hardware. FPGA based solutions are very attractive due to their flexibility, similar to that of CPUs. This flexibility comes at a very high energy cost, as shown in Fig. 1.

Looking at the energy efficiency (the amount of energy per unit operation) for a variety of chips from different categories, we observe a 1,000x gap in energy efficiency between microprocessors and dedicated designs. The root cause of this is architectural. Processors have general ALU-type processing unit(s) and large amounts of memory to support time-muliplexing of instructions and data into and out of the ALU(s). Dedicated chips have a variety of processing units, but are very expensive in low-volume and can't be programmed, so they can't be used for HPC applications. General-purpose DSPs are a viable compromise between microprocessors and dedicated designs. Recently, however, FPGA chips have started to gain attention with their increased computing capabilities. Look-up-table (LUT) based chips have energy efficiency similar to that of CPUs and are not very attractive alternatives to CPUs (CPUs are easier to program). Many today's FPGAs have dedicated kernels such as DSP slices, ARM cores, etc. These FPGAs have energy efficiency similar to DSP chips, but they are still 30-50x worse than dedicated chips. The root cause of energy inefficiency in these FPGAs is their interconnect architecture.

Today's FPGAs use 2D-mesh interconnect architecture shown in Fig. 5. Interconnect consists of switch boxes (shown as cross-points), connection points for the buses, and bus drivers (buffers). This architecture is not very scalable: it requires $O(N^2)$ interconnect switches for $N$ LUTs. For 1k processing units, this means 1M switches! To overcome this complexity issue, designers employ heuristics to reduce the number of switches. One of the ideas is to reduce connectivity around the edges, as shown in Fig. 5. Another idea is to reduce top-level connectivity in large designs and utilize local connections. These approaches are heuristic and lead to inefficient utilization of hardware resources. Readers may be have experienced that utilizing more than 80% of FPGA resources without sacrificing performance is a big challenge in commercial FPGA systems.

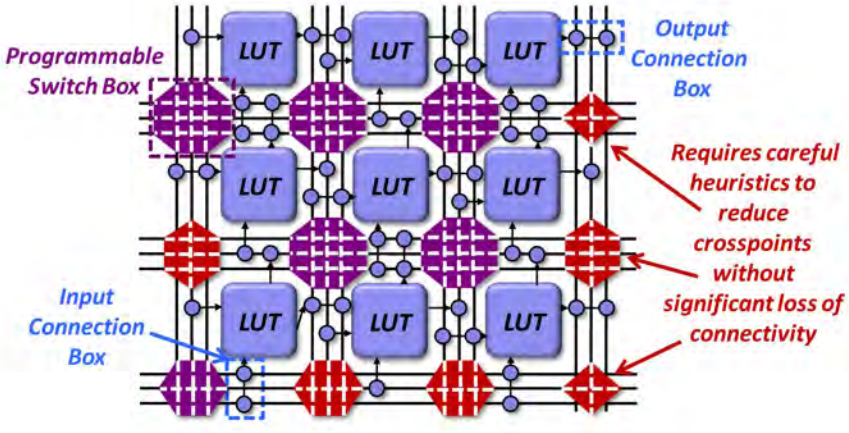



**Figure 5:** 2D-mesh interconnect architecture. $O(N^2)$ interconnect switches are required for full connectivity. Heuristics are used to reduce the network complexity. These heuristics result in non-deterministic routing.

Even after reductions in network complexity, interconnect still occupies over 75% of area in today's FPGAs. For example, Xilinx Virtex-5 chip has 1.1B transistors; 275M are used for logic, 875M (80%) are used for interconnect. Most of FPGA power is dissipated by the interconnect, as shown in Fig. 6. Further simplifying interconnect (without sacrificing connectivity) would have multiple benefits. First, the interconnect power will decrease. Second, due to reduced interconnect area, overall chip area will also reduce. Third, since the chip area is reduced, the size of wires (and wire capacitance) also reduces. The reduction in wire length and complexity implies further reduction in power. It also implies improvements in performance. This excess performance can be traded for increased energy efficiency, or simply used to improve computational efficiency. Finally, we benefit from reduced clock power since the clock is now distributed over a smaller area. Therefore, reduction in interconnect complexity is crucially important for improved computing power and performance.

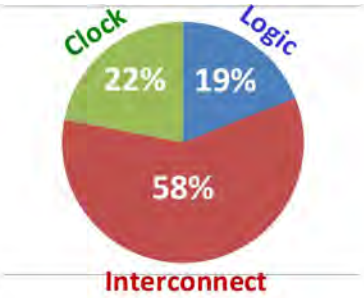



**Figure 6:** Power breakdown in a Virtex-5 FPGA.

**Proposed Network Architecture:** In response to the interconnect challenge, we propose to use a proprietary Konda hierarchical interconnect architecture. This interconnect architecture has greatly reduced complexity, $O(N \cdot \log_2 N)$, and it is based on fully deterministic routing. The concept of Konda network is to use simple unidirectional switches and 2x1 multiplexers to hierarchically connect the computing resources (LUTs, DSP slices, ARM IP, etc.).

Eliminating routing congestions and making the 2D circuit layout possible are the key enabling features of the Konda network. An example of $N = 8$ LUT design with Konda network is shown in Fig. 7. For complete routing $\log_2 8 = 3$ levels of switch matrices are needed. First, vertical tracks connect nearest LUTs, then horizontal tracks are used to connect LUTs at the next level, and finally vertical tracks are used to connect the last level of switches. This structure has full connectivity and completely deterministic 2D routing.

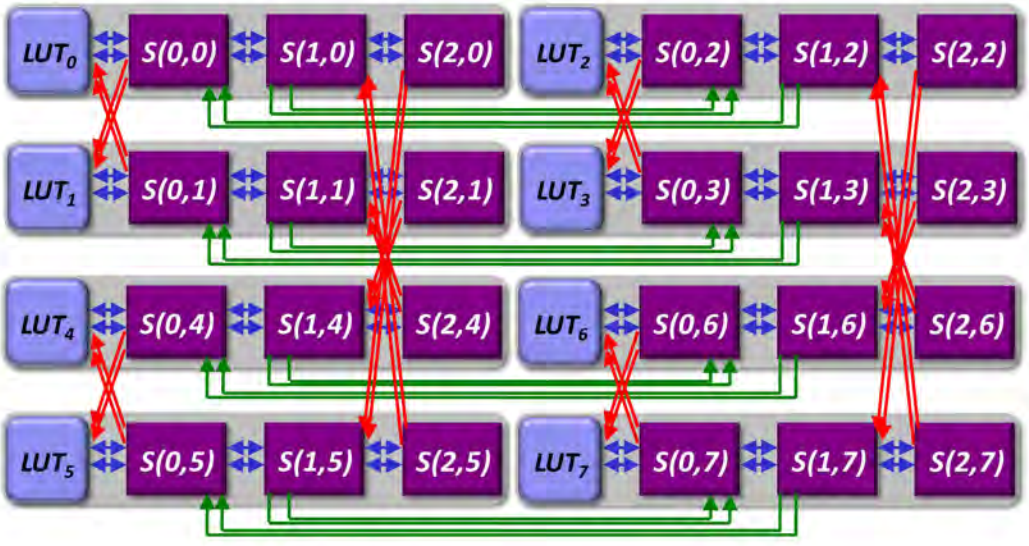



**Figure 7:** Konda interconnect network architecture and routing tracks for $N = 8$ LUTs.

The benefits of this network architecture were evaluated using Toronto20 benchmarks. Toronto 20 benchmark suite originated from an FPGA place-and-route challenge that was set up by University of Toronto Researchers [1] to encourage FPGA researchers to benchmark their software design tool chains on large circuits These 20 benchmarks are from real designs and the placed netlists are provided - for a given FPGA logic block consists of a 4-input look-up table (LUT) and a flip flop - to experiment with different routing architectures and routing algorithms. The existing results are experimented with 2D-Mesh network based routing network by providing partial bandwidth i.e., with different switch-box flexibility, connection-box flexibility and a certain number of channels. Konda hierarchical network is also experimented with partial bandwidth provisioning and the results are compared on various dimensions such as 1) number of cross points, 2) route length (delay) 3) performance 4) speed of routing and 5) routability. Konda hierarchical network performed better in several easily-measureable ways and the results are presented in Tables 2 and 3.

**Table 2:** Comparison of 2D-Mesh and Konda interconnect networks using Toronto20 behcmarks.

| Toronto20 Benchmark Information | | | | 2D-Mesh Network Simulation (Bidirectional wires) | | Konda Hierarchical Network Simulation (Unidirectional wires) | | |
|---|---|---|---|---|---|---|---|---|
| Name | Size | LUTs | Number of connections | Max channel width | Total cross-points | Total cross-points | Savings factor | Cross-points saved |
| alu4 | 40 | 1600 | 1514 | 9 | 177,174 | 58,737 | 3.02 | 118,437 |
| apex2 | 44 | 1936 | 1875 | 10 | 237,660 | 83,180 | 2.86 | 154,480 |
| apex4 | 36 | 1296 | 1243 | 11 | 175,890 | 52,482 | 3.35 | 123,408 |
| bigkey | 54 | 2916 | 1694 | 6 | 213,876 | 54,643 | 3.91 | 159,233 |
| clma | 92 | 8464 | 8302 | 10 | 1,026,780 | 359,846 | 2.85 | 666,934 |
| des | 63 | 3969 | 1347 | 7 | 338,730 | 57,044 | 5.94 | 281,686 |
| diffeq | 39 | 1521 | 1497 | 7 | 131,082 | 49,275 | 2.66 | 81,807 |
| dsip | 54 | 2916 | 1309 | 5 | 178,230 | 40,972 | 4,35 | 137,258 |
| elliptic | 61 | 3721 | 3604 | 9 | 408,510 | 129,507 | 3.15 | 279,003 |
| ex5p | 33 | 1089 | 1019 | 11 | 148,170 | 44,609 | 3.32 | 103,561 |
| ex1010 | 68 | 4624 | 4588 | 9 | 506,790 | 192,391 | 2.63 | 314,399 |
| frisk | 60 | 3600 | 3556 | 11 | 483,186 | 134,686 | 3.59 | 348,500 |
| misex3 | 38 | 1444 | 1383 | 10 | 177,900 | 58,866 | 3.02 | 119,034 |
| pdc | 68 | 4624 | 4535 | 15 | 844,650 | 239,484 | 3.52 | 605,166 |
| s298 | 44 | 1936 | 1929 | 6 | 142,596 | 63,956 | 2.23 | 78,640 |
| s38417 | 81 | 6561 | 6349 | 6 | 478,260 | 207,457 | 2.30 | 270,802 |
| s38584.1 | 81 | 6561 | 6291 | 7 | 557,970 | 184,030 | 3.03 | 373,940 |
| seq | 42 | 1764 | 1717 | 10 | 216,780 | 73,880 | 2.93 | 142,900 |
| spla | 61 | 3721 | 3644 | 12 | 544,680 | 171,676 | 3.17 | 373,004 |
| tseng | 33 | 1089 | 975 | 6 | 80,820 | 31,599 | 2.56 | 49,221 |

The benefits of Konda hierarchical network over 2D-Mesh network using Toronto20 Benchmarks are summarized in Table 4. Various configurations of Konda hierarchical network were tested for each benchmark and the results are verified as follows:

- All 20 benchmarks were routed by our algorithms in our network,

- Switches required to route was reduced significantly,
- Fundamental routing algorithms are proven,
- Speed of routing is proven,
- Benchmarks were profiled for Bandwidth requirements.

**Table 3:** Comparison of 2D-Mesh and Konda interconnect networks using Toronto20 behcmarks. In addition to considerable savings in the number of cross-points, Konda network uses has far better percentage utilization (fewer % is better) than the 2D-Mesh network.

| Toronto20 Benchmark Information | | 2D-Mesh Network Simulation (Bidirectional wires) | | Konda Hierarchical Network Simulation (Unidirectional wires) | | | Other Key Results of the Simulation | |
|---|---|---|---|---|---|---|---|---|
| Name | Size | Max Ch Width | Total Cross-pts | Total Cross-pts | Savings factor | Cross-pts saved | % Cross-pts used Konda | % Cross-pts used 2D-Mesh |
| alu4 | 40 | 9 | 177,174 | 58,737 | 3.02 | 118,437 | 7.9 | 66 |
| apex2 | 44 | 10 | 237,660 | 83,180 | 2.86 | 154,480 | 9.3 | 70 |
| apex4 | 36 | 11 | 175,890 | 52,482 | 3.35 | 123,408 | 9.4 | 60 |
| bigkey | 54 | 6 | 213,876 | 54,643 | 3.91 | 159,233 | 4.1 | 51 |
| clma | 92 | 10 | 1,026,780 | 359,846 | 2.85 | 666,934 | 8.1 | 71 |
| des | 63 | 7 | 338,730 | 57,044 | 5.94 | 281,686 | 2.9 | 33 |
| diffeq | 39 | 7 | 131,082 | 49,275 | 2.66 | 81,807 | 6.9 | 75 |
| dsip | 54 | 5 | 178,230 | 40,972 | 4,35 | 137,258 | 2.8 | 46 |
| elliptic | 61 | 9 | 408,510 | 129,507 | 3.15 | 279,003 | 7.0 | 63 |
| ex5p | 33 | 11 | 148,170 | 44,609 | 3.32 | 103,561 | 9.5 | 60 |
| ex1010 | 68 | 9 | 506,790 | 192,391 | 2.63 | 314,399 | 8.4 | 75 |
| frisc | 60 | 11 | 483,186 | 134,686 | 3.59 | 348,500 | 7.5 | 56 |
| misex3 | 38 | 10 | 177,900 | 58,866 | 3.02 | 119,034 | 8.7 | 66 |
| pdc | 68 | 15 | 844,650 | 239,484 | 3.52 | 605,166 | 10.5 | 56 |
| s298 | 44 | 6 | 142,596 | 63,956 | 2.23 | 78,640 | 7.1 | 89 |
| s38417 | 81 | 6 | 478,260 | 207,457 | 2.30 | 270,802 | 6.0 | 86 |
| s38584.1 | 81 | 7 | 557,970 | 184,030 | 3.03 | 373,940 | 5.3 | 66 |
| seq | 42 | 10 | 216,780 | 73,880 | 2.93 | 142,900 | 9.0 | 68 |
| spla | 61 | 12 | 544,680 | 171,676 | 3.17 | 373,004 | 9.3 | 63 |
| tseng | 33 | 6 | 80,820 | 31,599 | 2.56 | 49,221 | 6.7 | 78 |

**Table 4:** Summary of the benefits of Konda hierarchical network. Analytical and empirical results are shown, the numbers are relative to 2D-Mesh network.

| Criteria | Analytical | Empirical |
|---|---|---|
| Interconnect area | At most 1/3 | At most 1/3 |
| Connectivity | 2-3x | 2-3x |
| Interconnect Power | 1/5 to 1/10 | 1/5 to 1/10 |
| Interconnect Latency | 1/5 to 1/10 | 1/5 to 1/10 |
| Speed of compilation | Significantly faster | Significantly faster |
| Scalability across process generations | Close to linear | Close to linear |

The conclusions of simulation of Toronto20 benchmarks using Konda hierarchical network matched the benefits derived in empirical analysis. The generic routing tool created for Konda hierarchical network delivers consistent and predictable results. Based on the Toronto20 benchmark results it can be projected that the gap between ASIC's and FPGA's can be closed as shown in Fig. 8, which would significantly improve performance and energy efficiency of HPC hardware. In the proposed work, we will explore further technology improvements.


**Figure 8:** Konda interconnect network architecture has substantial benefits over today's FPGAs. It is projected to have ASIC-like energy efficiency, power, and performance. Such energy-efficiency levels are more than 100x better than general purpose processors.

### 2.4.1. Network Architecture and Routing Tools

We will next work on homogeneous and heterogeneous networks featuring arbitrary level of connectivity. The decision about the connectivity level will be aided with feedback from the mapping tools (Task 6) in order to minimize hardware utilization.

**Task 1) Routing Architectures for Homogeneous Blocks:** Routing tool will be developed for the FPGA with homogeneous blocks. Routing algorithms need to be developed for uni-terminal nets and multi-terminal nets. The hierarchical routing network may be a symmetric network where the number of inputs and the number of outputs are the same. The routing network may also be asymmetric network where the number of inputs and the number of outputs are not the same. Rearrangeably nonblocking and strictly nonblocking multi-terminal net algorithms will be implemented to demonstrate the routability and the speed of routing. Routing algorithms need to be implemented for configurations of Konda hierarchical network where some of the stages in the network may be partially connected and the other stages are fully connected. The LUT size of the network may be a perfect power of two or non-perfect power of two.

**Task 2) Routing Architectures for Heterogeneous Blocks:** We will also explore interconnect architectures suitable for heterogeneous blocks. The key architectural challenge is to adapt the Konda hierarchical network for FPGA architecture. A fully connected hierarchical network is an over-kill for FPGA applications. Our goal is to converge on the appropriate design of the routing network in three phases and also adopt it to many different applications end-user applications. Also we need to experiment with many varieties of hierarchical network designs such as Benes

network, butterfly fat-tree network and other optimizations related to properties of FPGA designs. One aspect is to analyze the locality typical in FPGA designs and optimizing or adopting Konda hierarchical network with optimum bandwidth for local connectivity and global connectivity. The typical LUT size that is known to be optimal in a 2D-Mesh routing network may not be optimal for Konda hierarchical network. This is because Konda hierarchical network provides richer connectivity with smaller switch and less number of tracks. Determining the appropriate length of the tracks is another aspect that will be addressed in this task.

### 2.4.2. Hardware Design

To fully demonstrate the benefits of the proposed interconnect architectures and routing tools, we will implement the network architectures on a series of chips. Hardware design tasks will concentrate on achieving two goals: 1) hardware demonstration of power, area, and performance benefits, 2) development of automated chip routers to facilitate technology transition.

**Task 3) Chip Demonstrations:** Multiple chip demonstrations are planned to further quantify the benefits of the interconnect technology, and to further optimize interconnects based on hardware experiments.

*Prior Work:* We have designed several chips prior to this program, as summarized in Table 5. This was a self-initiated self-supported work. The results of IBM-90 and TSMC-65 chips will be available in September 2010. The results will be made available to the OHPC community.

**Table 5:** Summary of FPGA chips built prior to the OHPC program.

| Chip ID | Features | Area | Power | Performance | Status |
|---|---|---|---|---|---|
| **IBM-90** | 1k LUTs | 6.5 $mm^2$ | 250 mW | 300-600 MHz | Lab testing |
| **TSMC-65** | 256 LUTs<br>240 DSPs<br>1 BRAM | 8 $mm^2$ | 500 mW | 400-700 MHz | Taped out 6/2010 |
| **IBM-45-SOI** | 512 DSPs | 4.4 $mm^2$ | 500 mW | 500-800 MHz | Taped out 6/2010 |

The chips summarized in Table 5 are an initial demonstration of hardware feasibility of the interconnect network. The chips also demonstrate the integration of heterogeneous blocks (LUT, DSP, BRAM) for small-scale examples. Before describing the features of proposed chips, below is the description of design methodology used in prior work.

Figure 9 illustrates hierarchical design approach that starts with switch-matrix design. The switch-matrix blocks are custom-designed to allow tiling and hierarchical expansion. Design techniques used here will become cornerstones for the automation (Task 4).

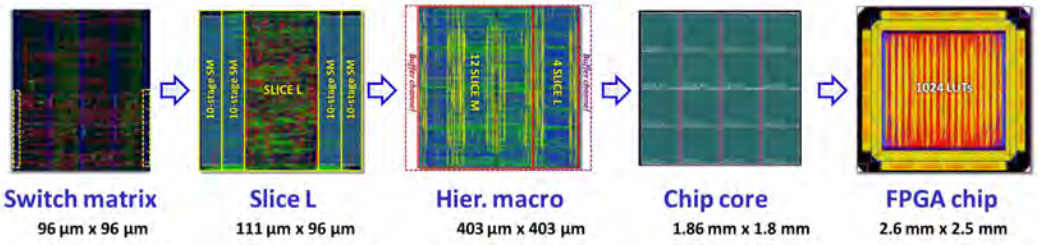



**Figure 9:** Herearchical design procedure starting with switch-matrix design, integration of a slice, a hierarchical macro, and chip-level integration.

The IBM-90 chip illustrates LUT-only design. Consistent with predictions from Tables 2 and 3, Konda network achieves at least 3x lower interconnect area. Conventional chips have over 75% of interconnect area. In our chip, we have 50% logic (LUTs) and 50% switches (wires), which confirms the 3x interconnect area reduction estimate. Even with nearly-full connectivity, our chip has only 50% of area of the interconnect (3x less than commercial).

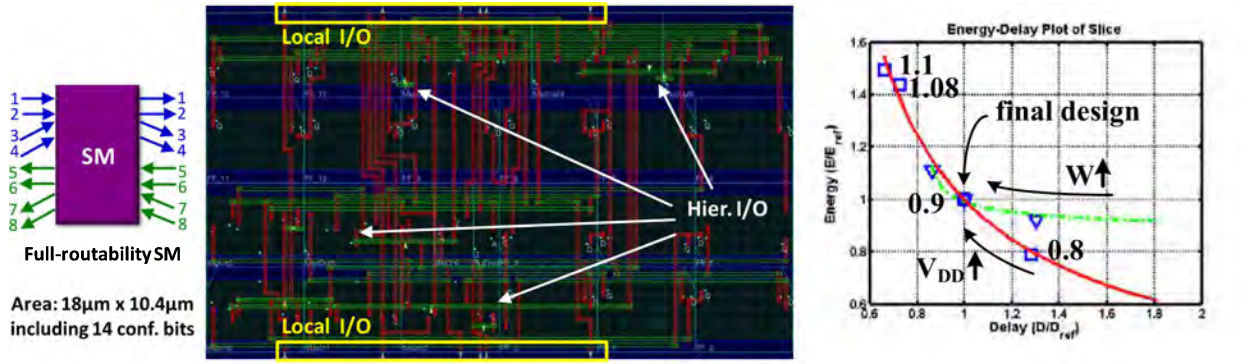



**Figure 10:** Detail of switch-matrix block (left), Energy-delay optimization of LUT macros (right).

Figure 10 shows the detail of the switch-matrix block. Local I/O connections allow tiling of layout macros, while pins in the middle are being used for hierarchical routing. Plot on the right shows energy-delay optimization after gate sizing and supply voltage tuning. We designed for 0.9 V supply (corresponding to the nominal/slow corner). The design is based on the sensitivity optimization methodology [6] that balances impact of all tuning variables. At a solution point, sensitivities to all variables are equal. In the energy-delay space, this means that the energy-delay lines obtained by tuning individual variables around a design point should be tangent. This is shown in the final design, where the $V_{DD}$ and sizing ($W$) lines have similar slopes at $V_{DD} = 0.9$ V. With these optimizations being made at the circuit level, we ensure that power efficiency considerations are propagated from system level down to the technology level. Our 1k FPGA is estimated to consume total of 250 mW of power when fully utilized. The energy efficiency per CLB slice is 0.96 pJ at 0.9V. We also performed deep pipelining to maximize performance. Synthesis estimates show a 600 MHz performance. This performance is significantly better than 450 MHz achieved by Xilinx Virtex-5 parts (Virtex-5 is built in a faster 65 nm technology).

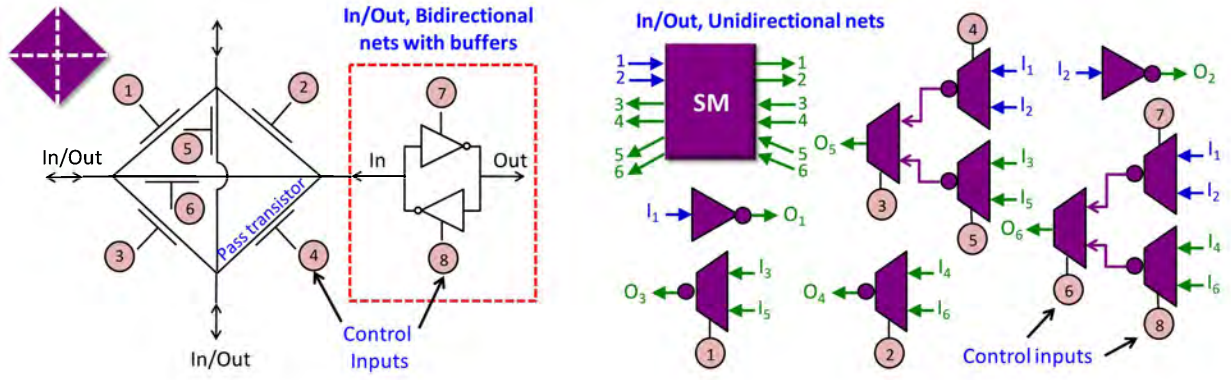



**Figure 11:** Switch-point in 2D-Mesh network highlighting bidirectional nets (left), Switch-matrix in Konda network (right) highlighting unidirectional nets.

A very important feature of Konda interconnect architecture is that it uses only unidirectional wires, as shown in Fig. 11. The 2D-Mesh architecture uses bidirectional nets as shown on the left. Going from bidirectional to unidirectional nets results in a lower switching net capacitance. Implementation of the Konda switch-matrix is done with simple 2x1 muxes.

After demonstrating the feasibility of Konda network architecture on chip, the next bit challenge is to support the integration of heterogeneous blocks (LUTs, DSPs, BRAMs, etc.). Also, one should explore irregular switch-matrix architecture to reduce top-level wiring. An irregular switch-matrix design shown in Fig. 12 is implemented on the TSMC-65 chip (Table 5).

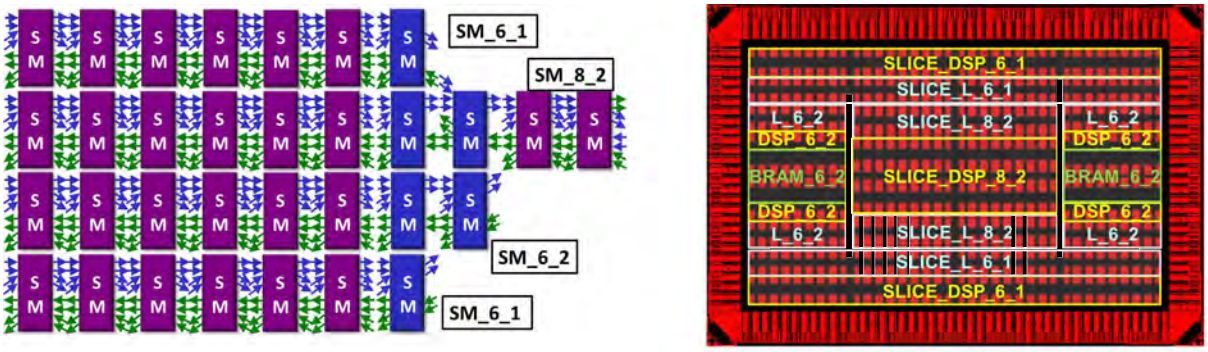



**Figure 12:** Irregular switch-matrix architecture to reduce top-level wiring (left), Chip demonstration of LUT, DSP, and BRAM modules using the irregular SM architecture (right).

The idea implemented in the network architecture from Fig. 12 is to use full connectivity only near the center of the chip. In our previous FPGA designs, long wires are routed across the entire chip to connect the bordering switch matrices at the topmost level. The drawback of these long wires is the requirement of many buffer insertions, consuming excessive power and routing area. The irregular switch matrix architecture reduces the number of top-level buffers by 95% since the bordering switch matrices now route through the center switch matrices to connect to the other side.

*Proposed Work:* The chips summarized in Table 5 are just an initial effort towards optimized FPGA implementation. This proposal will focus on hardware designs with reduced-complexity irregular network architectures developed in Tasks 1 and 2. Together with mapping tools from Tasks 5 and 6, we will be able to minimize level of connectivity required for chip-level routing. This will be demonstrated in actual hardware designs as explained below.

We plan to make use of the DARPA LEAP program for chip fabrication. We will demonstrate medium-scale designs for which regularity of layout cells, in addition to architecture regularity, will play a key role in improving tolerance to manufacturing variations. We will thus explore designs with regular layout geometries in IBM's 32nm SOI process. The evaluation of circuit metrics as compared to standard-cell based CMOS design will result in a library of FPGA building blocks which will be used for chip demonstrations. In addition to the IBM library cores and routing tools (Task 4), we will also consider TSMC libraries due to their general use and to provide additional options for technology transition.

In CMOS run A (see Sec 2.8.1), we will test the use of library IP for the integration of medium-scale FPGA processor (5K LUTs). Since 32nm SOI process is new and not yet fully tested by designers, we will work with homogeneous LUT-only design to minimize the risk of potential manufacturing and design issues. This chip is a 10x larger than the IBM-90 and will allow us to confidently explore mapping algorithms for this level of design complexity.

In CMOS run B (see Sec 2.8.1), we will design a chip with 15K DSP slices. The chip will be compliant with FMC expansion modules (160 I/O pins). This design will be able to support DSP-centric applications such as signal and information processing. The chip will be tested using BEE4 module (coming out in Fall 2010) from BEEcube. Such setup will allow us to do side-by-side comparison with Virtex-6 Xilinx FPGAs. We will work with BEEcube on HPC application benchmarking and will also welcome inputs from the DOD community.

In CMOS run C (see Sec. 2.8.1), we will demonstrate LUT/DSP/BRAM based design with over 15K LUTs, over 15K DSP slices, and adequate BRAM memory. The chip will be also compliant with FMC for testing with the BEE4 module. Chips B and C will make use of irregular network architecture and optimized connectivity as described in Task 4. The chips from CMOS run C will be used for inter-module communication with multiple BEE4 boards to show expandability to large HPC benchmarks.

**Task 4) Automated Chip Routing Tools:** To facilitate the integration of medium- and large-scale FPGA chips, and to enhance our technology transition capabilities, we will work on automated chip routing tools. The tools are intended to automate custom design strategies developed in our prior work. We will also automate design techniques further developed under Task 3, particularly CMOS runs A and B (see the scheduling chart in Sec. 2.8.1).

Advanced routing tools will need a library of switch-matrix blocks with varying degree of connectivity. Figure 13 shows example of full- and half-connectivity cells as well as full-to-half connectivity interface cells. The use of these simple cells, and others, will enable us to support network routers (developed in Tasks 1 and 2) with arbitrary level of connectivity.

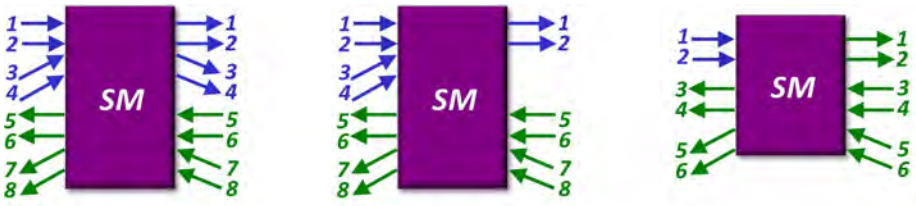



**Figure 13:** Switch-matrix (SM) blocks include full-connectivity (left), full-to-half-connectivity (middle) and half-connectivity (right) features.

An example of cell design for future automated routing is shown in Fig. 14. In the chip shown in Fig. 12, DSP slices have to be designed with fixed width due to size constraints from configuration SRAM blocks. In our architecture, we use wordline (WL) to drive SRAM modules on both sides (left and right of the WL circuits). WL routing is done in metal 3 (M3) as shown in Fig. 14. We must allow M3 tracks for neighboring SM. The routing channel for 7 bits of SRAM

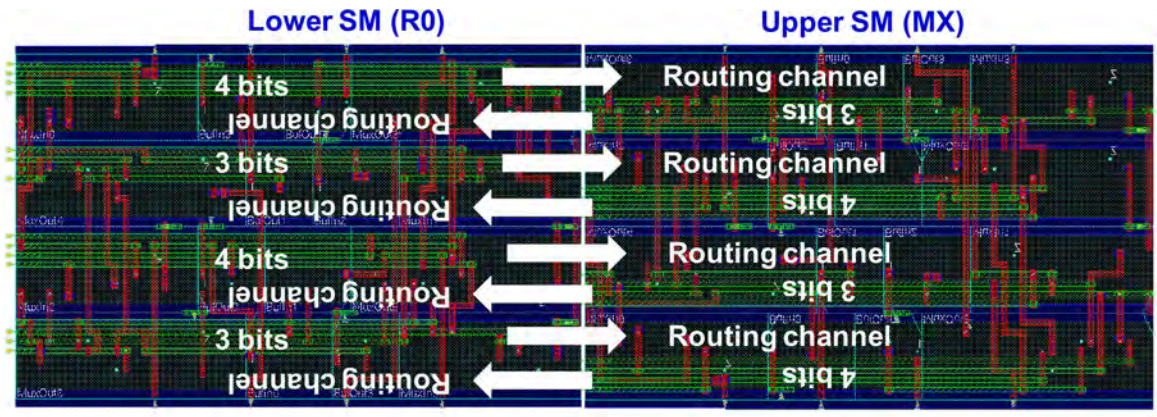



**Figure 14:** Switch matrix design showing detail of SRAM routing tracks. Upper SM (right) is a mirrored-version of the lower SM (left). Alternating 4/3 bits per row and custom muxes are used to facilitate 7-bit routing of SRAM configuration bits.

is made using alternating 4/3-bit horizontal tracks. We also make use of custom muxes to reduce redundant input inverters (details not shown on the figure). These concepts will be automated.

Automation of other routing tasks, in addition to the one illustrated in Fig. 14, will be performed. The outcome of Task 4 will be the router that can take arbitrary number of LUT, DSP, and BRAM cells and, for a given level of connectivity, provide routed chip that implements optimal network architecture developed in Task 2. This kind of routing capability will allow us to customize chip features and rapidly construct energy-efficient FPGAs for HPC applications (analogous to different Xilinx chip families, for example). The automated routing will also provide chip design community a tool for the utilization of our library macros. We will maintain library of macros in IBM 32nm SOI technology (for DOD community) and also TSMC 32/28nm technology (for DOD and commercial use).

### 2.4.3. Hardware Mapping

For an FPGA to be effectively used by its consumers, an automated mapping tool must be provided as well. Mapping tool for commercial FPGAs are provided to convert user-provided Verilog or VHDL into a gate-level design, and automatically place-and-route these gates onto the FPGA. As a result, the user has complete automation from Verilog/VHDL to a functional FPGA. The mapping and place-and-route software is a crucial component of this project, and major efforts ought to be allocated to provide an efficient tool.

**Gate-level Synthesis:** The first step of the mapping process is to create a mappable design from the Verilog or VHDL input. The process is called logic synthesis, an intricate procedure requiring complex algorithms.

To optimize our resource usage, we plan to adopt commercial synthesis tools such as Synopsys® Design Compiler or Cadence® RTL Compiler. Both these tools operates on a standard cell library that contains information regarding the timing and functional characteristics of each logic gate. The tool then converts the input design into a netlist consisting of gates from the standard cell library.

The main task here is to create a standard cell library mappable to our custom FPGAs. If the FPGA is constructed from 4-input LUTs, then the standard cell library ought to include different combinations of 2, 3, and 4-input logic gates. The FPGA mapper can then determine the appropriate values to program to each LUT based on the logic gate.

*Netlist Optimization:* Although the synthesized netlist is fully functional, it may not be optimal for our FPGA applications. The logic netlist should therefore be optimized by the mapper for area reduction and speed improvements. This is the second step of the mapping process.

In modern FPGAs, the majority of the area and delay are attributed to interconnects between logic gates. Therefore it is beneficial to maximize the logic function of each LUT instead of spreading the same function over many LUTs. To achieve such optimality, logic gates with less than 4 inputs are searched for logic recombination with its neighboring gates:

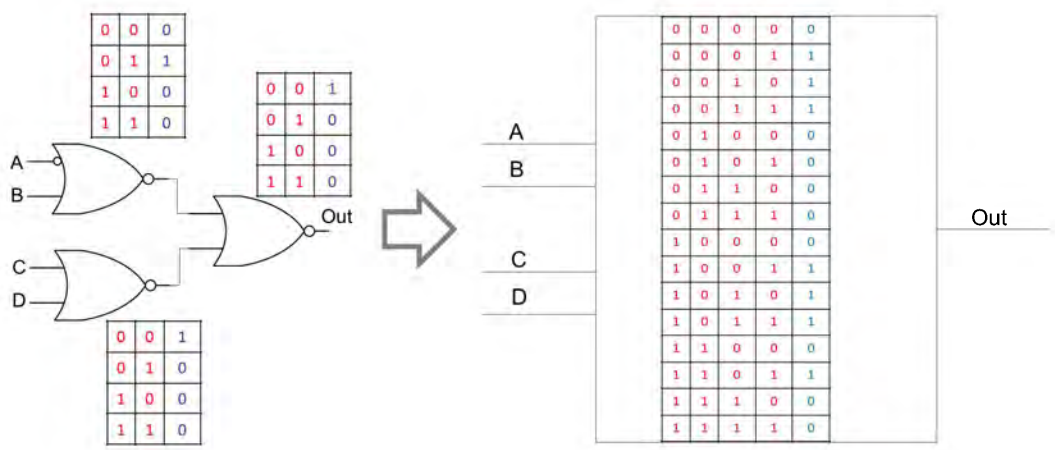



**Figure 15:** Illustration of gate-level synthesis.

Shown are two 2-input gates drive another 2-input gate. These 3 gates can be combined to a 4-input gate to fit into a single LUT instead of spreading over 3 LUTs, wasting both logic and routing resources. More strictly speaking, any sequential logic gates with a total unique input of 4 or less can be combined into a single 4-input LUT.

In our FPGAs, a 4-input LUT can be reprogrammed as two 3-input LUTs, where 2 of the inputs are shared. Two 3-input gates can potentially share a single LUT as long as the number of unique inputs is 4 or less. Two 2-input gates can always share a LUT as well. The mapper tool can exploit such feature during the placement process, as mentioned later.

**Task-5) Place & Route Algorithms and Tools:** Once the netlist has been optimized, place and route can begin. Each logic gate ought to be placed before it can be routed. Finding a suitable placement for each logic gate can greatly affect the performance of the final design, and poses a significant challenge to the tool.

The placement process is divided into coarse placement, which determines the gate partition, and fine placement, which determines the exact gate location in each partition. Gate partition takes place first, and the goal is to partition the gates into quadrants to minimize cross-partition

interconnects. This process can be modeled by an optimization problem, where the cost is total number of wires crossing horizontal, vertical, and diagonal boundaries. A penalty cost can be added to ensure even distribution of gates across partitions.

In most convex optimization problems, only the local minima can be determined based on the initial condition. Since an optimal initial condition cannot be determined, and the cost function may contain numerous local minima, a simulated-annealing based algorithm is used for gate partition. Based on the size of the design, numerous locally-optimal solutions can be found, and the lowest-cost solution is chosen.

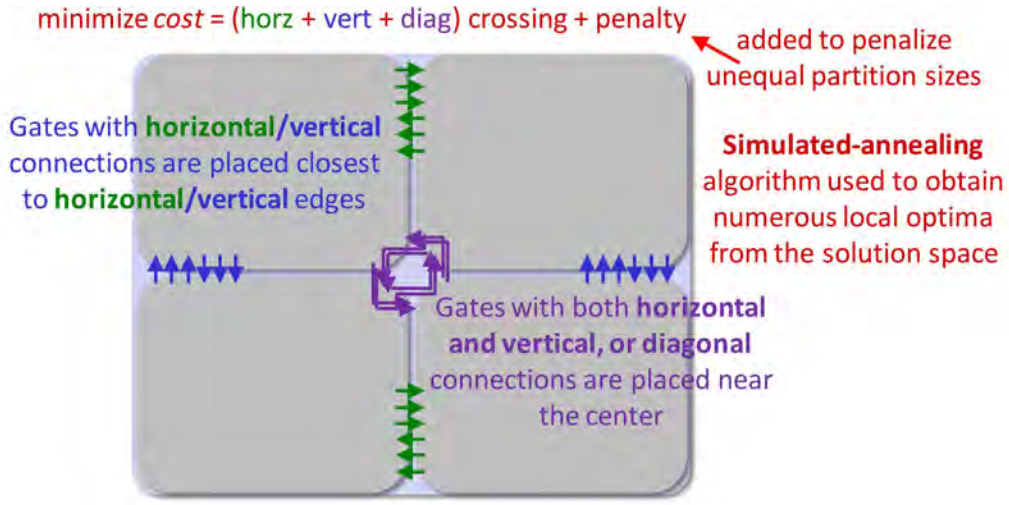



**Figure 16:** Mapper for hierarchical-interconnect FPGAs.

Once the gate partition is determined, first level of fine placement can proceed. The longest interconnects are those requiring diagonal connections across the area. These gates are placed near the center of the area, where the diagonal connections are the shortest. Gates with vertical and horizontal connections are then placed near their respective edges to minimize their wire connections.

*Hardware Routing:* Since the routing resources in FPGA are limited, routing should occur at the same time as placement. This prevents a gate from being placed at a non-routable location. When a gate is being considered for a location, all of its inputs and outputs should be located. The input and output gates that are already placed must be able to route to this location, else a new location must be determined. In cases where more than one possible routes exists, each routing candidate should be evaluated for interconnect length, and the shortest interconnect is chosen.

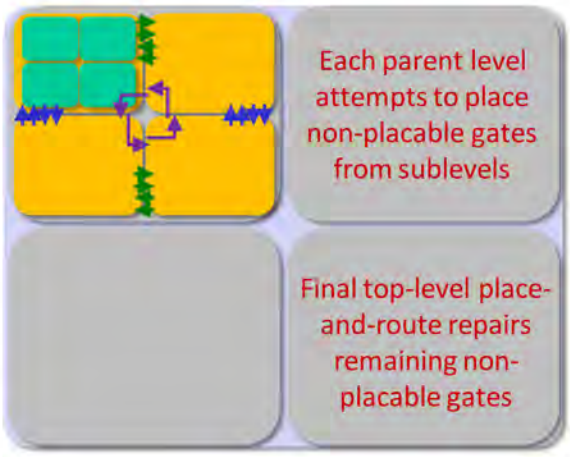



**Figure 17:** Recursive execution of sub-level PnR.

*Automated Place and Route:* The place-and-route tool can utilize recursive placement. Since all the partition-crossing gates are placed, all the non-placed gates in each partition are local to that partition, meaning they do not connect to any gates outside the partition. For each quadrant, the aforementioned place and route occurs again to place gates within the subquadrants, until all the quadrants (and subquadrants) are processed.

In some cases, a gate may not be placed inside the chosen partition, then other partitions at the level are considered for placement. If none of the partitions can accept the gate to be placed, a higher hierarchy is searched for placement.

**Task 6) Tools for Hardware Mapping:** The final step of the place-and-route process is the output the design. This step creates the exact bit sequence required to program the scan chain on the FPGA, which configures all the LUTs and interconnects to create the programmed function.

For each of our FPGA, we have knowledge of the exact bit location for each of the LUT configurations, as well as the switch-matrix configurations. For the logic block shown below, four LUTs are programmed as one configurable logic block. The scan-chain (SI) first controls internal configurations (such as 4-input/3-input mode, carry-chain propagation, register output, etc), and then controls each of the four LUT values. The corresponding configurations from the place-and-route output are then mapped to these bits on the scan-chain. The switch matrix bistream is determined in the similar fashion since all the interconnect configurations are already known from place-and-route.

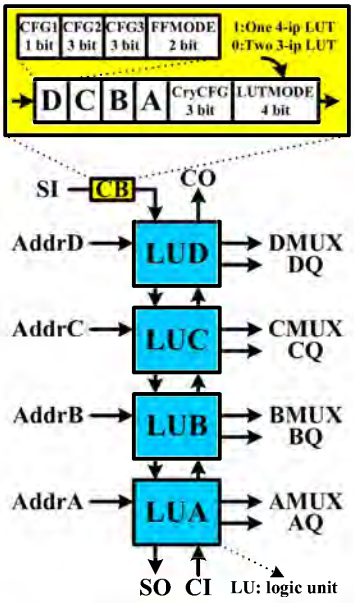



**Figure 18:** Configuration bits for a Slice-L (4 LUTs) block.

**Task 7) Demonstrations and Technology Transition:** We will use chips from CMOS runs B and C (see Sec 2.8.1) to demonstrate the benefits of our hardware as compared to Xilinx Virtex-6 chips by using the BEE4 module from BEEcube.

*Collaboration with BEEcube:* We will work with BEEcube (support letter attached at the end of Volume I) to do technology demonstration and initial transition to HPC applications. We will make use of future BEE4 platform consisting of 4 Virtex-6 FPGA chips (LX240 family) and featuring FMC interface (160 pins/chip). A custom PCB board with our FPGA will comply to the FMC interface specifications. BEE4 FPGA chips will be used to execute computations on our custom chips, as shown in Fig. 19. This setup will also allow side-by-side benchmarking of Virtex-6 FPGAs and our chips.

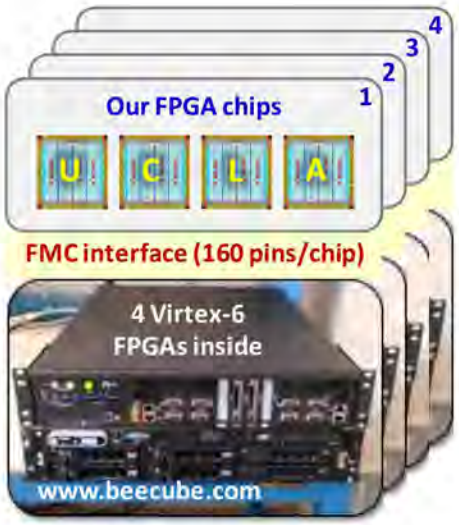



**Figure 19:** Technology demonstration and initial transition using BEEcube HPC technology.

To further demonstrate inter-module communication and scalability to larger systems, we will connect 4 BEE4/Chip modules, as shown in Fig. 19. We will use BEEcube HPC benchmarks for initial evaluations. We welcome inputs from DOD community and other teams in the OHPC program about example algorithms.

In addition to BEEcube benchmarks, we will explore parallel execution of neural spike sorting algorithms from UCLA Medical School, Department of Neurology. We have data from our scientific collaborators (Prof. Rick Staba, and Prof. Chris Giza) who monitor neural action potentials in human patients with acute epilepsy. Data recording (64 channels, 10 bits, 28 kS/s) over 3 weeks aggregates 2 TB of data per patient and presents an extreme signal processing challenge. We have tried to process one hour of data (60 GB) using a CPU cluster with 40 3 GHz processors. Although we sample at 30 kHz, the total run-time was 68 minutes due to sequential nature of CPU processing. When the same algorithm was mapped to an FPGA running with a 300 MHz clock, we estimated processing time to be 0.4 seconds. Since we can execute complete algorithm iteration in one clock cycle, we get a 10,000x improvement in execution (300 MHz / 30 kHz). The bottleneck is how fast we can feed the data into the FPGA, not the speed of the FPGA itself. We would like to collaborate with other teams in the OHCP program who are exploring storage bandwidth issues.

*Future Implications:* Upon successful demonstration with BEEcube, the technology can be further scaled up to a rack system as shown in Fig. 20. A number of FPGA nodes will be used to execute common operations. Optionally, one could have a small number of general-purpose CPU blades for non-standard operations. This configuration will require software development to abstract away hardware details from the user and can be a topic addressed by other OHPC teams. Finally, Konda network can also be applied for efficient rack-to-rack connectivity to produce ultra-low-power and ultra-high-performance HPC systems for extreme computations.

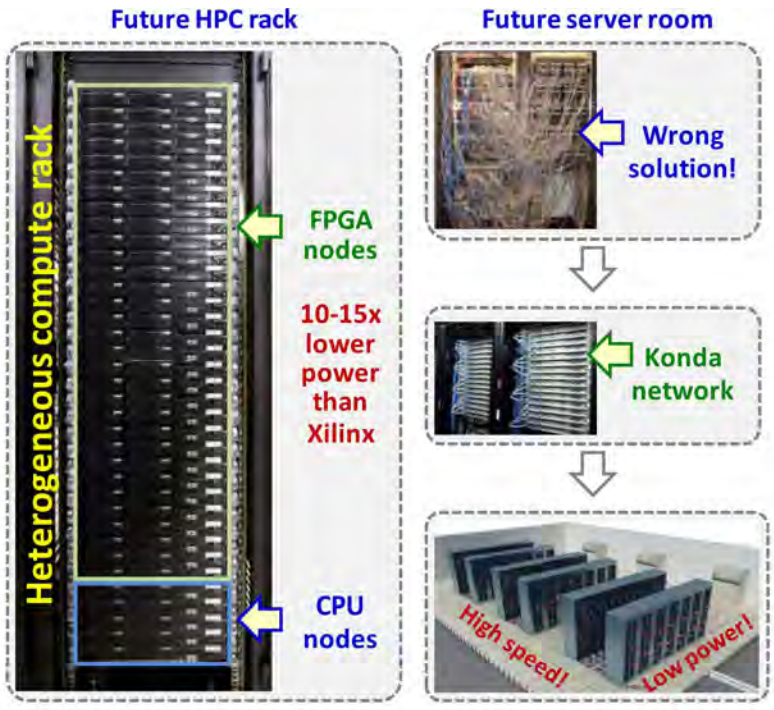



**Figure 20:** Future possibilities with our technology: FPGAs can be used in rack-scale systems (left), .Konda network technology can also provide superior rack-to-rack connectivity for server farms (right).

### 2.5. Statement of Work (SOW)

We propose to develop energy-efficient programmable hardware and supporting mapping tools. The hardware is based on proprietary Konda interconnect architecture that provides significant reduction in interconnect complexity as compared to existing FPGAs. The new architecture and supporting tools are projected to provide over a 15x improvement in energy efficiency while also considerably reducing chip area and improving performance.

**Task 1: Architectures for Homogeneous Blocks (Lead: *Konda*) $200K, Q1-Q3**

*Objective:* Define interconnect architecture and routing tools for designs with a given number of homogeneous blocks such as LUT or DSP slices.

*Approach:* Rearrangeably nonblocking and strictly nonblocking multi-terminal net algorithms will be implemented to demonstrate the routability and the speed of routing. Routing algorithms need to be implemented for configurations of Konda hierarchical network where some of the stages in the network may be partially connected and the other stages are fully connected. The LUT size of the network may be a perfect power of two or non-perfect power of two.

*Exit criteria:* When the chosen interconnect architecture demonstrates the optimal tradeoff between interconnect size and performance (as quantified by Toronto20 benchmarks).

*Deliverables:* Architectural diagram of the interconnect structure (block-level schematic).

**Task 2: Architectures for Heterogeneous Blocks (Lead: *Konda*) $200K, Q3-Q6**

*Objective:* Define interconnect architecture and routing tools for designs with a given number of heterogeneous blocks such as a combination of LUT, DSP slices, memory, and IP elements.

*Approach:* We will make use of the infrastructure developed for Task 1 and customize interconnects local to each type of heterogeneous block.

*Exit criteria:* Interconnect architecture with optimal size-performance tradeoff as quantified by Toronto20 benchmarks.

*Deliverables:* Architectural diagram of the interconnect structure (block-level schematic).

**Task 3: Chip Demonstrations (Lead: *Markovic*) $900K, Q1-Q11**

*Objective:* To demonstrate the feasibility of the interconnect architecture on different design complexity and compare performance and power with commercial FPGAs.

*Approach:* We will design and verify three FPGA chips with increasing level of complexity (5K, 15K, 45K LUTs). The chips will be constructed from custom-designed macros, including processing, memory, and interconnect blocks.

*Exit criteria:* Hardware demonstration of superior performance (>2x), energy (15x), and area metrics (>2x) as compared to commercial FPGAs.

*Deliverables:* Library of FPGA macros, chip demonstration results.

**Task 4: Automated Chip Routing Tools (Lead: *Markovic*) $100K Q4-Q5**

*Objective:* To automatically place-and-route an FPGA according to hardware requirements.

*Approach:* Library of FPGA macros for the technology of interest, automatic Verilog generation, supporting scripts for chip synthesis.

*Exit criteria:* Design and layout of an FPGA using the automated toolflow.

*Deliverables:* Scripts for synthesis and tools for automatic Verilog generation (that use the library of FPGA macros delivered in Task 3).

**Task 5: Place and Route Algorithms and Tools (Lead: *Markovic*) $300K, Q1-Q6**

*Objective:* Determine the optimal physical location and routing for each LUT / macro to maximize resource utilization and chip performance.

*Approach:* Partition LUT / macro blocks into sets with coarse and fine levels of granularity. Place and route gates for minimum interconnect delay. The algorithm repeats hierarchically until all levels of interconnect are placed and routed.

*Exit criteria:* Successful place-and-route of Chip A (5K LUTs) to its full interconnect utilization.

*Deliverables:* Software demonstration of an automated place-and-route flow.

**Task 6: Tools for Hardware Mapping (Lead: *Markovic*) $100K, Q3-Q4**

*Objective:* To map the place-and-routed design to a bitstream format for FPGA programming.

*Approach:* Creates the exact bit sequence based on the scan chain configuration implemented on chip. This configures all the LUTs and interconnects to execute the programmed function.

*Exit criteria:* Successful programming of scan chain with demonstrated functionality.

*Deliverables:* An automated tool for bitstream programming.

**Task 7: Demonstrations and Technology Transition (Lead: *Markovic*) $500K, Q7-Q12**

*Objective:* Demonstrate the benefits of our technology for HPC applications.

*Approach:* Use chips from CMOS runs B and C with the BEE4 platform (consisting of four Virtex-6 FPGA chips) to perform HPC benchmarking. The BEE4 FPGA chips will be used to execute computations on our custom chips and perform side-by-side comparison of Virtex-6 FPGAs against our chips.

*Exit criteria:* Functional HPC platform based on BEE4 and custom FPGA chips.

*Deliverables:* Results from HPC benchmarking, hardware demonstration of performance and energy efficiency on BEE4-based platform.

**Table 6:** Task Cost and Schedule

| Task / Cost | Year 1 | Year 2 | Year 3 | Total |
|---|---|---|---|---|
| Task 1: Homogeneous Architecture | $200K | - | - | $200K |
| Task 2: Heterogeneous Architecture | - | $200K | - | $200K |
| Task 3: Chip Demonstrations | $350K | $350K | $200K | $900K |
| Task 4: Automated Chip Routing | $50K | $50K | - | $100K |
| Task 5: Place-and-Route Algorithms and Tools | $200K | $100K | - | $300K |
| Task 6: Tools for Hardware Mapping | $100K | - | - | $100K |
| Task 7: Demonstrations and Technology Transition | - | $100K | $400K | $500K |

**2.6. Intellectual Property**

Venkat Konda has filed 10 patent applications and assigned them to Konda Technologies Inc. More patent applications are in the pipeline. The following is the complete list of patent applications:

[1] Large Scale Crosspoint Reduction with Nonblocking Unicast & Multicast in Arbitrarily Large Multi-stage Networks
- US Provisional Patent Application Number: 60/905,526
- Date Filed: March 6, 2007

[2] Fully Connected Generalized Multi-stage Networks
- US Provisional Patent Application Number: 60/940, 383
- Date Filed: May 25, 2007

[2a] Fully Connected Generalized Multi-stage Networks
- PCT Patent Application Serial Number: PCT/US08/56064
- Date Filed: March 6, 2008

[2b] Fully Connected Generalized Multi-stage Networks
- US Patent Application Serial Number: 12/530,207
- Date Filed: September 6, 2009

[3] Fully Connected Generalized Butterfly Fat Tree Networks
- US Provisional Patent Application Number: 60/940, 387
- Date Filed: May 25, 2007

[4] Fully Connected Generalized Multi-Link Butterfly Fat Tree Networks
- US Provisional Patent Application Number: 60/940, 390
- Date Filed: May 25, 2007

[4a] Fully Connected Generalized Butterfly Fat Tree Networks
- PCT Patent Application Number: PCT/US08/64603
- Date Filed: May 22, 2008

[4b] Fully Connected Generalized Butterfly Fat Tree Networks
- US Patent Application Number: 12/601,273
- Date Filed: November 22, 2009

[5] Fully Connected Generalized Rearrangeably Nonblocking Multi-Link Multi-stage Networks
- US Provisional Patent Application Number: 60/940, 389
- Date Filed: May 25, 2007

[6] Fully Connected Generalized Strictly Nonblocking Multi-Link Multi-stage Networks
- US Provisional Patent Application Number: 60/940, 392
- Date Filed: May 25, 2007

[7] Fully Connected Generalized Folded Multi-stage Networks
- US Provisional Patent Application Number: 60/940, 391
- Date Filed: May 25, 2007

[7a] Fully Connected Generalized Multi-link Multi-stage Networks
- PCT Patent Application Serial Number: PCT/US08/64604
- Date Filed: May 22, 2008

[7b] Fully Connected Generalized Multi-link Multi-stage Networks
- US Patent Application Serial Number: 12/601,274
- Date Filed: November 22, 2009

[8] VLSI Layouts of Fully Connected Generalized Networks
- US Provisional Patent Application Number: 60/940, 394
- Date Filed: May 25, 2007

[8a] VLSI Layouts of Fully Connected Generalized Networks
- PCT Patent Application Number: PCT/US08/64605
- Date Filed: May 22, 2008

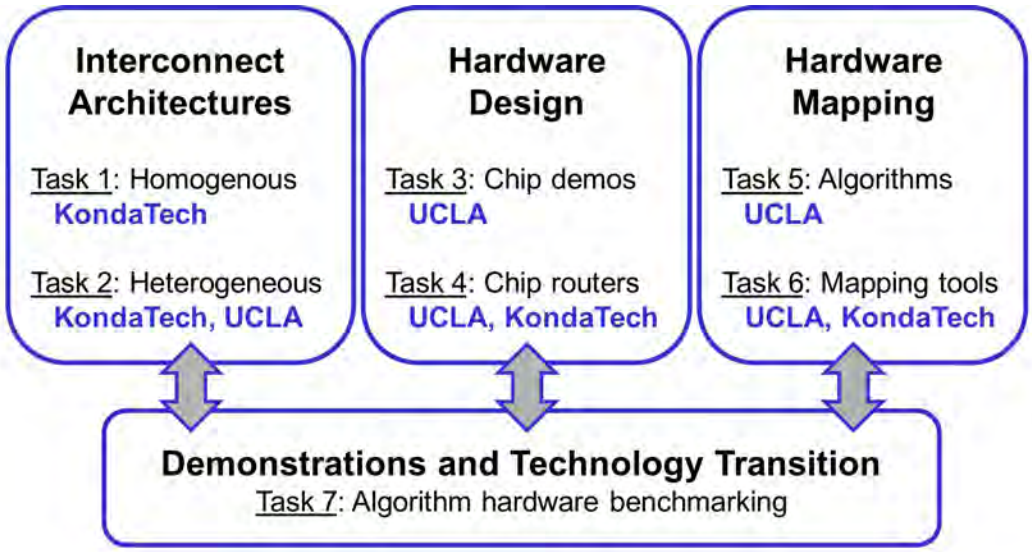
[8b] VLSI Layouts of Fully Connected Generalized Networks
- US Patent Application Number: 12/601,275
- Date Filed: November 22, 2009

[9] VLSI Layouts of Fully Connected Generalized Networks with Locality Exploitation
- US Provisional Patent Application Number: 61/252, 603
- Date Filed: October 16, 2009

[10] VLSI Layouts of Fully Connected Generalized and Pyramid Networks
- US Provisional Patent Application Number: 61/252, 609
- Date Filed: October 16, 2009

### 2.7. Management Plan

Program management plan is shown in the figure below.




UCLA and KondaTech will closely work together to provide demonstrations and technology transfer to the DoD community. Below is a description of various tasks and their interaction.

**Routing Architectures:** KondaTech will be responsible for the development of interconnect architectures and supporting routing tools. This includes both homogeneous-block (Task 1) and heterogeneous-blocks (Task 2) architectures. UCLA will provide information about building blocks (e.g., LUT, DSP, memory) for Task 2. The developed architectures and routing tools will be benchmarked using standard Toronto20 FPGA benchmarks.

UCLA will be responsible for hardware design and hardware mapping efforts.

**Hardware Design:** Chip demonstrations (Task 3) will be initially made using theoretical routing architecture concepts developed at KondaTech. In this phase, we will investigate types of chip routing procedures that need to be automated during chip design. Custom routing of low-level interconnects will be enabled by the regularity of the interconnect architecture. KondaTech will provide input into automated chip routers (Task 4) to ensure that routing tools are properly transferred to chip design. We will then make use of the chip routers for the final chip design.

**Hardware Mapping:** UCLA will lead the hardware mapping effort, which goes in conjunction with chip design. Here, we will focus on developing algorithms (Task 5) that would optimally map algorithms to the newly developed interconnect architectures. We also have the capability to do wordlength optimization and high-level architecture transformations prior to mapping. The algorithm mapping will attempt to minimize resource utilization and power, and also maximize performance. The details of the mapping algorithms will be abstracted away from the user by developing mapping tools (Task 7) to provide automated algorithm mapping onto hardware.

**Demonstrations and Technology Transition:** We will demonstrate the execution of complete algorithms in order to validate power and performance gains of our technology. We will actively solicit and welcome inputs from the DOD community about the algorithmic examples that would best serve the demonstration of hardware and mapping tools.

**Demonstration Platform:** We will work with **BEEcube** to execute initial technology transition plan. BEEcube is now a well recognized provider of high-performance processing technology. The technology is based on FPGA hardware, a library of IP cores, and software development tools for high-performance computing and other applications. We will use BEEcube technology for our chip demonstrations. In particular, we will make use of the FMC expansion modules on their hardware platforms to control our chips. This includes programming of the chips and program execution. The 160-pin connection slots based on VITA Standard 57.1 provide BEE-to-chip interface. With this setup, we will be able to boost the performance of the existing hardware and quantify the benefits of our technology in actual computing environment. We will use four hardware units from BEEcube and setup inter-module communication in order to demonstrate scalability of our design (as described in Section 2.4).

**Team size and composition:**

*UCLA team:*
Dejan Markovic, PI
Four full-time graduate students to work on hardware design (Tasks 3 and 4), hardware mapping (Tasks 5 and 6), and technology demonstrations. They will also collaborate with Dr. Konda on Task 2. Each task will require the effort of two full-time students.

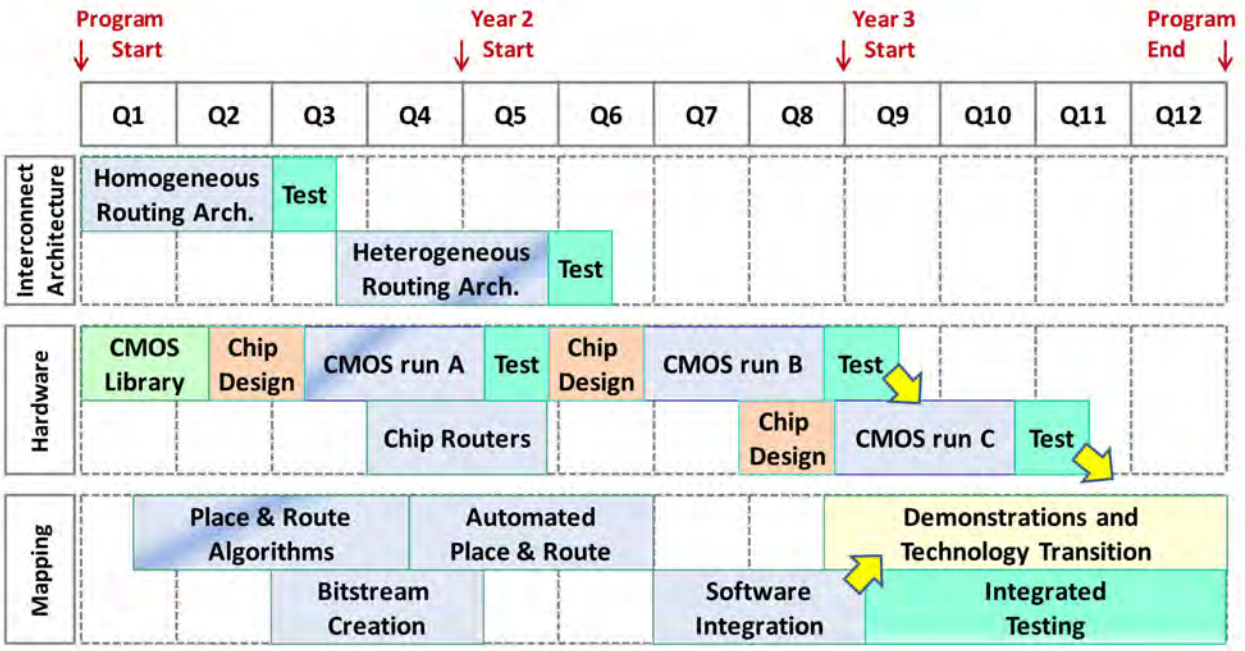
*KondaTech:*
Venkat Konda, Consultant

UCLA and KondaTech will work closely to maximize the impact of our technology.

### 2.8. Schedule and Milestones

Project schedule, task description, and management plan are described in this section.

#### 2.8.1. Schedule Graphic




Key deliverables from the program will include (*due dates are referenced to the program start*):

(1) Layout library of FPGA building blocks in IBM's 32nm SOI technology (available through the DARPA LEAP program). *Due: after 4 months.*

(2) Routing architectures for homogeneous blocks (e.g. LUTs) with varying degree of connectivity. Deliverable: software benchmarking results. *Due: after 8 months.*

(3) Routing architectures for heterogeneous blocks (LUTs, DSP slices, BRAMs, other IP) with varying degree of connectivity. Deliverable: software benchmarking results. *Due: after 17 months.*

(4) Test results from CMOS run A to demonstrate small-scale integration (< 5k LUTs). Deliverable: hardware measurements. *Due: after 15 months.*

(5) Test results from CMOS run B to demonstrate medium-scale integration (< 10k LUTs). Deliverable: hardware measurements. *Due: after 26 months.*

(6) Test results from CMOS run C to demonstrate large-scale integration (< 20k LUTs). Deliverable: hardware measurements. *Due: after 32 months.*

(7) Tools for generating a bitstream for a mapped design. *Due: after 12 months.*

(8) Tools for performing place-and-route of the optimized netlist for FPGA programming. *Due: after 15 months.*

(9) Tools for integrating place-and-route tool with existing testing solutions. *Due: after 24 months.*

(10) Hardware and tool flow demonstrations for relevant DOD algorithms; commercialization of technology. *Due: after 36 months.*

### 2.8.2. Detailed Task Description

**Part I: Network Architectures and Routing Tools**
We will next work on homogeneous and heterogeneous networks featuring arbitrary level of connectivity. The decision about the connectivity level will be aided with feedback from the mapping tools (Task 6) in order to minimize hardware utilization.

**Task 1: Routing Architectures for Homogeneous Blocks**
Routing tool will be developed for the FPGA with homogeneous blocks. Routing algorithms need to be developed for uni-terminal nets and multi-terminal nets. The hierarchical routing network may be a symmetric network where the number of inputs and the number of outputs are the same. The routing network may also be asymmetric network where the number of inputs and the number of outputs are not the same. Rearrangeably nonblocking and strictly nonblocking multi-terminal net algorithms will be implemented to demonstrate the routability and the speed of routing. Routing algorithms need to be implemented for configurations of Konda hierarchical network where some of the stages in the network may be partially connected and the other stages are fully connected. The LUT size of the network may be a perfect power of two or non-perfect power of two.

**Task 2: Routing Architectures for Heterogeneous Blocks**
The key architectural challenge is to adapt the Konda hierarchical network for FPGA architecture. A fully connected hierarchical network is an over-kill for FPGA applications. Our goal is to converge on the appropriate design of the routing network in three phases and also adopt it to many different applications end-user applications. We will experiment with many varieties of hierarchical network designs. One aspect is to analyze the locality typical in FPGA designs and optimizing or adopting Konda hierarchical network with optimum bandwidth for local connectivity and global connectivity. The typical LUT size that is known to be optimal in a 2D-Mesh routing network may not be optimal for Konda hierarchical network. This is because Konda hierarchical network provides richer connectivity with smaller switch and less number of tracks. Determining the appropriate length of the tracks is another aspect that will be addressed.

**Part II: Hardware Design**
To fully demonstrate the benefits of the proposed interconnect architectures and routing tools, we will implement the network architectures on a series of chips. Hardware design tasks will concentrate on achieving two goals: 1) hardware demonstration of power, area, and performance benefits, 2) development of automated chip routers to facilitate technology transition.

**Task 3: Chip Demonstrations**
In CMOS run A, we will test the use of library IP for the integration of medium-scale FPGA processor (5K LUTs). This chip is 10x larger than the IBM-90 and will allow us to confidently explore mapping algorithms for this level of design complexity.

In CMOS run B (see Sec 2.8.1), we will design a chip with 15K DSP slices. The chip will be tested using BEE4 module (coming out in Fall 2010) from BEEcube. Such setup will allow us to do side-by-side comparison with Virtex-6 Xilinx FPGAs. We will work with BEEcube on HPC application benchmarking and will also welcome inputs from the DOD community.

In CMOS run C (see Sec. 2.8.1), we will demonstrate LUT/DSP/BRAM based design with over 15K LUTs, over 15K DSP slices, and adequate BRAM memory. The chips from CMOS run C will be also used for inter-module communication with multiple BEE4 boards to show expandability to large HPC benchmarks.

**Task 4: Automated Chip Routing Tools**
To facilitate the integration of medium- and large-scale FPGA chips, and to enhance our technology transition capabilities, we will work on automated chip routing tools. The tools are intended to automate custom design strategies developed in our prior work. We will also automate design techniques further developed under Task 3, particularly CMOS runs A and B.

**Part III: Hardware Mapping**
For an FPGA to be effectively used by its consumers, an automated mapping tool must be provided as well. The mapping and place-and-route software is a crucial component of this project, and major efforts ought to be allocated to provide an efficient tool.

**Task 5: Place and Route Algorithms and Tools**
Finding a suitable placement for each logic gate can greatly affect the performance of the final design, and poses a significant challenge to the tool. The placement process is divided into coarse placement, which determines the gate partition, and fine placement, which determines the exact gate location in each partition. Gate partition takes place first, and the goal is to partition the gates into quadrants to minimize cross-partition interconnects. This process can be modeled by an optimization problem.

Since the routing resources in FPGA are limited, routing should occur at the same time as placement. In cases where more than one possible routes exists, each routing candidate should be evaluated for interconnect length, and the shortest interconnect is chosen. We will hierarchically extend the partition and place-and-route within an automated flow.

**Task 6: Tools for Hardware Mapping**
The final step of the place-and-route process is the output the design. This step creates the exact bit sequence required to program the scan chain on the FPGA, which configures all the LUTs and interconnects to execute the programmed function. We will make the mapping tool compliant with existing FPGA design environments such as Xilinx XSG/EDK toolset.

**Task 7: Demonstrations and Technology Transfer**
We will use chips from CMOS runs B and C to demonstrate the benefits of our hardware as compared to Xilinx Virtex-6 chips by using the BEE4 module from BEEcube as a test platform for HPC benchmarking. A custom PCB board with our FPGA will comply to the FMC interface specifications. BEE4 FPGA chips will be used to execute computations on our custom chips. This setup will also allow side-by-side benchmarking of Virtex-6 FPGAs and our chips. To further demonstrate inter-module communication and scalability to larger systems, we will connect 4 BEE4/Chip modules in an evaluation platform.

### 2.8.3. Project Management and Interaction Plan

UCLA and KondaTech will closely interact during the program. Our interaction plan consists of several means of communication:

- We will conduct weekly teleconference meetings using desktop sharing software
- Due to geographic proximity, Dr. Konda will visit UCLA once a month to meet with UCLA team and conduct detailed discussions about the project
- The PI will additionally interact with Dr. Konda regarding project management

Project management is illustrated in Section 2.7 and also summarized in Table 7.

**Table 7:** Task Interaction between the PI and Dr. Konda.

| Person / Task | Task 1 | Task 2 | Task 3 | Task 4 | Task 5 | Task 6 | Task 7 |
|---|---|---|---|---|---|---|---|
| D. Markovic | | + | + | + | + | + | + |
| V. Konda | + | + | | + | | + | + |

KondaTech (V. Konda) will be responsible for the development of interconnect architectures (Tasks 1 and 2). UCLA will provide information about building blocks (e.g., LUT, DSP, memory) for Task 2 and assist in verification of interconnect architectures.

UCLA (D. Markovic) will be responsible for hardware design and hardware mapping efforts (Tasks 3 to 6). KondaTech will assist in automating chip routers (Task 4) to ensure integration of the interconnect architectures from Tasks 1 and 2. The expertise of KondaTech will also be used to transition mapping software to commercial tool environments.

UCLA and KondaTech will work together on HPC demonstrations described in Section 2.4.

### 2.9. Personnel, Qualifications, and Commitments

**Dejan Markovic** is an Assistant Professor of Electrical Engineering at the University of California, Los Angeles. He completed the Ph.D. degree in 2006 at the University of California, Berkeley. His current research is focused on integrated circuits for emerging radio and healthcare systems, design with post-CMOS devices, optimization methods and CAD flows.

Prof. Markovic's research accomplishments include sensitivity-based circuit optimization [6] and DSP architecture optimization [11] for reduced power and area. As a demonstration of these concepts, his group has designed a number of complex digital chips for parallel data processing. Representative chips shown in Fig. 21 show performance range by 5 orders of magnitude (kHz to multi-GHz) and power density range of 3 orders of magnitude ($\mu W/mm^2$ to $mW/mm^2$).

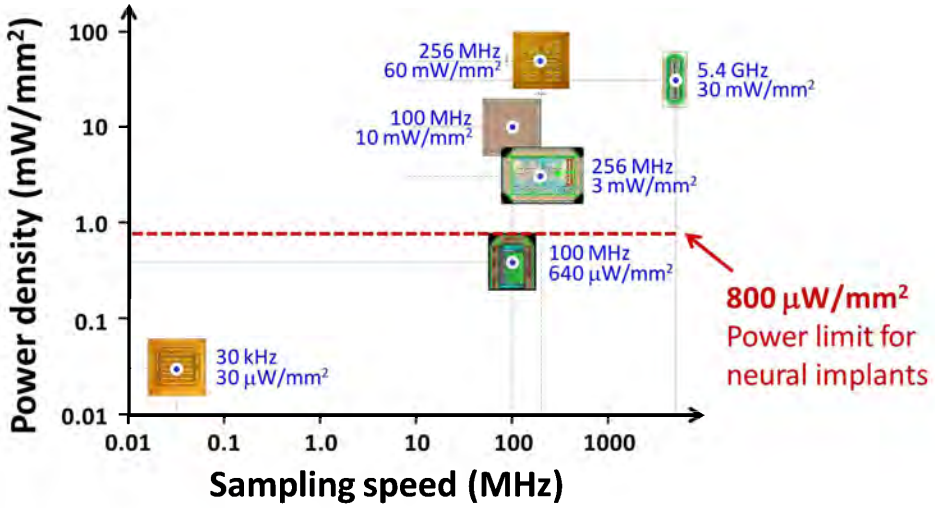



**Figure 21:** Sample chips designed by PI's group showing broad range in performance and ultra-low power density.

The PI's research in low power has been recognized by multiple awards:

- **2007 David J. Sakrison Memorial Prize** (Best Ph.D. Dissertation at UC Berkeley), awarded to the PI for his contributions to low-power digital circuit design.
- **2008 Outstanding MS Thesis Award**, UCLA EE Dept, received by R. Nanda, for her M.S. Thesis titled: "DSP Architecture Optimization in Matlab/Simulink Environment," June 2008.
- **2010 Outstanding MS Thesis Award**, UCLA EE Dept, received by V. Karkare, for his M.S. Thesis titled: "A 130 uW, 64-Channel, Spike-Sorting DSP Chip," Dec. 2009.
- **2010 DAC/ISSCC Student Design Contest Winner**, awarded to Chia-Hsiang Yang for his paper titled "A 2.89mW 50GOPS 16x16 16-Core MIMO Sphere Decoder."

PI's group has unparalleled infrastructure for the design and optimization of digital chips, based on a number of tools developed and maintained over the past decade. PI's key publications in the area of low-power design are provided in [2-16].

**Venkat Konda** is an inventor, experienced entrepreneur and the CEO of Konda Technologies which he founded in 2007 based on a breakthrough layout using only horizontal and vertical tracks for Benes/BFT hierarchical networks, seminal rearrangeably and strictly non-blocking multicast routing algorithms with an architecture optimum with switch cost, power and performance. Venkat is currently in the process of commercializing the IP in FPGA interconnects, System-on-Chip interconnects and warehouse-scale datacenter switches. Prior to it, Venkat invented seminal algorithms for rearrangeably and strictly non-blocking multicast routing algorithms for Clos Networks and founded a startup Teak Networks, to commercialize into packet switch fabrics which are also applicable to design cheaper optical cross connects. Venkat received PhD degree in Computer Science & Engineering from the University of Lousiville, KY in 1992, and M.S in Electrical Engineering from the Indian Institute of Technology, Kharagpur in 1988.

Table of individual time commitments is provided below:

| Key Individual | Project | Pending/Current | 2010 | 2011 | 2012 |
|---|---|---|---|---|---|
| **Dejan Markovic** | HEALICs | Current (Co-PI) | 176 hours | 176 hours | 176 hours |
| | STT-RAM | Current (Co-PI) | 176 hours | 176 hours | 176 hours |
| | NEMS | Current (Co-PI) | 176 hours | 176 hours | 176 hours |
| | NSF CAREER | Current (PI) | 88 hours | 88 hours | 88 hours |
| | C2S2 | Current (PI) | 88 hours | 88 hours | 88 hours |
| | NVL | Pending (Co-PI) | 176 hours | 176 hours | 176 hours |
| | FPGA | Proposed | 176 hours | 176 hours | 176 hours |
| **Venkat Konda** | FPGA | Proposed | 1000 hours | 1000 hours | 1000 hours |

*Note:* Dejan Markovic is a Co-PI on three DARPA projects, two of which can directly benefit to the OHPC program. Namely, STT-RAM can be used for the realization of FPGA memory blocks. Also, zero-leakage NEM relay switches can be used for effective realization of FPGA switch-matrix blocks. PI's commitment to the proposed work is already evidenced by self-initiated and self-supported work described in Sec 2.4.1. The OHPC program will, therefore, not add a significant workload to the PI.

**2.10. Organizational Conflict of Interest Affirmations and Disclosure**

None.

**2.11. Human Use**

None.

**2.12. Animal Use**

None.

### 2.13. Statement of Unique Capability Provided by Government or Government-funded Team Member

Not applicable.

**2.14. Government or Government-funded Team Member Eligibility**

None.

**2.15. Facilities**

The description of UCLA and KondaTech facilities is provided below.

**Dejan Markovic, PI**

*Office:* UCLA Engineering IV Building, Room 56-147E (approx. 140 sq. ft).

*Graduate student offices:* UCLA Engineering department allocates the required office space for graduate students from a common pool. The PI has 14 graduate students.

*Computing resources:* The PI and his students have access to a 10-node high-performance linux-based compute cluster, 4 windows-based remote desktop servers. Hardware resources are complemented with software tools for chip design (Cadence, Synopsys, Mentor), algorithm design (Matlab, Simulink), and FPGA prototyping tools (Xilinx, Synplicity).

*Laboratory space:* The PI has access to several labs equipped with chip instrumentation for the testing of digital circuits. He is primarily using Integrated Circuits and Systems Lab (ICSL) at UCLA EE department. The equipment includes signal generators, spectrum analyzers, logic analyzers, high-speed oscilloscopes, and a high-speed probe station.

**Venkat Konda, Consultant**

*Office:* Konda Technologies, 6278, Grand Oak Way, San Jose, CA (approx. 100 sq. ft).

*Computing resources:* Dr. Konda has a server with two quad-core AMD Athlon 64x2 processors and fedora Linux operating system, two windows-based desktop/laptop machines.

No Government Furnished Property is required for conduct of the proposed research.

**Referenes**


[1] [Online], available: http://www.eecg.toronto.edu/~vaughn/challenge/challenge.html

[2] D. Marković, C. C. Wang, L. Alarcon, T.-T. Liu, and J. M. Rabaey, "Ultralow-Power Design in Near-Threshold Region," Proceedings of the IEEE, vol. 98, no. 2, pp. 237-252, Feb. 2010.

[3] C.-H. Yang and D. Marković, "A Flexible DSP Architecture for MIMO Sphere Decoding," IEEE Trans. Circuits & Systems I, vol. 56, no. 10, pp. 2301-2314, Oct. 2009.

[4] V. Wang, K. Agarwal, S.R. Nassif, K.J. Nowka, and D. Marković, "A Simplified Design Model for Random Process Variability," IEEE Trans. Semiconductor Manufacturing, vol. 22, no. 1, pp. 12-21, Feb. 2009.

[5] D. Marković, B. Nikolić, and R.W. Brodersen, "Power and Area Minimization for Multidimensional Signal Processing," IEEE Journal of Solid-State Circuits, vol. 42, no. 4, pp. 922-934, Apr. 2007.

[6] D. Marković, V. Stojanović, B. Nikolić, M.A. Horowitz, and R.W. Brodersen, "Methods for true energy-performance optimization," IEEE Journal of Solid-State Circuits, vol. 39, no. 8, pp. 1282-93, Aug. 2004.

[7] F. Chen, et al., "Demonstration of Integrated Micro-Electro-Mechanical Switch Circuits for VLSI Applications," in Proc. IEEE Int. Solid-State Conference (ISSCC'10), Feb. 2010, pp. 26-27.

[8] V. Karkare, S. Gibson, and D. Marković, "A 130-uW, 64-Channel Spike-Sorting DSP Chip," in Proc. IEEE Asian Solid-State Circuits Conference (A-SSCC'09), Nov. 2009, pp. 289-292.

[9] C.-H. Yang and D. Marković, "A 2.89mW 50GOPS 16×16 16-Core MIMO Sphere Decoder in 90nm CMOS," in Proc. IEEE European Solid-State Circuits Conference (ESSCIRC'09), Sep. 2009, pp. 344-348.

[10] F. Chen, H. Kam, D. Markovic, T.-J. King Liu, V. Stojanovic, and E. Alon, "Integrated Circuit Design with NEM Relays," in Proc. Int. Conf. on Computer Aided Design (ICCAD'08), Nov. 2008, pp. 750-757.

[11] R. Nanda, C.-H. Yang, and D. Markovic, "DSP Architecture Optimization in Matlab/Simulink Environment," in Proc. Int. Symp. on VLSI Circuits (VLSI'08), June 2008, pp. 192-193.

[12] D. Markovic, C. Cheng, B. Richards, H. So, B. Nikolic, and R.W. Brodersen, "ASIC Design and Verification in an FPGA Environment," in Proc. Custom Integrated Circuits Conference (CICC), Sep. 2007.

[13] D. Markovic, B. Richards, and R.W. Brodersen, "Technology Driven DSP Architecture Optimization within a High-Level Block Diagram Based Design Flow," in Proc. 40th Asilomar Conf. on Signals, Systems and Computers, Nov. 2006. (Invited)

[14] D. Markovic, B. Nikolic, and R.W. Brodersen, "A 70 GOPS Multi-Carrier MIMO Chip in 3.5mm2 and 34mW," in Proc. IEEE Int. Symposium on VLSI Circuits (VLSI), June 2006, pp. 196-197.

[15] R. W. Brodersen, M.A. Horowitz, D. Markovic, B. Nikolic, and V. Stojanovic, "Methods for true power minimization," in Proc. Int'l Conf. on Computer Aided Design (ICCAD), Nov. 2002, pp. 35-42. (Invited)

[16] V. Stojanovic, D. Markovic, B. Nikolic, M.A. Horowitz, and R.W. Brodersen, "Energy-delay tradeoffs in combinational logic using gate sizing and supply voltage optimization," in Proc. 28th European Solid-State Circuits Conference (ESSCIRC), Sept. 2002, pp. 211-14.

39465 Paseo Padre Parkway
Suite 3700
Fremont, CA 94538
510.252.1136 (P)
888.700.8917 (F)

August 3, 2010

Dr. William Harrod
DARPA TCTO

Dear Dr. Harrod:

I have reviewed the proposal entitled "Energy-Efficient Butterfly FPGA Hardware and Programming Tools," to be submitted by Dejan Markovic and his colleagues to DARPA TCTO.

I find this work of significant value to the development of our future HPC products and am interested to have my engineers interact with UCLA team during the course of this project to ensure that the final outcome can be smoothly transferred to a product.

I look forward to working with Dejan Markovic and his colleagues on this research.

Sincerely,

Dr. Chen Chang
Founder, CEO
BEEcube, Inc.
39465 Paseo Padre Parkway Suite 3700
Fremont, CA 94538
Phone: (510) 252-1136

# EXHIBIT 16


# DARPA Guide to Broad Agency Announcements and Research Announcements

## November 2016

Office ADPM when there have been material changes to the content of the briefing. Any Review Team Member who does not attend the ethics briefing will be required to document and self-certify the date of his or her last ethics briefing in the COI Self-Certification form.

Prior to proposal review, all Review Team Members shall be required to complete and submit a written self-certification, for the record, to document any known or apparent COIs or stating that they have none relevant to reviewing BAA proposals, as well as any other requirements regarding information access during the Scientific Review Process. Review Team Members complete this form after receipt of proposals. The Technical Office will retain the self-certification forms as part of the documentation in accordance with paragraph 2.E. below. The briefing charts and the self-certification form are available on the DARPA portal on the GC home page.

The PM is responsible for ensuring that each Review Team Member has access to or receives a copy of both the briefing charts and the self-certification form. After verifying that each member of the Review Team has sufficiently completed the self-certifications forms, the PM will review the forms with the CO and GC regarding potential COIs and appearance issues in the self-certifications, as necessary. The PM will brief all support contractor personnel having access to the proposals and ensure that no support contractor personnel have any COIs. Support contractor personnel with COIs participating in the Scientific Review Process must work out their participation in the process with GC, the CO, and the PM. The PM must also ensure that support contractor personnel have a nondisclosure agreement on file signed when they began their duties with DARPA. The PM shall remind them of the restrictions and requirements that are contained in that agreement as they relate to the handling and review of proposal material in accordance with section 2.E. below. A sample of a nondisclosure agreement is available in DI 70, "Contractor Relationships: Inherently Governmental Functions, Prohibited Personal Services, and Organizational Conflicts of Interest."

2.F.2. Scientific Review Training. The CO will attend the Scientific Review Team Kick-off Meeting and provide training on how to sufficiently document proposal reviews.

2.G. Protection of Sensitive Data. All participants in the Scientific Review Process (including SMEs and SETAs) are prohibited from, unless permitted by law, knowingly disclosing contractor bid, or proposal information, or source selection information in accordance with FAR 2.101, and the Procurement Integrity Act, 41 U.S.C. §§ 2101-2107 (implemented in FAR 3.104). Unauthorized disclosure of proprietary or confidential information, either before or after the award, is prohibited by the Trade Secrets Act, 18 U.S.C. § 1905, the Privacy Act, 5 U.S.C. § 552a, and by other laws and regulations. Prior written authorization from DIRO, or the CO must be obtained prior to releasing protected information outside the Scientific Review Team. The requirement for prior written authorization does not apply to the personnel associated with standard operational support activities such as preparing/processing/reviewing funding requests for selected proposals by Financial/Comptroller personnel, or archiving solicitation documentation on the Agency server or SharePoint sites by information technology or SETA support personnel.

The PM shall monitor and maintain all source selection information (as defined by FAR 2.101) within a secured physical and network area. This includes ensuring that information

# EXHIBIT 17

Gmail

**Venkat Konda <venkat@kondatech.com>**

# Re: Closed licensing deal with QuickLogic

**Dejan Markovic** <dejan@ee.ucla.edu> Sun, Oct 10, 2010 at 6:38 PM
To: Venkat Konda <venkat@kondatech.com>

Venkat,

Congratulations! This looks like a great opportunity. I notice they are doing lots of end products and less of chip design - is that true? Anyhow, it seems like a very nice place - I am really happy for you.

We should hear from DARPA by the end of the month hopefully - will be in touch.

Best regards,
Dejan

On Fri, Oct 8, 2010 at 4:37 PM, Venkat Konda <venkat@kondatech.com> wrote:

> Dejan,
>
> Hope you are doing well!
>
> I am happy to announce that I have closed a non-exclusive licensing (of Konda FPGA routing network) deal with QuickLogic (they make programmable ASICs, previously they were an FPGA company).
>
> I already have started working with QuickLogic (www.quicklogic.com) transferring the technology into their products.
>
> I want to share this great news with you!
>
> Regards,
>
> Venkat

# EXHIBIT 18

Gmail

Venkat Konda <venkat@kondatech.com>

# Re: FPGA technology - licensing

**Dejan Markovic** <dejan@ee.ucla.edu> Thu, Jan 13, 2011 at 8:12 AM
To: Lorenzo CALI <lorenzo.cali@st.com>
Cc: Venkat Konda <venkat@kondatech.com>, Pierluigi ROLANDI <pierluigi.rolandi@st.com>

Hi Lorenzo,

Tue 8am PDT works for me.

Venkat, the number to dial is:

* (866) 505-6908
* Code: 5544069

Dejan

On Thu, Jan 13, 2011 at 1:27 AM, Lorenzo CALI <lorenzo.cali@st.com> wrote:
> Hi Dejan, Venkat,
>
> Is ok for you if we move this call to next Tuesday Jan.18th at 5pm CET / 8am PDT ?
> Today is not working for us.
>
> Thanks,
> Lorenzo
>
>
> -----Original Message-----
> From: Venkat Konda [mailto:venkat@kondatech.com]
> Sent: Wednesday, January 12, 2011 7:29 AM
> To: 'Dejan Markovic'; Lorenzo CALI; Pierluigi ROLANDI
> Cc: venkat@kondatech.com
> Subject: RE: FPGA technology - licensing
>
> Dejan,
> Appreciate very much for the introduction to ST Micro.
>
> Pigi, Lorenzo:
> I am excited to get introduced to you electronically.
> Still in jet lag as I landed in San Francisco this afternoon.
> Have successfully transferred Konda Hierarchical routing technology to
> QuickLogic in the last 3 months.
> Look forward to the conference call.
>
> Regards,
> Venkat
>
> Venkat Konda, PhD
> Founder/CEO
> Konda Technologies Inc.
> 6278 Grand Oak Way
> San Jose, CA 95135
> Cell # 408-472-3273
> E-mail: venkat@kondatech.com
>
>
> -----Original Message-----
> From: dejan.ucla@gmail.com [mailto:dejan.ucla@gmail.com] On Behalf Of Dejan

> Markovic
> Sent: Tuesday, January 11, 2011 9:58 AM
> To: Lorenzo CALI'; Pier Luigi ROLANDI; Venkat Konda
> Subject: FPGA technology - licensing
>
> Pigi, Lorenzo,
>
> I just talked to Venkat - he just landed coming back from India where he
> licensed and successfully transferred the technology to QuickLogic.
> He would be happy to talk to ST about similar arrangements.
>
> To get the ball rolling, we can all get together on a telecon where we can
> make introductions and plan ahead.
>
> We have regular telecon Thu 8am PST, perhaps we can try 7:30am PST (4:30pm
> your time)?
>
> Best regards,
> Dejan
>
>

# EXHIBIT 19

2011 VLSI CIRCUITS SYMPOSIUM KYOTO

## *SECOND ANNOUNCEMENT AND CALL FOR PAPERS*

Sponsored by
Japan Society of Applied Physics and IEEE Solid-State Circuits Society
In Cooperation with Institute of Electronics, Information and Communication Engineers
and IEEE Electron Devices Society

# 2011 SYMPOSIUM ON VLSI CIRCUITS

**Rihga Royal Hotel Kyoto, Kyoto, Japan**
**Wednesday - Friday, June 14 - 17, 2011**
**(June 14 Short Course, June 15 – 17 Technical Sessions)**

*Chair:*
Masayuki Mizuno
Renesas Electronics Corp.
1753 Shimonumabe Nakahara-ku
Kawasaki-city
Kanagawa 211-8668 Japan
Tel: +81-44-435-5445
Fax:

*Co-Chair:*
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*Secretary/Publications:*
Hideyuki Kabuo (Japan)
Panasonic Corp.

*Publicity:*
Makoto Takamiya (Japan)
The University of Tokyo

*Treasurers:*
Ren-ichi Yamada (Japan)
Hitachi Ltd.

David Scott (USA)
TSMC Technologies, Inc.

*Local Arrangements:*
Masao Ito (Japan)
Renesas Electronics Corp.

*Short Course Organizer:*
Kazuhiko Kajigaya (Japan)
Elpida Memory, Inc.

The 2011 Symposium on VLSI Circuits will continue to provide integrated-circuit designers an opportunity to meet and present their important new works in all aspects of VLSI circuits in the successful atmosphere established at previous meetings. The **VLSI Circuits Symposium** and the **VLSI Technology Symposium (see the reverse side)** will overlap for two days to allow more *opportunities for participants to interact and synergize on topics of mutual interest related to technology scaling, embedded memories, power reduction, and design-for-manufacturing (DFM).*

**The scope of the Symposium on VLSI Circuits includes innovative techniques in the following areas:**

- Systems and circuits for wireless communications
- Digitally-assisted and digitally-implemented RF/analog circuits and systems
- Circuit designs to address challenges of scaled CMOS technologies - e.g. DFM, variability, reliability
- Complex SoC systems describing new architectures and implementations including behavioral modeling
- Frequency generation and clock distribution
- Digital circuit techniques
- Memory circuits; especially for embedded memories in scaled technologies
- Analog and mixed signal circuits such as data converters, PLL and amplifiers
- Power management circuits, including linear and switching voltage regulators and voltage references
- Circuits related to energy harvesting, battery management and renewable energy topics
- Wireline transceivers and I/O design spanning from on-chip, chip-to-chip and long-reach applications
- Circuits and systems for sensors and displays, including those for biomedical and healthcare applications
- Circuits utilizing emerging device technologies

Papers will be considered on the basis of originality, innovation and advancing the field. Prototype implementation and measured results will be considered favorably in the ratings.

### SUBMISSION OF PAPERS

Prospective authors must submit camera-ready papers in the format of two pages to the following web site:

**http://www.vlsisymposium.org**

The hard copy submission will not be accepted. The papers should be submitted in final form and, if accepted, will be published as submitted. The technical content beyond the abstract of the accepted paper must not be announced, published, or in any way put in the public domain prior to the Symposium. Submissions from industry and universities are both encouraged. Partial travel expense support for students who are presenting papers is available upon request.

### BEST STUDENT PAPER AWARD

The selection will be based upon the quality of the paper and the presentation. The student who receives the Best Student Paper Award will be presented a monetary award and a certificate at the opening session of the 2012 Symposium. The student must be enrolled as a full-time student at the time of submission, be the leading author and the presenter of the paper, and must indicate in the web submission form that this is a student paper to be considered for this award.

**Paper Submission Deadline is 17:00 (JST), January 24, 2011**

### VLSI CIRCUITS SHORT COURSE

The one-day short course will be held on June 14, 2011. Details will be given in the VLSI Circuits Symposium Advance Program, which will be posted on the web by the middle of April, 2011.

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# EXHIBIT 20

13-3

# A 1.1 GOPS/mW FPGA Chip with Hierarchical Interconnect Fabric

Cheng C. Wang, Fang-Li Yuan, Henry Chen, Dejan Marković

Electrical Engineering Department, University of California, Los Angeles, CA

**Abstract**

A 2048 look-up-table FPGA with a radix-2 hierarchical interconnect network is realized in 3.94mm$^2$ in 65-nm CMOS. It has an interconnect-to-logic area ratio of 1:1, which is a 3–4x reduction from modern FPGAs while allowing up to 100% resource utilization. As a proof of concept, it is designed with standard cells, achieving 16.4 GOPS/mm$^2$ at 370MHz. Peak energy efficiency of 1.1 GOPS/mW is measured at 0.5V.

## Introduction

Field-programmable gate arrays (FPGAs) are effective for rapid verification and prototyping of VLSI designs. They are also used in products that require periodic hardware changes and short time to market. However, FPGAs incur penalties in area (17–54x), speed (2.5–6.7x), and power (5.7–62x) over standard-cell ASICs [1], hindering their expansion into ASIC markets. The overhead is primarily due to interconnects, which account for over 75% of area and delay.

For over 20 years, FPGAs have used 2D-mesh interconnects, where look-up tables (LUTs) are placed in configurable logic blocks (CLBs), and arrays of switch boxes are placed at interconnect crossings (Fig. 1). Since a full array requires too much area, various heuristics are used to simplify switch-box arrays at the cost of resource utilization. Yet 80% of the 1.1B transistors on Virtex-5 are used for interconnects [2]. This paper demonstrates an FPGA with hierarchical interconnects where interconnect area is 51%, a 3–4x reduction from commercial FPGAs while preserving connectivity. An energy efficiency of 1.1 GOPS/mW is the highest among reported FPGAs. The chip is tested up to 400MHz.

## Hierarchical Interconnect Architecture

The key issue with 2D-mesh is scalability; the number of switch boxes grows as $O(N^2)$ with the number of LUTs. Using Rent's rule, interconnect complexity is still $O(N^{1.75})$ for random logic, requiring FPGA size to scale much faster than Moore's Law. In the proposed hierarchical interconnect, a folded Beneš network is employed to reduce the complexity to $O(N \cdot logN)$ [3]: 4 LUTs are connected via 2 stages of switch matrices (SMs), and another 4 LUTs are connected with a 3$^{rd}$ SM stage (Fig. 2a). Each SM has 4 unidirectional connections per direction. Although this architecture reduces interconnect complexity, each SM stage doubles the routing congestion. This $O(N)$ congestion makes physical design difficult.

To alleviate congestion, routing is alternated between x-y directions to reduce congestion to $O(N^{0.5})$ (Fig. 2b). At every hierarchy, the LUTs near the center are interconnected to create shorter routes, and the edge routes are longer. This gives routing tools options for faster paths on timing-critical routes.

The test chip has 2048 4-input LUTs: 1024 LUTs form 256 Logic CLBs, 896 LUTs form 224 DSP CLBs, and 128 LUTs form 16 Block RAMs (BRAMs) of 1kb each. In practice, the majority of the logic connections are local, requiring fewer connections on upper hierarchies. Therefore full connectivity is preserved up to 6 SM stages (Fig. 3a), then half-connectivity SMs are used to reduce the complexity of upper hierarchies. This partitions the interconnect into 3 sub-networks: $N_{8:2}$, $N_{6:2}$, and $N_{6:1}$. The chip is divided into 16 macros (Fig. 3b). Macros $N_{8:2}$ are centered for shorter top-level routing, branching into $N_{6:2}$ and $N_{6:1}$. Each of the macros contains 32 CLBs—a combination of Logic, DSP, and BRAM (Fig. 3c).

## Circuit Implementation

The CLBs include four 4-input LUTs with selectable asynchronous/synchronous output stages (Fig. 4a). Each LUT is configurable as one 4-input LUT or two 3-input LUTs with up to 4 unique inputs. A Logic CLB includes a carry chain to support 4b additions where Propagate and Generate are driven from LUTs. The Logic CLB is especially useful when two outputs per bit are required, such as in 3:2 compressors.

The DSP CLB (Fig. 4b) has a LUT combiner to support 5/6-input LUTs, and a carry chain that is configurable as one 8b or two 4b adders. The adder cells are shared with a 4b×4b Wallace-tree multiplier. Based on the configuration, the appropriate outputs are sent to the output stage. Due to the level of configurability, the synthesized CLB has 50 logic gates on its critical path (shaded), amounting to a 1.1ns delay.

Configuration bits are required to control CLBs and SMs, but traditional SRAM arrays are not suitable because all bits cannot be accessed simultaneously. A scan chain is adopted in [4] to control 6 CLBs, but it is not scalable to larger designs. Therefore an SRAM-based bit cell (BC) is designed where the output of each BC is directly routed to the configuration inputs of CLBs and SMs (Fig. 5a). The BC area is 5x smaller than a DFF-based scan cell. The bit-line (BL) and word-line (WL) controls are implemented as scan chains to write one row of BCs at a time. The BC arrays are local to each CLB, so only the BL and WL controls are propagated to top level. Overall, the memory area is reduced (Fig. 5b), and total interconnect area is 51%, a 3–4x reduction over 2D-mesh [5] for a fixed logic area.

## Automated Mapper

An automated mapper is developed to map RTL onto this FPGA. A standard-cell library of LUT functions is created to enable logic synthesis using commercial tools. The LUT netlist is imported into an automated, custom place-and-route tool that generates the bitstream for FPGA programming. This tool is also used during architecture design to evaluate interconnect connectivities by mapping Toronto20 benchmarks.

## Measurement Results

Our chip achieves 16.4 GOPS/mm$^2$ when all Logic and DSP CLBs are utilized, executing 175 16b accumulators at 370MHz. Since a 16b adder uses 2 DSP CLBs or 4 Logic CLBs, the DSP adders are faster, reaching 400MHz. Performance is hindered by equipment limitations due to a 0.25ns input-clock jitter at 400MHz. The energy-delay curve and the power breakdowns for minimum delay and minimum energy are shown in Fig. 6.

In comparison, [4] has no interconnects, the full-custom CLB in 32-nm LVT is 2.5x faster, but achieves 2.6 GOPS/mW at 0.34V for 8b operations, which is 0.65 GOPS/mW for 16b (2 CLBs per operation at half the speed). With interconnects, our 65-nm chip reaches 1.1 GOPS/mW at 0.5V.

Leakage is well-controlled even without power gating. A 1.08 GOPS/mW is attainable with only 112 DSP accumulators active and most of the Logic CLBs idle (Table I). The FIR filter achieves 274MHz due to longer routing, but interconnect delay is still under 50%. The 2×2 MIMO FFT uses 10 BRAMs to implement various delay lines. With many control signals and a critical path of 11 CLBs, the FFT achieves 83MHz.

Figure 7 shows the die photo. The top 3 metal layers (out of 9) are sparsely used, leaving ample room for larger designs.

**Acknowledgments**

We thank STMicroelectronics and C. Yang for helpful discussions.

**References**

[1] I. Kuon *et al.*, *Found. Trends in Elec. Design*, 2008.
[2] I. Bolsens, *MPSOC*, 2006.
[3] V. Konda, *U.S. Patent 2010/0172349*.
[4] A. Agarwal *et al.*, *ISSCC Dig. Tech. Papers*, 2010.
[5] M. Lin *et al.*, *FPGA '06*.

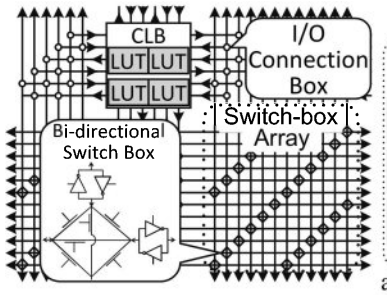



**Figure 1:** 2D-mesh interconnect.

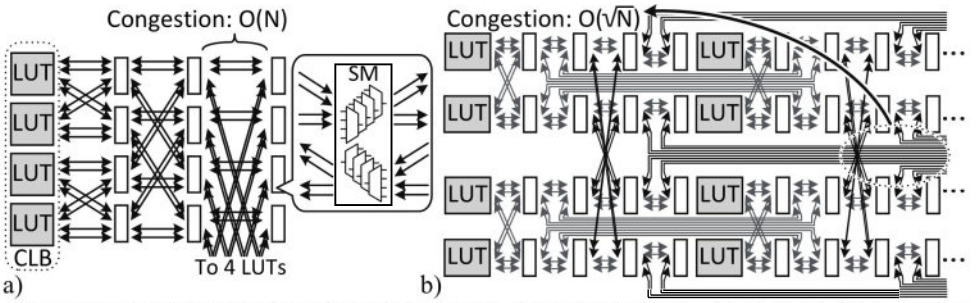



**Figure 2:** a) Hierarchical routing of 8 LUTs (4 shown) using SMs, b) alternated x-y routing.

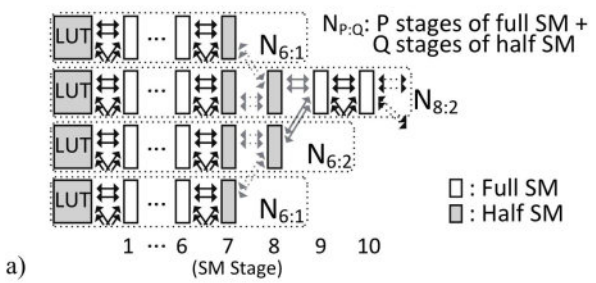



**Figure 3:** a) Interconnect architecture of 2048 LUTs, floorplan of b) SM network, c) CLB placement.

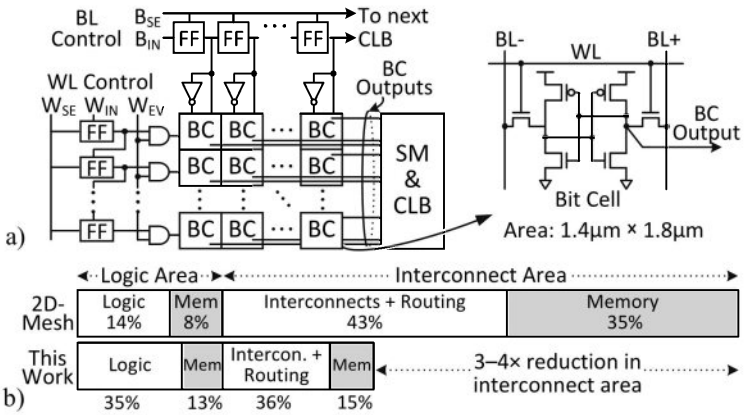



**Figure 5:** a) Bit cell (BC) configuration circuitry, b) area comparisons of 2D-mesh vs. this chip for a fixed logic area.

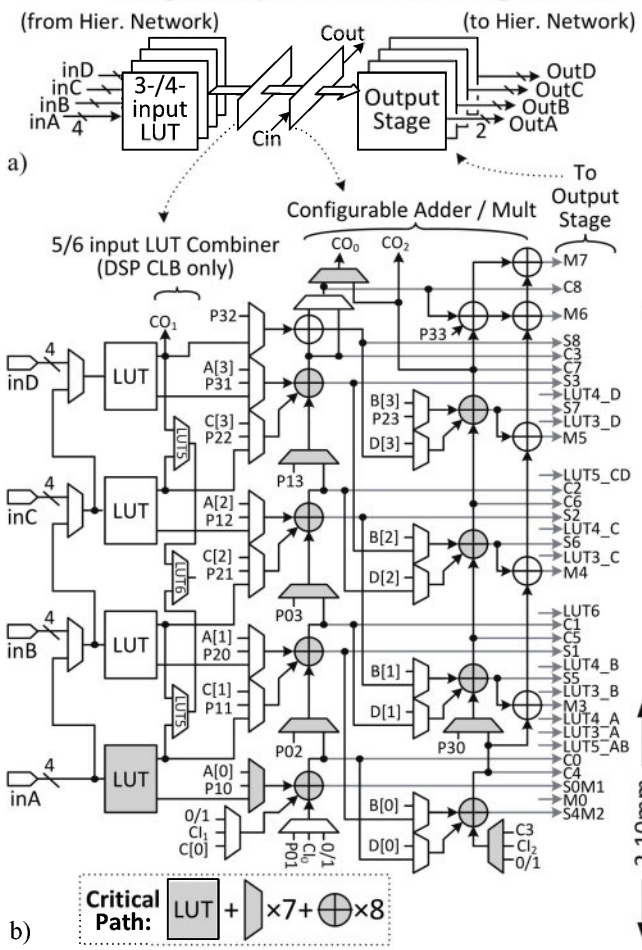



**Figure 4:** a) CLB block diagram and b) DSP CLB schematic.

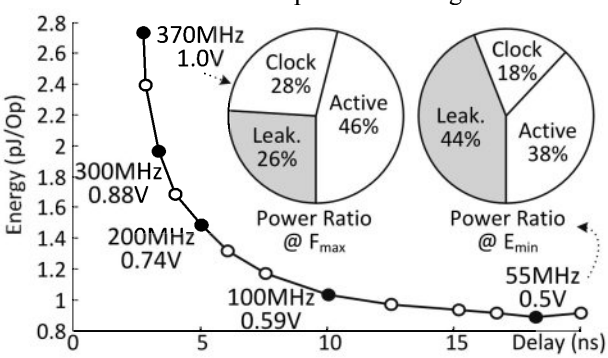
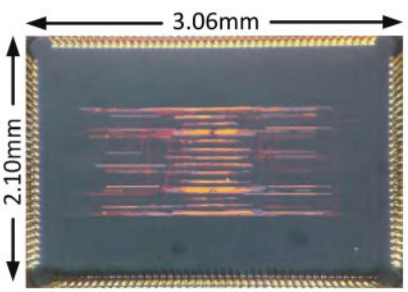



**Figure 6:** Energy-delay curve of the mapped 175 16b accumulator with power breakdown at $F_{max}$ and $E_{min}$ (insets).

**TABLE I:** MEASUREMENT RESULTS.

| Design \ Result | Resource Utilization | | | Performance | | | |
|---|---|---|---|---|---|---|---|
| | Logic (256) | DSP (224) | BRAM (16) | Power (mW) | $V_{DD}$ (V) | Freq. (MHz) | GOPS /mW |
| 175 Logic+DSP 16b Accum. | 256 | 224 | 0 | 179<br>8.6 | 1.0<br>0.50 | 370<br>55 | 0.36<br>1.13 |
| 112 DSP 16b Accum. | 4 | 224 | 0 | 123<br>6.2 | 1.0<br>0.51 | 400<br>60 | 0.57<br>1.08 |
| 32-tap 16b FIR Filter | 132 | 209 | 0 | 120<br>10.2 | 1.0<br>0.56 | 274<br>50 | 0.21<br>0.45 |
| 2×2 MIMO 64-point FFT | 196 | 93 | 10 | 82.7<br>26.5 | 1.0<br>0.78 | 83<br>40 | 0.05<br>0.07 |




| | |
|---|---|
| Technology | 65nm 1P9M CMOS |
| Core $V_{DD}$ | 0.34 to 1.0V |
| Frequency | 40 to 400MHz |
| I/Os | 75 bidirectional |
| Core Size | 2.52mm × 1.56mm |
| Gate Count | 2.73M |
| CLB Count | 256 Logic, 224 DSP |
| Block RAMs | 16 128×8b |
| Config. Bits | 297,472b |

**Figure 7:** Die micrograph and chip summary.

# EXHIBIT 21

Gmail

**Venkat Konda <venkat@kondatech.com>**

# Re: Greetings from Stanford | follow-up

**Venkat Konda** <vkonda@gmail.com> Thu, Apr 11, 2013 at 10:14 AM
To: Dejan Markovic <markovic@stanford.edu>
Cc: Venkat Konda <venkat@kondatech.com>

Hi Dejan,

Nice to hear from you. I am doing well.
Glad to know you are on sabbatical at Stanford now.
Sure we can meet at mutual convenience.

Regards,
Venkat

On Tue, Apr 9, 2013 at 5:56 PM, Dejan Markovic <markovic@stanford.edu> wrote:

> Hi Venkat,
>
> How have you been? I am at Stanford on sabbatical for one year and touching base. It would be great to catch up sometime over a coffee or lunch/dinner. Let me know when you are available.
>
> Thanks,
> Dejan

# EXHIBIT 22

ABSTRACT OF THE DISSERTATION

# Building Efficient, Reconfigurable Hardware using Hierarchical Interconnects

by

Chengcheng Wang

Doctor of Philosophy in Electrical Engineering

University of California, Los Angeles, 2013

Professor Dejan Marković, Chair

In the semiconductor industry today, ASICs are able to offer 10x-1000x higher energy and area efficiencies than non-dedicated chips, such as programmable DSP processers, field-programmable gate arrays (FPGAs), and microprocessors. Not surprisingly, SoCs today have become an integration of many ASIC blocks, each performing a few dedicated tasks. The growing size of modern SoC chips, accelerated by the increasing demands for functionalities, has exposed the major drawback of ASIC: design cost. These large SoCs are re-designed a few times a year to rectify hardware-bugs and to support new features. Because ASICs are not reconfigurable, even the smallest hardware change would require a re-design. Additionally, design cost is rising exponentially with every technology generation.

The rising design cost of ASICs has exposed a huge need today: efficiency and flexibility must co-exist. But among flexible hardware candidates, microprocessors and programmable DSP

processors are far too slow to meet the throughput requirements of ASICs. FPGAs do come close in terms of performance, but are extremely inefficient due to its high energy and large area overhead. We must bridge the huge gap in efficiency for FPGA to become a viable contender to ASICs.

The primary culprit for FPGA inefficiency is interconnect, which accounts for over 75% of area and delay. For over 20 years, 2D-mesh network has been the back-bone of FPGA interconnects, but full connectivity in a 2D-mesh require O(N2) switches, requiring interconnects to grow much faster than Moore"s Law. As a result, various heuristics are used to simplify switch-box arrays at the cost of resource utilization, but interconnect area of modern FPGA is still around 80%. This work builds FPGA using hierarchical interconnects based on Beneš networks, requiring O(N·log·N) switches. Although Beneš is commonly used in telecommunication, this work is its first silicon realization of a FPGA. To realize a highly efficient interconnect architecture, significant pruning of the network is required. Novel techniques such as fast-path U-turns and unbalanced branching are also implemented. A custom place-and-route software is developed to map benchmark designs on a variety of interconnect candidates. From mapping results, the architecture is updated based on network utilization until an optimized design is converged. The large area of FPGA chip requires aggressive power gating (PG), but interconnect signals often lack spatial locality, make it block-level PG difficult. A novel PG circuit technique is developed to power-gate individual interconnect switches with very small overhead in area and performance. Such technique requires fundamental circuit changes, even modifying the CMOS inverter.

With innovations in chip architecture, circuit design, and extensive software development, this work has demonstrated 5 user-mappable FPGAs (from 1K–16K LUTs) all

with around 50% interconnect area: a 3–4x reduction from commercial FPGAs while preserving connectivity. An energy efficiency of 1.1 GOPS/mW is the highest among reported FPGAs, and is 22x more efficient than the most efficient commercial FPGA today, significantly bridging the efficiency gap between FPGA and ASIC.

# TABLE OF CONTENTS

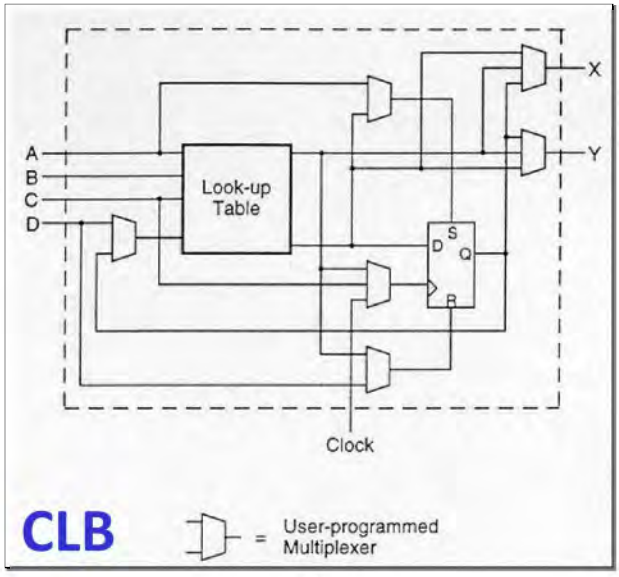
# CHAPTER II

# FPGA Interconnects: the Source of its Inefficiency

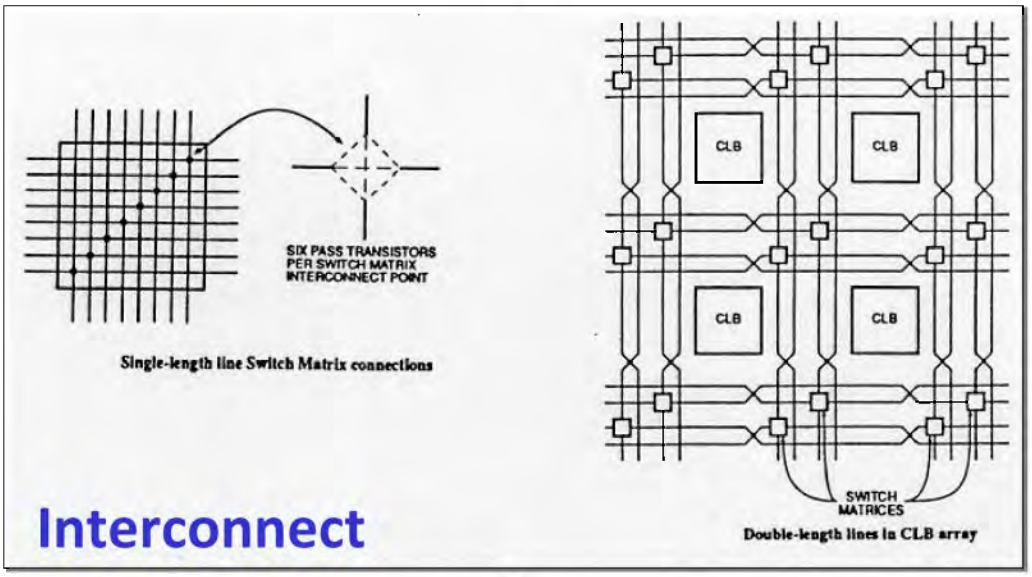
## 2.1 Brief History of FPGAs

The concept of a reconfigurable hardware started over 30 years ago, but it was regarded as prohibitively expensive because of its large overhead in area over ASICs. Transistors were expensive, and no one wanted to pay the huge area penalty for reconfigurability. Fortunately, the semiconductor industry rapidly expanded at the pace of Moore‟s law, and such large area overhead became more tolerable, finally leading to a first FPGA by Xilinx Corporation in 1985. The original FPGA, XC2000 series, had 64 or 128 look-up-tables (LUTs). As shown in Figure 2.1 a), each configurable-logic block (CLB) contains just one LUT and one selectable flip-flop. With so few CLBs, the interconnect network is also simple. The interconnects run in x- and y-direction around the CLBs, twisting with every segment, and some of the intersections have switch matrices placed diagonally, consisting of 6 pass-transistors per switch (Figure 2.1 b) [Brown92].

The initial perceptions of the XC2000 were “small, slow, expensive, and „different‟” [Alfke07], but the XC3000 introduced in 1987 became very successful even with very rudimentary software support. Fast-forward to today, FPGAs can support up to 500,000 LUTs per die, and the largest Xilinx Virtex-7 even supports 2 million LUTs using Stacked-Silicon Technology (Figure 2.2) [Saban12].




a)




b)

Figure 2.1: Schematic diagram from a Xilinx XC2000 of a) CLB and b) interconnects.

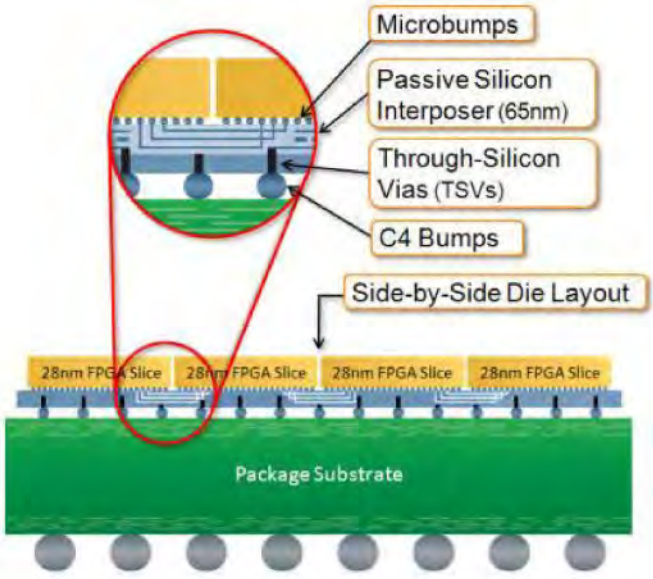
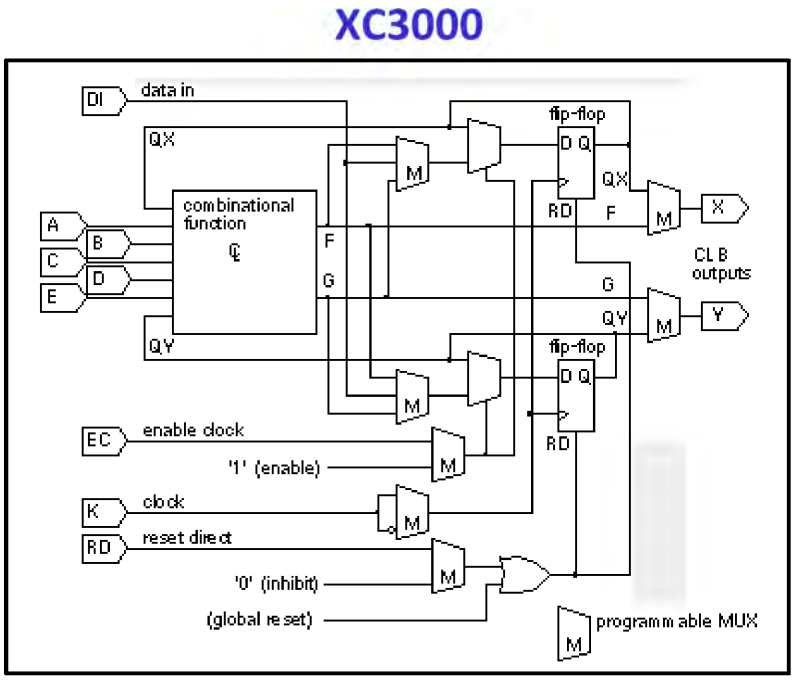


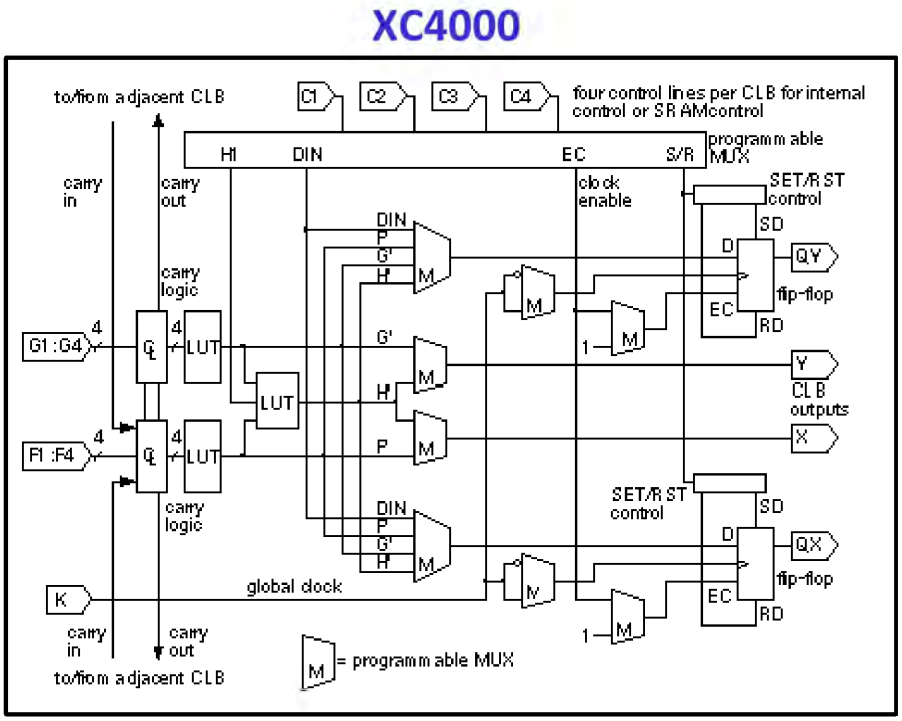

Figure 2.2: Illustration of Stacked-Silicon Technology in Xilinx Virtex-7.

Due to yield and fabrication constraints, each die is limited to around 500,000 LUTs, occupying 529 $mm^2$ in 28nm. "Stitching" the 4 chips together requires a very large interconnect bandwidth, far greater than that offered by standard packaging solutions. Therefore, a 65-nm passive silicon interposer is mounted onto the 4 FPGA dies to create a high-bandwidth interconnect, providing more than 10,000 connections between each adjacent die. For communication with external I/Os, the interposer uses through-silicon vias (TSVs) to connect the FPGA die to the C4 bumps on the package. Although the stacked silicon technology is not monolithic, many of the performance and cost benefits of a 3-D monolithic FPGA from [Lin07] still apply.

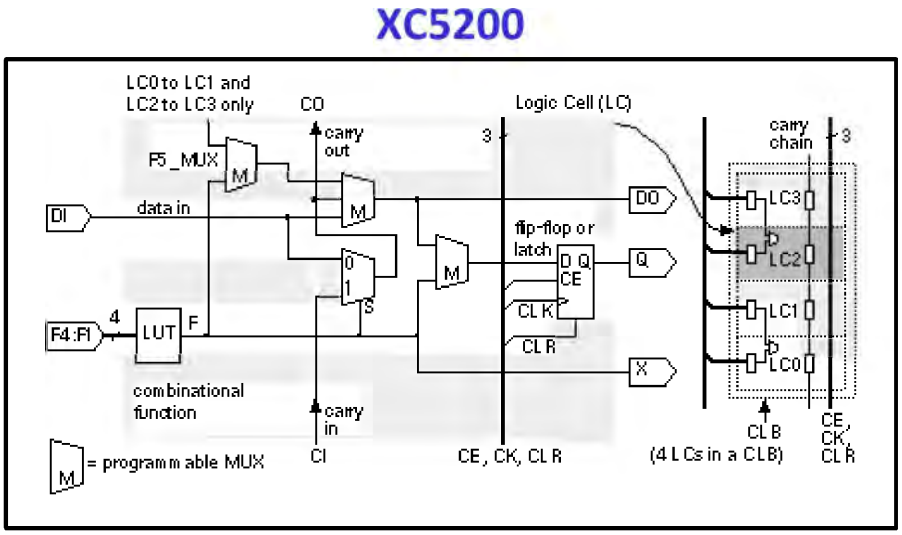
Of course, FPGA progressions are more than just area expansion, the CLB core of the FPGAs has also evolved over the years (Figure 2.3) [Rose93]. Many features are added to implement commonly-used ASIC features very effectively, such as multiple flip-flops with clock-enables (XC3000), a dedicated ripple-carry chain (XC4000), and LUT-combining multiplexers (XC5200).


XC3000
DI
data in
QX
combinational function
A
B
C
D
E
F
G
QY
flip-flop
D Q
RD
M
X
CLB outputs
Y
EC
enable clock
'1' (enable)
K
clock
RD
reset direct
'0' (inhibit)
(global reset)
programmable MUX

a)


XC4000
to/from adjacent CLB
C1
C2
C3
C4
four control lines per CLB for internal control or SRAMcontrol
programmable MUX
H1
DIN
EC
S/R
carry in
carry out
carry logic
clock enable
SET/RST control
SD
D
QY
QX
flip-flop
RD
G1:G4
F1:F4
LUT
G'
H'
P
Y
X
CLB outputs
global clock
K
= programmable MUX

b)




c)

Figure 2.3: CLB diagram of Xilinx a) XC3000, b) XC4000, and c) XC5200.

Over the past ten years, CLB sizes grew even more. Xilinx has transitioned to four 4-input LUTs per CLB in its Virtex-4 [XlinxV408], then to four 6-input LUTs per CLB in Virtex-5 [XlinxV512]. The newer Virtex-6 and 7 even have dual flip-flops mated to each of the 6-input LUTs (Figure 2.4) [XilinxV6CLB12].

The newer CLBs place an even greater emphasis on software design. The performance of the FPGA depends heavily on the mapping algorithm – packing critical-path gates within a CLB would provide much faster performance than spreading the critical path across multiple CLBs. Since the interconnect network cannot provide full connectivity across all CLBs (Chapter III), packing LUTs locally into CLBs can reduce the number of I/Os required by the CLB [Betz98], and the software tool also needs to provide quality place-and-route results to ensure feasible design mapping.

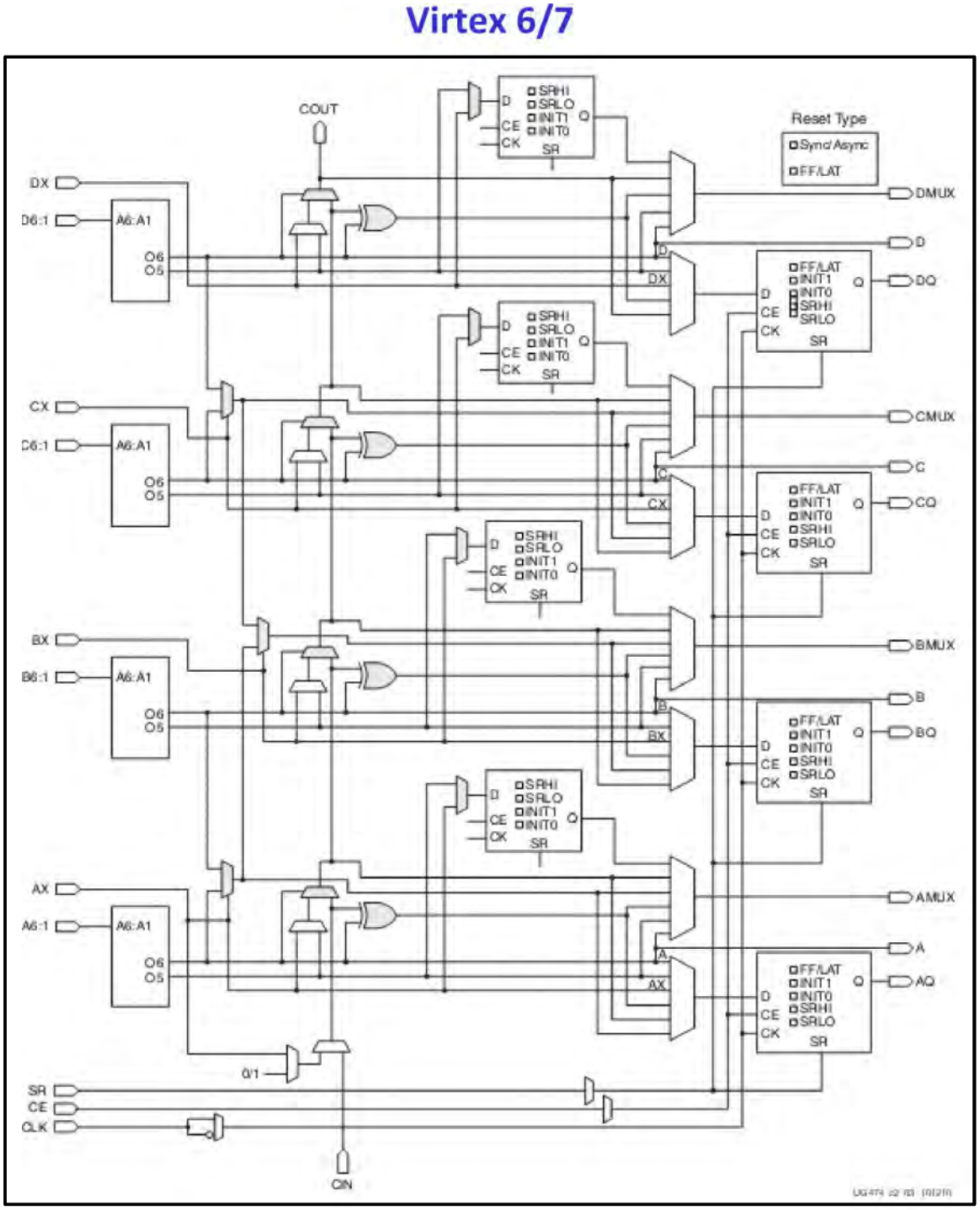



Figure 2.4: CLB diagram of Xilinx a Virtex-6 and 7 series FPGA.

Over the years, the FPGA software support has developed into a complete design suite. With extensive support for automated design mapping from HDL into bitstream, very little effort is required by the end-user. High-level synthesis tools even support mapping software programs (such as C or Matlab models) directly onto the FPGA. This many layers of abstraction provide a simple user experience, but it also shields us from seeing the intricate details of a FPGA design, especially interconnect routing.

## 2.2 Interconnects: the Backbone of an FPGA

In FPGA design, great emphasis is placed on the CLBs and other programmable blocks, and documentations are widely available. On the other hand, interconnects have mostly remained in the dark. Although FPGAs have grown enormously in size since the XC2000, the fundamental interconnect architecture still remains (Figure 2.5). In 2D-mesh interconnects, LUTs are placed in configurable logic blocks (CLBs), and interconnects run in the x- and y- direction surrounding the CLBs. I/O connection switches tie the CLB I/O to the interconnect network. Arrays of switch boxes are placed at interconnect crossings to select and buffer the programmed path. Each switch-box contains pass-transistors programmable by the configuration memory. Since a full switch-box array at every interconnect crossing requires too much area, various heuristics are used to simplify the arrays at the cost of interconnect connectivity [DeHon99, Tessier00, Lin09]. In Figure 2.5, the example network only implements switch boxes along one main diagonal and two sub-diagonals of the switch-box array. In this simplistic case, each interconnect trace enters a switch-box at every interconnect crossing, the selected path is then buffered to drive the next trace.

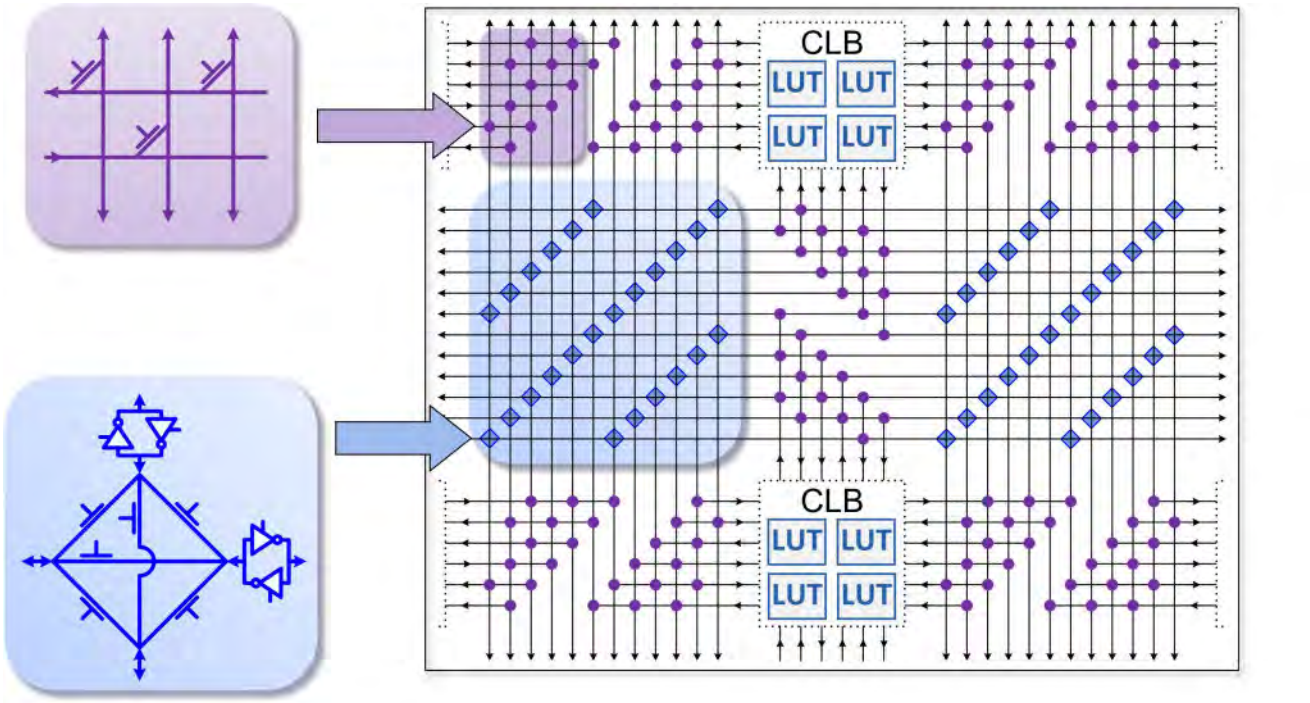



Figure 2.5: A sample 2D-mesh architecture with I/O connections and switch boxes.

To improve routing performance and add path diversity, each interconnect trace can be heuristically designed to travel for 1, 2, 4, 6, or even more CLBs before reaching the next switch. A path from one switch to the next is called a "hop". From an illustration in Xilinx XC4000 interconnects (Figure 2.6) [XilinxXC99], we see different interconnects labeled as "single", "double", "quad", "long", or even "global" based on the distance of each hop. Coming out of a CLB, a signal can be connected to a selection of hop lengths, giving the router freedom to choose a longer or shorter hop based on its routing requirements. Modern FPGAs have also migrated towards uni-directional routing, thus removing bi-directional buffers and significantly reducing interconnect loading [Lemieux04, Lee06].

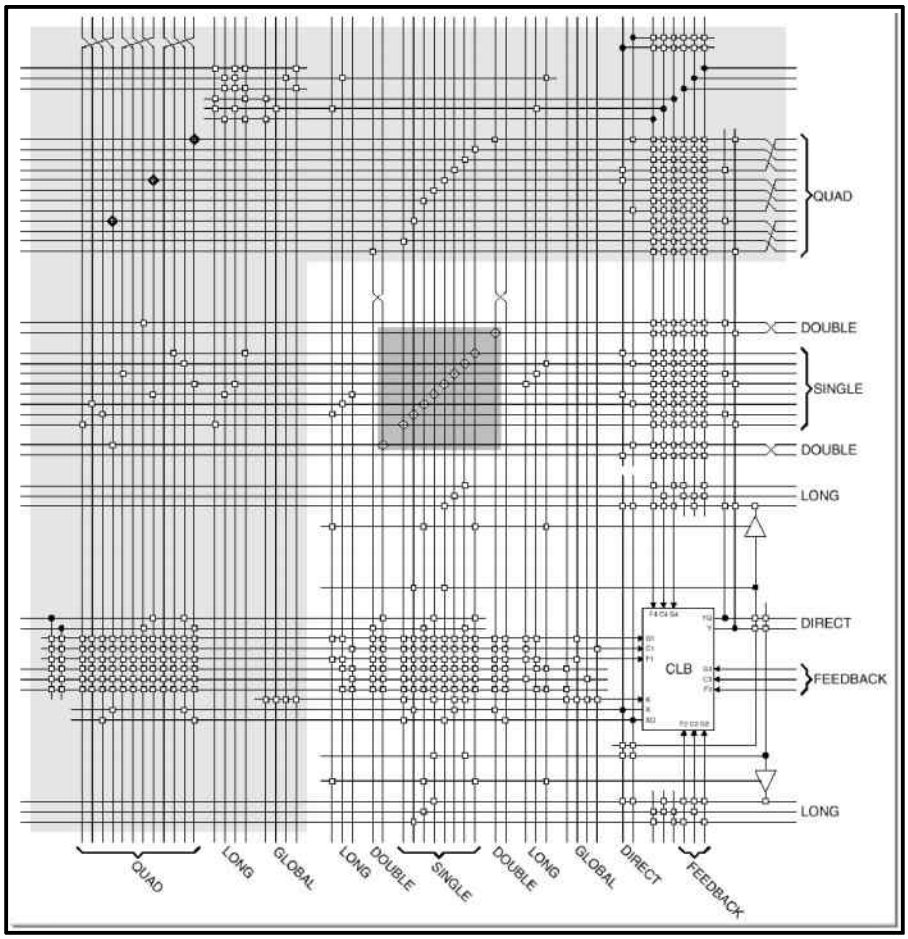



Figure 2.6: Interconnect architecture of a Xilinx XC4000 FPGA [XilinxXC99].

With extensive techniques in interconnect pruning, along with ever more complex CLBs, one may expect the FPGA area to be dominated by CLBs. It is called a "gate-array" after all. Surprisingly, even with such heuristics, 80% or more of the area on modern FPGAs are occupied by interconnects [Bolsens06]. The interconnect area is actually 4 times the logic area! In addition, interconnect also accounts for the majority of the delay and power in today"s FPGAs (Figure 2.7). The reality could be even worse: if we were to remove the larger IP blocks and accelerators from the FPGA, and compare the area of interconnect versus the area of CLBs, the ratio could be closer to 10:1.

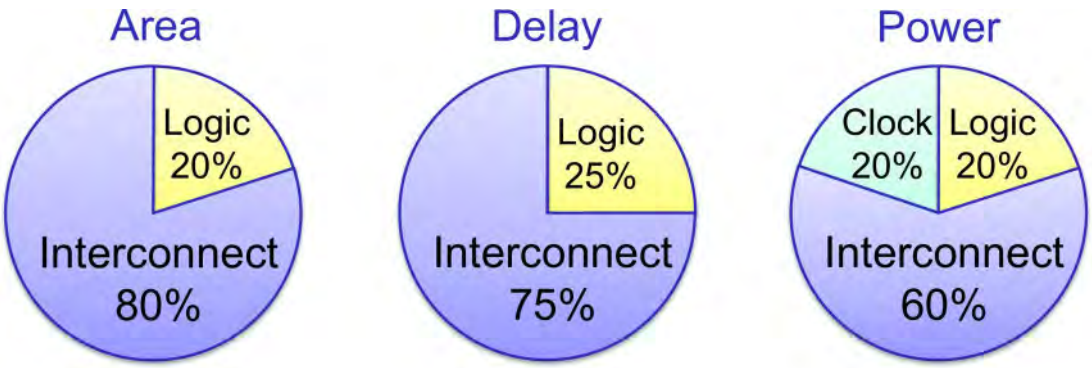



Figure 2.7: Area, delay and power breakdown of a modern 2D-mesh FPGA.

## 2.3 Scaling a 2D-mesh Network

The key cause for interconnect overhead is the scalability of 2D-mesh interconnects. In the worst case, the number of switch boxes grows as $O(N^2)$ with the number of LUTs. Although heuristics are able to reduce the number of switches, there is a limit. Rent"s rule ($T = t \cdot g^p$) can be used to model interconnects, where $g$ is the number of gates, exponent $p$ is the Rent"s coefficient for modeling the number of I/Os, and $t$ is a constant of proportionality. In typical cases, the interconnect complexity per logic block is $O(N^{0.75})$ for random logic, which is still $O(N^{1.75})$ for a chip of $N$ logic blocks [Landman71].

For very regular designs, such as a memory banks, the complexity per logic is $O(N^{0.5})$. Since FPGA mapping software employs intelligent gate placements, the logic is not completely random, but it is certainly not as regular as memory banks. We therefore expect the actual Rent"s exponent $p$ to be between 0.5 and 0.75 [Tessier00]. But for very large designs (large $N$), $O(N^{0.5})$ to $O(N^{0.75})$ provides too large of a range for this model to be useful. Nevertheless, it provides us theoretical lower and upper bounds on interconnect complexity.

Even using an optimistic exponent of $p = 0.5$, the total complexity of $O(N^{1.5})$ still

requires FPGA sizes to scale much faster than Moore"s Law. Figure 2.8 shows the interconnect expansion from Xilinx Virtex-4 to Virtex-5 [XlinxV506, Minev09]. Adding 50% of interconnect logic per CLB poses a significant area increase even for just 1 product generation. Scaling $N$ from 64 in XC2000 to 500,000 in modern FPGAs, it becomes clear why interconnect area is a key concern today.

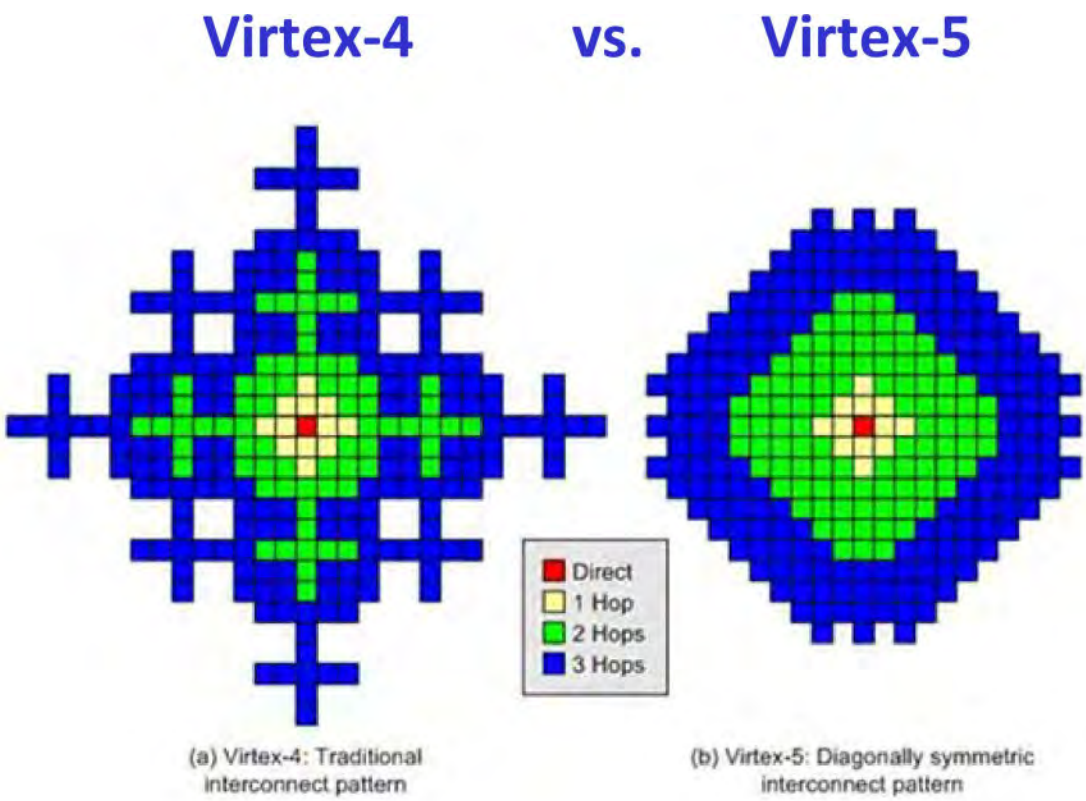



Figure 2.8: Interconnect resources per CLB for Xilinx Virtex-4 vs. Virtex-5 [XlinxV506].

In more recent years, many have proposed asynchronous architecture for FPGAs, aiming to improve its performance [Teifel04, Teifel204, Manohar06]. Such techniques have claimed to achieve > 1 GHz performance from FPGAs by using asynchronous hand-shake and token-based heavy pipelining. However, such technique failed to recognize the root cause of FPGA overhead, which is the scalability of the interconnect area. In contrast, asynchronous FPGAs require a 3x

overhead in interconnect area: replacing 1 signal with 3 asynchronous hand-shake signals, further exacerbating the effect of interconnect overhead. Whenever signal fan-outs are required, complex acknowledgement circuitry is required to wait for the slowest path to return the token before passing it on. More recent work by [LaFrieda10] acknowledged the large area and power overhead required by asynchronous FPGAs, and proposed a two-phase logic and voltage-scaling in the acknowledge signals to reduce the power consumption, but the large overhead in area remains. Although asynchronous FPGAs claims to run up to 3x faster than their synchronous counterparts, the 3x penalty in interconnect area will quickly nullify any performance advantages on large designs. Recent work in [Devlin11] uses dual pipeline (separate pipelines for precharge and evaluation phases) to further improve asynchronous performance, but requires 5 physical wires for 1 interconnect signal. Clearly, these approaches are not scalable to larger designs. For efficient, high-performance FPGAs, what we need is an interconnect architecture that is scalable in area and performance, and not brute-force circuit implementations.

## 2.4 Hierarchical Network – A Scalable Solution

To address the non-scalability of 2D-mesh, we adopted a hierarchical interconnect architecture based on a Beneš network. In telecommunication, Clos,Beneš, and similar hierarchical networks are well-known to be rearrangeably non-blocking network for point-to-point connections, and are commonly used in communications [Clos53, Benes62, Kleinrock77, Yang99, Dally04]. There has not been a silicon realization of a Beneš network for FPGAs until this work. To demonstrate its feasibility, the original Beneš network is first modified into a realizable FPGA architecture.

As a demonstration, we start with 2 LUTs, each with just 2 inputs and 2 outputs (Figure

2.9). This network requires 3 stages, and each stage uses 2x2 switch matrices (SMs) for signal routing. Each SM can support both uni-cast and multi-cast of incoming signals, as shown. This network is rearrangeably non-blocking for uni-cast, meaning the signal routing can be rearranged to support arbitrary LUT-to-LUT connections.

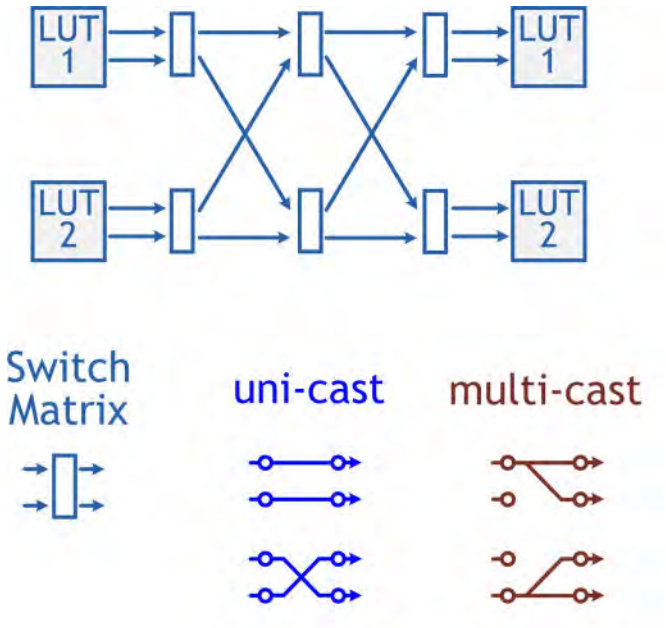



Figure 2.9: A simple 3-stage Beneš network connecting 2 LUTs.

In FPGA applications, it is common to use 4 to 6 input LUTs with 2 outputs. To illustrate a 4-input, 2-output LUT network, the 3 stage network is recursively extended to a 5-stage network (Figure 2.10), and can be further extended to larger networks. This network remains non-blocking for uni-cast, and because there are only half as many LUT outputs as inputs, it is virtually non-blocking even for multi-cast based on our simulations. Since each LUT only has 2 outputs, the red SMs can always multi-cast the signals, and can be removed. In addition, the 4 inputs to a LUT may arrive in any order, therefore the gray SMs can be removed as well. Note that for some CLBs, such as DSP accelerators or control signals, the inputs may not arrive in any order, and in those cases the grey SMs must remain. For simplicity, the center 3 stages are

abstracted as a single 4-input, 4-output SM, which is essentially a 2-bit 2x2 switch because it propagates two paths in each direction. The simplified diagram is shown on the bottom of Figure 2.10.

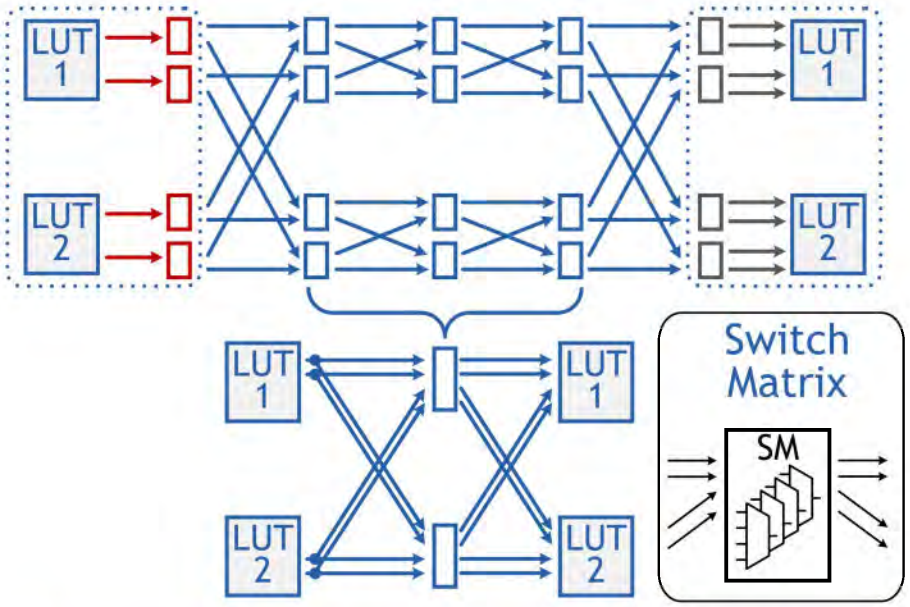



Figure 2.10: A 5-stage Beneš network merged into a 3-stage using 2-bit 2x2 switches.

Scaling to a larger network, we observe one key problem with the original Beneš network. Figure 2.11 shows an 8-LUT network using 5 SM stages. The downside is that *all* paths are required to traverse on all 5 stages regardless of the physical distance between the source and destination. As shown in Figure 2.11, LUT 7 and 8 are physically adjacent to each other, but the network requires the signal to traverse through all hierarchies while a simple switch in the first stage would suffice. Another issue with this network is input/output locality. In an FPGA, the input and output of a LUT is coming from one hardware block, but in this network, the inputs and outputs are split across two sides of the network. Since this diagram is not representing physical implementation, it can be misleading to the FPGA designer.

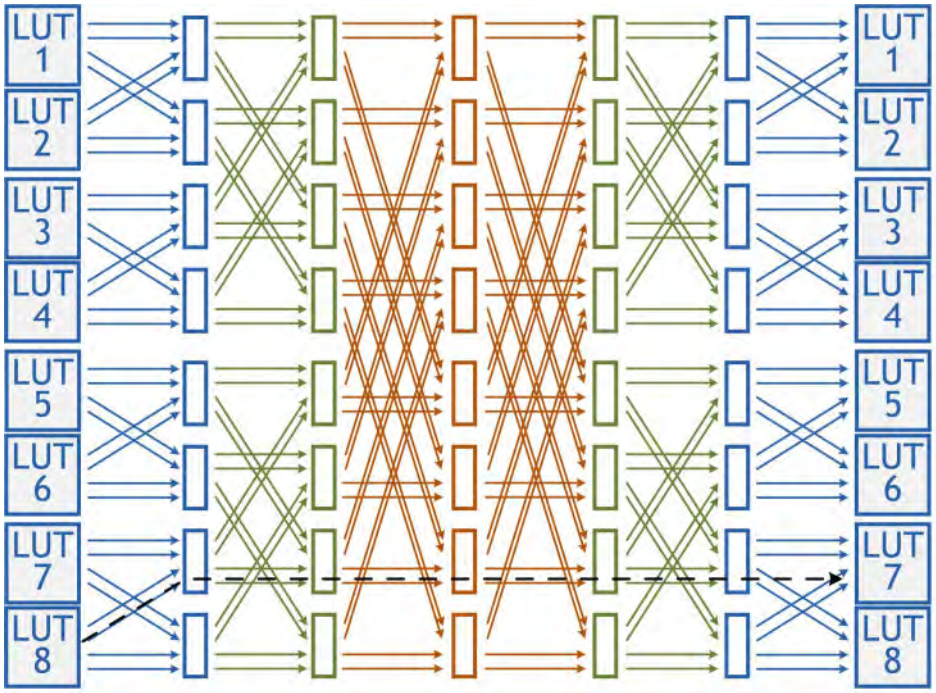



Figure 2.11: A 5-stage Beneš network connecting 8 LUTs.

To avoid traversing unnecessary hierarchies to speed up interconnect routing, and to provide an interconnect that closely resembles the physical implementation, we employ a folded Beneš network (Figure 2.12), also called a fat-tree network by [Leiserson85]. This similar architecture has been employed in supercomputing machines, such as the Connection Machine CM-5 with 256, 544, and even over 1000 processing nodes [Leiserson96].

As shown, 4 LUTs are connected via 2 stages of SM, and another 4 LUTs are to be connected with a 3rd SM stage. This effectively leads to an interconnect complexity of $O(N \cdot \log N)$, which scales much better than $O(N^2)$ in 2D-mesh interconnects.

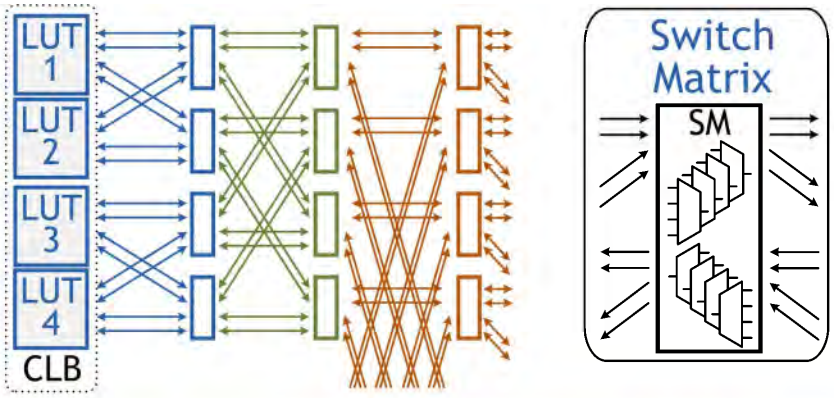



Figure 2.12: A 3-stage folded Beneš network connecting 8 LUTs (4 LUTs shown).

Although drawn with 2 arrows, each trace is actually 2 uni-directional signals. Each switch matrix then performs 4 uni-directional connections both upwards and downwards. Signals will come from the LUT output, traverse up to the required hierarchy, and traverse back down to the LUT input. Because the network is still rearrangeably non-blocking, full connectivity can be obtained.

Although this architecture reduces interconnect complexity by reducing the number of switches, routing congestion remains an issue. In Figure 2.12, the first SM stage has 2x2 wires crossing each other, but the second stage has 4x4 wires crossing, and the 3rd stages has 8x8. Each additional SM stage doubles the routing congestion. This O($N$) congestion requires much larger area for higher level SMs, making physical design more difficult and less area-efficient.

Fortunately, implementing a Beneš network on silicon gives us freedom in both x- and y-directions. Although [Manuel 07] illustrated a manual layout method for a Beneš layout on a 1-dimensional array, most silicon implementations allow for a 2-dimensional layout. To alleviate congestion, routing is alternated between the x-y directions, doubling the routing congestion for every 2 stages. The routing congestion is reduced from O($N$) to O($N^{\frac{0.5}{}}$) (Figure 2.13), and the fully symmetrical implementation also eases physical design.

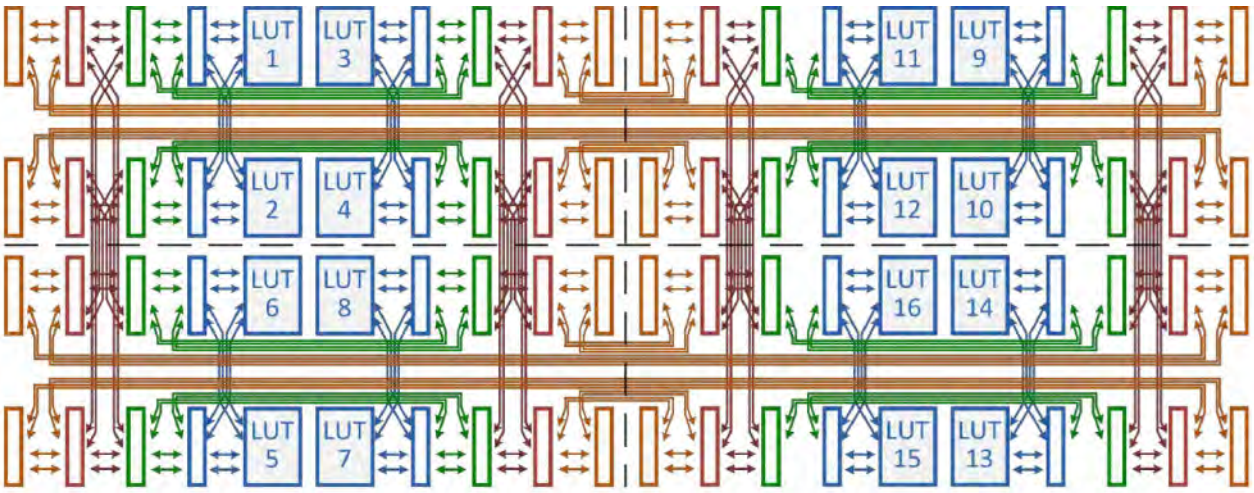



Figure 2.13: A hierarchical Beneš interconnect architecture using alternated x-y routing.

Another change from the original Beneš network is unequal wire lengths. At every hierarchy, the LUTs near the center are connected to create shorter routes, and the LUTs near the edges have longer routes. In terms of logic connectivity, this wiring difference is an isomorphic transformation from the original network, thus the interconnect connectivity remains unchanged [Wu80, Duato02, Konda08]. Yet this difference in wire lengths gives routing tools options for faster paths on timing-critical routes. In physical design, this also allows the center routes to remain at the lower metal layers without crossing over the longer routes on the upper metal layers, further avoiding congestion.

## 2.5 Prior Attempts at Hierarchical FPGAs

Numerous publications have discussed hierarchical FPGA implemented as tree-of-meshes (Figure 2.14) [Greenberg88, Lai97, Tsu99, Wong04, DeHon04]. It is a limited bisection network, where the mesh connectivity decreases for upper hierarchies. In some implementations [Tsu 99], even connectivity at local levels is limited. Additionally, a centralized routing network is required at every hierarchy, which increases routing congestion, and central switches are still

based on 2D-mesh. The layout in [Greenberg88] intelligently distributes the meshes across the layout into "cubies", but the complexity of every hierarchy remains that of a mesh-based switch.

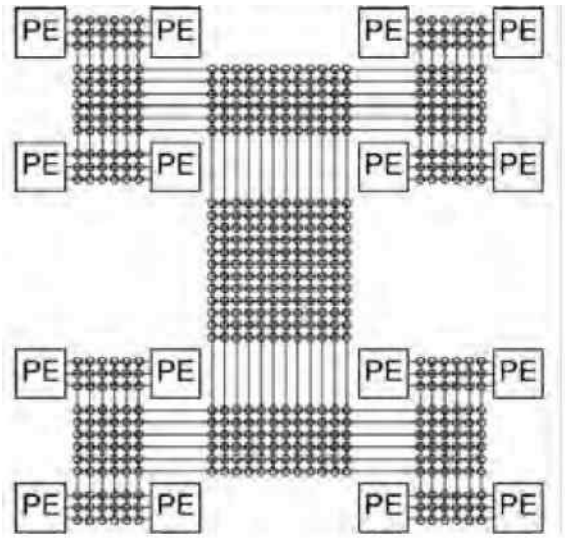



Figure 2.14: A hierarchical interconnect architecture using alternated x-y routing [DeHon04].

Unlike tree-of-mesh interconnects, our Beneš interconnect architecture evenly distributes routing across all LUTs instead of crowding them into centralized "hubs," easing routing congestion and shortening the wire length significantly. This is different from the butterfly layout in [DeHon00, Wong04] where centralized hubs are used, but hubs are distributed across different "cubies," thus requiring each signal to traverse across different hubs in different cubies just to switch hierarchy, significantly increasing interconnect delay.

There is one known silicon implementation of a tree-of-mesh FPGA, the hierarchical, synchronous reconfigurable array (HRSA) [Tsu99]. The architecture uses a Radix-4 topology with centralized switches and bi-directional routing. Rent"s exponent of 0.5 is used, so every hierarchy prunes the interconnect connectivity by 50%. Due to the centralized hubs used in this architecture, processing elements (PEs, equivalent to LUTs) that are physically close to each other may be required to use a detour routing. A heuristic is then employed to add "shortcuts" to

connect these PEs using additional wiring (Figure 2.15).

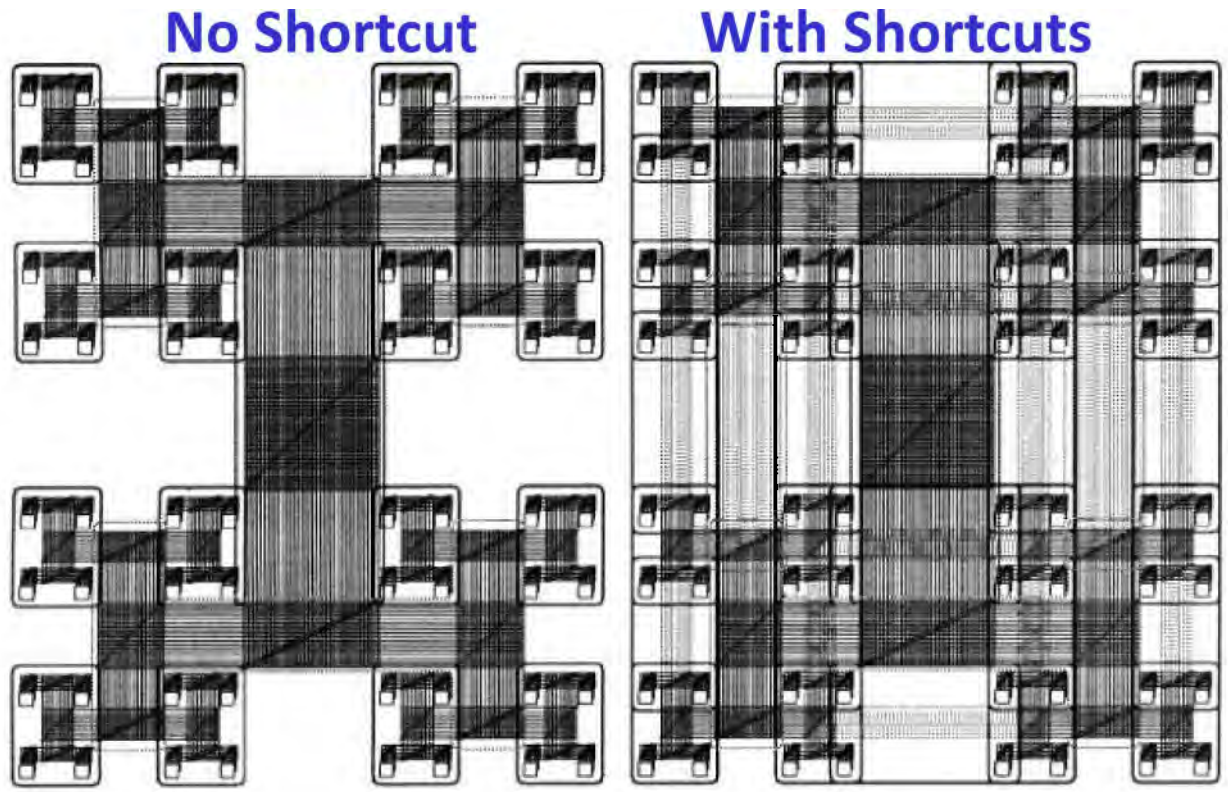



Figure 2.15: The HSRA architecture without (left) and with (right) wiring shortcuts.

The HSRA architecture was able to maintain good operation frequency due to its heavy pipelining, but the interconnect network with a Rent‟s exponent of 0.5 offered “very limited” connectivity. There has not been a follow-up chip after the original HSRA in 1999.

A multilevel hierarchical FPGA was published by [Mrabet06], although no silicon realization is attempted. The architectures use a Radix-4 topology with a Rent‟s exponent of 1, but only on the downward paths. The upward path, on the other hand, provides no path diversity (Figure 2.16). Therefore, the overall path diversity of this architecture is very limited, and the interconnect connectivity when mapping real-world designs is about 30-50%, often requiring a 2K-LUT FPGA to map 1K-LUT designs.

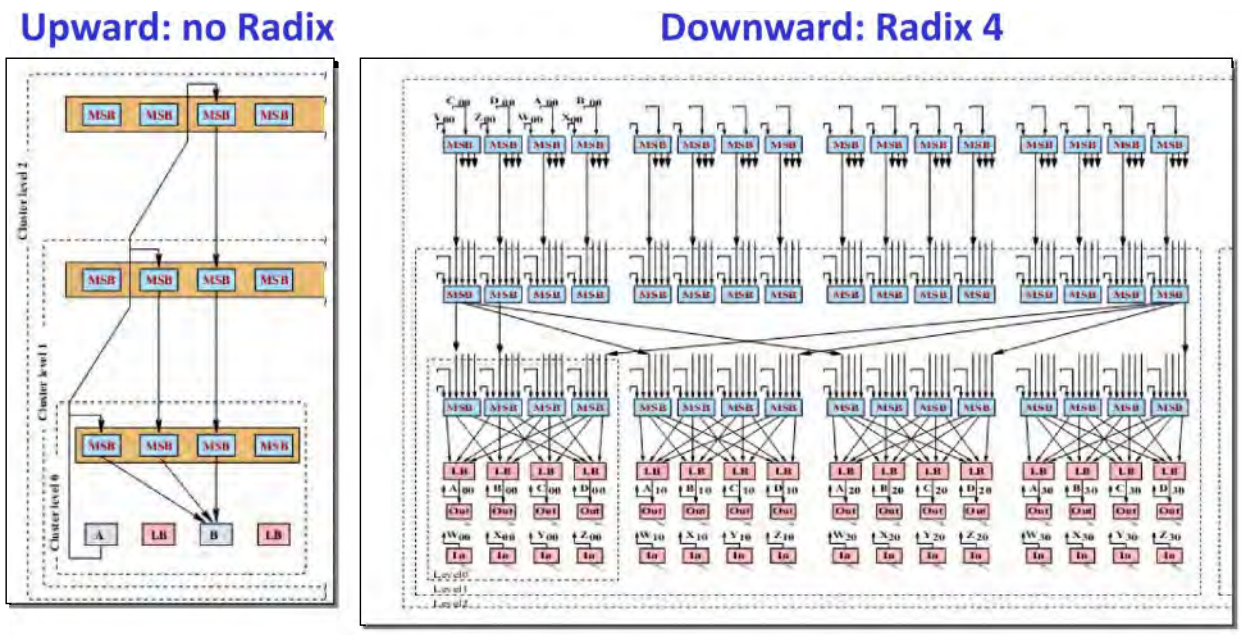



Figure 2.16: The multilevel hierarchical FPGA architecture.

## 2.6 Our Challenges

Although hierarchical FPGA has great appeal on paper, it has not received much attention in practice. The main reason is that it has yet to demonstrate *any* advantage over 2D-mesh: its 30-50% logic utilization is significantly lower than the 85% utilization achievable by commercial FPGAs, and it has yet to demonstrate any notable performance, power, or area advantage. The speed improvement in HRSA is due to heavy pipelining, not interconnect improvements.

On the other hand, commercial FPGAs today are already very mature products, often made as full-custom designs with state-of-the-art processes (and needing more than 10 layers of metal). The CAD tools are also capable of delivering very high quality-of-results (QoR) within a easy-to-use framework.

For our work to be considered worthwhile, we need to demonstrate and realize a

hierarchical FPGA with significant benefits in performance and efficiency. To demonstrate its practical values, software development is also needed to allow users to map their own designs. Overall, this project requires innovation and extensive work in creating an interconnect architecture, realizing it in silicon, and developing software tools to demonstrate its advantages. These details are covered in the following chapters of this thesis.

# CHAPTER III

# Architecture Design of Hierarchical FPGAs

## 3.1 Realizing Large-Scale Beneš Networks

To illustrate the silicon realization of the Beneš network, we start with the architecture design applied to our two FPGAs. The two chips shown in this dissertation have approximately 10× difference in logic capacity, and have different interconnect architecture as well. The first chip is a more straight-forward implementation, while the second chip utilized extensive architectural optimization techniques illustrated in Section 3.3 through 3.7.

The first test chip we published in [Wang11] contained 2048 look-up-tables (LUTs), each with 4 inputs and 2 outputs. Built on a Radix-2 architecture, it requires 11 levels of interconnects. Since every level translates to one SM stage, 11 levels of SMs are required. To ensure 100% connectivity in all cases, every LUT would need to have 11 levels of SM to preserve the full Beneš network. Using the 2D-layout method illustrated in Figure 2.13, expanding from 4 stages for 16 LUTs to 11 stages for 2048 LUTs would still be feasible to route, but it would occupy a significant amount of area. According Rent"s rule, this brute-force implementation represents a Rent"s exponent of $p = 1$. Realistically, there is no need to implement an interconnect network with more than $p = 0.75$ connectivity, as the area penalty associated with building larger interconnects far outweighs the benefits from chip utilization [Tessier00].

Mathematically speaking, implementing a network with $p < 1$ requires interconnect pruning at every stage. For example, when $p = 0.75$, every additional stage should implement 25% fewer wires than the previous stage. For FPGA realizations, there are three key reasons that

make this exact implementation impractical.

First, mapping FPGA design is a very non-deterministic process that depends heavily on the design to be mapped and the algorithms used by the place-and-route (P&R) software. The design to be mapped can have a Rent"s exponent $p$ anywhere between 0.5 and 0.75, which is a very wide range for interconnect routing. A very regular design, such as a feed-forward finite-impulse-response (FIR) filter, combined with a high-quality P&R tool, could be easily mapped onto an architecture with $p = 0.5$. On the other hand, a more complex design such as fast Fourier transform (FFT) will consume significantly more interconnect resources. There is no single exponent that can accurately represent all design complexities.

Second, the interconnect utilization is uneven across the SM stages. An effective P&R software would attempt to keep most of the signals local, thus shortening the critical path and reducing the active wire lengths. As a result, it is important to have sufficient routing resources for the lower levels to provide sufficient path diversity for the P&R tool. It can be worthwhile to use a Rent"s exponent of $p = 1$ for the lower hierarchies, and use a more aggressive pruning (e.g. $p = 0.5$) for the upper hierarchies. From our architecture evaluations, pruning the lower hierarchies, even with $p = 0.75$, can lead to sever routing problems and performance degradation.

Lastly, and most importantly, the FPGA architecture needs to be realized in a 2-dimensional layout, and its large size can lead to a very complex physical design if not planned carefully. As shown in Figure 3.1, an efficient physical implementation can allow the FPGA chip designer to start with creating just one LUT macro and its SMs. Although the interconnect wire length between the macros can be different, the hardware logic and the I/O port for each macro are identical. The fully symmetrical architecture allows the LUT macro to be replicated throughout the entire chip, drastically improving design time. The designer can also add more

hierarchies to the physical design flow, such as creating a 4-LUT macro out of the 1-LUT macro, then creating a 16-LUT macro from the 4-LUT macro. However, if the interconnect is to be pruned at every stage, the regularity of the layout can no longer be preserved: assuming all LUTs have SMs at stage 1, using $p = 0.75$, only 75% of the LUTs will have stage-2 SM, and only 56% of the LUTs will have stage-3 SM, and so on. Without regularity in the layout, not only will the interconnect take much longer to design, the reduced SM does not necessarily lead to reduced area. In Figure 3.1, if SMs are reduced for LUT 4, 8, 12, and 16, it would leave a gap in the middle of the layout because the surround macros are larger. This results in a worst-case situation of lost interconnect connectivity *and* lower layout density due to wasted area. When pruning SMs, the designer needs to make sure the reduced SM actually leads to reduced area, and must not over-complicate the layout process. This requires very judicious SM pruning at very strategic locations.


Figure 3.1: A hierarchical macro-based implementation of a 2D-Beneš network.

Overall, realizing a large Beneš network in FPGAs requires 3 things to keep in mind: interconnect connectivity, layout regularity, and layout density.

## 3.2 Implementing a 2048-LUT FPGA Interconnect

The 2048-LUT test chip requires 11 levels of interconnects. To preserve interconnect connectivity for lower levels, we maintained connectivity (Rent"s $p$ = 1) until SM stage 7, followed by 2 stages of $p$ = 0.5, and full connectivity for the top 2 stages. One quadrant of the FPGA architecture is shown in Figure 3.2: the quadrant is divided into 4 macros, each containing 128 LUTs. Inside each 128-LUT macro, all the LUT macros are identical; they are implemented similarly to Figure 3.1, but with 7 stages of SM per LUT. The half-SMs shown in yellow allow 2 out of 4 inputs to propagate upwards, realizing Rent"s $p$ = 0.5. Two concatenated half-SMs leads to a top-level connectivity of 25%.

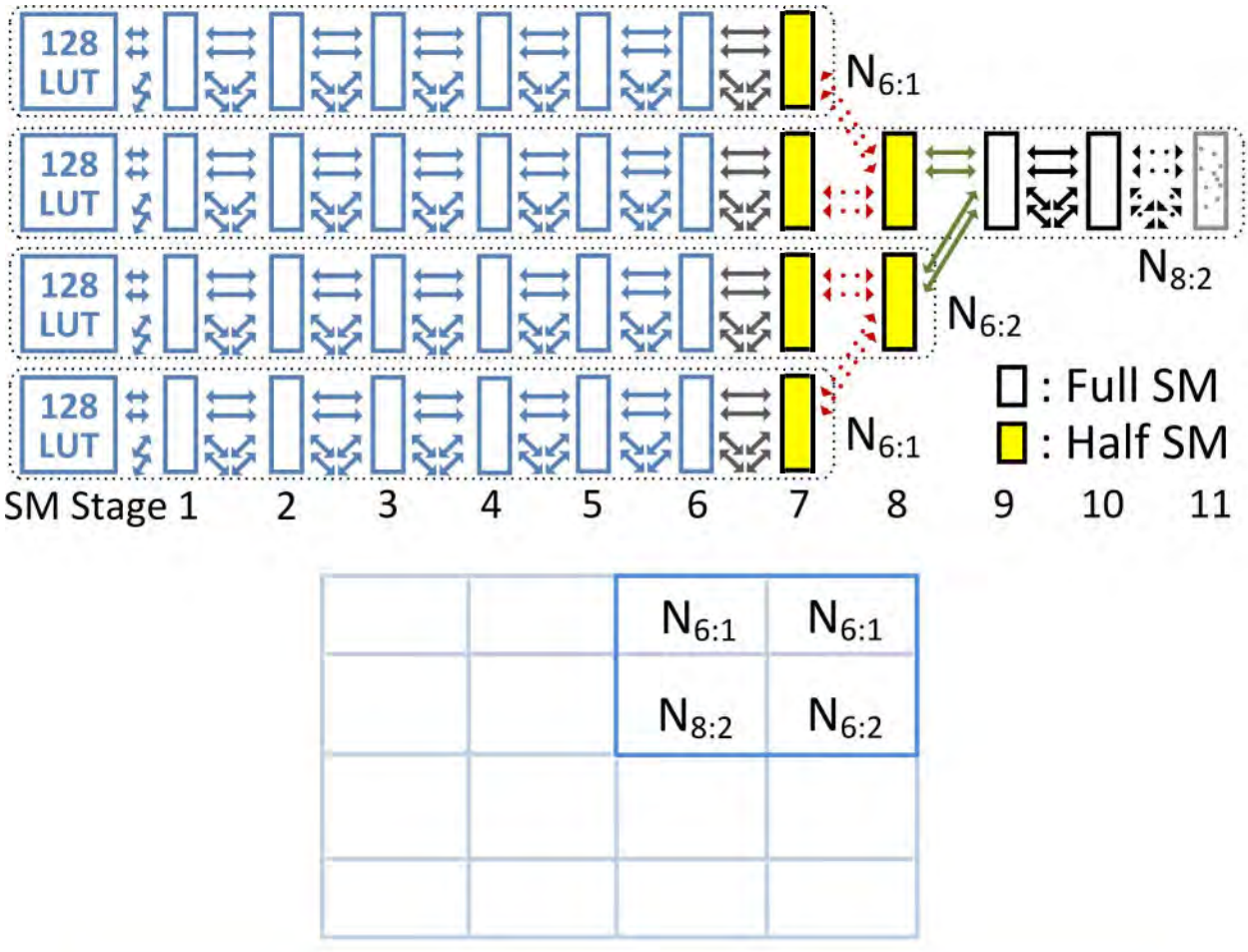



Figure 3.2: Interconnect architecture for our 2048-LUT FPGA, one quadrant shown.

The interconnect network is partitioned into three sub-networks: $N_{8:2}$, $N_{6:2}$, and $N_{6:1}$, where $N_{P:Q}$ represent a network of P full-SMs and Q half-SMs. Intelligent SM-pruning also requires the pruned SM to translate to an area reduction. From the architecture in Figure 3.2, it is clear that the 3 types of SM macros, $N_{8:2}$, $N_{6:2}$, and $N_{6:1}$, will each occupy a different area, because they each contain different number of SM stages. $N_{8:2}$ is the largest macro, followed by $N_{6:2}$, with $N_{6:1}$ being the smallest. To avoid gaps in the layout area, all SMs have the same width. Therefore $N_{6:1}$ macros are shorter. $N_{6:2}$ is also shorter than $N_{8:2}$, leading to some open space. In Chapter V, we will see that the opened space is used by Block RAMs. Because BRAM CLBs are larger than regular CLBs, the area pieces together very densely.

The top level of the chip is shown in Figure 3.3 with the 4 hierarchies of top-level wires shown in colors corresponding to those in Figure 3.2. The top-level layout is symmetrical in the x- and y- direction, allowing the single 512-LUT quadrant to be replicated to form the other 3 quadrants. The chip is divided into 16 macros of 128 LUTs each: macros with $N_{8:2}$ interconnects are placed near the center for shorter top-level routing, branching into $N_{6:2}$ on the left and right. $N_{8:2}$ and $N_{6:2}$ then both branch into $N_{6:1}$ on the top and bottom. This physical placement avoids long wires at the top level, and therefore minimizes interconnect buffers and further reduces area.

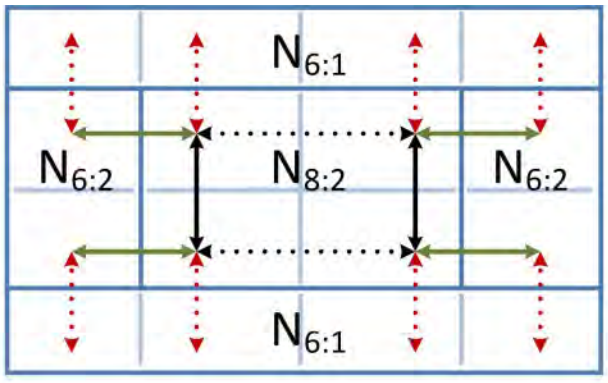



Figure 3.3: Interconnect architecture for our 2048-LUT FPGA, one quadrant shown.

This 2048-LUT architecture is relatively straightforward, using only 2 types of SMs to form 3 types of LUT macros. Scaling into larger designs with even more hierarchies, more advanced architectural techniques are used to further optimize the design. They are highlighted in the following sections (3.3 – 3.6).

## 3.3 Radix-3 Boundary-less Interconnect

Although hierarchical routing"s O($N$·log$N$) complexity is much better than O($N^2$) from 2D-mesh, it is sometimes inefficient for local routing if the leaves are crossing a high-radix boundary. For example, In Figure 3.4a), LUT 8 and 9 are neighbors, but signals have to traverse up 4 stages of network, and then zig-zag their way down the hierarchy to for LUTs to communicate with each other. Such lack of spatial locality is not desirable.

One method to shorten the nearest-neighbor routing lengths is an isomorphic transformation, as shown in Figure 3.4b). Connections from LUT 8 to LUT 9 can now traverse directly up to stage 4, make a U-turn, and traverse straight down. In terms of connectivity, it is well known that isomorphic butterfly structures maintain the same logic connectivity [Wu80]. Although the wire length travelled has reduced, the number of switches has not: the signal still needs to traverse up and down 4 hierarchies for communication between LUT 8 and 9.

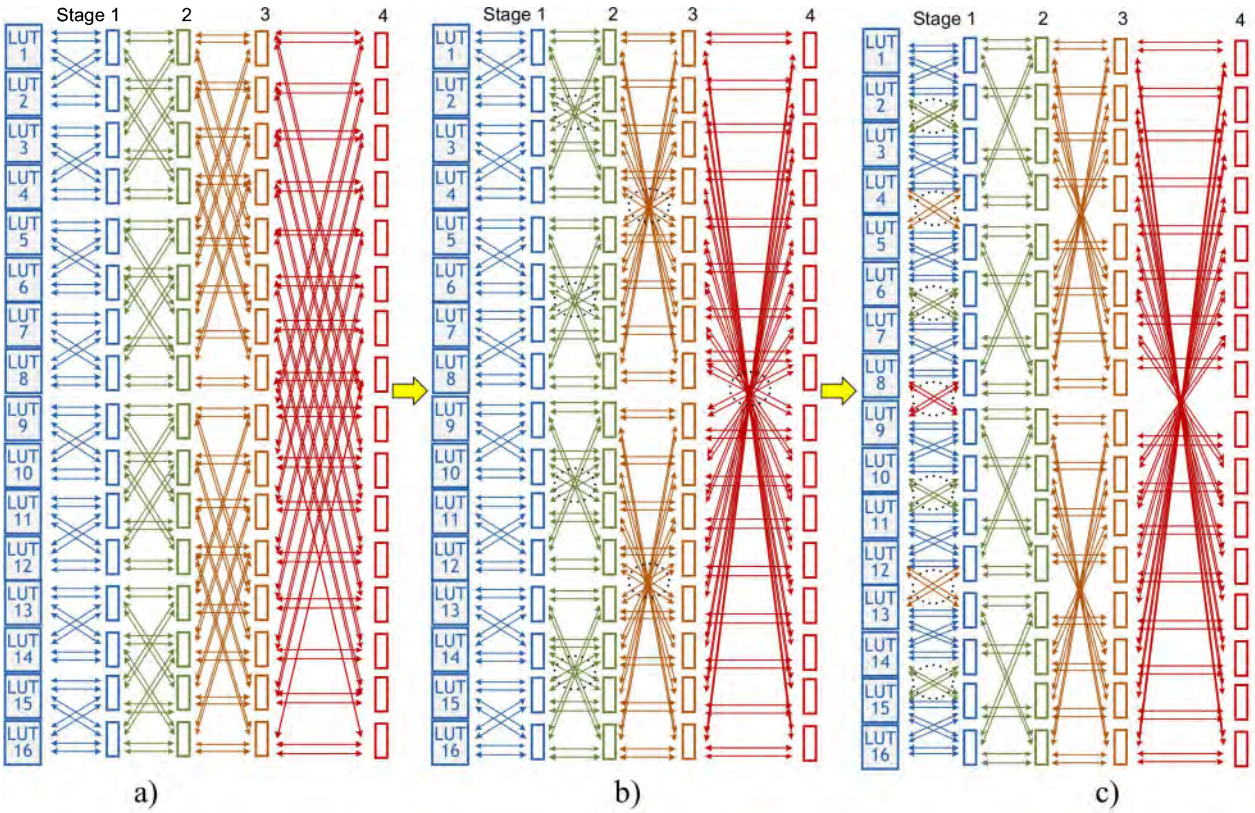



Figure 3.4: a) An original 16-LUT Beneš network, b) with isomorphic transformation to shorten nearest-neighbor lengths, and c) with boundary-less radix-3 switches in stage 1.

In this section, we propose a method of applying higher radix switches on the lower SM levels to utilize spatial locality in routing, allowing efficient interconnect routing for direct neighbors. We call such network a boundary-less radix-3 network [Wang13].

To convert a radix-2 network to a boundary-less radix-3 network, we first identify the center 2x2 routing of each stage, shown in the dashed circle in Figure 3.4b). It is noted that such center 2x2 routing only connects across an interconnect length of 1 ($2^0$). The first stage transformation into a radix-3 boundary-less interconnect is shown in Figure 3.4c). All center 2x2 routing in the dashed circles are moved to stage 1. This converts stage 1 into a radix-3 interconnect, and all stage-1 switches are capable of communicating with their immediate neighbors, both up and down the SM stages.

With stage 1 completes, we now convert stage 2 to a boundary-less radix-3 switch. We first identify the remaining center 2x2 routing above stage 2 (Figure 3.5a), shown in dashed circles. Note that these 2x2 routings only connect across an interconnect length of 3 ($2^1$+1). These 2x2 routings are then moved down to between stages 1 and 2 (Figure 3.5b), converting the second stage into a radix-3 boundary-less interconnect.

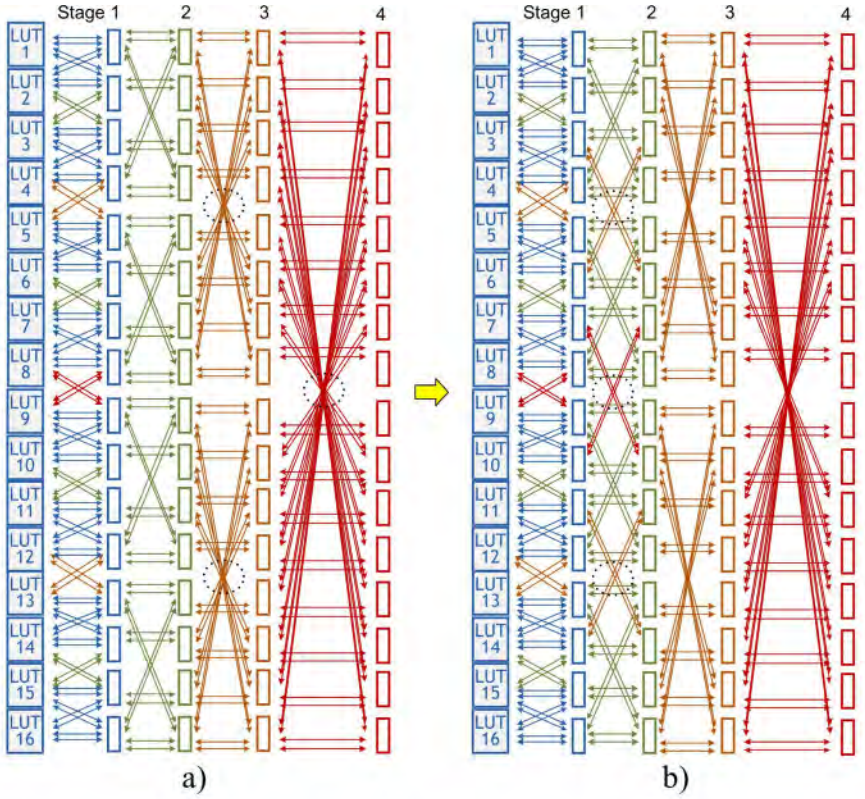



Figure 3.5: A 16-LUT Beneš network with a) boundary-less radix-3 switches in stage 1, and b) with boundary-less radix-3 switches in stages 1 and 2.

The same transformation continues for stage 3-4: we first identify the remaining center 2x2 switches above stage 3, shown in dashed circle (Figure 3.6a). For stage 2-3, we can note the remaining 2x2 switches are actually double pairs, one for LUTs 6−11, and one for LUTs 5−12. The inner 2x2 of the double pair connects across a distance of 5 ($2^2$+1), while the outer 2x2 connects across a distance of 7 ($2^2$+3). To maintain consistency, we then move the center double

pair from stage 3-4 (dashed circle) down to stage 2-3 (Figure 3.6b), transforming stages 2-3 into a boundary-less interconnect. It is clear that this stage-by-stage transformation can be continued to the top of the hierarchy. Alternatively, the designer may also choose to stop the transformation at any hierarchy, and preserve the remaining upper hierarchies as traditional radix-2 network.

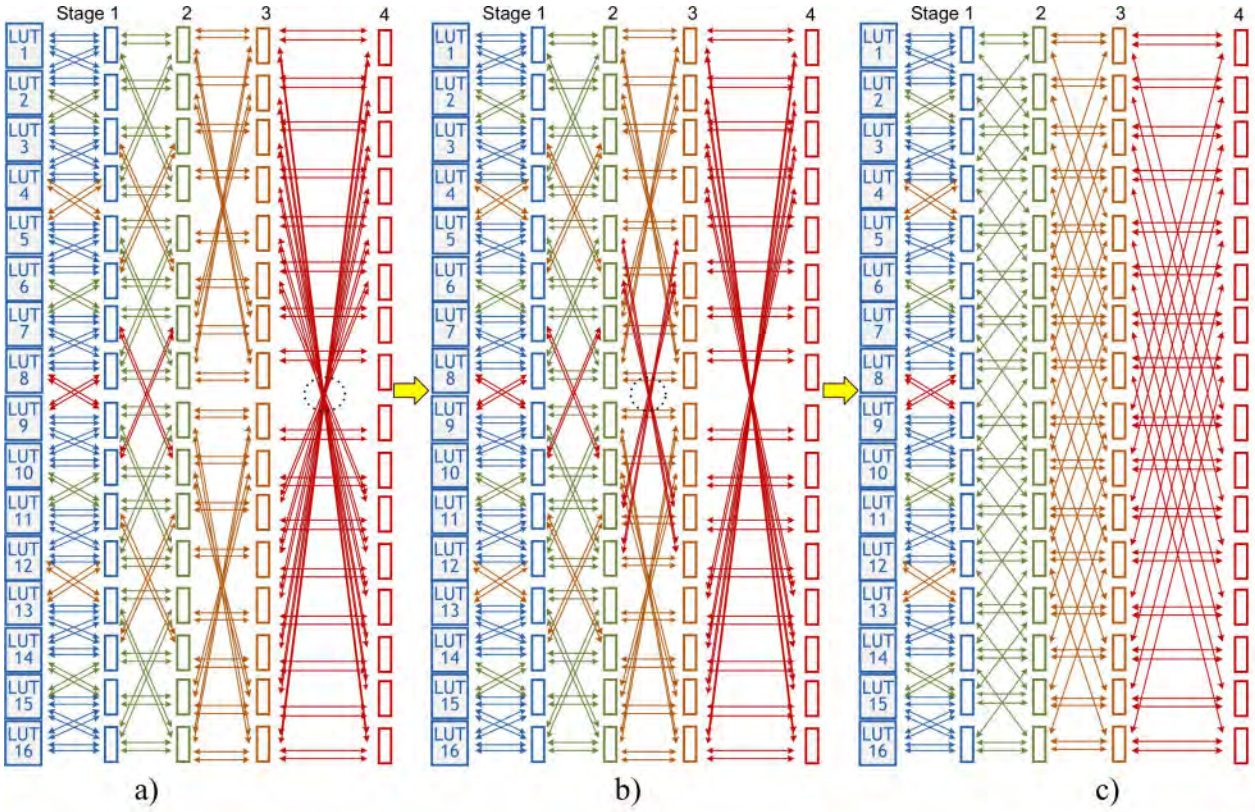



Figure 3.6: A 16-LUT Beneš network, a) with boundary-less radix-3 switches in stages 1 and 2, b) with boundary-less radix-3 switches in stage 1-3, and c) rearranged for distributed routing.

From the intermediate result in Figure 3.6b), we have shown that 50% of the wires branching out above stage 1 have been removed, and the wires on the bottom-most stage have doubled. Since the upper-stage wires are long, and the bottom-stage wires are very short, such tradeoff results in significant wire-length reduction for the architecture. Though shown for a 16-LUT example, this methodology can be extended to a network of arbitrary size.

From this illustration, we see that all stages above stage 1 have unevenly distributed

routing: some switches have to connect more routing than others. This scenario occurs because the wires above stage 1 have been reduced by 50%. To form a regular routing pattern, one method is to evenly re-distribute the interconnect routing: the dual routes branching out of stages 1-4 are re-distributed across all switches, resulting in the final routing architecture shown in Figure 3.6c). We see that the re-distributed routes for stages 1-4 use only single 2x2 butterflies, as opposed to the double 2x2 butterflies used below stage 1.

Given the 50% wiring reduction above stage 1, an alternative method of wire re-distribution is to prune the number of switches above a certain hierarchy. As shown in Figure 3.7a), one method is to prune the switches in stage 3 by moving some wires to a double wire, reducing the number of stage-3 switches by half. Since the remaining stage-3 switches are centered, this results in shorter interconnect length for stage 3-4, and reduces the number of switches in stage 4 by 50%.

Another method is to prune the switches in stage 4 by moving some wires to a double wire, reducing the number of stage-4 switches by half (Figure 3.7b). This can allow the stage-4 switches to reside on 1 half of the network, which can be useful in reducing the wire length of upper hierarchies. For example, for the 2048-LUT FPGA in Figure 3.2, SM stages 7 and 8 can benefit from this technique because the wires are merged toward the center, where the $N_{8:2}$ interconnects reside.

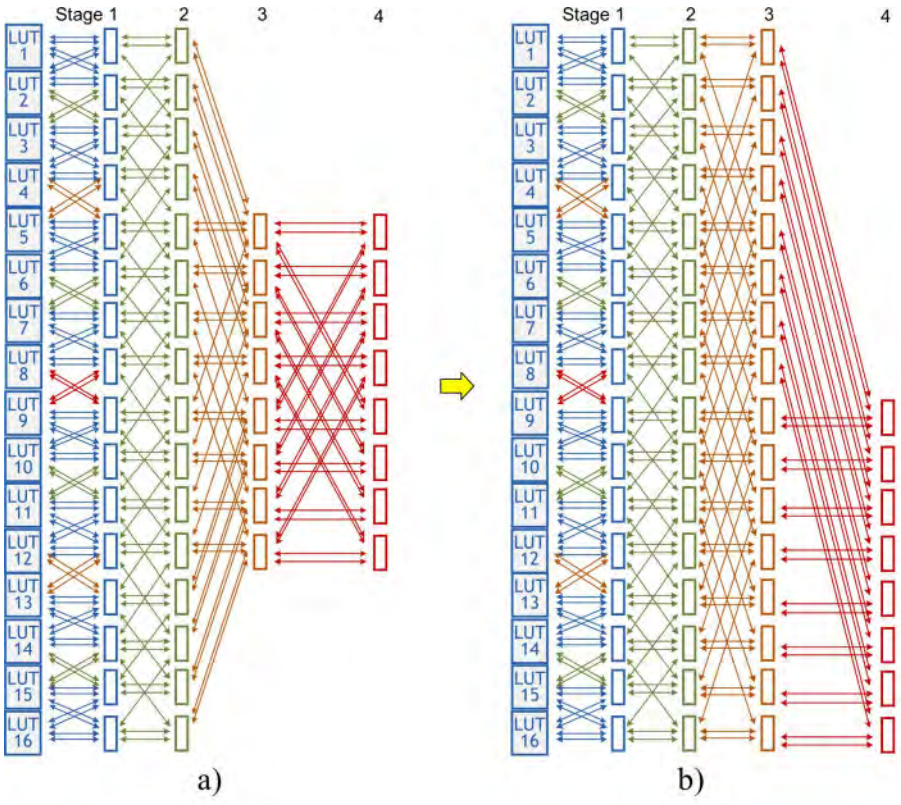



Figure 3.7: A boundary-less radix-3 network with switches pruned at a) stage 3 and b) stage 4.

Although the illustrations above use a radix-3 boundary-less architecture as an expansion to radix-2, it is not limited to this case. For example, a radix-6 architecture can be used as an expansion to radix-4; a radix-12 architecture can be used as an expansion to radix-8; and so on.

For the sake of completeness, Figure 3.8a) illustrates a radix-4 Fat Tree using 4x4 switches. Two stages of radix-4 switches are required to implement a 16-LUT network. To construct a boundary-less network, we first identify the wires in stage 1-2 that have a distance of 4 ($4^0$): these wires are bolded in Figure 3.8a). These selected wires are then moved down to below stage 1 (Figure 3.8b) to form a boundary-less network in the first stage. The center switches for LUTs 5-12 are radix-6, while LUTs 1-4 and LUTs 13-16 are only radix-5 in this illustration because they rest on the boundary of the network.

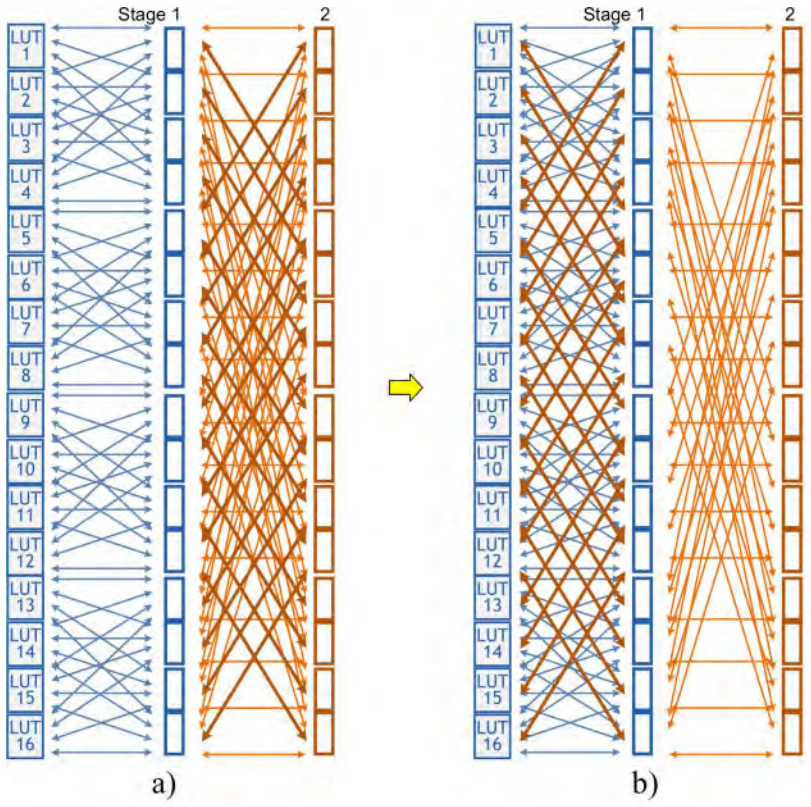



Figure 3.8: a) An original radix-4 16-LUT Beneš network and b) with boundary-less radix-6 switches in stage 1.

## 3.4 Fast-Path Interconnect

In VLSI designs, there usually exists a critical path, that is, a path that is more difficult to meet timing constraints. In most VLSI designs, the vast majority of the paths do not reside on the critical path, but those that are on the critical path usually determine the performance of the entire design. We therefore propose an addition to the interconnect SMs to allow faster performance for critical-path gate: fast path.

In the example in Figure 3.9a), we see an example routing from LUT 2 to LUT 16. One possible route is highlighted. Beneš network offers many path diversity (thus it is rearrangeably

non-blocking; without path diversity, the network offers very limited connectivity (such as [Mrabet06] from Section 2.5)), and we are simply choosing one path as an example. The signal needs to traverse up to stage 4 before U-turning back down. With the addition of fast-path, signals are allowed to travel from the LUT output directly to all SMs within its macro (Figure 3.9b). Therefore, the signal is able to travel directly from the output of LUT 2 to the SM on stage 4, and then U-turning back down. Following the macro-based design methodology highlighted in Figure 3.1, a LUT is placed with all its SMs in one macro during physical design, so adding fath-path routing within the macro does not add any interconnect routing outside the macro.

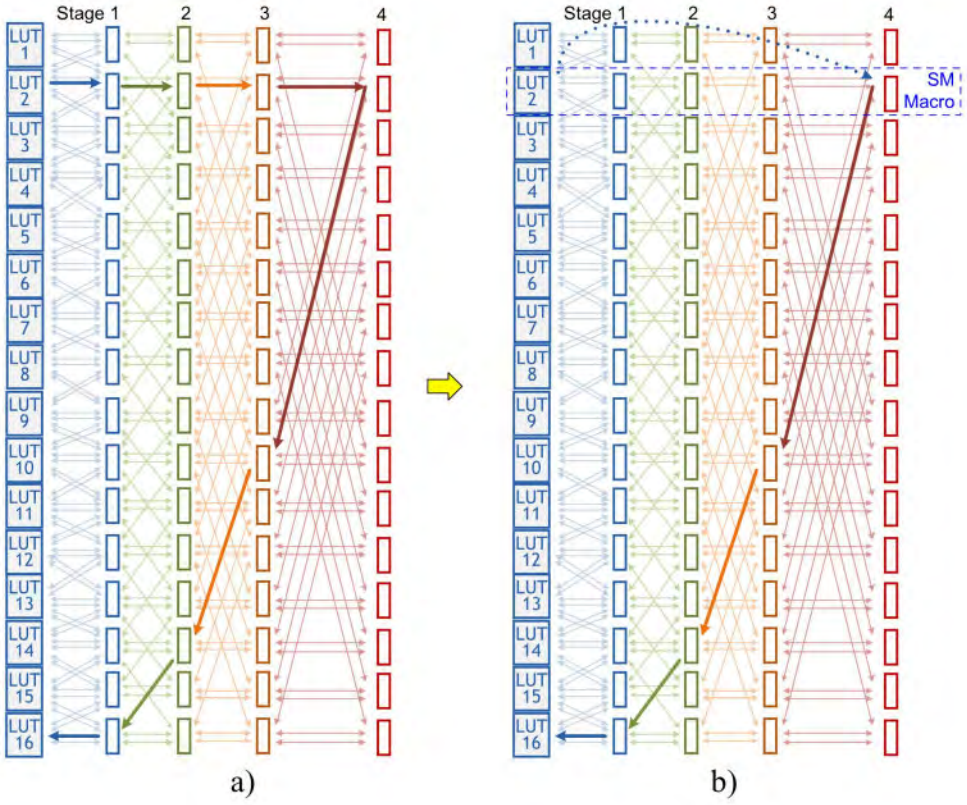



Figure 3.9: A routing example from LUT 2 to 16 a) without fast path and b) with fast path.

For each point-to-point connection, there is always at least one fast-path available, but other routes that conflict with the fast-path routes must take the slower route. In a timing-driven place-and-route flow, this gives the software tool freedom to choose a faster path for more

timing-critical routes.

In cases where routing obstructions occur, it is sometimes still possible to utilize portions of a fast-path, and use regular routing for the remainder of the routes. One such example is illustrated in Figure 3.10a), although it would be ideal to have fast-path directly connected to SM stage 4, the router can still connect fast-path to SM stage 3, and use regular routing to complete the route. In other cases, it is sometime impossible to use any fast-path, and regular routing must be used entirely (Figure 3.10b). Even under such cases, path-diversity allows for many routing choices, and the boundary-less radix-3 network sometimes even allows for fewer SM stages. In Figure 3.10b), one example route requires 4 SM stages, while another requires just 3 SM stages. It is up to the timing-driven P&R tool to select the faster path for timing-critical nets.

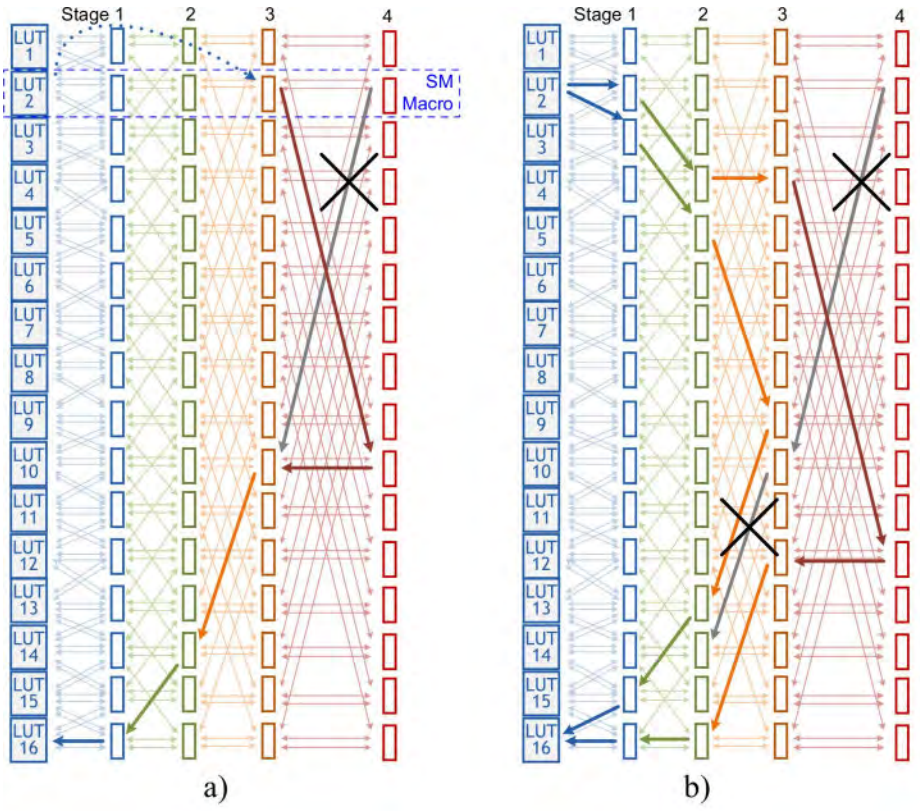



Figure 3.10: A routing example with routing obstruction that a) still allows a slower fast-path and b) allowing no fast-path.

## 3.5 Interconnect Cost vs. Gate Cost

In an FPGA, upper-level interconnects are often required to travel long distances, and it would be beneficial to reduce the number of these nets. On the other hand, interconnect switches are also a dominating factor for chip area, and it would be beneficial to reduce the number of these gates as well. Although it is ideal to reduce both, there also exists a trade-off between these two factors.

From the simple example in Figure 3.11, the two types of SMs have the same gate cost. Actually the 4-input muxes in Figure 3.11b) cost more when implemented as a traditional mux, as it takes three 2-input muxes to implement. As a static parallel mux (Chapter IV), a 4-input mux occupies as much area as two 2-input muxes. The muxes in Figure 3.11a) only allow for odd-to-odd and even-to-even switching, but the SM has double the number of muxes.

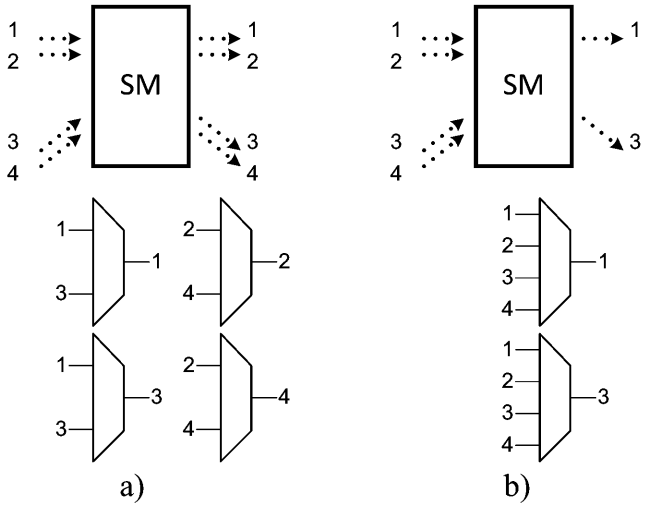



Figure 3.11: Two SM design with same gate cost, but a) with more wiring than b).

In terms of connectivity, the design in Figure 3.11a) is superior. For example, if input (1) travels to output (1), the design in Figure 3.11b) will not be able to send another signal in the horizontal direction. But the design in a) is still able to send another signal through output (2) as long as it does not need to route input (3). Overall, design in a) provides more path diversity for

routing.

A different scenario arises when the wire lengths are long, and signals (3) and (4) would need to be buffered (sometimes more than once). When the wires are long and the buffers are large, the signal buffering area can easily outweigh the mux area. In this case, the design in a) is clearly inferior: it requires double the number of buffers but does not provide double the connectivity of b).

For lower-level SMs, where the wiring is short and does not require additional buffers, it is beneficial to use limited-input muxes, but implement more of them to improve path diversity. For upper-level SMs with high wiring cost, it is beneficial to reduce to number of wires, in which case full-input muxes should be used, but fewer should be implemented to save wiring cost.

## 3.6 Local Interconnect vs. Branch Interconnect

In FPGA, interconnect wiring is expensive, because it contributes to routing congestion and buffer gate area. But local interconnects are much cheaper to implement. In traditional Beneš networks, each SM provides just as much local interconnects as branch interconnects (Figure 3.12), even though interconnects that branch to long wires cost significantly more hardware area. To reduce hardware, it is more effective to prune branch interconnects before pruning local interconnects. Local interconnects alone can also contribute to path diversity. In the example in Figure 3.12 (right), the fastest route from LUT 2 to LUT 14 is using the fast path, but let us assume two downward paths between SM stage 1 and 2 are blocked by other timing-critical signals. In this case, a design with traditional SM switches would be required to take a longer route, but a SM design with more local interconnects (4 in this example) can still provide a downward path for this route.

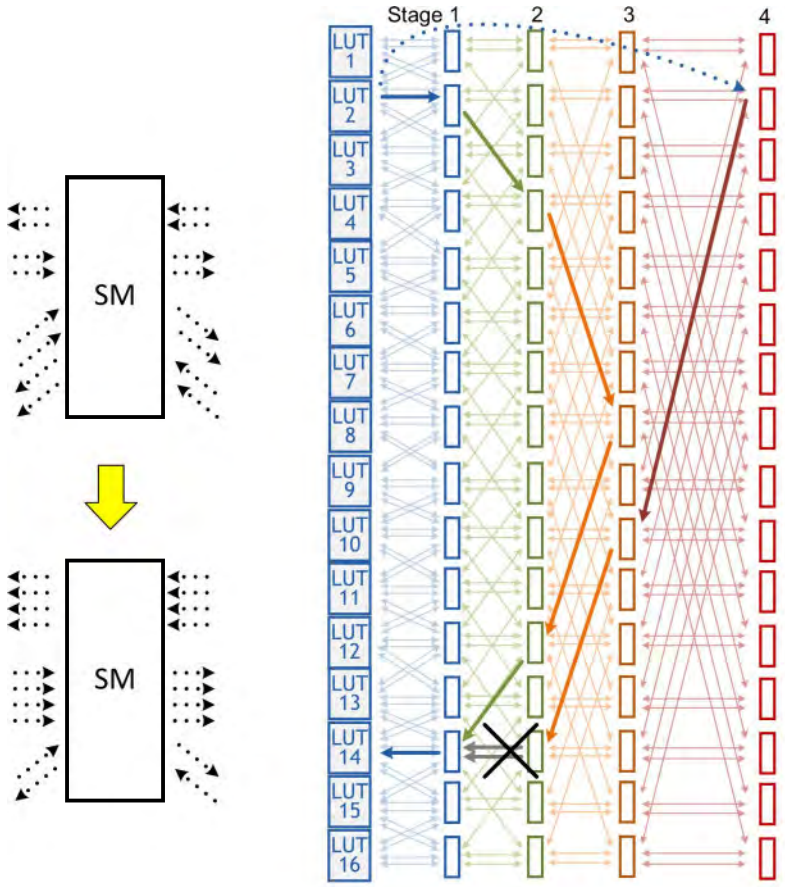



Figure 3.12: An example where traditional-Beneš based SM experiences local interconnect congestion, whereas a SM design with more local interconnects can utilize the fast path.

An example SM design with 4 local interconnect and 1 branch interconnect is shown in Figure 3.13. When implemented as a SM macro, the local interconnects are contained inside the macro. Compared to the traditional-Beneš based SM design, the new design reduces the interconnect wiring in and out of the macro by 50%, but doubles the local interconnects. Such SM design is very effective for upper-level SMs where the branch interconnects are expensive. This essentially follows the same optimization strategy from Section 3.5: it adds more wires and uses simpler muxes when the wire cost is low, but use larger muxes and fewer wires when the wire costs are high.

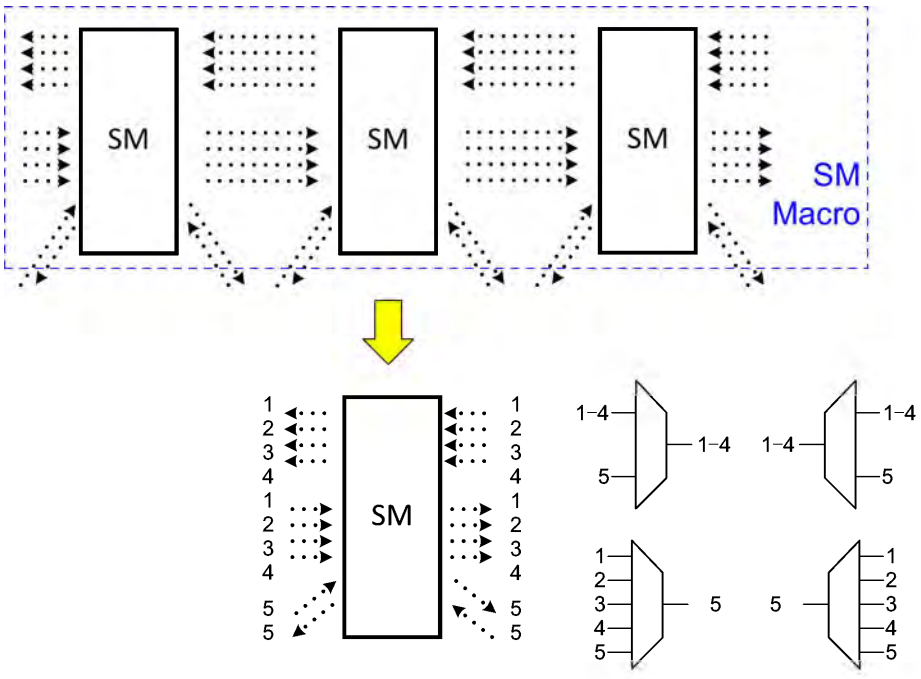



Figure 3.13: A switch-matrix example with more local interconnects than branch interconnects.

## 3.7 Micro-architecture of a Switch Matrix

A switch matrix (SM) is the most commonly used building block in the hierarchical FPGA – our FPGA has more than 10x as much SMs as LUTs. It is therefore important to have an SM design that is as small as possible, yet provides sufficient connectivity. Figure 3.14 shows an example SM micro-architecture of a radix-3 SM used in our most recent FPGA (details in Section 3.8). Not surprisingly, a SM consists of simply of a collection of muxes. The number of SM outputs determines the number of muxes it needs, but we need to carefully decide how much connectivity to build into each mux, for that has a large impact on the SM area, which has a significant impact on the final chip area.

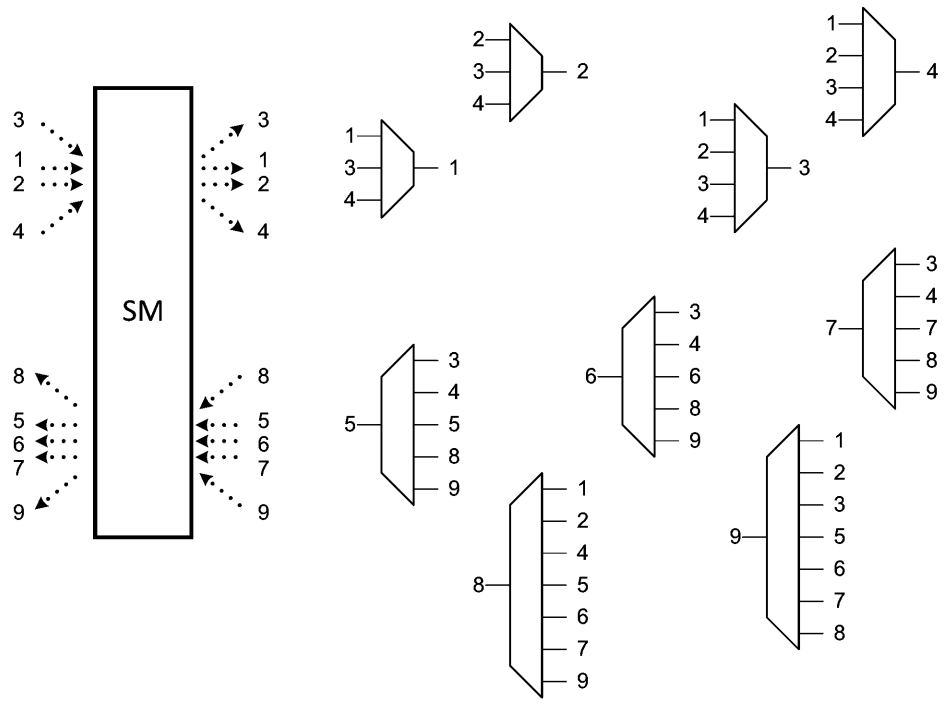



Figure 3.14: Internal mux interconnect of an example radix-3 switch matrix.

In Figure 3.14, signals 1–4 are upstream signals. Signals 1 and 2 travel internally inside the SM macro, and signals 3 and 4 are branches. From the mux design of 1 and 2, we see the first pruning heuristic: muxes 1 and 2 are allowed to propagate only signals 1 and 2 upwards, respectively, and both 3 and 4 are allowed. This is because outputs 1 and 2 travel in the same path. Not allowing switching between paths 1 and 2 has minimal impact on routing results, but reduces the mux complexity for 1 and 2. Using this simplification, the incoming signal from branch 3 and 4 will be assigned to path 1 or 2 (or both if decided by the router), and remain in the assigned path until it branches out again.

Similar approach applies for the downward paths: incoming signals can be assigned downward paths 5, 6, or 7, and are not allowed to switch between these paths until the signal branches out again. For U-turns, another simplification can be made. For example, there is no need to U-turn from input 1 and 2 back down to output 5, 6, or 7, because they come from the

same SM. There is never a need to ascend one hierarchy and U-turn back to the same SM. Similarly, output 8 travels back to the same SM that input 3 is coming from, so there is no need to performance that U-turn either; the same case applies to output 9 and input 4.

These micro-architectural techniques are effective in reducing SM complexity, thus reducing area and improving mux performance. But even with these techniques, the muxes still poses a large overhead on area and performance. Many circuit-level techniques are applied to implement these SMs efficiently, as discussed in Chapter IV.

## 3.8 Implementing a 16K-LUT FPGA Interconnect

In the previous 2048-LUT FPGA chip (Section 3.2), the architecture was optimized manually, and two types of SMs are utilized. To fully demonstrate the scalability of hierarchical interconnects, the new FPGA has expanded the interconnect architecture by 10x. Since there is no theoretical method to calculate the optimal connectivity at every level of the hierarchy, we have also developed a software tool to map designs onto our architecture (Chapter VI), which allows us to explore the optimal interconnect architecture using an iterative, closed-loop design process: we explore different architectures by mapping benchmarks and commonly-used designs, then examine the interconnect usage across different SM stages and locations, then refine the architecture accordingly and perform the mapping process again.

This FPGA consists of 16K "LUTs" arranged on a 64×320 array. Because it is a heterogeneous FPGA (Chapter V), each "LUT" is limited not to a look-up table, but is more like a SM macro that provides I/O capabilities: in this case, each SM macro provides 5 inputs and 2 outputs to any CLBs, logic, memory, DSP, or others. For example, a SLICE L CLB contains 30 inputs and 12 outputs, it therefore requires 6 SM macros to implement its interconnect; on the

other hand a DSP CLB requires 165 inputs and 66 outputs, requiring 33 SM macros in a 3×11 array.

The SM architecture of the 16K-LUT FPGA is shown in Figure 3.15 and 3.16. Figure 3.15 illustrates the lower 10 SM levels on a 1-dimensional drawing, although physical implementation is 2-D. Figure 3.16 illustrates the top-level physical architecture, highlighting wiring for the top 5 SM stages. The SM architecture is symmetrical across horizontal bisection, and is composed of 7 types SM macros, ranging from 10 to 14 stages of SM. The bottom 10 stages of SM are common across all SM macros, and are illustrated in Figure 3.15.

The CLB-input requirements in this chip ranges from 30, 35, 165, or 180 inputs, therefore the switch matrix in this architecture is chosen to contain 5 inputs and 2 outputs as a common denominator. From Figure 3.15, it shows each LUT to provide 5 inputs and 4 outputs, that is because each output is multi-casted to both local and branch interconnects, similar to the multi-cast concept from Section 2.4. The bottom 5 stages of the SM utilizes boundary-less radix-3 interconnect, providing short routing distance to neighbors and providing extra path diversity for the network. Above stage 5, we transition back to a radix-2 network to save interconnect area. Additionally, having all radix-3 network in all hierarchies would make the entire architecture boundary-less, which drastically increases place-and-route time. The current timing-driving routing algorithm is based on breadth-first search, and by having radix-2 in the upper hierarchies, the P&R tool is able to converge more quickly due to its reduced search radius. From our P&R evaluations, a radix-3 to radix-2 transition at SM stage 5 provides sufficient path diversity and routing performance.

This SM architecture uses 2 local interconnects per SM on the upward path, but 3 local interconnects per SM on the downward path. This is due to the assistance of fast-path, which

allows many signals to travel directly from the LUT output to the upper-level SM without occupying local interconnects along the way. This alleviates the routing congestion upwards, but does not alleviate the congestion downwards (the fast-path signals still need to traverse downwards on regular interconnects).

Another key distinction between the lower 5 SM stages and upper stages are the upward branch interconnects. From Figure 3.15, we the lower 5 SM stages to have branching on the upward path, but above stage 5, upward branching has been pruned, and only local upward interconnects remain. The exception is for SM stages 10, 11, and 12, for those stages allow the SM to branch upwards upon the termination of the SM macro. As shown in Figure 3.15, the SMs on the bottom half only have 9 stages, and therefore must branch into the SMs on the top half at stage 10 to continue signal propagation, else the signal would reach a "dead-end". This pruning methodology trades off local vs. branch interconnects: it allows branching when the wire costs are low, therefore providing more path diversity, but for the upper hierarchies, path diversity is sacrificed to reduce interconnect congestion and gate area. However, local interconnects are not pruned even for upper hierarchies, because those wire costs remain low, and having 3 local interconnects on the downward paths provides additional path diversity without increasing the area significantly.

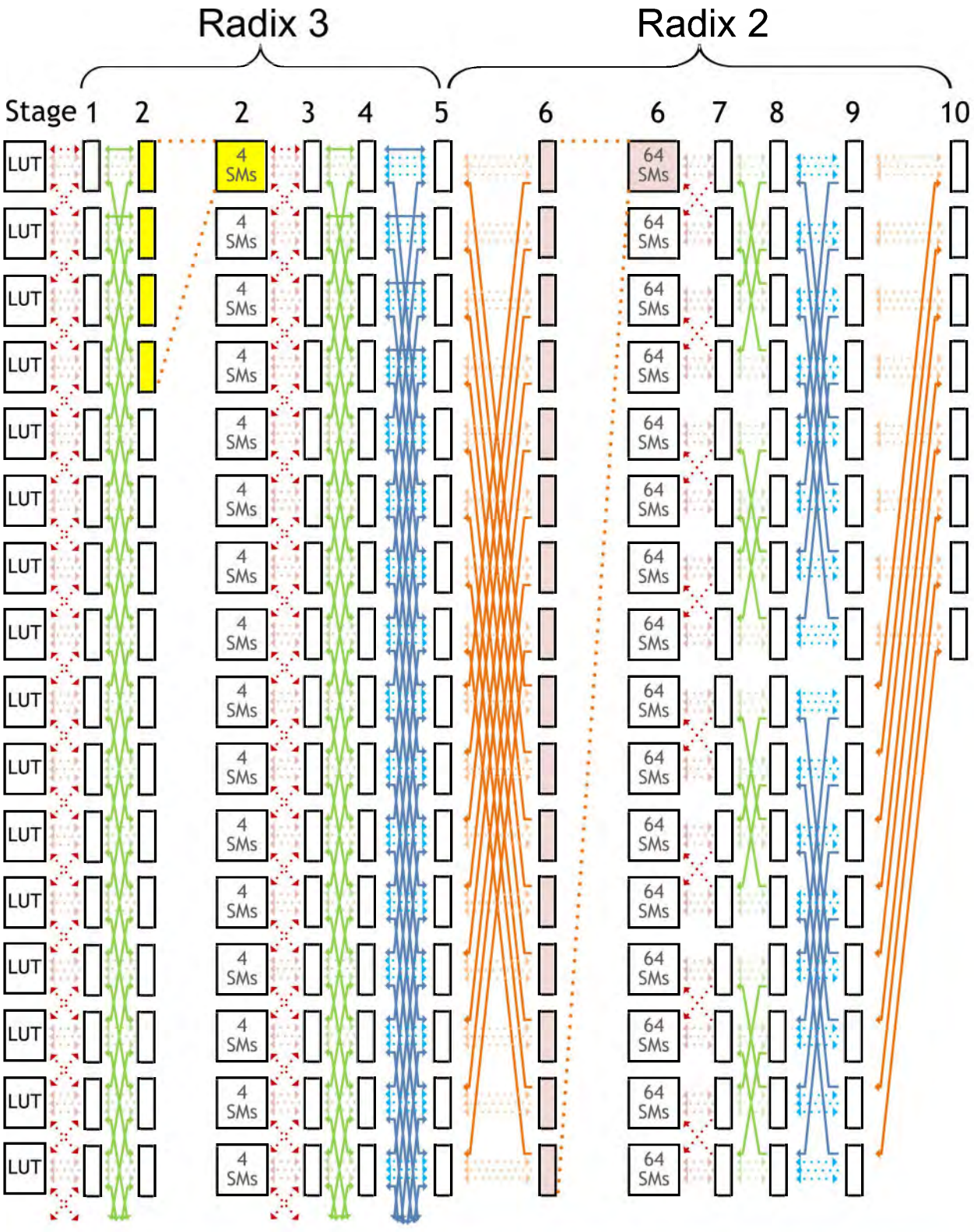



Figure 3.15: 1-D SM architecture of the 16K-LUT FPGA, showing the lower 10 SM stages.

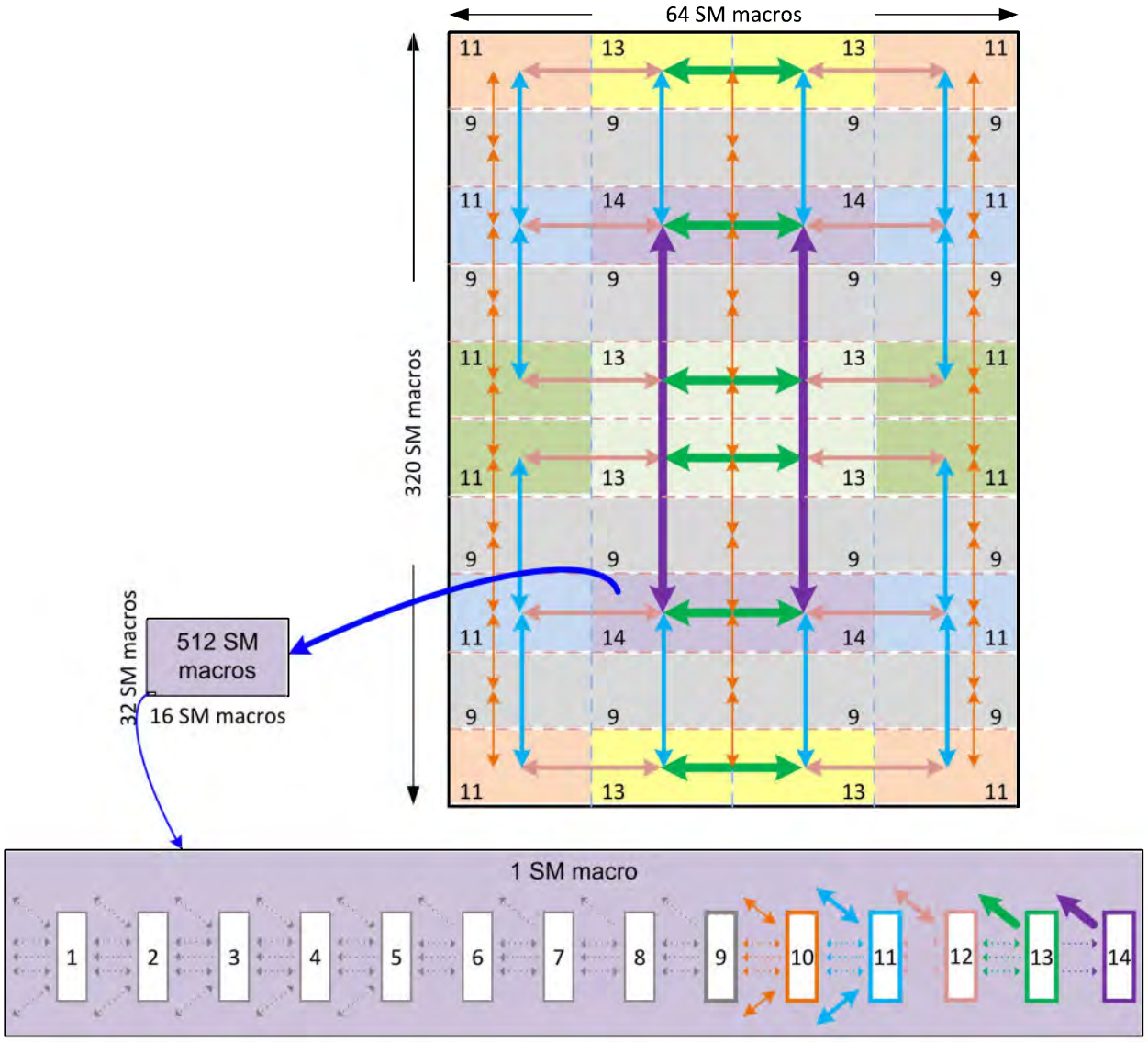



Figure 3.16: 2-D SM architecture of the 16K-LUT FPGA, showing the top 5 stages of wiring.

In the top level, the SM architecture is divided into 40 macros, each containing 512 SM macros. From the iterative interconnect optimization process, we"ve converged to an architecture shown in Figure 3.16. There are 7 types of SM macros, shown in 7 different colors. The most commonly-used SM macro has 9 stages, spanning across rows 2, 4, 7, and 9. The remaining SM macros have 11, 13, or 14 stages of SM (labeled in Figure 3.16). The largest SM has 14 stages, shown in the inset of Figure 3.16. These SMs reside in the center of the top and bottom halves of

the network.

Figure 3.16 also illustrates the mixed-radix implementation in the top level. SM stages 10 and 11 are actually radix 3, but are not boundary-less (with the exception of some stage-10 routing that crosses the horizontal bi-section). This is partially because the number of rows (320) is not a radix-2 number. Without utilizing radix-3 SM, another stage of SM would be required. However, since 320 is not much larger than 256, adding a SM stage appears wasteful. The other reason is due to the wiring cost of stage-14 routing, which needs to span half the height of the FPGA. This results in very long wires, and are very expensive to buffer. To reduce the requirements on the number of stage-14 routing, boundary-less stage-10 routes are implemented along the horizontal bisection. This addition allows gates that are placed near the horizontal bisection to use the shorter, and faster, stage-10 routing. Only the gates that are required to communicate across the entire chip need to occupy stage-14 routing.

The final architecture in Figure 3.16 is arrived through extensive iterative improvements to the architecture. The automated P&R flow (Chapter VI) greatly expedited the evaluation process, and gives us confidence in the routability and performance of the optimized design. The architecture techniques discussed in 3.3−3.6 have greatly improved the routing quality of the interconnect network, and reduced interconnect area. Although we have expanded from 3 types of SM macros to 7, it remains a feasible implementation. The circuit-level implementation of the interconnect are detailed in Chapter IV, and the physical integration details are discussed in Chapter V.

## 5.5 Coarse-Grained CLBs for the 16K-LUT FPGA

Since this chip primarily targets high-throughput communication applications, we have integrated two coarse-grain accelerators. The first block is a 16-core, highly-efficient communications DSP accelerator, reconfigurable to perform many common communications algorithms very efficiently. The 16-core architecture is illustrated in Figure 5.15. Core-to-core communications utilize both local, fast-path interconnects running vertically and horizontally, as well as a 4-stage hierarchical interconnect network spanning the 16 cores.

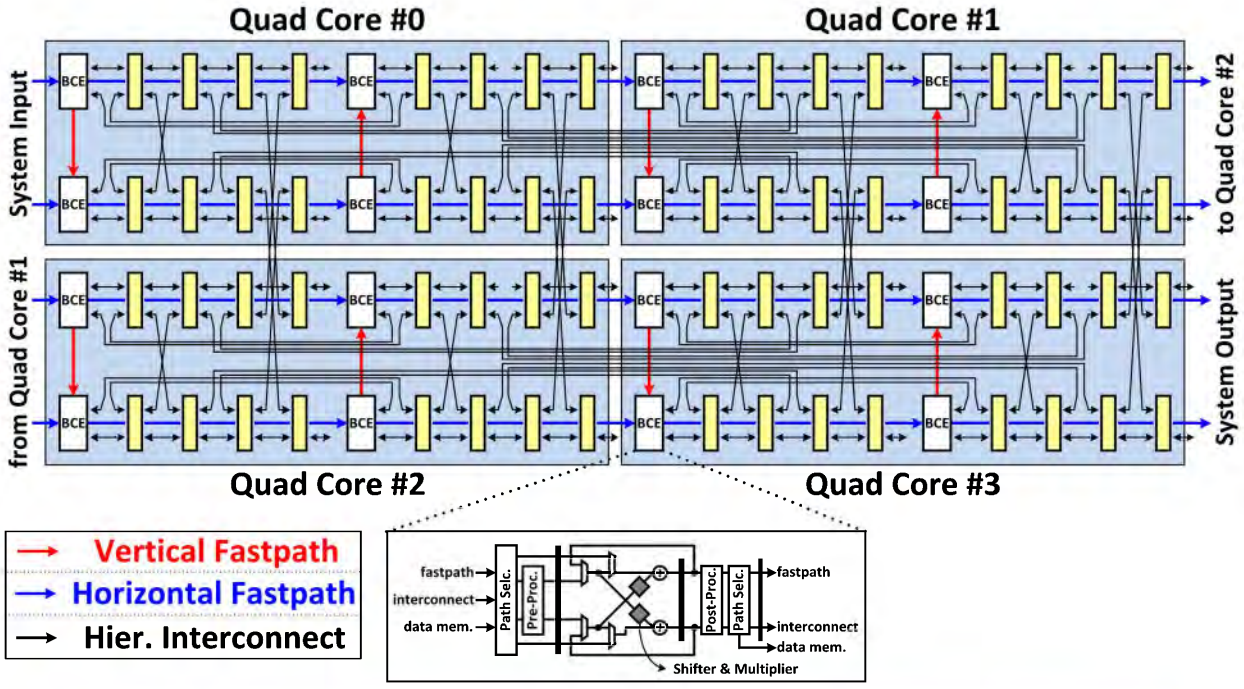



Figure 5.15: Core schematic and interconnect architecture of a 16-core DSP processor.

Each core is realized using radix-2 butterfly architecture, performing 2×2 matrix computations, called a butterfly-computation element (BCE). This provides the versatility for various fundamental 2×2 operations, e.g. permutation, CORDIC, multiplication-and-accumulation (MAC), unitary transformation, etc. Higher level of integration such as multi-stage pipeline is achievable with multiple cores. Each BCE is designed to be run-time reconfigurable

reached the bottom hierarchy, resulting in a partition size of 1 CLB. The corresponding CLB is then placed in the current partition.

## 6.4 FPGA Routing

Due to the large overhead of interconnect area, FPGA routing is performed on very limited routing resources. In our hierarchical FPGA design, the interconnect architecture is also designed to provide just sufficient routing resources to avoid area waste. As a result, FPGA routing places large emphasis on the quality of the software router. The router need to not only resolve all routing congestions, minimize critical-path, and complete the task in a reasonable (hours of less) run-time even for large designs.

As shown in Figure 6.5, the hierarchical interconnect architecture was implemented to have many path diversities, therefore improving connectivity. However, not all paths result in the same timing performance, as illustrated by the routing preferences. It is generally preferred to travel the shortest routings, using fast-path whenever possible, to reduce overall interconnect capacitance. But in the case of routing congestion, re-routing must be done, and some nets may be required to take non-preferred routes.

Modern routers generally employ global routing before detailed routing. The purpose of global routing is to provide a best-case timing performance of the design, and to estimate routing congestion. Being agnostic to routing congestion, the router is able to perform global routing very quickly, such as using the shortest-path algorithm [Nair82] and [Nair87]. In our hierarchical interconnects, the hierarchical architectures allows for very deterministic global routing. The router may utilize fast-path to perform no branching on the upward path, make a U-turn at the required hierarchy, and the downward path is very deterministic (computed by the radix-2

boundaries).

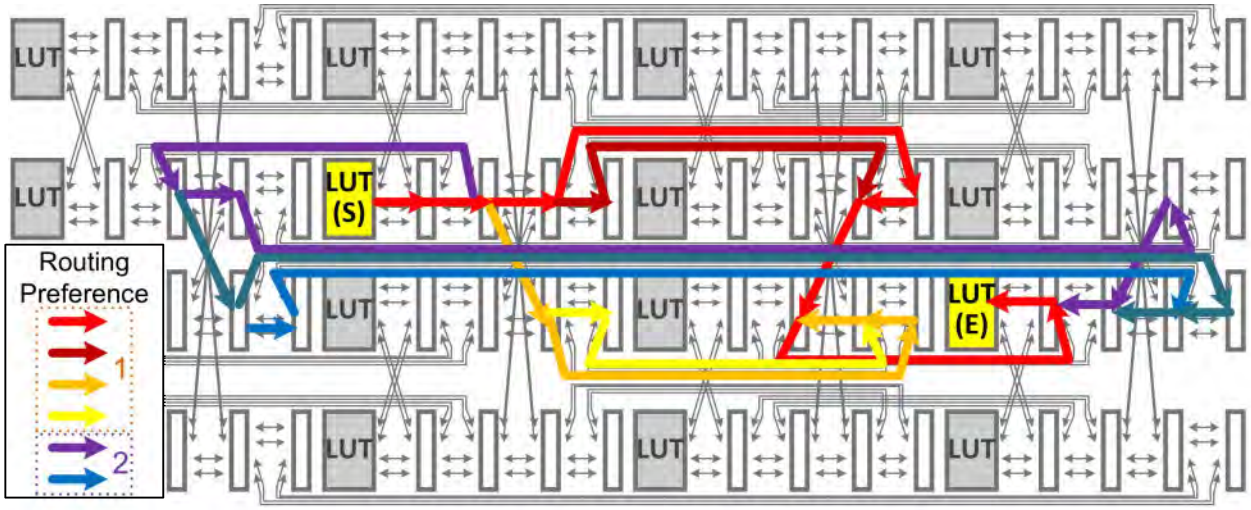



Figure 6.5: A routing-preference example for a point-to-point connection, LUT (S) to LUT (E).

Global routing gives the router valuable information, such as timing feasibility and routing congestion, but all congestions must be resolved for the design to be realizable. The initial version of our router employs rip-up-and-reroute detailed routing to resolve routing congestions [Dees81]. However, the algorithm we implemented was not timing-driven, and is dependent on the routing order of the nets. Therefore the routing results often have inconsistent timing, and sometimes fail to converge. Unsatisfied with our routing results, we implemented a new routing algorithm to the PathFinder router [McMurchie95, Ebeling95].

The PathFinder is a negotiation-based router that iteratively improves routing congestion by de-touring the lesser-performance-critical gates. It is able to incorporate global routing and detailed routing into a unified algorithm. The first iteration of the router is performed only based on interconnect delay, and not routing congestion, resulting in a minimum-delay design with many routing conflicts. However, the router does not attempt to rip-up the conflicting nets, instead it reroutes the design iteratively, but each successive iteration places a higher cost on routing conflicts. Eventually, the cost of routing through a faster, congested net will outweigh the

# EXHIBIT 23

Gmail

**Venkat Konda <venkat@kondatech.com>**

# Flavio Bonomi invited you to “Venkat-Dejan-Cheng-Flavio”.

**Flavio Bonomi** <noreply@insideicloud.icloud.com> Mon, Jan 27, 2014 at 8:20 PM
Reply-To:
2_BY44MNPXOICCUP7BIC6F3MIIUYAMF2WP2UM7TNOZEUIJR6ZTORNA3JBBOJCQQIB6EO6FKOHUDO5B4@imip.me.com
To: venkat@kondatech.com


## Flavio Bonomi invited you to “Venkat-Dejan-Cheng-Flavio”.

| | |
|---|---|
| when | Tuesday, January 28, 2014, 4:30 PM - 6:00 PM |
| location | Flavio's Office<br>526 Lowell Ave<br>Palo Alto CA 94301 |
| invitees | **Cheng Wang, Dejan Markovic** and you.<br>See replies… |

**Accept** **Decline** **Maybe**

iCloud



**iCal-20140127-202012.ics**
5K

# EXHIBIT 24

## 27.5 A Multi-Granularity FPGA with Hierarchical Interconnects for Efficient and Flexible Mobile Computing

Cheng C. Wang[1], Fang-Li Yuan[1], Tsung-Han Yu[2], Dejan Markovic[1]

[1]University of California, Los Angeles, CA, [2]Qualcomm, Irvine, CA

Following the rapid expansion of mobile computing in the past decade, mobile system-on-a-chip (SoC) designs have off-loaded most compute-intensive tasks to dedicated accelerators to improve energy efficiency. An increasing number of accelerators in power-limited SoCs results in large regions of "dark silicon." Such accelerators lack flexibility, thus any design change requires a SoC re-spin, significantly impacting cost and timeline. To address the need for efficiency and flexibility, this work presents a multi-granularity FPGA suitable for mobile computing. Occupying 20.5mm$^2$ in 40nm CMOS, the chip incorporates 2,760 fine-grained configurable logic blocks (CLBs) with 11,040 6-input look-up-tables (LUTs) for random logic, basic arithmetic, shift registers, and distributed memories, 42 medium-grained 48b DSP processors for MAC and SIMD operations, 16 32K×1b to 512×72b reconfigurable block RAMs, and 2 coarse-grained kernels: a 64-8192-point fast Fourier transform (FFT) processor and a 16-core universal DSP (UDSP) for software-defined radio (SDR). Using a mix-radix hierarchical interconnect, the chip achieves a 4× interconnect area reduction over commercial FPGAs for comparable connectivity, reducing overall area and leakage by 2.5×, and delivering a 10-50% lower active power. With coarse-grained kernels, the chip's energy efficiency reaches within 4-5× of ASIC designs.

Although commercial FPGAs can come close to ASICs in performance, they are highly inefficient due to their high energy and a large area overhead. This is mainly due to the programmable interconnect. For over 20 years, a 2D-mesh network has been the backbone of FPGA interconnect, but full connectivity in a 2D mesh requires O(N$^2$) switches, requiring interconnects to grow faster than Moore's Law O(N). As a result, various heuristics are used to simplify switches at the cost of resource utilization, but the interconnect area is still ~4× the logic area in modern FPGAs. By effectively pruning a Beneš network, a hierarchical interconnect network is realized where the number of switches is less than O(N·logN), allowing us to maintain an interconnect-to-logic-area ratio of 1:1.

The O(N·logN) complexity of Beneš network is well-known in telecommunications, but such a network is seldom used in hardware primarily due to its implementation complexity. In a traditional Beneš, wirelength doubles for every stage. With an equal number of wires for all stages, this leads to long, congested wires in the upper hierarchies. An efficient implementation requires pruning the upper hierarchies, and we alternate the routing in the x- and y-directions so wirelength doubles every *two* stages [1]. Another drawback is the delay across radix boundaries. As shown in Fig. 27.5.1, communication between neighboring computing elements (CE) 4 and 5 requires 3 hierarchies. A boundary-less radix-3 network is created to restore spatial locality by shifting all local connections to the lower switch matrices (SMs). In the simplified illustration, radix-3 SMs are used in the lower stages to increase local bandwidth, allowing even fewer radix-2 SMs in the upper hierarchies. For improved timing and reduced power, fast-path routing allows hops directly to the required hierarchy level, routing only half the network on the return path. Our router automatically assigns fast-path interconnect based on congestion and timing.

Boundary-less radix-3 SMs are used in the lower 5 hierarchies (Fig. 27.5.2), and pruned radix-2 switches are used from stage 6 to 14, except stage 10 and 11. Stage 10 employs boundary-less radix-3 across the horizontal bisection to improve bisection bandwidth. The top-level connectivity (stage 14) is pruned to only 5%. This is a result of closed-loop optimization by mapping various FPGA benchmarks, then pruning or expanding each stage based on congestion and performance. To ease physical design, the chip is divided into 40 interconnect regions, each with 512 SM macros, with 9 to 14 stages per SM macro.

The fine-grained and medium-grained CLBs offer behavior identical to commercial FPGAs, allowing for a direct comparison of interconnects by executing identical netlists. To target common communications designs, two coarse-grained kernels were implemented. A 64-8192-point reconfigurable FFT is beneficial for digital baseband processing. It has a small dedicated memory, and interconnects to the FPGA memory to realize the long delay lines for 2048-8192-point FFTs. A 16-core UDSP targets a variety of SDR algorithms, where each core is reconfigurable for arbitrary 2×2 matrix operations using a flexible instruction-set architecture. Unlike the medium-grained DSP processor, the 2×2 butterfly core in the UDSP is very efficient for complex arithmetic, capable of many SDR functions, such as filtering, equalization, CORDIC, and sphere decoding by simply concatenating multiple butterfly stages. FFT and UDSP both connect to the interconnect network.

Power gating (PG) is desirable for large chips, but each interconnect signal often traverses many blocks, making block-level PG ineffective. A fine-grained PG is needed for individual switches. Traditional PG becomes very inefficient because the footer PG transistor is no longer shared by the entire block, so it cannot be made very large (Fig. 27.5.3), but a smaller footer can degrade performance by 30-50%. To power gate without a footer, a PG branch is added to the mux, and the pass-gate is separated into NMOS and PMOS segments, where enabling PG leaves the output floating, reducing the coupling capacitance on neighboring wires. When conducting, the NMOS segment is driven by PMOS pass-gates, thus it can rise much faster than the PMOS segment driven by NMOS pass-gates, which settles to $V_{DD}$-$V_t$ (and vice versa). This results in larger transient leakage, but does not degrade performance significantly, because the output current is the *difference* of the pull-up and pull-down branches. A small high-$V_t$ keeper pulls together the NMOS and PMOS voltages to overcome the $V_t$ drop. This results in a 5-10% performance penalty, but reduces leakage by more than 50% (now gate-leakage dominated). The output floats during PG, so it cannot drive a CMOS gate, but can only enter a pass-gate that can be disabled during PG. Over 90% of the switches utilized this PG scheme, except those driving long wires that require buffer insertion.

With over 9 million configuration bits, an automated mapping tool is developed. The tool supports two modes (Fig. 27.5.4). Mode 1 maps an identical netlist as used by commercial FPGAs for a direct comparison of performance, power, and area utilization: the user design is first synthesized using commercial tools, then the output netlist is parsed into our custom tool, which performs timing analysis, floorplan, placement, routing, and bitstream generation for our FPGA. Mode 2 incorporates our coarse-grained kernels into the P&R flow. Although the configuration SRAM cells are distributed throughout our FPGA, their word-lines (WL) and bitlines (BL) are organized as one large memory for easy initialization. The FPGA core can only be powered on after configuration finishes.

Measurement results of our FPGA with CLBs, and with coarse-grained kernels are compared against processors, a commercial FPGA, and an ASIC (Fig. 27.5.5). Although the CLBs alone achieve over 1.5GOP/mW, an energy efficiency of 0.86GOPS/mW is achievable when mapping an FIR filter, which is 4× more efficient than commercial FPGA (both in 40nm). An 8× efficiency gain can be achieved by using UDSP kernels. FFT operations, which are dominated by memory and control, are 13× more energy efficient when mapped to the FFT kernel instead of CLBs. A 2-2.5× reduction in leakage is attained from smaller chip area and fine-grained PG, even with the disadvantage of dual-oxide transistors. Our chip is built with standard-cells, yet we are often within 20% of the performance of high-end FPGAs, though our software is still improving.

With efficient interconnect, our FPGA is within 20× of ASIC efficiency for most designs (Fig. 27.5.6). Coarse-grained kernels further improve the efficiency, bringing it within 4 to 5× of ASICs. The key to coarse-grained efficiency is to identify compact, reconfigurable kernels that improve efficiency, apply to a variety of applications, and leverage existing FPGA resources where possible. Our chip (Fig. 27.5.7) is able to attain the energy efficiency suitable for mobile applications while maintaining the full flexibility of an FPGA.

*Acknowledgments:*
The authors thank Dr. Sanjay Raman and DARPA for funding support.

*References:*
[1] C.C. Wang, *et al.*, "A 1.1 GOPS/mW FPGA Chip with Hierarchical Interconnect Fabric," *IEEE Symp. VLSI Circuits*, pp. 136-137, 2011.
[2] Z. Yu, *et al.*, "An 800 MHz 320 mW 16-Core Processor with Message-Passing and Shared Memory Inter-Core Communication Mechanisms," *ISSCC Dig. Tech. Papers,* pp. 64-65, 2012.
[3] "FFT Implementation on the TMS320C5535 DSP," *TI Technical Reference Manual*, pp. 111-134, 2012.
[4] T-H. Yu, *et al.*, "A 7.4 mW 200 MS/s Wideband Spectrum Sensing Digital Baseband Processor for Cognitive Radios," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2235-2245, 2012.
[5] F-L. Yuan, *et al.*, "A 256-Point Dataflow Scheduling 2x2 MIMO FFT/IFFT Processor for IEEE 802.16 WMAN," *Asian Solid-State Circuits Conf.*, pp. 309-312, 2008.
[6] J. Thompson, *et al.*, "An Integrated 802.11a Baseband and MAC Processor," *ISSCC Dig. Tech. Papers,* pp. 126-127, 2002.

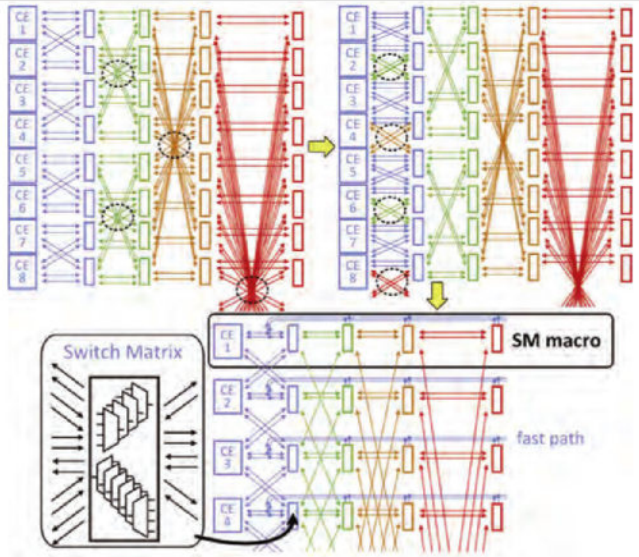



Figure 27.5.1: A boundary-less radix-3 Beneš network.

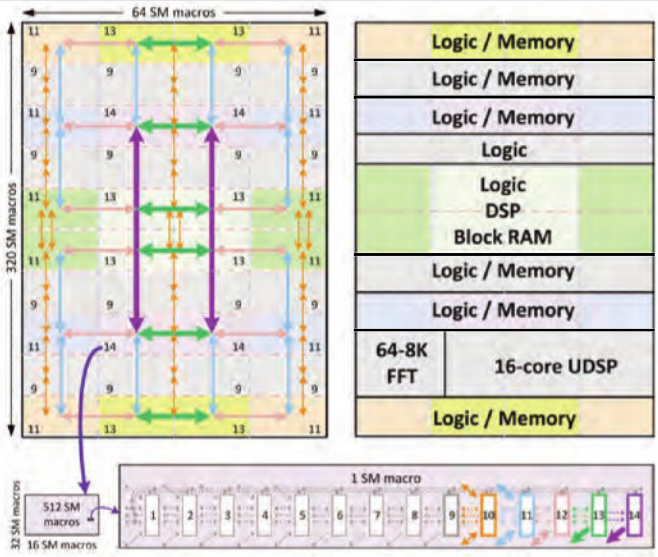



Figure 27.5.2: Interconnect and resource allocation.

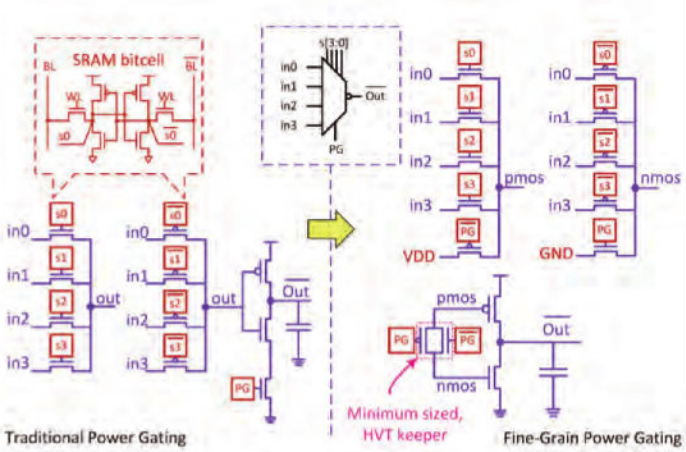



Figure 27.5.3: Multiplexer with traditional and fine-grain PG.

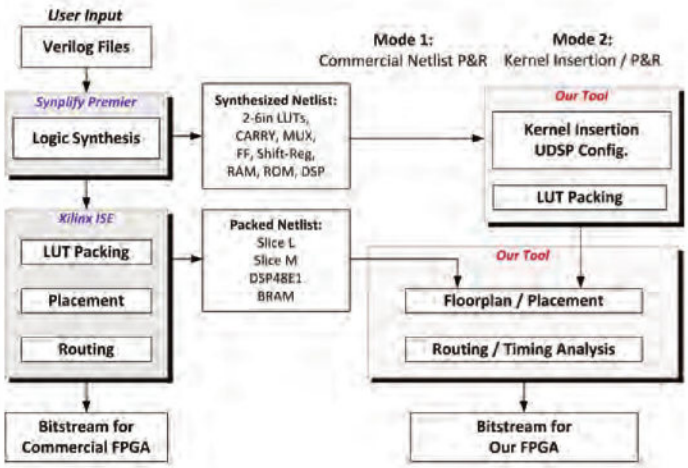



Figure 27.5.4: Automated place-and-route flow (2 modes).

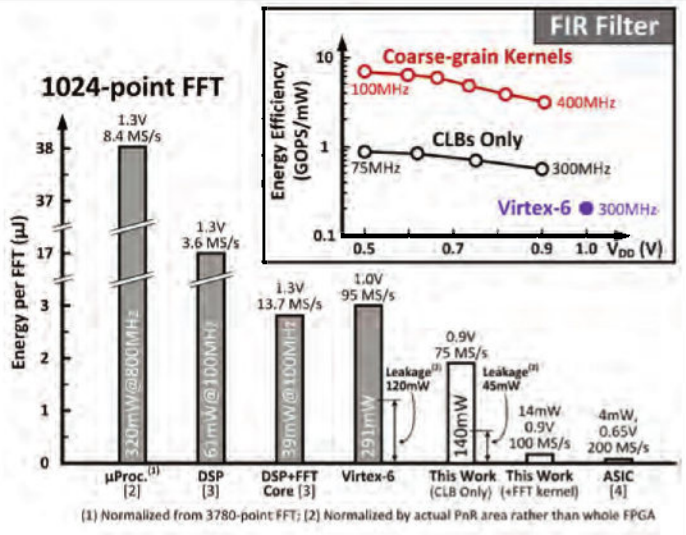



Figure 27.5.5: Comparisons of throughput and efficiency.

Fine-grain and Medium-grain CLBs Only

| Resources | Utilization | | | Virtex-6* | | This Work | | ASIC | | | Energy Eff. gap vs. ASIC (norm.) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | L/M | DSP | BRAM | Freq. (MHz) | Power (mW) | Freq. (MHz) | Power (mW) | Freq. (MHz) | Power (mW) | Tech. (nm) | |
| | 2760 | 42 | 16 | | | | | | | | |
| 256-point MIMO FFT [5] | 916 | 4 | 4 | 180 | 270 | 140 | 135 | 64 | 25 | 180 | 12× |
| | | | | | | 80 | 48 | | | | |
| K-best + depth first Sphere Decoder | 1255 | 0 | 0 | 200 | 250 | 140 | 129 | 16 | 3 | 90 | 15× |
| | | | | | | 70 | 58 | | | | |
| Software-Defined Radio Tx Front End | 1594 | 38 | 0 | 39 | 287 | 35 | 213 | 60 | 50 | 65 | 13× |
| | | | | | | 23 | 117 | | | | |
| 802.11a Rx Baseband [6] | 1824 | 0 | 6 | 66 | 271 | 55 | 219 | 20 | 203 | 250 | 15× |
| | | | | | | 20 | 60 | | | | |

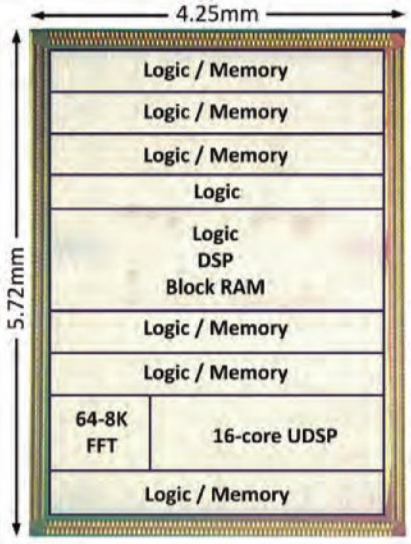
*The Virtex-6 (6VLX75T) FPGA has 11640 Slice L/Ms, 288 Slice DSPs, and 156 BRAMs.

CLBs and Coarse-grain Kernels

| Resources | Utilization | | | FFT | UDSP | This Work | | ASIC | | | Energy Eff. gap vs. ASIC (norm.) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | L/M | DSP | BRAM | | | Freq. (MHz) | Power (mW) | Freq. (MHz) | Power (mW) | Tech. (nm) | |
| | 2760 | 42 | 16 | 1 | 16 | | | | | | |
| Software-Defined Radio Tx Front End | 664 | 26 | 0 | 0 | 12 | 80 | 166 | 60 | 50 | 65 | 4× |
| | | | | | | 30 | 50 | | | | |
| 802.11a Rx Baseband [6] | 701 | 0 | 6 | 1 | 5 | 60 | 88 | 20 | 203 | 250 | 5× |
| | | | | | | 20 | 21 | | | | |

Figure 27.5.6: Example designs and ASIC efficiency gap.

27




| | |
|---|---|
| Technology | 40nm 1P10M CMOS FO4 16.3ps (TT) |
| Core $V_{DD}$ | 0.5 to 0.9V |
| Frequency | ≤ 400 MHz |
| Energy Efficiency | ≤ 7 GOPS/mW |
| I/Os | 350 bidirectional (171 bonded) |
| Core Size | 3.8mm × 5.3mm |
| Transistor Count | 143 million |
| L/M CLB | 2176 Logic 576 Memory |
| DSP CLB | 42 MAC/SIMD Processor |
| Block RAMs | 16 36Kb BRAM |
| Config. Bits | 9,279,168 |

**Figure 27.5.7: Die micrograph and chip summary.**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# EXHIBIT 25

Gmail **Venkat Konda <venkat@kondatech.com>**

# Re: Thank you for the Meeting of IP topics: Memoir Systems, Konda Technologies, Hier Logic

**Dejan Markovic** <markovic@stanford.edu> Wed, Mar 5, 2014 at 8:17 PM
To: Venkat Konda <venkat@kondatech.com>
Cc: Sundar Iyer <sundaes@memoir-systems.com>, Chengcheng Wang <cheng2wang@gmail.com>, Dejan Markovic <markovic@stanford.edu>, "fgbonomi@gmail.com" <fgbonomi@gmail.com>

Indeed. Thank you, Sundar. We'll be in touch.

Best regards,
Dejan

On Wed, Mar 5, 2014 at 7:47 PM, Venkat Konda <venkat@kondatech.com> wrote:

> Sundar,
>
> Thank you very much for the meeting today @ your office.
> Appreciate very much for sharing your experiences of IP Business.
> It is extremely helpful, informative, and for me some personal deja vu feelings :=).
>
> I will stay in touch.
>
> Regards,
> Venkat
>
> ---
>
> **From:** Caitlin Williams <cwilliams@memoir-systems.com>
> **To:** Dejan Markovic <markovic@stanford.edu>
> **Cc:** Venkat Konda <venkat@kondatech.com>; Chengcheng Wang <cheng2wang@gmail.com>; Sundar Iyer <sundaes@memoir-systems.com>
> **Sent:** Monday, March 3, 2014 10:28 AM
> **Subject:** RE: Meeting of IP topics: Memoir Systems, Konda Technologies, Hier Logic
>
> Dejan,
>
> Confirmed, I'll send out a calendar invite.
>
> Please note our address is: 2350 Mission College Blvd. STE 1275 (12th floor), Santa Clara, Ca. 95054
>
> Please call me @ 408 507 4118 for any last min. changes.
>
> Best Wishes,
>
> Caitlin Williams
> Memoir Systems, Inc.
> 2350 Mission College Blvd. # 1275
> Santa Clara, CA 95054
> O: +1 408 550 2382 x104
> M: +1 408 507 4118

Breakthrough Memory Performance

**From:** Dejan Markovic [mailto:markovic@stanford.edu]
**Sent:** Monday, March 03, 2014 10:24 AM
**To:** Caitlin Williams
**Cc:** Dejan Markovic; Venkat Konda; Chengcheng Wang; Sundar Iyer
**Subject:** Re: Meeting of IP topics: Memoir Systems, Konda Technologies, Hier Logic

Hi Caitlin,

Sure - Wed 4pm works.

Thanks,
Dejan

On Mon, Mar 3, 2014 at 10:23 AM, Caitlin Williams <cwilliams@memoir-systems.com> wrote:
Hi Dejan,

Can we schedule for this Wednesday (March 5th) at 4pm (PST) at Memoir's office?

Kindly let me know,

Caitlin Williams
Memoir Systems, Inc.
2350 Mission College Blvd. # 1275
Santa Clara, CA 95054
O: +1 408 550 2382 x104
M: +1 408 507 4118
Breakthrough Memory Performance

**From:** Dejan Markovic [mailto:markovic@stanford.edu]
**Sent:** Sunday, February 23, 2014 5:48 PM
**To:** Caitlin Williams
**Cc:** Dejan Markovic; Venkat Konda; Chengcheng Wang; Sundar Iyer

**Subject:** Re: Meeting of IP topics: Memoir Systems, Konda Technologies, Hier Logic

Hi Caitlin,

March 3rd is wide open, March 5th anytime after 12pm is fine.

Thanks,
Dejan

On Sun, Feb 23, 2014 at 5:18 PM, Caitlin Williams <cwilliams@memoir-systems.com> wrote:
Hi Dejan,

What is your availability on March 3rd or 5th?

Best Wishes,

Caitlin Williams
Memoir Systems, Inc.
2350 Mission College Blvd. # 1275
Santa Clara, CA 95054
O: +1 408 550 2382 x104
M: +1 408 507 4118
Breakthrough Memory Performance

---

**From:** Sundar Iyer
**Sent:** Friday, February 21, 2014 3:56 PM
**To:** Dejan Markovic
**Cc:** Venkat Konda; Chengcheng Wang; Caitlin Williams
**Subject:** RE: Meeting of IP topics: Memoir Systems, Konda Technologies, Hier Logic

[moved Flavio to bcc:]

Yes, would be great to meet together.

Caitlin -- can you co-ordinate with Venkat, Dejan and Cheng to find a mutually good time?

Cheers,
Sundar.

---

**From:** Dejan Markovic <markovic@stanford.edu>
**Sent:** Thursday, February 20, 2014 9:22 PM
**To:** Sundar Iyer
**Cc:** Dejan Markovic; Flavio Bonomi; Venkat Konda; Chengcheng Wang; Caitlin Williams
**Subject:** Re: Meeting of IP topics: Memoir Systems, Konda Technologies, Hier Logic

Sundar,

The week after next is good. Mon-Wed and Fri would work best for me.
I am fine to meet all together or separately - whichever you prefer.

Thanks,
Dejan

On Wed, Feb 19, 2014 at 12:13 PM, Sundar Iyer <sundaes@memoir-systems.com> wrote:
Flavio -- Appreciate the introduction, and it was really nice talking to you yesterday.

Venkat, Dejan -- My schedule for the coming week is really compressed. Is it possible to meet the week after next? That would take us into the first week of March? I am cc'ing Caitlin, who is my admin. If there is anything urgent, then let me know and I can pull it in.

I suppose we need two different meetings? One with Venkat and one with Dejan/Cheng Wang?

Regards,
Sundar.

Sundar Iyer
Co-founder and CEO
Memoir Systems Inc.
2350 Mission College Blvd. # 1275
Santa Clara, CA 95054
O: +1 408 841 4342
M: +1 650 575 9659
Breakthrough Memory Performance



---

**From:** Venkat Konda <venkat@kondatech.com>
**Sent:** Wednesday, February 19, 2014 11:19 AM
**To:** Dejan Markovic; Flavio Bonomi; Sundar Iyer
**Cc:** Chengcheng Wang; Venkat Konda

**Subject:** Re: Meeting of IP topics: Memoir Systems, Konda Technologies, Hier Logic

Sundar,
I heard from Flavio that you are doing great!
it has been a while since we met.

Sundar, Flavio,
Appreciate setting up this meeting.
I am fairly open.
Please propose your convenient time.

Regards,
Venkat

---

**From:** Dejan Markovic <markovic@stanford.edu>
**To:** Flavio Bonomi <fgbonomi@gmail.com>
**Cc:** Chengcheng Wang <cheng2wang@gmail.com>; Venkat Konda <venkat@kondatech.com>; Sundar Iyer <sundaes@memoir-systems.com>
**Sent:** Tuesday, February 18, 2014 11:22 PM
**Subject:** Re: Meeting of IP topics: Memoir Systems, Konda Technologies, Hier Logic

Thanks, Flavio, for the introduction.
Sundar, look forward to meeting you in person. How about sometime next week?

Best regards,
Dejan
On Feb 18, 2014 9:26 AM, <fgbonomi@gmail.com> wrote:
Sundar,

please (re)-meet Venkat Konda, of Konda Technologies, and Dejan Markovich and Cheng Wang from UCLA and Hier Logic.
I have discussed your respective technologies in face to face meetings already.

I would like to see you all meeting to share some of your experiences on IP licensing and business models.
Thanks.,
Flavio

# EXHIBIT 26

Gmail

**Venkat Konda <venkat@kondatech.com>**

# Flex-logix is Infringing Konda interconnect IP; ChengCheng Wang's UCLA PhD Dissertation is a blatant copy of Konda Technologies granted Patent(s)

**venkat@kondatech.com** <venkat@kondatech.com> Sun, Mar 27, 2016 at 5:34 PM
Reply-To: venkat@kondatech.com
To: "shirish@formation8.com" <shirish@formation8.com>, "peter.hebert@luxcapital.com" <peter.hebert@luxcapital.com>, "ceo@flex-logix.com" <ceo@flex-logix.com>, "geofftate@flex-logix.com" <geofftate@flex-logix.com>, "chancellor@ucla.edu" <chancellor@ucla.edu>, "jmurthy@seas.ucla.edu" <jmurthy@seas.ucla.edu>, "llackman@ita.ucla.edu" <llackman@ita.ucla.edu>
Cc: BV Jagadeesh <bvjagadeesh@gmail.com>, "fgbonomi@gmail.com" <fgbonomi@gmail.com>, "ram@reddyz.com" <ram@reddyz.com>, Venkat Konda <venkat@kondatech.com>, Dejan Markovic <dejan@ee.ucla.edu>

**This e-mail is sent/cc'ed to the following people:**
**Flex-Logix Technologies:**
Geoff Tate, CEO
Peter Hebert, Co-founder/Managing Director of Lux Capital
Shirish Sathaye, General Partner of Formation 8, Foundation Capital

**University of California, Los Angeles:**
Gene David Block, Chancellor
Jayathi Murthy, Dean of HS School of Engineering and Applied Science
Les Lackman, Deputy Director, Institute for Technology Advancement

**Konda Technologies, Inc:**
BV Jagadeesh, Investor, Managing Partner, KAAJ Ventures, CEO Net Scalar and Co-founder/CTO Exodus Communications.
Ram Reddy, Investor, Chairman/Founder&CEO Global Industry Analysts, President Elect & Programs' Chair TiE

Flavio Bonomi, CEO Nebilolo Technologies, Formerly Head of R&D Cisco Systems

**Subject: 1) Flex-logix is built by Infringing Konda Technologies interconnect IP!**
**2) ChengCheng Wang's UCLA PhD Dissertation is a blatant copy of Konda Technologies granted Patent(s)!**
**3) Your urgent attention/action desired!**

Respected Flex-logix board members: Geoff, Peter, and Shirish:
Respected UCLA Administrators: Gene, Jayathi, and Les:

Prof. Vaugh Betz, Dept. of Electrical Engineering, University of Toronto asked me when I visited his office on December 18, 2015, if Flex-logix is implementing Konda Technologies FPGA interconnect IP! That was a surprise and total shock to me. Since then till today I have investigated what Flex-logix has been doing.

I am Venkat Konda, Founder/CEO of Konda Technologies. A brief about Konda Technologies and me is given at the end of the email.

I am writing this email (without any legal actions) with all the details since I have tremendous respect for all the above listed People, all of you are inventors, educators, and practitioners. Konda Technologies investors know Shirish personally and also the well-known litigation attorneys I consulted with in the past few months regarding the current email subject matter know Shirish very well. Furthermore late Professor Rajiv Motwani of Stanford University introduced me to Shirish in the past and so I met/interacted with Shirish personally in the past. I believe we can resolve the issues mentioned in this mail by ourselves. And I am willing to fully cooperate from Konda Technologies side.

**Executive Summary of this mail:**

1. The core multi-stage network part of Chengcheng Wang's PhD Dissertation titled "Building Efficient, Reconfigurable Hardware using Hierarchical Interconnects" accepted in 2013 by Electrical Engineering, UCLA under the advisor Prof. Dejan Markovic is a blatant copy of Konda Technologies US Patent US 8,898,611 titled, "VLSI Layouts of Fully Connected Generalized and Pyramid Networks with Locality Exploitation".
2. The subject matter in US Patent US 8,898,611 was first submitted to USPTO by Konda Technologies in November 2, 2007 and January 1, 2008. (Complete details about Konda Technologies US Patent US 8,898,611 are given below)
    a. I first discussed about the subject matter of US Patent US 8,898,611 with Dan Avida, General Partner, Opus Capital and Prof. Serge Plotkin, Computer Science Department, Stanford University during my interactions with them in July/August 2007.
3. Dr. Flavio Bonomi introduced me to Prof. Dejan Markovic of UCLA by email and soon I talked to Dejan on the phone for the first time on January 13, 2009. With the promise that ITA/UCLA will fund Konda Technologies, Dejan Markovic invited me to UCLA in October 12-13, 2009. Dejan introduced me to Prof. Les Lackman, UCLA/ITA. And I presented Konda Technologies Technology and Business Value proposition to Prof. Lackman. The same day Dejan requested me to present Konda Technologies IP to his students, one of the student is Chengcheng Wang.
    a. Prof. Lackman rejected to fund Konda Technologies with in a day for the fact that Konda Technologies IP was developed outside UCLA. (This is a clear proof that neither Dejan nor any of his students including Chengcheng Wang have ever worked before on multi-stage networks particularly for their application/use in FPGA fabrics.
    b. I clearly told Dejan and his students that Konda IP is a patented technology and Konda Technologies is a registered California Corporation.
    c. About an year later, during August 1-10, 2010, Prof. Dejan Markovic called me on the phone and said he is applying for a DARPA BAA grant proposal and he wanted to use Konda IP in the proposal.
    d. I told him he has to get a license to use Konda IP. He said he will license Konda IP if he gets the DARPA BAA funding.
    e. He sent a BAA proposal and asked me to fill in the details with Konda IP, which I did.
    f. Later about two months later he told me that DARPA BAA grant was not approved.
    g. During this time he told me on the phone that his students are implementing published Konda IP in a test chip. I again warned him to check on the legal issues before any further use of Konda IP. His answer was as a University professor he can work on any published literature. That is how it ended there.
    h. Clearly Dejan and his students have learned about multi-stage networks and their application for FPGA Fabrics from me starting from October 12-13, 2009 and started infringing Konda IP since August 2010 if not before.

4. Since October 2010, Dejan spoke to me or met me a few times, but he never mentioned that his student Chengcheng Wang is doing a PhD Dissertation in multi-stage networks for FPGA fabrics.
    a. Most recently on January 28, 2014, I met both Dejan and Wang at Flavio Bonomi's home in Palo Alto.
    b. During the conversation they said they are in the process of raising funds to build a company but did not tell me in what product/market.
    c. Dejan however mentioned, "They may have to get a license from Konda Technologies". But did not give any further details about their company. I cautioned Dejan to check Konda Patents on the web and if they need to license Konda IP.
5. Since December 18, 2015 during my investigation of Flex-logix value proposition, I learned to my utmost shock that Chengcheng Wang got a PhD Dissertation on multi-stage interconnect for FPGA Fabrics by blatantly infringing Konda Patents. This is beyond my wildest imagination - under the guidance of Dejan Markovic, Chengcheng Wang getting a PhD Dissertation on a patent protected technology by blatantly copying Konda Patent. I have no idea what these two people were thinking and doing.
    a. I have done a thorough investigation by reading Chengcheng Wang's PhD Dissertation, Patent applications filed by them based on PhD Dissertation and Flex-logix core value proposition with the help of well-known Patent litigation attorneys.
    b. I have provided the details of infringement in a separate section in the mail below.
    c. But briefly to make the point, In PCT application of Konda Patent #4, which Chengcheng Wang cited in bibliography of his PhD Dissertation, I wrote about the existence of Konda Patent #5 in "Cross reference to the related applications" Line 19-26; Page 2 and also lines 3 - 8; page 14. Surely Chengcheng Wang must have read these lines and must have realized about Konda Patent #5.
    d. Moreover during my presentation to Dejan's students on October 12, 2009, I mentioned about unpublished Konda patents. Also briefly mentioned about locality Optimizations of Konda patent #5.
6. A few times I mentioned to Dejan Markovic that I have patent protected multi-state networks for FPGA fabrics to the extent that if anybody uses multi-stage network for FPGA fabrics will infringe Konda Patents.
    1. Both Dejan and Chengcheng ignored my statements.
    2. So there is no way Flex-logix can change their current architecture and yet build products in multi-stage networks for FPGA fabrics.
7. Relevant link on Flex-logix website http://www.flex-logix.com/take-action/
    1. SUPERIOR INTERCONNECT
        1. Flex Logix utilizes a new breakthrough interconnect architecture: less than half the silicon area of traditional mesh interconnect, fewer metal layers, higher utilization and higher performance. **The ISSCC 2014 paper detailing this technology won the ISSCC Lewis Winner Award for Outstanding Paper.** Previous recent winners of this top award include Nvidia, Bosch, Sandisk and Toshiba.
8. The above reference on Flex-logix website clearly mentions Flex-logix value proposition is breakthrough interconnect architecture.
    1. And the above quoted ISSCC 2014 paper is - **A Multi-Granularity FPGA with Hierarchical Interconnects for Efficient and Flexible Mobile Computing" authored by** Cheng C. Wang1, et.al.
    2. The first figure namely FIG 27.5.1 in this paper - A boundary-less radix-3 Benes Network, is directly coming from Chengcheng Wang's PhD Dissertation. And this concept is blatant copy from Konda Patent #5.
9. So this is clear evidence that the technology Flex-logic implemented is directly infringing Konda Patent #5 and also other Konda patents.
10. Chengcheng Wang and Dejan Markovic submitted a patent application titled "Network Architecture for Boundary-Less Hierarchical Interconnects" filed with China Patent

Application Number: 2014/80026152.7 and European Patent Application Number: 2014/765825 must be withdrawn immediately. Since they did not file a corresponding US Patent, it is clearly evident that Chengcheng Wang and Dejan Markovic are knowingly infringing Konda Patents.

11. Chengcheng Wang and Dejan Markovic have been knowingly, willfully and in spite of several warnings by me in the past years, infringing Konda Patents.
12. Flex-logix must immediately stop using, marketing and selling all products infringing Konda Technologies patents.
13. UCLA must immediately take action on the copied/plagiarized Chengcheng Wang's PhD Dissertation. Without copied Konda Patent #5, I personally would not call this a PhD Dissertation.
14. I hope Chengcheng Wang and Dejan Markovic will plead guilty (and so help you in immediate investigation of the subject matter of this email) and avoid further disrepute/disgrace to them and to the institutions/organizations they represent. Otherwise I am fully prepared with all the legal proceedings.
    1. Without written permission, implementing a patent protected IP by University professors/students is also illegal.
    2. Do these two people think implementation of infringed IP gets a PhD Dissertation and they can build an IP company?
    3. First these two people must be educated how to respect others IP before building an IP company like Flex-logix.
15. If I do not hear from you by April 8th, 2016, I would assume you are ignoring me. And I will be left with the only alternative which is to follow up with legal action.

Sincerely,
Venkat Konda
Founder/CEO
Konda Technologies Inc.
E-mail: venkat@kondatech.com
Cell # 408-472-3273

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**Details of Konda Patents Granted pdf files at the given links:**

Konda Patent #1 - US8270400 https://patents.google.com/patent/US8270400B2/en
Konda Patent #2 - US8170040 https://patents.google.com/patent/US8170040B2/en
Konda Patent #3 - US8363649 https://patents.google.com/patent/US8363649B2/en
Konda Patent #4 - US8269523 https://patents.google.com/patent/US8269523B2/en
Konda Patent #5 - US8898611 https://patents.google.com/patent/US8898611B2/en
Konda Patent #6 - This is issued in February 2016 (Not published yet as patent)
There are more patents in the pipeline.

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**Details of Konda Patent #5 that was blatantly copied by Chengcheng Wang in his PhD Dissertation:**

- **VLSI Layouts of Fully Connected Generalized Networks with Locality Exploitation**
  - Docket # M-0046 US

- US Provisional Patent Application Number: 60/984, 724
- Date Filed: November 2, 2007

- **VLSI Layouts of Fully Connected Generalized and Pyramid Networks**
  - Docket # M-0047 US
  - US Provisional Patent Application Number: 61/018, 494
  - Date Filed: January 1, 2008

- **VLSI Layouts of Fully Connected Generalized and Pyramid Networks with Locality Exploitation**
  - Docket # S-0046 PCT
  - PCT Patent Application Serial Number: PCT/US08/82171
  - Date Filed: November 2, 2008
  - Notice received from PCT that this is Withdrawn, (since I did not pay filing fee) on: February 17, 2009
  - THESE PATENTS WERE AGAIN RESUBIMITTED AS IS AS BELOW, AS THEY WERE NEVER PUBLISHED IN THE PUBLIC DOMAIN.

- **VLSI Layouts of Fully Connected Generalized Networks with Locality Exploitation**
  - Docket # M-0048 US
  - US Provisional Patent Application Number: 61/252, 603
  - Date Filed: October 16, 2009

- **VLSI Layouts of Fully Connected Generalized and Pyramid Networks**
  - Docket # M-0049 US
  - US Provisional Patent Application Number: 61/252, 609
  - Date Filed: October 16, 2009

**5) VLSI Layouts of Fully Connected Generalized and Pyramid Networks with Locality Exploitation**

- Docket # S-0048 PCT
- PCT Patent Application Serial Number: PCT/US10/52984
- Date Filed: October 16, 2010
- Published on March 14, 2013: WO 2011047368 A2

**Herein after called "Konda Patent # 5") VLSI Layouts of Fully Connected Generalized and Pyramid Networks with Locality Exploitation**

- Docket # V-0048 US
- US Patent Application Number: 13/502,207
- US Patent Number: US 8,898,611
- Date of Patent: November 25, 2014

**VLSI Layouts of Fully Connected Generalized and Pyramid Networks with Locality Exploitation**

- Docket # V-0052 US (Continuation Patent)
- US Patent Application Number: 14/522,599
- Date Filed: October 24, 2014
- Published on February 12, 2015: US 20150046895 A1

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**Details of Konda Patents #1 - 4 that were infringed by Chengcheng Wang in his PhD Dissertation:**

- **Large Scale Crosspoint Reduction with Nonblocking Unicast & Multicast in Arbitrarily Large Multi-stage Networks**
  - Docket # M-0036 US
  - US Provisional Patent Application Number: 60/905,526
  - Date Filed: March 6, 2007

- **Fully Connected Generalized Multi-stage Networks**
  - Docket # M-0037 US
  - US Provisional Patent Application Number: 60/940, 383
  - Date Filed: May 25, 2007

**Fully Connected Generalized Multi-stage Networks**

- Docket # S-0036 PCT
- PCT Patent Application Serial Number: PCT/US08/56064
- Date Filed: March 6, 2008
- Published on March 14, 2013: WO 2008109756 A1

**Herein after called "Konda Patent # 1") Fully Connected Generalized Multi-stage Networks**

- Docket # V-0036 US
- US Patent Application Serial Number: 12/530,207
- Date Filed: September 6, 2009
- US Patent Number: US 8,270,400
- Date of Patent: September 18, 2012

1. **********
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- **Fully Connected Generalized Butterfly Fat Tree Networks**
  - Docket # M-0038 US
  - US Provisional Patent Application Number: 60/940, 387
  - Date Filed: May 25, 2007

- **Fully Connected Generalized Multi-Link Butterfly Fat Tree Networks**
  - Docket # M-0040 US
  - US Provisional Patent Application Number: 60/940, 390
  - Date Filed: May 25, 2007

**Fully Connected Generalized Butterfly Fat Tree Networks**

- Docket # S-0038 PCT
- PCT Patent Application Number: PCT/US08/64603
- Date Filed: May 22, 2008
- Published on March 14, 2013: WO 2008147926 A1

**Herein after called "Konda Patent # 2") Fully Connected Generalized Butterfly Fat Tree Networks**

- Docket # V-0038 US
- US Patent Application Number: 12/601,273
- Date Filed: November 22, 2009
- US Patent Number: US 8,170,040
- Date of Patent: May 1, 2012

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- **Fully Connected Generalized Rearrangeably Nonblocking Multi-Link Multi-stage Networks**
  - Docket # M-0039 US
  - US Provisional Patent Application Number: 60/940, 389
  - Date Filed: May 25, 2007

- **Fully Connected Generalized Strictly Nonblocking Multi-Link Multi-stage Networks**
  - Docket # M-0042 US
  - US Provisional Patent Application Number: 60/940, 392
  - Date Filed: May 25, 2007

- **Fully Connected Generalized Folded Multi-stage Networks**
  - Docket # M-0041 US
  - US Provisional Patent Application Number: 60/940, 391
  - Date Filed: May 25, 2007

**Fully Connected Generalized Multi-link Multi-stage Networks**

- Docket # S-0039 PCT
- PCT Patent Application Serial Number: PCT/US08/64604
- Date Filed: May 22, 2008
- Published on March 14, 2013: WO 2008147927 A1

**Herein after called "Konda Patent # 3") Fully Connected Generalized Multi-link Multi-stage Networks**

- Docket # V-0039 US
- US Patent Application Serial Number: 12/601,274
- Date Filed: November 22, 2009
- US Patent Number: US 8,363,649
- Date of Patent: January 29, 2013

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- **VLSI Layouts of Fully Connected Generalized Networks**
  - Docket # M-0045 US
  - US Provisional Patent Application Number: 60/940, 394
  - Date Filed: May 25, 2007

**VLSI Layouts of Fully Connected Generalized Networks**

- Docket # S-0045 PCT
- PCT Patent Application Number: PCT/US08/64605
- Date Filed: May 22, 2008
- Published on March 14, 2013: WO 2008147928 A1

**Herein after called "Konda Patent # 4") VLSI Layouts of Fully Connected Generalized Networks**

- Docket # V-0045 US
- US Patent Application Number: 12/601,275
- Date Filed: November 22, 2009
- US Patent Number: US 8,269,523
- Date of Patent: September 18, 2012

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**Complete Details of infringement by Chengcheng Wang in his PhD Dissertation:**

**Details about the Teachings of Konda Patents and applications:**

1. Konda Patents # 1-3 teach about (both rearrangeably and strictly) nonblocking multicasting of various types of multistage networks including Benes network, Butterfly Fat Tree Network and numerous isometric transformations.
2. Konda Patent # 4th is major door opener for the implementation of multistage networks in FPGA fabrics using only horizontal and vertical wires. (This is major breakthrough for layouts of multi-stage networks and their isometric transformations in a 2D grid which is a key requirement for FPGA fabrics)
   a. This patent is very well acknowledged by many University professors and Industry experts.
   b. Chengcheng Wang refers to this patent in his PhD dissertation. But passingly mentions it to unprofessionally inflate the contribution of his PhD Dissertation.
3. Konda Patent #5 teaches about some key optimizations for FPGA fabrics -> Nearest neighbor connectivity for any to any neighboring CLBs/LUTs, additional connections

(pyramidal networks based connections where you can bring additional flexibility as needed).

4. Konda Patent #6 teaches lot more optimizations and savings. Not only Mux structures, but also global wires are cookie-cuttable just like traditional FPGA fabrics. Significantly more area, power, performance improvements.
5. There are more patent applications in the pipeline.
6. Konda Technologies has already non-exclusively licensed all Konda patents and applications to a few FPGA vendors who have already brought them into production in multiple generations so far.

**Details about Chengcheng Wang's PhD Dissertation and the infringement details:**

Read the chapter 3 of PhD Dissertation. (This is blatant copy of Konda Patent #5.)

1. In Bibliography, on page 153 he quoted Konda patent #4 as, [Konda08] V. Konda, "VLSI layouts of fully connected generalized networks," *WO 2008/147928*, World Intellectual Property Organization, Dec. 2008.
2. Only at one place, i.e., on Page 28, Konda Patent #4 is referred, I am copy/pasting that line. - In terms of logic connectivity, this wiring difference is an isomorphic transformation from the original network, thus the interconnect connectivity remains unchanged [Wu80, Duato02, Konda08].
    a. This is a meaningless reference. He completely downplayed the value of my Konda Patent #4, just to inflate the contribution of his PhD Dissertation.
3. The priority art date of 4th patent is 2007 but he referred to it as 2008. (minor point)
4. Chapter 3, pp 33-57, **Architecture Design of Hierarchical FPGAs** ..... .....**33**
    a. This chapter is a blatant copy of Konda patent #5. It is the core value of this PhD Dissertation. I will not call this PhD dissertation.
    b. Whereas I call 2's BW, 4's BW, 8's BW etc. and locality exploitation and illustrate including with Figs 3A-D, 4A-C, 5, 6 7, 8A-8L, PhD Dissertation calls them boundary-less radix-3 network/connections.
    c. Whereas I call additional pyramidal connections with illustrations including Fig 8A-8L, PhD Dissertation calls it as fast path.
5. As I already mentioned above, this subject matter was first submitted to USPTO by Konda Technologies in November 2, 2007 and January 1, 2008.
6. When I was doing my PhD Dissertation in early 90's, I had a constant worry "what if the idea that I got was something already invented by somebody else". And I had to throw away three excellent ideas since I later found out that they were already done and published by somebody else. Those were the pre-web days where we have to search through micro-fiches and other archaic methods.
    a. Did Wang never have that worry?
    b. Did he never check if anybody had the same idea invented by somebody before him?
    c. In his case, he also knows who he is competing with. Did he never check on Konda Patents frequently?
    d. Compared to my PhD days, today he has Web. And still he never checked if I did any follow on work?
    e. My daughter who is currently a freshman at Stanford University told me her Teaching Assistant, who is a PhD Candidate in mathematics department, for her "Linear Algebra" told her he has to throw away the idea he invented was found out to be invented already before. So Dejan, you never educate your students about checking their ideas for originality?

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**Details of Patents filed by Chengcheng Wang and Dejan Markovic based on Chengcheng Wang's PhD Dissertation and hence are directly infringing Konda Patents: (All these patent applications were assigned to UCLA, I believe)**

1. A Radix-3 Network Architecture for Boundary-Less Hierarchical Interconnects
    a. US Provisional Patent Application Number: 61/786,676
    b. Date Filed: March 15, 2013

    a. Network Architecture for Boundary-Less Hierarchical Interconnects
        1. PCT Patent Application Number: PCT/US14/29407
        2. Date Filed: March 14, 2014
        3. Published on September 18, 2014: WO 2014144832 A1

    a. Network Architecture for Boundary-Less Hierarchical Interconnects
        1. China Patent Application Number: 2014/80026152.7
        2. Date Filed: 3-December-2013

    a. Network Architecture for Boundary-Less Hierarchical Interconnects
        1. European Patent Application Number: 2014/765825
        2. Date Filed: 1-October-2014
        3. Published on 20-January-2015: WO 2014144832 A1

1. **Wang and Dejan DID NOT FILE A CORRESPONDING US APPLICATION on or after October 1, 2014 when European Patent was filed!!!**
    a. **So they surely know they cannot get it granted in US due to Konda Patent #5 which was already granted. So They MUST know that they are infringing Konda patents.**
    b. **The above two applications submitted in China and Europe must be withdrawn immediately. As prior art anywhere in the world is prior art for any patent application in any country.**

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# Konda Technologies at a Glance

- Founded in 2007, A California C Corporation
- An intellectual property company providing chip & system level interconnect technology solutions
-
- Venkat Konda PhD - CEO
- Founder/CTO Teak Technologies
- Founder/CEO Teak Networks
- Invented strictly & rearrangeably nonblocking multicast solutions for Clos, Benes, Butterfly Fat Tree Networks (Solved a ~60 year old open research problem)
- Deterministic switching fabric technologies for true QoS, low latency and multicast
- 16 years research, development and teaching in high scale, high performance interconnection networks, architectures & Scheduling; Parallel Compilers

- Masters in Electrical Engineering, IIT Kharagpur, India
- PhD in parallel computing, University of Louisville, KY
- R&D and management experience at Teak Technologies, Velio, Infineon, Mitsubishi Research Laboratories & nCube Corporation.
- Holds multiple patents in double digits in the areas of non blocking multi-stage multicast switching networks, Routing Algorithms, Layouts

# EXHIBIT 27

Gmail

**Venkat Konda <venkat@kondatech.com>**

# Flex Logix Response Re: Flex-logix is Infringing Konda interconnect IP; ChengCheng Wang's UCLA PhD Dissertation is a blatant copy of Konda Technologies granted Patent(s)

**geoff tate Flex Logix** <geoff@flex-logix.com> Thu, Apr 7, 2016 at 10:03 AM
To: Venkat Konda <venkat@kondatech.com>
Cc: Shirish Sathaye <shirish@formation8.com>, Peter Hebert <peter.hebert@luxcapital.com>, Cheng Cheng Wang <cheng@flex-logix.com>, Dejan Marković <dejan@flex-logix.com>, Neil Steinberg <neils@swpatentlaw.com>, Earl Weinstein <eweinstein@research.ucla.edu>, Chu Benjamin <BChu@research.ucla.edu>, Rita.Hao@ucop.edu, chancellor@ucla.edu, jmurthy@seas.ucla.edu, llackman@ita.ucla.edu, "Cc: BV Jagadeesh" <bvjagadeesh@gmail.com>, fgbonomi@gmail.com, ram@reddyz.com, geoff tate <geoff@flex-logix.com>, Daniel Hansen <dhansen@mh-llp.com>

Dear Mr. Konda,

Our patent counsel, with the help of members of Flex Logix's technical staff, has reviewed your correspondence and analyzed the facts to reach the following assessments, which have been reviewed with our Board of Directors.

First, your accusations attacking the integrity and conduct of Drs. Markovic and Wang are untenable. Not only are they are unsupported by the facts – including the facts presented in your email -- your accusations of copying and professional dishonesty are inappropriate. Even a brief consideration of a timeline of the publication dates of the patents and applications you focus on in your email makes that clear.

Second, what Konda Technologies intellectual property, specifically, are you alleging to be incorporated into the Flex Logix products? To the extent understood, your emails focus on U.S. Patents 8,898,611 and 8,269,523. We have reviewed those patents and have determined that Flex Logix's products do not employ the technology of those patents -- and, as such, we believe a license is unnecessary.

Third, if you believe we have incorrectly evaluated Konda Technologies' intellectual property we would be happy to receive an explanation so we could better understand your reasoning. Please let us know.

Geoff Tate, CEO

www.flex-logix.com
NOTE OUR NEW ADDRESS:
2465 Latham Street, Suite 100
Mountain View, California 94040, USA

> On Mar 28, 2016, at 7:37 AM, DEJAN MARKOVIC <dejan@ucla.edu> wrote:
>
> ---------- Forwarded message ----------
> From: <venkat@kondatech.com>
> Date: Sun, Mar 27, 2016 at 5:34 PM
> Subject: Flex-logix is Infringing Konda interconnect IP; ChengCheng Wang's UCLA PhD Dissertation is a blatant copy of Konda Technologies granted Patent(s)
> To: "shirish@formation8.com" <shirish@formation8.com>, "peter.hebert@luxcapital.com" <peter.hebert@luxcapital.com>, "ceo@flex-logix.com" <ceo@flex-logix.com>, "geofftate@flex-logix.com" <geofftate@flex-logix.com>, "chancellor@ucla.edu" <chancellor@ucla.edu>, "jmurthy@seas.ucla.edu" <jmurthy@seas.ucla.edu>, "llackman@ita.ucla.edu" <llackman@ita.ucla.edu>
> Cc: BV Jagadeesh <bvjagadeesh@gmail.com>, "fgbonomi@gmail.com" <fgbonomi@gmail.com>, "ram@reddyz.com" <ram@reddyz.com>, Venkat Konda <venkat@kondatech.com>, Dejan Markovic <dejan@ee.ucla.edu>

# EXHIBIT 28

Gmail **Venkat Konda <venkat@kondatech.com>**

# Hierlogix a former name for Flex-logix is Infringing Konda interconnect IP; ChengCheng Wang's UCLA PhD Dissertation is a blatant copy of Konda Technologies granted Patent(s)

**venkat@kondatech.com** <venkat@kondatech.com> Thu, Apr 7, 2016 at 9:15 AM
Reply-To: venkat@kondatech.com
To: "llackman@ita.ucla.edu" <llackman@ita.ucla.edu>
Cc: "fgbonomi@gmail.com" <fgbonomi@gmail.com>, Dejan Markovic <dejan@ee.ucla.edu>, Venkat Konda <venkat@kondatech.com>

Dear Prof. Lackman,

It looks like Hierlogix, listed on your website, is an earlier name of Flex-Logix?

Companies | ITA

> Companies | ITA
>
> Below is a List of some ITA-Supported Companies and Projects BruinPa
> tch
>
> View on **www.ita.ucla.edu** Preview by Yahoo

So since ITA funding these two people have been drawing salaries infringing Konda IP. (Moreover Konda Technologies business is adversely affected by Hierlogix/Flexlogix)
Disqualification of Wang's PhD Dissertation is a separate thread going on with UCLA.

But ITA funding plagiarized work at UCLA is a different topic and needs to be addressed by ITA immediately.
What are your policies and how soon do you take action against them?

Markovic:
You have time till tomorrow (Friday April 8th) for you two to plead guilty and make this case simple. You two should immediately admit your stupidity and save everybody's time.
Otherwise it is evident there is a deeper conspiracy behind all of this organized by you, particularly. And we will make sure repercussions will be severe for **BOTH** of you, starting with legal action.

Sincerely,
Venkat Konda PhD
Founder/CEO
Konda Technologies Inc.
E-mail: venkat@kondatech.com
Cell # 408-472-3273

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**From:** "venkat@kondatech.com" <venkat@kondatech.com>
**To:** "shirish@formation8.com" <shirish@formation8.com>; "peter.hebert@luxcapital.com" <peter.hebert@luxcapital.com>; "ceo@flex-logix.com" <ceo@flex-logix.com>; "geofftate@flex-logix.com" <geofftate@flex-logix.com>; "chancellor@ucla.edu" <chancellor@ucla.edu>; "jmurthy@seas.ucla.edu" <jmurthy@seas.ucla.edu>;

"llackman@ita.ucla.edu" <llackman@ita.ucla.edu>
**Cc:** BV Jagadeesh <bvjagadeesh@gmail.com>; "fgbonomi@gmail.com" <fgbonomi@gmail.com>; "ram@reddyz.com" <ram@reddyz.com>; Venkat Konda <venkat@kondatech.com>; Dejan Markovic <dejan@ee.ucla.edu>
**Sent:** Sunday, March 27, 2016 5:34 PM
**Subject:** Flex-logix is Infringing Konda interconnect IP; ChengCheng Wang's UCLA PhD Dissertation is a blatant copy of Konda Technologies granted Patent(s)

**This e-mail is sent/cc'ed to the following people:**
**Flex-Logix Technologies:**
Geoff Tate, CEO
Peter Hebert, Co-founder/Managing Director of Lux Capital
Shirish Sathaye, General Partner of Formation 8, Foundation Capital

**University of California, Los Angeles:**
Gene David Block, Chancellor
Jayathi Murthy, Dean of HS School of Engineering and Applied Science
Les Lackman, Deputy Director, Institute for Technology Advancement

**Konda Technologies, Inc:**
BV Jagadeesh, Investor, Managing Partner, KAAJ Ventures, CEO Net Scalar and Co-founder/CTO Exodus Communications.
Ram Reddy, Investor, Chairman/Founder&CEO Global Industry Analysts, President Elect & Programs' Chair TiE

Flavio Bonomi, CEO Nebilolo Technologies, Formerly Head of R&D Cisco Systems

**Subject: 1) Flex-logix is built by Infringing Konda Technologies interconnect IP!**
**2) ChengCheng Wang's UCLA PhD Dissertation is a blatant copy of Konda Technologies granted Patent(s)!**
**3) Your urgent attention/action desired!**

Respected Flex-logix board members: Geoff, Peter, and Shirish:
Respected UCLA Administrators: Gene, Jayathi, and Les:

Prof. Vaugh Betz, Dept. of Electrical Engineering, University of Toronto asked me when I visited his office on December 18, 2015, if Flex-logix is implementing Konda Technologies FPGA interconnect IP! That was a surprise and total shock to me. Since then till today I have investigated what Flex-logix has been doing.

I am Venkat Konda, Founder/CEO of Konda Technologies. A brief about Konda Technologies and me is given at the end of the email.

I am writing this email (without any legal actions) with all the details since I have tremendous respect for all the above listed People, all of you are inventors, educators, and practitioners. Konda Technologies investors know Shirish personally and also the well-known litigation attorneys I consulted with in the past few months regarding the current email subject matter know Shirish very well. Furthermore late Professor Rajiv Motwani of Stanford University introduced me to Shirish in the past and so I met/interacted with Shirish personally in the past. I believe we can resolve the issues mentioned in this mail by ourselves. And I am willing to fully cooperate from Konda Technologies side.

# EXHIBIT 29

Gmail **Venkat Konda <venkat@kondatech.com>**

# Re: Response to Mr. Konda's email of May 16

**venkat@kondatech.com** <venkat@kondatech.com> Fri, May 20, 2016 at 12:35 AM
Reply-To: venkat@kondatech.com
To: geoff tate Flex Logix <geoff@flex-logix.com>
Cc: Neil Steinberg <neils@swpatentlaw.com>, "shirish@formation8.com" <shirish@formation8.com>, "peter.hebert@luxcapital.com" <peter.hebert@luxcapital.com>, "cheng@flex-logix.com" <cheng@flex-logix.com>, "dejan@flex-logix.com" <dejan@flex-logix.com>, Venkat Konda <venkat@kondatech.com>

Geoff,

Wow! That is a lightening fast response.
So you admit you do not have any additional information as I asked for in VI) 4).
Sure as you wish my litigation attorney will send claims charts with a law suit ASAP. Thanks for welcoming it you yourself.
If you think my interpretation is wrong let me know by today, Friday 20th.
No need to respond otherwise.

To these two guys,
You two have secretly dug your own deep grave for years and in tandem spectacularly nosedived into it. Don't worry we will get it also published in Forbes.
I have worried I might lose the opportunity to sue you two, if the company settles before. Now I am pretty excited!

Sincerely,
Venkat Konda

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**From:** geoff tate Flex Logix <geoff@flex-logix.com>
**To:** venkat@kondatech.com
**Cc:** Neil Steinberg <neils@swpatentlaw.com>; geoff tate <geoff@flex-logix.com>
**Sent:** Wednesday, May 18, 2016 11:43 AM
**Subject:** Response to Mr. Konda's email of May 16

Hello Mr. Konda,

We have reviewed your recent email.

We definitely do not agree with your analysis or your position(s).

If you proceed as you say in VI) 5), we will review your patent counsels' analysis and claim charts.

Geoff Tate, CEO

flexlogix Technologies, Inc.

www.flex-logix.com
2465 Latham Street, Suite 100
Mountain View, California 94040, USA

On May 16, 2016, at 10:01 PM, venkat@kondatech.com wrote:

Geoff,

As part of my response to UCLA, I went through the PhD Dissertation thoroughly multiple times and also I had to change my patent litigation attorney who works on a contingency fee basis, so I am responding three weeks later.

**I)** I am providing further details on how these two have blatantly copied the layouts in Konda patents and presented them as theirs. Refer to the section below with the heading "Details of how the student plagiarized and has been continuously infringing since 2009".

**II) My Significant accomplishments in Multi-stage based FPGA Interconnects since 2007:**

I have mentioned in my March 27, 2016 mail that I talked to Dan Avida, General Partner, Opus Capital and Prof. Serge Plotkin, Computer Science Department, Stanford University in July/August 2007.

a) Prof. Serge Plotkin was a student of MIT Professor Leiserson who was the inventor of Butterfly Fat Tree Networks. And they applied them in parallel and distributed computing.

b) Prof. Plotkin has validated Layouts of Konda Patents for FPGA Fabrics and Dan Avida was ready to fund Konda technologies in July 2007.

c) It was me who chose licensing model at that time and did not take the funding. [At that time I have filed Konda Patents #1-4 and Konda Patent #5 and discussed about them with both Dan and Prof. Plotkin.

d) Since then I have continued with the licensing model and never talked to any VC for funding. And continued by raising angel funding only. [In fact, with Opus Capital also, Sachin Maheshwari, then associate for Dan Avida contacted me rather than me approaching them in 2007.]

e) However I have worked with four different FPGA vendors and completely knowledgeable about FPGA fabrics and their tools of almost all vendors but one.

f) As I mentioned before Konda Patents #6 and onwards are significant improvements over previous ones. These improvements were possible only because I have mastered the prevailing 2D-Mesh based FPGA Fabrics used by prevailing vendors.

i) So what these two is infringing and presented to you is inferior technology.

**Finally I have patent protected every aspect of multi-stage networks for FPGA Fabrics.**
**I told these two in 2009. They ignored it. I hope you won't do the same mistake now.**

**III) My last meeting with these two guys @ Dr. Sundar Ayer, CEO of Memoir Systems office on March 5, 2014:**

1) Four of us, I, these two guys and Sundar were in the meeting. [Sundar Ayer with his PhD Dissertation @ Stanford Univeristy built company "Nemo Systems" with his PhD Advisor Prof. Nick Mckeown, and sold to Cisco. Later on he has founded another company "Memoir Systems" where we met him on March 5, 2014. in October 2014, Sundar, CEO and sold Memoir Systems to Cisco as well.] This meeting was set up by Flavio.

2) During the meeting with all four of us in the room, **Wang clearly told he does not have any IP and** their model is different and will provide GDS blocks. [Of course at that time I was not aware that this guy did a PhD Dissertation in FPGA interconnects]. Two weeks after this meeting, I called up Sundar and expressed my concern about Wang's comments and if these guys are using Konda interconnect they will be in trouble. Even then I was under the impression their product is some non-FPGA chip. [Sundar can validate Wang's comments in that meeting.]

**3) This is another clear proof that these guys know they do not have any interconnect IP and they have been cheating everybody, including you.**

**IV) Please see below what Flavio thinks of these two guys (copy/pasted one of his emails to me)**

**V) Please see below how desperate is Dejan and approached Lux Capital in 2009 for Konda IP.**

**VI)**

1) I have been extremely patient and respectful to three of you. I kept this information to the people only in the emails listed so far.

2) I have provided several details of how these two have been infringing Konda Patents. (I have even more whole lot of emails and information)

3) I even warn you to watch your back, before the student runs away with the infringed technology to China.

4) If you still think that my analysis is wrong and I have incorrectly reached the conclusion that these two guys have been infringing Konda Patents, please share the relevant information/pointers by Friday May 20th. Otherwise I would assume you agree with my analysis and position.

5) In spite of all these details if your position still does not change, I will sign up with my new patent counsel on a contingency fee basis and follow up with Claims's Charts for all Konda Patents.

6) If you agree with my position, please let me know. I have a proposal where all three of your interests are absolutely not compromised. And we can resolve the issue in an amicable and mutually beneficial way.

a) In such a case I am open to meet Geoff.
b) Or our attorneys can meet.
c) Or if you have any proposals.

Sincerely,

Venkat Konda, PhD
Founder/CEO
Konda Technologies Inc.
E-mail: venkat@kondatech.com
Cell # 408-472-3273

**********

## Details of how the student plagiarized and has been continuously infringing since 2009:

I am cutting and pasting the following paragraphs from the PhD Dissertation "In Chapter 2.4 titled "Hierarchical Network - A Scalable Solution", last paragraph of Page #27, and the first paragraph of Page #28 including the Fig 2.13".

"Fortunately, implementing a Beneš network on silicon gives us freedom in both x- and y- directions. Although [Manuel 07] illustrated a manual layout method for a Beneš layout on a 1-dimensional array, most silicon implementations allow for a 2-dimensional layout. To alleviate congestion, routing is alternated between the x-y directions, doubling the routing congestion for every 2 stages. The routing congestion is reduced from O(N) to O(N $^{0.5}$) (Figure 2.13), and the fully symmetrical implementation also eases physical design.

(Actual Figure 2.13 is not pasted here)
Figure 2.13: A hierarchical Beneš interconnect architecture using alternated x-y routing.

Another change from the original Beneš network is unequal wire lengths. At every hierarchy, the LUTs near the center are connected to create shorter routes, and the LUTs near the edges have longer routes. In terms of logic connectivity, this wiring difference is an isomorphic transformation from the original network, thus the interconnect connectivity remains unchanged [Wu80, Duato02, Konda08]. Yet this difference in wire lengths gives routing tools options for faster paths on timing-critical routes. In physical design, this also allows the center routes to remain at the lower metal layers without crossing over the longer routes on the upper metal layers, further avoiding congestion."

The paper referenced in the above pasted first paragraph is: (It is also attached in this mail)
[Manuel07] P. Manuel, W. K. Qureshi, A. William, A. Muthumalai, "VLSI layout of Benes networks,", J. of Discrete Math. Sci. & Cryptography, vol. 10, no, 4, pp. 461-472, 2007.

## I. What is essential for Multi-stage Networks to be used as FPGA Fabrics:

1) All the switches/Muxes corresponding to each LUT/CLB need to be placed together - let me call it a block.
2) These blocks are arranged in general in rectangle in a 2d-grid.
3) The global wires need to be either horizontal or vertical wires only.
The prevailing 2D-Mesh based FPGA fabrics satisfy the above three points..
The VLSI layouts for multi-stage networks including Benes and BFT Networks disclosed in Konda Patents #4, #5, etc satisfy multi-stage the above three points as well.

## II. The contribution of VLSI Layouts for Benes Networks by [Manuel07]:

1) This paper presents VLSI layout for any r-dimensional Benes Networks to produce the smallest possible grid area on a single 2D-plane.
a) Note they do not assume there are several metal layers available to route wires and their layout is on a strictly single 2D-plane.
b) Assuming each switch in Benes Network is a node, the proposed 2D-layout satisfies the following conditions:
i) Each edge between any two nodes of Benes Network has a separate trace corresponding to the layout in the single 2D-plane (i.e the layout is edge-disjoint for all the corresponding edges in the Benes Network)

ii) No edge will traverse on a node unless it is incident in the corresponding switch of the Benes Network.

2) The layout is based on the idea that Benes Network consists of several 4-cycles. Each 4-cycle is topologically a diamond (or rhombus) with 4 nodes and 4 edges.

3) Then the layout is performed using the following two rules:

1) Each normal diamond is stretched to a rectangle as in Figure 4 (refer to the paper).

2) Each pair of Nested diamonds is stretched along the grid lines as in Figure 5 (refer to the paper).

4) Finally the proposed layout for a 3-dimensional Benes Network is given in Figure 6 (refer to the paper).

## III. Why [Manuel07] layouts are totally irrelevant FPGA Fabrics:

1) The switches corresponding to each LUT/CLB are NOT placed together (i.e. in a separate block). In fact if you observe the Figure 6, they are all jumbled up or randomly mixed up.

2) All the links in [Manuel07] layouts are diamonds and all four links in each diamond correspond to "L" shape links in the layout. i.e., Each "L" link is part Vertical and part Horizontal link. [So there is no concept of straight links and cross links as in Konda Patents.]

3) This layout is not a rectangular.

a) For example a 3-dimensional Benes Network's layout (refer to Figure 6) has three rows of nodes with nodes in each row being 1, 4, 1, 8, 1, 4, 1, 16, 1, 4, 1, 8, 1, 4 and 1.

**So essentially the VLSI Layouts presented in [Manuel07] does not meet even one point presented above in I) for it to be used for FPGA Fabrics. Even the authors of Manuel07 DID NOT claim the layout is applicable for FPGA Fabrics.**

## IV. How the student manipulated in the PhD Dissertation:

Now focus on the paragraphs I cut pasted above from the PhD Dissertation how the student is misrepresenting the facts and trying to mislead the reader.

1) Focus on this line - "Although [Manuel07] illustrated a manual layout method for a Beneš layout on a 1-dimensional array, most silicon implementations allow for a 2-dimensional layout."

a) First the VLSI Layouts of Benes Networks presented in [Manuel07] is a 2-dimensional layout. (For example the paper in Section 4.0 Conclusion clearly claims "This VLSI layout of B(r) is laid in a square area"). And the paper clearly claims the objective of the VLSI layout presented is to achieve lower bound on the area. How can there be "area" if it is not laid out in 2-dimensions?

i) But the student claims the layout is on a 1-dimensional array and most silicon implementations allow for 2-dimensional layout??? what are those "most silicon implementations"? These must be by copying layouts Konda Patents?

2) Now focus on "Fortunately, implementing a Beneš network on silicon gives us freedom in both x- and y- directions".

i) What "freedom in both x- and y- directions" the student talking about? Is the freedom coming from by copying layouts in Konda patents hence the concepts of X- and y-directions (i.e. vertical and horizontal directions)?

3) Now focus on "To alleviate congestion, routing is alternated between the x-y directions, doubling the routing congestion for every 2 stages. The routing congestion is reduced from O(N) to O(N $^{0.5}$) (Figure 2.13), and the fully symmetrical implementation also eases physical design."

i) There you go. **The student blatantly copies Layout in Konda Patents in Figure 2.13.** And he writes it in such as way that it is some how extrapolated from 1-dimensional array layout of [Manuel07] by him and with the freedom to in x- and y- directions. Blatant cheating!

ii) To reemphasize, Figure 2.13 is complete copy of layout disclosed in Konda Patents!

iii) And the student did not even mention about the layouts in Konda Patents anywhere in the PhD Dissertation.

4) To summarize, [Manuel07] presents layout with "L" shaped links. And I am questioning "how those "L" links give freedom to the student to apply in x- and y- dimensions?".

5) I do not see the the student mentioning about layouts in Konda Patents by giving credit to Konda. Don't the layouts in Konda Patents show how to apply in x- and y- dimensions, by using the student's words?

6) Do I need to repeat myself about the dates I gave a presentation in UCLA/ITA, and to the prof. and his students, priority dates and publication dates of Konda Patents, when this

PhD dissertation was written, when the student & Prof. filed the patent application we discussed in the previous mail?

i) It is clearly evident that student has been infringing Konda Patents by blatantly copying the complete diagrams. Do you still need Claims Chart's to prove it?

ii) Further more the student uses "double links" (and two wires with double sided arrows to actually represent four wires with single sided arrows) in almost all the interconnect diagrams in the PhD Dissertation, which are required for non-blocking multicast as disclosed in Konda Patents. So when the student is using "double links" through out, doesn't it demonstrate the student completely understands Konda Patents and blatantly copying them.

iii) In Chapter 3.1, page # 33, the student clearly wrote Figure 2.13 is extended to 2048 LUTS and it resulted in Figure 3.1. So Figure 3.1 and all the interconnect figures in the PhD dissertation are blatant copies of the layouts in Konda Patents.

a) Another important point is observe the title of Figure 3.1 namely "Figure 3.1: A hierarchical macro-based implementation of a **2D-Beneš network**."

1) I coined the term "2D-Benes Network" and I have used it in Konda Business and Technology Presentations, soft copies of which I shared with these two guys. I have not used the term '2D-Benes Network" in Konda Patents. So these two guys studied my business and technology presentations thoroughly. **So the cheaters are caught!** The student uses the term "2D-Benes Network" only at this place (and in the corresponding place in the "List of Figures" section) in the entire PhD Dissertation without defining what it means!!! That is how the student left an unintentional trail and got caught.

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**What Flavio thinks of these two guys:** (I am cutting and pasting the email from Flavio on February 28, 2016. I can also provide the original email )

**From:** Flavio Bonomi <fgbonomi@gmail.com>
**To:** venkat@kondatech.com
**Sent:** Sunday, February 28, 2016 3:52 PM
**Subject:** Re: Nice catching up with you @ your office on Jan, 7th 2016!!!

Venkat,
Are you making progress in your defense against the crooks ?
Please let me know if I can be of help.
Thanks,
Ciao,
Flavio

**********

**Mr. Markovic has approached Lux Capital on October 12, 2009 and he is talking only about Konda IP. Even though I told him I was not looking for VC funding.** (I am cutting and pasting the email from Dejan on October 12, 2009. I can also provide the original email )

**From:** Dejan Markovic <dejan@ee.ucla.edu>
**To:** Shahin Farshchi <shahin.farshchi@luxcapital.com>
**Cc:** Armond Hairapetian <armond@starportsys.com>; Dejan Markovic <dejan@ee.ucla.edu>
**Sent:** Monday, October 12, 2009 11:29 PM
**Subject:** Re: Armond, meet Dejan

Shahin,

Thanks very much for the introduction.

Armond,

I have a very exciting opportunity that needs immediate action. It's about an FPGA with ASIC performance (I am very well aware of many dead FPGA companies, but this is >5x better than today's startups such as Abound Logic). Some of the technology is outside of UCLA (it's patented) and I need help to pull it in. It would be great if you have time to talk / meet sometime soon.

Best regards,
Dejan

Dejan Markovic
Assistant Professor, UCLA EE Dept.
56-147E Eng-IV Bldg, 420 Westwood Plz.
Los Angeles, CA 90095-1594
Office: (310) 825-8656
Mobile: (510) 612-2998
Fax: (310) 206-8495
Email: dejan@ee.ucla.edu
URL: http://www.ee.ucla.edu/~dejan

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**From:** Geoffrey Tate <geoff@flex-logix.com>
**To:** venkat@kondatech.com
**Cc:** Neil Steinberg <neils@swpatentlaw.com>; geoff tate <geoff@flex-logix.com>
**Sent:** Sunday, April 24, 2016 6:17 AM
**Subject:** April 24th reply Re: Response to Mr. Konda's email of 7 April which was received at 1158am

Hello Mr. Konda,

I asked our Patent Counsel to review your latest email of April 16th and after consideration we still do not agree with your position.

Our assessment is unchanged and our position is the same as in my April 7th email to you.

We will certainly consider any additional facts and listen to any new analysis you wish to provide us.

Geoff Tate, CEO
Flex Logix

> On Apr 16, 2016, at 3:30 AM, venkat@kondatech.com wrote:

Geoff,

I have provided sufficient information for you to make an informed decision already.

Being from a reputed university, I used to have lot of respect for these two guys. Once I learned about PhD Dissertation blatantly copying Konda Patent(s), I had no respect to either of those two. [On January 7, 2016, I met Flavio at his office and informed him about PhD Dissertation and asked Flavio if he knew about Wang doing a PhD Dissertation in FPGA interconnects. He was utterly shocked as well, as it is new to him also.]

When you said the technical staff reviewed - is it these two guys and people who report to them? If technical staff provides garbage to patent counsel what is the point?

**I)** The patent application you attached Pub. No US2016/0034625A1 is coming straight out of his PhD Dissertation. It is supposed to be fundamental interconnect patent application by these two guys for you to have funded Flex-logix. The value proposition of it is a joke.
None of the claims are allowable.
The way the claims are written they clearly knew about Konda Patents. (The corresponding provisional application was filed March 15, 2013).
They did not stop proceeding to infringe Konda Patents even then.

**II)** Observe Claim 1. "computing element can connect to at least two nearest neighboring computing elements via Stage 1 Switch". That is supposed to be the key value of this claim. Now observe FIG 3C of Konda Patent #2 (Patent No. US 8,170,040). Inputs of Computing element IS2 connect to outputs of two nearest neighboring elements OS1 and OS3 via Stage 1 switch MS(1,1). [All the connections are clearly shown in diagram FIG 3C]
So Claim 1 is not allowable. Similarly all the independent claims are NOT allowable. [There are numerous other examples with diagrams in Konda Patents 1, 2 & 3 with switches of size d1*d2, where d1 > 1 and d2 > 1.]
By the way, I will never write such silly claims.
**They cannot even modify or write new claims without infringing Konda Patents! The figures and specification reveal the infringement anyway.**

**III)** Net result:
1) These two guys started PhD Dissertation by infringing Konda Patents.
2) And submitted PhD Dissertation with infringing Konda Patents.
3) Nothing novel, nothing unobvious. And so PhD Dissertation contributes nothing new.

**IV)** On January 28, 2014, when I met these two guys @ Flavio home, in the middle of the conversation Wang said, he has implemented radix-3 networks. Then I told him radix-3 is inefficient in several ways compared to radix-2 or even radix-4 and explained the rationale. [At that time both Flavio and I DO NOT know that this guy did a PhD Dissertation in FPGA interconnects. Otherwise why would I share that information to them.]
Now observe the titles and dates of the Interconnect patent application these two guys filed.
a) Provisional application is titled "A Radix-3 Network Architecture for Boundary-Less Hierarchical Interconnects".
b) PCT application was filed on March 14, 2014 i.e., after we met @ Flavio home. And the title is "Network Architecture for Boundary-Less Hierarchical Interconnects". **They dropped Radix-3 from the title.**
c) Of course, the US Application and Europe application are titled same as PCT application. What would you call them now?

**V)** This guy's PhD Dissertation is centered completely on radix-3 networks. **From a product point of view this is very inefficient.** [If these guys aborted radix-3 in the current implementation it is because they learned from me at Flavio's home.]

**VI) My Expertise in Interconnects:**
1) In 2001, I invented rearrangeably and strictly non-blocking multicast solution for 3-stage Clos Network (These patents were granted long time ago). (These solutions are as seminal as original Charles Clos's Unicast solutions, published in 1951] This is 60-year old research problem, which helped me found Teak Technologies, a switch fabric company. [During these days I met Flavio. Since then Flavio knows what all I have been doing.]
2) On January 23, 2007, I met Dr. Dale Wong, co-founder of Leopard logic. He was very impressed with my multicast solutions for 3-stage Clos Network and encouraged me to apply

them for FPGA interconnects. [He also told me he @ Leopard logic tried to apply Benes Networks for FPGAs but failed.]

a) Couple of weeks later I met Dale again and told him, 3-stage networks are not appropriate for FPGAs. So I pursued Benes/BFT networks and I came up with multicast solutions for Benes/BFT networks as well (These are Konda Patents #1, #2 and #3). He was very impressed but then told me that is not the key issue. The key issue is lack of VLSI layouts for Benes/BFT networks just the same way as 2D-Mesh networks.

b) I met him again a couple of weeks later, and I told him I came up with VLSI layouts for Benes/BFT networks in a 2D-grid with only horizontal and vertical wires (This is Konda Patent #4). This time he was even more impressed and murmured I wish you were with us before Leopard logic failed.

c) Since then, I showed VLSI layouts in Konda Patent #4 to numerous experts in the industry and academia. Everybody has validated them. (I have a complete list of whom I got it validated with)

d) For example, in 2007, in Cisco systems when I showed them to Dr. Bill Lynch (Procket Networks co-founder). (Flavio was in this meeting and he already validated.) Bill said, very impressive, I attempted to solve the same problem and could get either vertical or horizontal wires correctly but not both and I gave up on it.

e) In September 2007, I showed it to a fellow/expert in one of the FPGA companies (I am not providing the name of the person and company). After he looked at the layouts he immediately reacted that "I have least respect for people like you who come knocking our doors that they have this IP and that IP, But this is exceptional and I have never seen this before!".

f) Konda patent #4 is major breakthrough for Benes/BFT networks to be used in FPGA interconnects!!!

3) PhD dissertation absolutely implements Konda patent #4 layouts and all the optimizations in Konda Patent #5.

**VII)** If the first interconnect patent application (based on infringing Konda patents) has zero value, what additional improvements you are talking about in your current product.

**VIII)** 1) Their interconnect knowledge is shallow.

2) Their patent and IP knowledge is shallow. [At the least they should know that to do a product, they must have license to all parts of the product. They themselves have no IP on their own.]

3) Of course without any hesitation, I question their intellect, integrity and honesty.

**IX)** Since March 27, 2016, I expected these two to plead guilty like "we did not what patenting is, we did not know what claims are, we did not know what anticipatability in patent claims since engineering graduate schools do not teach about patenting, we did not know that make, use, sell or offer to sell patented IP even in an university is infringement, we were not wise and careful enough to NOT do a PhD by infringing patented Konda IP after inviting Venkat for a seminar to explain his inventions."
However I still cannot forgive the student for

1) completely downplaying the value of Konda Patent #4 in his dissertation;

2) for blatantly copying Konda patent #5;

3) During the filing of the corresponding provisional patent application you sent in March 2013, they must have realized the mistake, doing a PhD Dissertation, they made while writing claims.

4) Dejan met me numerous times since October 2009 - Once his student is doing PhD dissertation:

a) he could have ignored me even if I talked to him,

b) he could have said there may be a conflict of interest and let us not talk,

c) or he should not have brought the topic when we ever we met.

Instead he always collected information including, how I am progressing with Konda Technologies, which customers I am talking to etc.

As I have stated before, my position remains the same on both their integrity and honesty as well as your product infringing Konda Patents.

Venkat Konda, PhD
Founder/CEO
Konda Technologies Inc.
E-mail: venkat@kondatech.com

Cell # 408-472-3273

P.S: UCLA has already split the case into two issues 1) Patent Infringement and 2) Plagiarism.

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**From:** geoff tate Flex Logix <geoff@flex-logix.com>
**To:** Venkat Konda <venkat@kondatech.com>
**Cc:** geoff tate <geoff@flex-logix.com>; Neil Steinberg <neils@swpatentlaw.com>
**Sent:** Friday, April 8, 2016 11:11 AM
**Subject:** Response to Mr. Konda's email of 7 April which was received at 1158am

Dear Mr. Konda,

We have taken your allegations seriously and reviewed your inputs in detail.

As we have stated before, regarding your interactions at UCLA with Dr. Wang and Dr. Markovic, we have reviewed your allegations but do not agree with your conclusions.

Regarding your last point, a US Patent Application was filed in September 2015 and published February 4, 2016 — see attached.

The internal details of our implementation of EFLX embedded FPGAs are not public. Significant work in optimizing for embedded FPGA applications was done when we started the company. We have reviewed your patents against our implementation and do not see a need to license your patents.

If you have additional facts you wish to supply we will consider them.

If you have new information as to why you think our conclusions are incorrect we will certainly review that seriously as well.

Geoff Tate, CEO

www.flex-logix.com
NOTE OUR NEW ADDRESS:
2465 Latham Street, Suite 100
Mountain View, California 94040, USA

<Manuel07.pdf>

# EXHIBIT 30

Gmail

Venkat Konda <venkat@kondatech.com>

## Thank you for the meeting on Yesterday (Tuesday 30th)

**Venkat Konda** <venkat@kondatech.com>
Reply-To: Venkat Konda <venkat@kondatech.com>
To: geoff tate Flex Logix <geoff@flex-logix.com>
Cc: Venkat Konda <venkat@kondatech.com>

Hi Geoff,

Thank you for the meeting yesterday.
I gave a lot of thought afterwards. I have a proposal with which I believe we can reach a logical and practical settlement with everybody being happy.
I am open tomorrow afternoon or Friday afternoon.
Otherwise please suggest your convenient times.

Thanks,
Venkat

---

**From:** geoff tate Flex Logix <geoff@flex-logix.com>
**To:** Venkat Konda <venkat@kondatech.com>
**Sent:** Saturday, May 20, 2017 9:33 AM
**Subject:** Re: Tuesday 30th @ 230pm -- Re: Your voicemail

confirmed. thanks,

Geoff Tate, CEO

flexlogix Technologies, Inc.

www.flex-logix.com
2465 Latham Street, Suite 100
Mountain View, California 94040, USA

> On May 20, 2017, at 09:09, Venkat Konda <venkat@kondatech.com> wrote:
>
> Geoff,
>
> Appreciate.
> I will take 3:30pm which would give more cushion.
>
> Thanks again,
> Venkat
>
> Sent from my iPhone
>
> On May 20, 2017, at 6:27 AM, geoff tate Flex Logix <geoff@flex-logix.com> wrote:
>
> Hi Venkat,
>
> We could do 3pm or 330pm Tuesday if that helps - let me know.
> If your flight is delayed you can email me.
> If Tuesday doesn't work we can talk the week of June 5th.
> Thanks,
>
> Geoff Tate, CEO
>
> <FlexLogic Color-01 CROPPED 50 pixels high.jpg>
>
> www.flex-logix.com
> 2465 Latham Street, Suite 100
> Mountain View, California 94040, USA
>
> > On May 19, 2017, at 7:30 PM, Venkat Konda <venkat@kondatech.com> wrote:
> >
> > Hi Geoff,
> >
> > Tue 2:30pm works. However I will be flying in from Saint Louis that day.
> > So I asked for Wednesday.
> > In case we need to touch base hope the number I called is your cell#.
> >
> > Thanks,
> > Venkat

Sent from my iPhone

On May 19, 2017, at 6:40 PM, geoff tate Flex Logix <geoff@flex-logix.com> wrote:

Hi Venkat,

Wednesday 31st I have meetings.

Let's meet Tuesday 30th May as I proposed.

See you then.

Thanks,

Geoff Tate, CEO

<FlexLogic Color-01 CROPPED 50 pixels high.jpg>

www.flex-logix.com
2465 Latham Street, Suite 100
Mountain View, California 94040, USA

> On May 19, 2017, at 5:55 PM, Venkat Konda <venkat@kondatech.com> wrote:
>
> Hi Geoff,
>
> Sorry, I missed your call.
> Thank you for the response.
> Tuesday works for me. However Wednesday 31st would be preferable, time I am flexible. Please suggest if it works.
> Also not sure if the number I called is your cell #. Please confirm.
>
> Thanks,
> Venkat
>
> Venkat Konda, PhD.
> Founder/CEO
> Konda Technologies Inc.
> E-mail: venkat@kondatech.com
> Cell # 408-472-3273
>
> ---
>
> **From:** geoff tate Flex Logix <geoff@flex-logix.com>
> **To:** Venkat Konda <venkat@kondatech.com>
> **Cc:** geoff tate <geoff@flex-logix.com>
> **Sent:** Friday, May 19, 2017 5:27 PM
> **Subject:** Your voicemail
>
> Hello Venkat,
>
> I received your voicemail.
>
> I doubt that we can reach a settlement.
>
> But I am willing to listen.
>
> I am out of town next week.
>
> Let's meet Tuesday 30th May at 230pm at Starbucks, 750 Castro Street, Mountain View.
>
> Thanks,
>
> Geoff Tate, CEO
>
> <FlexLogic Color-01 CROPPED 50 pixels high.jpg>
>
> www.flex-logix.com
> 2465 Latham Street, Suite 100
> Mountain View, California 94040, USA

AT&T Unified Messagi

The attached message was recently left in your AT&T Unified Messaging℠ mailbox. We are sending you this email because you have asked for your messages to be forwarded to this address.

Voicemail transcription

H oh hi jeff this is Venkat Konda. I am ... wondering if we can meet toreach a settlement. My phone number is (408) 472-3273. Please letme know if that is possible. I just want to reach out to you if there is away that we can settle by talking. Thank you.



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# EXHIBIT 31

Gmail

**Venkat Konda <venkat@kondatech.com>**

# Response to your Friday 14 July Proposal

**geoff tate Flex Logix** <geoff@flex-logix.com> Sun, Jul 16, 2017 at 1:43 PM
To: Venkat Konda <venkat@kondatech.com>
Cc: geoff tate <geoff@flex-logix.com>

Hi Venkat,

I appreciate your making a proposal dramatically lower than in the past.

But as I warned you on Friday, the Flex Logix Board does not accept the proposal.

We do not need a license to your patents, and your proposal is still much higher than our position.

We remain willing to pay [redacted] for a full license with right to sublicense.

Thanks,

Geoff Tate, CEO

flexlogix Technologies, Inc.

www.flex-logix.com
2465 Latham Street, Suite 100
Mountain View, California 94040, USA

> On Jul 15, 2017, at 5:46 PM, Venkat Konda <venkat@kondatech.com> wrote:
>
> Geoff,
>
> Yes I agree with this point also.
>
> Thanks,
> Venkat

---

**From:** geoff tate Flex Logix <geoff@flex-logix.com>
**To:** Venkat Konda <venkat@kondatech.com>
**Cc:** geoff tate <geoff@flex-logix.com>
**Sent:** Saturday, July 15, 2017 5:34 PM
**Subject:** Re: We are diverging, not converging

Hi Venkat,

I was typing fast since i have a lot to do before my trip.

So to make sure it is clear, i should have said:
The license to your patents is for all of your patents and anything (patents/divisionals/claims) stemming from your patents or any existing filings with any patent office worldwide.

Thanks,

Geoff Tate, CEO

<FlexLogic Color-01 CROPPED 50 pixels high.jpg>

www.flex-logix.com
2465 Latham Street, Suite 100
Mountain View, California 94040, USA

On Jul 15, 2017, at 5:16 PM, Venkat Konda <venkat@kondatech.com> wrote:

Geoff,

Ok. I understand.
I AGREE with your following offer.

> What i understood Friday morning was
> 1. [redacted] of our embedded FPGA revenues annually, which is greater
> 2. we get a license for your patents, as of now, so that we have no future dispute, with a right to sublicense to our customers for use in embedded FPGA
>
> I am happy with your above proposal. And again I agree it.

Thanks,
Venkat

---

**From:** geoff tate Flex Logix <geoff@flex-logix.com>
**To:** Venkat Konda <venkat@kondatech.com>
**Cc:** geoff tate <geoff@flex-logix.com>
**Sent:** Saturday, July 15, 2017 4:50 PM
**Subject:** Re: We are diverging, not converging

Hi Venkat,

> What i understood Friday morning was
> 1. [redacted] of our embedded FPGA revenues annually, which is greater
> 2. we get a license for your patents, as of now, so that we have no future dispute, with a right to sublicense to our customers for use in embedded FPGA

Geoff Tate, CEO

<FlexLogic Color-01 CROPPED 50 pixels high.jpg>

www.flex-logix.com
2465 Latham Street, Suite 100
Mountain View, California 94040, USA

On Jul 15, 2017, at 4:35 PM, Venkat Konda <venkat@kondatech.com> wrote:

Geoff,

Not sure where we diverged. is the issue on "revenues from embedded FPGA Vs. revenues on all of your products incorporating Konda interconnect patents"? Please clarify. We can also talk on the phone if needed.

Thanks,
Venkat

---

**From:** geoff tate Flex Logix <geoff@flex-logix.com>
**To:** Venkat Konda <venkat@kondatech.com>
**Cc:** geoff tate <geoff@flex-logix.com>
**Sent:** Saturday, July 15, 2017 4:25 PM
**Subject:** We are diverging, not converging

Hi Venkat

What i understood Friday morning was
1. [redacted] of our embedded FPGA revenues annually, which is greater
2. we get a license for your patents, as of now, so that we have no future dispute, with a right to sublicense to our customers for use in embedded FPGA

The proposal you have below i think is a change from what we discussed.
In any case, if the below is your proposal, it is not acceptable.

I was not optimistic the Board would approve the proposal as I understood it on Friday - your proposal today is not even worth forwarding to them.

So let me re-state our position:

1. We do not need a license to your patents
2. The Board has authorized me to settle immediately for [redacted] in return for a license, with right to sublicense, for all your patents and any future divisionals/claims stemming from any existing filings. This offer is not open-ended: you can choose to accept it this month but we have no obligation to extend it into the future.

Thanks,

Geoff Tate, CEO

<FlexLogic Color-01 CROPPED 50 pixels high.jpg>

www.flex-logix.com
2465 Latham Street, Suite 100
Mountain View, California 94040, USA

On Jul 15, 2017, at 4:08 PM, Venkat Konda <venkat@kondatech.com> wrote:

Hi Geoff,

I understand. Please allow me to make my complete proposal in this email.
We can also talk on the phone if needed - My cell # 408-472-3273.

I am copying your language verbatim and answering one by one for clarity.

## I. Your two points copy/pasted below:

1) we do not believe we infringe anything so we don't need to license them - if we take a license it is to resolve and dispose of this issue
2) at a minimum for any proposal that my board would consider, we need a license, with right to sublicense, for any patents/claims you currently have or eventually arise from any filings you have made at the time of the agreement with any patent office in the world. this includes divisional, amendments, claims that come from any filings as of the time of the agreement. the license and sublicense is for embedded FPGA.

**My Answer:**
For the above, my proposal is ONLY for the first year payment an additional [redacted]. (Total payable in two installments, if you prefer)

**So the complete proposal** is: [redacted] revenues of all your products incorporating Konda interconnect patents.

---

## II. Your 3rd point:

3) We can exclude filings that are first made after the agreement, if there is one.

**My Answer:**
Not sure if I understand it. But let me make this simple below.

---

## III. The remaining option we talked about:

In addition to your points 1 & 2 above, if you need future Konda interconnect patents (future proofing).

**My Proposal:**
An additional [redacted] whichever is greater.

**So the complete proposal** is: [redacted] of all your products incorporating Konda interconnect patents.

---

**IV. Your last line:**
Let me know if your proposal of [redacted] or our embedded FPGA semiconductor IP (GDS, etc) licensing revenues is for the license above.

**My Answer:**
For the sake of clarity, In the above line the revenues are calculated for all the products you will make, incorporating Konda Interconnect Patents.

Please let me know if you this is agreeable.

Thanks,
Venkat

---

**From:** geoff tate Flex Logix <geoff@flex-logix.com>
**To:** Venkat Konda <venkat@kondatech.com>
**Cc:** geoff tate <geoff@flex-logix.com>
**Sent:** Saturday, July 15, 2017 10:59 AM
**Subject:** Re: Confirming your proposal from this morning's meeting 14 July 2017

Hi Venkat,

Sorry - i have family visiting this weekend.

The issue is what patents are licensed.
1) we do not believe we infringe anything so we don't need to license them - if we take a license it is to resolve and dispose of this issue
2) at a minimum for any proposal that my board would consider, we need a license, with right to sublicense, for any patents/claims you currently have or eventually arise from any filings you have made at the time of the agreement with any patent office in the world. this includes divisional, amendments, claims that come from any filings as of the time of the agreement. the license and sublicense is for embedded FPGA.
3) We can exclude filings that are first made after the agreement, if there is one.

When we met i thought #1 and #2 were clear. But that's why i thought we should make sure we agree in writing.

Let me know if your proposal of [redacted] or our embedded FPGA semiconductor IP (GDS, etc) licensing revenues is for the license above.

Thanks,

Geoff Tate, CEO

<FlexLogic Color-01 CROPPED 50 pixels high.jpg>

www.flex-logix.com
2465 Latham Street, Suite 100
Mountain View, California 94040, USA

On Jul 14, 2017, at 6:18 PM, Venkat Konda <venkat@kondatech.com> wrote:

Geoff,

I am not sure where the confusion is.
I am willing to give what you are asking. (In fact I myself proposed those options also).
I thought you will give a proposal for it.
But if you want me to I can give it too.
Let us meet tonight @ 9pm or after, alternatively tomorrow @ your convenience so that we can reach a settlement.

Thanks,
Venkat

Sent from my iPhone

On Jul 14, 2017, at 4:07 PM, geoff tate Flex Logix <geoff@flex-logix.com> wrote:

I just got back to my office from multiple meetings.

I just noticed your comment below — this makes your proposal unacceptable. We have said before that any license needs to be such that we never have to negotiate with you again. If that's your position we cannot even consider this proposal.

Thanks, Geoff

**My offer is only for the currently interfering/overlapping parts of both of our patents/patent applications like "2D-Layout", "Mesh connections" etc.**

**1) If you want to license all Konda interconnect technology (As I said before it includes significantly more area, power, performance, routing time improvements), You need to give me an offer.**
**2) In addition to 1) if you need future Konda interconnect patents (future proofing), you need to give me an offer.**

Geoff Tate, CEO

<FlexLogic Color-01 CROPPED 50 pixels high.jpg>

www.flex-logix.com
2465 Latham Street, Suite 100
Mountain View, California 94040, USA

> On Jul 14, 2017, at 2:26 PM, Venkat Konda <venkat@kondatech.com> wrote:
>
> Geoff,
>
> In the past, one potential licensees asked me for a reference from the previous licensees, typically about my personality, interaction experience with me, and some high level good comments about Konda interconnect Technology etc.
> (For example one licensee gave a reference that I delivered more than what I promised like I improved the routing speed compared to what they had before (which they did not expect prior).
>
> Hope you have looked all my inline comments on each item.
>
> Thanks,
> Venkat

---

**From:** Geoff Tate Flex Logix <geoff@flex-logix.com>
**To:** Venkat Konda <venkat@kondatech.com>
**Cc:** geoff tate <geoff@flex-logix.com>
**Sent:** Friday, July 14, 2017 2:12 PM
**Subject:** Re: Confirming your proposal from this morning's meeting 14 July 2017

I dont understand #2 re good reference letters -- please explain.
Thanks

Geoff Tate
CEO
Flex Logix Technologies, Inc.
www.flex-logix.com
NOTE OUR NEW ADDRESS
2465 Latham Street
Mountain View, CA 94040 USA

Sent from iphone: please excuse typos!

On Jul 14, 2017, at 13:25, Venkat Konda <venkat@kondatech.com> wrote:

Hi Geoff,

Just got into my office and checking your mail.
Thank you for the meeting today.
I have a few important corrections **(inline in RED Block letters)...**

**1) I need advertisement on your website that you licensed Konda interconnect technology.**
**2) I also need good reference letters.**
**3) That is what I could think of for now. if there are any common reasonable license agreement items we missed to include, we can discuss.**

**Also I need an assurance by Monday 7/17/17 if you need more time beyond.**

Otherwise for any other things to discuss I am available anytime to meet to discuss even during the weekend.

Please let me know if you agree with my corrections.

Thanks,
Venkat

---

**From:** Geoffrey Tate <geoff@flex-logix.com>
**To:** Venkat Konda <venkat@kondatech.com>
**Cc:** geoff tate <geoff@flex-logix.com>
**Sent:** Friday, July 14, 2017 10:38 AM
**Subject:** Re: Confirming your proposal from this morning's meeting 14 July 2017

Sorry - I made a typo on the first email. Please confirm this version.
(I replaced “your” with “Flex Logix” re right to sublicense
Thanks, Geoff

> On Jul 14, 2017, at 10:28 AM, Geoffrey Tate <geoff@flex-logix.com> wrote:
>

> Hello Venkat,
>
> Thank you for taking the time to meet with me this morning.
>
> Before I send your proposal on to my Board, I would like to make sure I have the correct understanding.
>
> I think your proposal is:
>
> Effective as of signing of a contract, to be done quickly, if we agree:
> - [redacted] payment shortly after signing
> - then on each following anniversary the greater of [redacted] of revenues of embedded FPGA GDS licensing (license fees and royalties)

**Each beginning of the anniversary you pay [redacted] at the end of that year.**
**Also revenue is for all of your products in which you use Konda interconnect technology (i.e. embedded FPGA GDS or any FPGA or any other products you may introduce in future using Konda interconnects )**

> - in return we have a license to any or all of your current and/or future patents that may be required for our embedded FPGA products

**My offer is only for the currently interfering/overlapping parts of both of our patents/patent applications like "2D-Layout", "Mesh connections" etc.**

**1) If you want to license all Konda interconnect**

**technology (As I said before it includes significantly more area, power, performance, routing time improvements), You need to give me an offer.**
**2) In addition to 1) if you need future Konda interconnect patents (future proofing), you need to give me an offer.**
**3) I am also open for any services from me. Please let me know.**

> - and we have the right to sublicense, only for the use of Flex Logix' embedded FPGA products, to all of our customers
**YES. Sublicensing is only Flex Logix's embedded FPGA blocks, but NOT directly Konda Patents.**

> - this agreement to last for the life of any patents that are required
**YES**

>
> Please confirm.
>
> I will then forward and will advise when I get responses from my board members.- as I mentioned because of vacation/travel it may take longer than typically.
>
> Thank you,
>
> Geoff Tate
> CEO Flex Logix

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# EXHIBIT 32

Gmail

**Venkat Konda <venkat@kondatech.com>**

# Due Date Expired: Sunday May 20, 2018 11:59PM PDT; Konda never will give license to Flex-logix!

**Venkat Konda** <venkat@kondatech.com> Sun, May 20, 2018 at 11:58 PM
To: geoff tate Flex Logix <geoff@flex-logix.com>, peter.hebert@luxcapital.com, gregory.stone@mto.com
Cc: Venkat Konda <venkat@kondatech.com>

Dear Geoff, Pierre. Peter and Gregory:

The Due date Sunday May 20, 2018 11:59PM PDT expired! Now Konda Technologies will never give license to Flex-logix!

On Saturday 19th Gregory left a VM for me and after that I called back and left a VM. If you are interested I am open for **one and only one meeting with no time limit.** I am hoping for an amicable business meeting to see if we can reach a settlement. If you agree for this one meeting, I will try my best to be collaborative to work with you. I have my proposal as follows for a settlement.

**With the discovery of those two DARPA proposals and the follow-on developments, I will put the key points of my proposal as follows:**

1. Get a non-exclusive license from Konda Technologies and have absolutely no issues with Konda IP for ever. (Trust me Konda will fully support Flex-logix to become successful)
2. Withdraw/abandon all the interconnect patents and patent applications Wang and Markovic filed. Promise that they will never do it in future in writing.
3. [redacted]
4. Transfer Wang and Markovic's complete equity to Konda.
5. Regardless I will push forward with ISSCC/IEEE, UCLA and DARPA on both those two guys to disqualify the PhD Dissertation and the two papers they published (If they happen to publish more papers that I am not aware as of now, they will also be vacated), by proving research misconduct, willful patent infringement and fraud.
6. By choosing the licensing model, I have worked with almost all the prevailing FPGA interconnects in the market and patent-protected multi-stage interconnect based FPGA fabric. Implementation is not a rocket science.

(I will add other smaller points like giving publicity to Konda IP on your website, etc. later)

From March 27, 2016 since my first email I have been saying those two guys stole Konda IP and presented the stolen interconnect IP to you as if it is theirs. THAT PROVED TRUE with those two DARPA documents.
Also as I have been saying I am NOT trying to take advantage of what those two guys did. But I am trying to be fair to you and Flex-logix, which is what I have been saying and **doing** all along including now.
[redacted]

If you are interested please call with the times of your convenience, **please DO come to the meeting with your proposal with the consent of all the people involved which is a MUST** and let us explore if we can reach a settlement. **This is only one meeting.** Otherwise I am NOT interested in this phone tag play.

Once again, the Due date Sunday May 20, 2018 11:59PM PDT expired! Now Konda Technologies will never give license to Flex-logix!

Sincerely,
Venkat

Venkat Konda, PhD
Founder/CEO
Konda Technologies Inc.

E-mail: venkat@kondatech.com
Cell # 408-472-3273
Web: www.kondatech.com

On Fri, May 18, 2018 at 10:08 PM, Venkat Konda <venkat@kondatech.com> wrote:

> Dear Geoff, Pierre. Peter and Gregory:
>
> The two DARPA proposals I sent to you on May 6th were also submitted to UCLA and IEEE on May 7th.
> On Wednesday 16th, I was @ UCLA. I spoke to UCLA counsel who told that me that the evidence in those two DARPA proposals along with other documents I submitted while they are still reviewing them for Research Misconduct and Willful Patent infringement allegations will also fall into a third and bigger category of fraud etc. which will lead to disciplinary actions from the highest offices of UC. And UCLA already provided that 3rd department with all the details and suggested me to submit the evidence to the 3rd department as well.
>
> After I left a message with Gregory's office on Wednesday evening, I received a voice mail from Gregory this morning @10:03 AM while I was on another call this morning. I have called back Gregory @ 1:26PM this afternoon but could only leave a voicemail. As of this moment I do not have legal representation. Realistically speaking I will not have legal representation during the next two days.
>
> As I said, May 20th is the birthday of one of the Saint I follow. So it is a sacred day for me and hence I will stick to what I said before.
> I will make myself available anytime to reach an amicable settlement on both 19th and 20th.
>
> I have provided so many details of information all along.
> [redacted]
>
> Please let me know if any of you want to meet me to explore an amicable settlement before the due date May 20th 11:59 PDT.
>
> Sincerely,
> Venkat
>
> Venkat Konda, PhD
> Founder/CEO
> Konda Technologies Inc.
> E-mail: venkat@kondatech.com
> Cell # 408-472-3273
> Web: www.kondatech.com
>
> On Sun, May 13, 2018 at 11:58 PM, Venkat Konda <venkat@kondatech.com> wrote:
>
> > Dear Geoff, Pierre and Peter:
> >
> > I have not heard from you so far after I submitted the crucial evidence last week.
> > May 20th isn the birthday of one of the Saint I follow. So it is a sacred day for me and hence I will stick to what I said before.
> >
> > Please let me know if you want to meet me to explore an amicable settlement before the due date May 20th.
> >
> > With the discovery and the submission of DARPA proposals, I am also in the process of signing up with an attorney. And if you prefer to engage with my attorney for the settlement talks, please let me know.
> >
> > Sincerely,
> > Venkat
> >
> > Venkat Konda, PhD
> > Founder/CEO
> > Konda Technologies Inc.
> > E-mail: venkat@kondatech.com
> > Cell # 408-472-3273
> > Web: www.kondatech.com

On Sun, May 6, 2018 at 11:58 PM, Venkat Konda <venkat@kondatech.com> wrote:

Dear Geoff, Pierre and Peter:

A gentle remainder...
Exactly 2 more weeks for the due date: - **Sunday May 20, 2018 11:59PM PDT**; I am open to settle by then OR Konda Technologies never will give license to Flex-logix.

[redacted]

Also while trying to put together formal complaint to UCLA, IEEE and DARPA, I have been **revisiting** all the information and relevant documents I collected since I first found out on December 18, 2015 i.e. what Wang and Markovic did. **In this process, just three days ago for the first time, I found two very very critical documents (TWO DARPA PROPOSALS SUBMITTED IN 2010). Now I am going to describe about those two documents.**

**These two DARPA proposals were completely written by Wang and Markovic (Konda's contribution is Konda Bio, Konda Technologies patent portfolio, schedule of SOW) (Both of them are attached with this mail):**

**1) DARPA Proposal submitted in June 2010 (Due Date: June 23, 2010);**
Proposal #: D082-014-0673; Title of Proposed Effort: Regular Geometry Micro-Cells and Design Tools for Butterfly FPGA

**2) DARPA Proposal submitted in August 2010 (Due Date: August 6, 2010);**
Title: Energy-Efficient Butterfly FPGA Hardware and Programming Tools

I could not locate these two DARPA proposals until three days ago. Furthermore I could not anticipate such a valuable information/proof will be available in these two DARPA proposals since I first found out about what Wang and Markovic did. How did I miss them till now? If only I found them sooner, my job would have been lot lot more easier to prove this case. I am kicking myself.

Once I started reading these two DARPA proposal completely written by Wang and Markovic, I again GOT THE SHOCK OF MY LIFE.
What kind of daredevilry by these two?
What kind of daylight robbery by these two?
What kind of utter stupidity?

[redacted]

**What the two DARPA grant proposals reveal:**

1. Clearly proves that Wang and Markovic have read and thoroughly understood "Konda Technologies Business and Technology Presentation to ITA/UCLA dated October 12, 2009". (This is illegal as Wang does not have permission to read this Konda Technologies confidential document")
2. Clearly proves that Wang and Markovic were aware of Konda Technologies Complete Patent Portfolio by June/August 2010.
    1. To be clear there were 10 provisional patent applications, 5 PCT applications and 5 US patent applications were filed by Konda and assigned to Konda Technologies by June/August 2010.
3. Clearly Wang has already did 3 chips with the complete details given in the August 6, 2010 DARPA Proposal. (In early 2010, Markovic told Konda on the phone that his students were implementing Konda routing fabric Konda in a chip. Then Konda warned Markovic not to implement without taking license from Konda Technologies. Markovic responded saying that as a University professor he can pull out any public document including patents/paten applications and implement them. Then Konda replied that it is not true and advised Markovic to consult an attorney.)
    1. Immediately after October 12, 2009 meeting Wang started reading and understanding Konda Technologies proprietary documents and patent applications and implementing them in a chip. Otherwise how would he have 3 chips implemented by August 6, 2010? In August DARPA proposal it is stated that Chip 1 was run December 2009 itself.
    2. In one of Flex-logix's press releases, it was mentioned that Wang did 5 chips while he was @ UCLA. So two more chips must have been taped out after August 2010.
4. Clearly proves that I shared lot of Konda Technologies activities to Markovic such as which potential customers I have been meeting and which customers I am consulting with.
5. Both these DARPA proposals were written by Wang. The language, writing style, the diagrams are same as in the Wang's PhD Dissertation.
6. Now if you refer to what I wrote about the research misconduct and patent infringement previously with details about 2011 VLSI Circuits Symposium paper, 2013 PhD Dissertation and 2014 ISSCC paper, (all three were written and submitted much after these TWO DAPRA proposals were written), it is clearly evident of research misconduct by Wang and Markovic.
7. Furthermore the diagrams clearly illustrate that Konda interconnect itself has scrambled inlet/outlet links between LUTs and first stage switches. (This is what they claimed as CLAIMS in the interconnect patent they got granted) Clear proof infringement as well as plagiarism.
8. To prove willful patent infringement by Wang and Markovic, I do not need to provide claim charts anymore as the text and diagrams are the same as in the DARPA proposals as well as Wang and Markovic 2 papers, PhD Dissertation and patents they got granted.
9. Also Wang filed a patent applications (after leaving UCLA) and as part of Flex-logix whcih he gets them granted. Wang describes that Konda interconnect subsumes "pyramid networks" in the DARPA proposals. A pyramid network is comprises both hierarchical connections and mesh connections. This FLex-logix patent applications (and its continuation applications) plagiarizes mesh connections. (So DARPA proposals also prove that Wang"s Flex-logix's patent is also submitted by plagiarizing Konda IP).

[redacted]

I hope this will give clear proof to you of what those two did.
Please propose the times if you would like to meet me to reach a settlement before the due date May 20, 2018.
I will do my very best for a settlement until May 20, 1018.

Sincerely,
Venkat

Venkat Konda, PhD
Founder/CEO
Konda Technologies Inc.
E-mail: venkat@kondatech.com
Cell # 408-472-3273
Web: www.kondatech.com

On Sun, Apr 29, 2018 at 11:58 PM, Venkat Konda <venkat@kondatech.com> wrote:

> Dear Geoff, Pierre and Peter:

# EXHIBIT 33

Gmail

**Venkat Konda <venkat@kondatech.com>**

# Formal submission of Wang Markovic for BOTH Plagiarism and Patent Infringement 8-1-2018

**Venkat Konda** <venkat@kondatech.com> Wed, Aug 1, 2018 at 6:15 PM
To: "Wakimoto, Roger M" <rwakimoto@conet.ucla.edu>, "Pollack, Ann" <apollack@research.ucla.edu>
Cc: "Modlin, Claudia" <cmodlin@research.ucla.edu>, "Drown, Steven" <steven.drown@ucop.edu>, Venkat Konda <venkat@kondatech.com>

**Wang Markovic Plagiarism, Infringement, Fraud D...**

Dear Vice Chancellor and Prof. Wakimoto:

To follow up on my email to you on July 20, 2018, I am submitting my formal complaint about Cheng Wang and Dejan Markovic's Plagiarism, Infringement, Fraud Details by stealing Konda Technologies Patents/IP.
Please find the attached zipped folder for details.

**Prof. Prasant Mohapatra, UC Davis** has been helping me since June 2016 (i.,e for over two years) regarding this case. Prof. Mohapatra has served as CS Dept. Chair, Dean and Vice-provost in Graduate education to name a few. He is recently promoted as **Vice Chancellor of Research, UC Davis.** Prof. Mohapatra's research area is interconnection networks since 1980s and hence he is an expert in this research area and also a veteran expert witness in several other patent infringement cases. I have his validation for all my claims in this case as well. Please advise if you want me bring him to the investigation.

I have submitted a 57 page document namely "Wang Markovic Plagiarism, Patent Infringement and Fraud Details - SV2.0" which gives lot of elaborate details about this case.
I have also presented Claim Charts of infringement (for 7 Konda patents including continuation patents) in the folder. **So please consider this submission for both Research Misconduct as well as willful patent infringement. Please introduce me to the department in UCLA which handles Patent Infringement.**
And of course all the relevant documents are submitted.

**Once again key clarification:** The two 2010 DARPA proposals are themselves NOT plagiarized documents. But they are proof for clear and strong evidence of plagiarism by Wang and Markovic in 2014 ISSCC paper, 2013 Phd Dissertation, 2011 VLSI circuits symposium paper by Wang and Markovic.

Konda Technologies patents and IP is my livelihood. Please resolve this case ASAP. Since UCLA investigates and resolves this case by research area experts this is extremely crucial and valuable to me.

Once again I have utmost respect for universities including UCLA. I will never implicate UCLA for what Wang and Markovic did. I would rather donate funds to UCLA than implicate UCLA. For me universities including UCLA are the most sacred places.

I am only protecting Konda IP. I am fighting for the complete credit of Konda Research.
I would continue to expose what Wang and Makovic did.

I would like to get a personal meeting immediately with you to give a presentation of whatever I submitted which I believe makes it easier for you to investigate.

Please advise if anything is missing in my submission. This sort of complaint is of course new to me and so please guide me to do it the appropriate way ASAP.
I eagerly look forward to your approval of me giving a presentation of plagiarism in a face to face meeting @ UCLA and proposal of your convenient dates.

Sincerely,
Venkat

Venkat Konda, PhD
Founder/CEO

Konda Technologies Inc.
E-mail: venkat@kondatech.com
Cell # 408-472-3273
Website: www.kondatech.com

On Fri, Jul 20, 2018 at 10:08 AM, Venkat Konda <venkat@kondatech.com> wrote:

> Dear Vice Chancellor and Prof. Wakimoto:
>
> I am in receipt of the email you sent yesterday July 19, 2018.
>
> Your assessment that the two DARPA proposals submitted by Professor Dejan Markovic and Dr. Chengcheng Wang DOES NOT contain plagiarized material (text and figures) is CORRECT.
>
> However my claim is those two DARPA Documents submitted by Professor Dejan Markovic and Dr. Chengcheng Wang PROVIDE CLEAR AND STRONG EVIDENCE/PROOF that the three publications 2011 VLSI Circuits Symposium paper, 2013 PhD Dissertation and 2014 ISSCC paper CONTAIN PLAGIARIZED MATERIAL (text and figures), because for example whatever is identified as "Konda Network" and "Hierarchical Konda Interconnect Architecture" in the two DARPA documents is directly plagiarized in the three publications namely 2011 VLSI Circuits Symposium paper, 2013 PhD Dissertation and 2014 ISSCC paper. (I have attached Version 2 of those DARPA proposals in this mail. This version I have added lot more details of what is plagiarized in the three publications as well as patents filed while at UCLA and Flex-logix.)
> When I visited UCLA on May 16, 2018 and had a phone call with Mr Steven Drown on the same day, I also mentioned to him that those two DARPA Documents submitted by Professor Dejan Markovic and Dr. Chengcheng Wang PROVIDE CLEAR AND STRONG EVIDENCE/PROOF that the three publications 2011 VLSI Circuits Symposium paper, 2013 PhD Dissertation and 2014 ISSCC paper CONTAIN PLAGIARIZED MATERIAL (text and figures),
>
> Also in your response, there is no feedback regarding the details I gave in the folder "Wang-Markovic research misconduct", so I believe you forgot to review that material where I provided details of plagiarism in the three publications namely 2011 VLSI Circuits Symposium paper, 2013 PhD Dissertation and 2014 ISSCC paper.
>
> **********
>
> Now I am copy/pasting the following 9 points I wrote in my May 7, 2018 email to you. I am highlighting in RED and also underlining the lines where I communicated that PLAGIARISM was performed in the three publications namely 2011 VLSI Circuits Symposium paper, 2013 PhD Dissertation and 2014 ISSCC paper.
>
> **What the two DARPA proposals clearly prove:**
>
> 1. Clearly proves that Wang and Markovic have read and thoroughly understood "Konda Technologies Business and Technology Presentation to ITA/UCLA dated October 12, 2009". (This is illegal as Wang does not have permission to read this Konda Technologies confidential document")
> 2. Clearly proves that Wang and Markovic were aware of Konda Technologies Complete Patent Portfolio by June/August 2010.
>    1. To be clear there were 10 provisional patent applications, 5 PCT applications and 5 US patent applications were filed by Konda and assigned to Konda Technologies by June/August 2010.
>    2. So Wang deliberately and knowingly did neither cite these patents (and the material they wrote in in the two DARPA documents) nor compare with them in 2011 VLSI Circuits Symposium paper, 2013 PhD Dissertation and 2014 ISSCC paper.
> 3. Clearly Wang has already done 3 chips with the complete details given in the August 6, 2010 DARPA Proposal. (In early 2010, Markovic told Konda on the phone that his students were implementing Konda routing fabric Konda in a chip. Then Konda warned Markovic not to implement without taking license from Konda Technologies. Markovic responded saying that as a University professor he can pull out any public document including patents/paten applications and implement them. Then Konda replied that it is not true and advised Markovic to consult an attorney.)
>    1. Immediately after October 12, 2009 meeting Wang started reading and understanding Konda Technologies proprietary documents and patent applications and implementing them in a chip. Otherwise how would he have 3 chips implemented by August 6, 2010? In August DARPA proposal it is stated that Chip 1 was run December 2009 itself.
>    2. In one of Flex-logix's press releases, it was mentioned that Wang did 5 chips while he was @ UCLA. So two more chips must have been taped out after August 2010.
> 4. Clearly proves that I shared lot of Konda Technologies activities to Markovic such as which potential customers I have been meeting and which customers I am consulting with.
> 5. Both these DARPA proposals were written by Wang. The language, writing style, the diagrams are same as in the Wang's PhD Dissertation.

6. Now if you refer to what I wrote about the research misconduct and patent infringement with details about 2011 VLSI Circuits Symposium paper, 2013 PhD Dissertation and 2014 ISSCC paper, (all three were written and submitted/published much after these TWO DAPRA proposals were written), it is clearly evident of research misconduct by Wang and Markovic.
7. Furthermore the diagrams in DARPA proposals clearly illustrate that Konda interconnect itself has scrambled inlet/outlet links between LUTs and first stage switches. (However this is what they claimed as CLAIMS in the interconnect patent they got granted) Clear proof for infringement as well as plagiarism.
8. To prove willful patent infringement by Wang and Markovic, I do not need to provide claim charts anymore as the text and diagrams are the same as in the DARPA proposals as well as in Wang and Markovic 2 papers, PhD Dissertation and patents they got granted.
9. Wang clearly acknowledges Konda patents (and the material in the two DARPA documents) are seminal and the 2D BFT layout is extremely valuable but does neither cite about these layouts in any of his publications nor compare with them.

**********

I certainly understand I provided lot of information in text form and perhaps that is the reason why you missed those key points. **So I request the following, please consider:**

1. I will provide the tables and pictures to illustrate the evidence of plagiarism more clearly so that misunderstandings are eliminated.
2. Also please allow me to visit UCLA and give a presentation of the research misconduct to explain everything to the people who are going to perform initial investigation
3. Please propose your convenient dates for me to visit UCLA.

Once again I have utmost respect for universities including UCLA. I will never implicate UCLA for what Wang and Markovic did. I would rather donate funds to UCLA than implicate UCLA. For me universities including UCLA are the most sacred places.

I am only protecting Konda IP. I am fighting for the complete credit of Konda Research.
I would continue to expose what Wang and Makovic did.

**Once again, while I am yet to file the formal complaint, I have the following questions:**

1. Can I submit the allegations in phases like
    1. Research Misconduct I have described in this email thread (Sort of first order Research Misconduct allegations). I will also add complete background story of my interaction with them throughout the allegation period.
    2. Research Misconduct - Complete specific technical details with plagiarized diagrams, text with clear references to the specific pages in the documents they published as well as Konda Technologies documents, tables of specific elements or concepts plagiarized, falsified and/or fabricated.
    3. Patent Infringement - Claim charts and also evidence to demonstrate willful patent infringement.
2. Do I have to submit all of the above at a time i.e. before you begin investigation
3. Will there be interaction with UCLA after I submit the complaint.

Please keep asking me for details as I have lot more information.
I eagerly look forward to your approval of me giving a presentation of plagiarism in a face to face meeting @ UCLA and proposal of your convenient dates.

Sincerely,
Venkat

Venkat Konda, PhD
Founder/CEO
Konda Technologies Inc.
E-mail: venkat@kondatech.com
Cell # 408-472-3273
Website: www.kondatech.com

On Thu, Jul 19, 2018 at 12:31 PM, Pollack, Ann <APollack@research.ucla.edu> wrote:

Dear Dr. Konda:

Please see the attached letter from Vice Chancellor Wakimoto.

Thank you,

Ann Pollack

Assistant Vice Chancellor – Research

UCLA

10889 Wilshire Boulevard, Suite 900

Telephone: 310-794-0387

e-mail: apollack@research.ucla.edu

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# EXHIBIT 34

Gmail

**Venkat Konda <venkat@kondatech.com>**

# OK meet you as planned -- Re: 3pm Monday @ Starbucks, 750 Castro, Mt View -- Re: To reach a resolution

**geoff tate Flex Logix** <geoff@flex-logix.com> Mon, Jul 9, 2018 at 1:24 PM
To: Venkat Konda <venkat@kondatech.com>
Cc: geoff tate <geoff@flex-logix.com>

Hi Dr. Konda,

OK i'll see you 3pm at the usual starbucks 750 Castro Mt View.

Geoff Tate, CEO

flexlogix Technologies, Inc.

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www.flex-logix.com
2465 Latham Street, Suite 100
Mountain View, California 94040, USA

On Jul 9, 2018, at 1:22 PM, Venkat Konda <venkat@kondatech.com> wrote:

Dear Geoff,

Let us meet and discuss.
Look forward to meeting you @ 3PM.

Regards,
Venkat

Venkat Konda, PhD
Founder/CEO
Konda Technologies Inc.
E-mail: venkat@kondatech.com
Cell # 408-472-3273
Web: www.kondatech.com

On Mon, Jul 9, 2018 at 1:17 PM, geoff tate Flex Logix <geoff@flex-logix.com> wrote:

> Dr. Konda,
>
> I can meet with you if your alternatives are consistent with :
>
> > If and when you are ready for a serious discussion let me re-iterate the key terms that we have already told you such a settlement must contain
> > - Dr. Konda and Kondatech must license all patents worldwide, that are now issued or that issue from any filing already made as of the date of the settlement, to Flex Logix and it's licensees
> > - Dr. Konda and Kondatech must cease all negative statements about Flex Logix and it's Co-Founders and retract allegations made to UCLA and ISSCC
> > - In return Flex Logix would pay [redacted]
>
> If so, I still can meet at 3pm today.
> Please advise.

Geoff Tate, CEO

<FlexLogic Color-01 CROPPED 50 pixels high.jpg>

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2465 Latham Street, Suite 100
Mountain View, California 94040, USA

On Jul 9, 2018, at 12:33 PM, Venkat Konda <venkat@kondatech.com> wrote:

Dear Geoff,

You seem to misunderstand what I wrote.

[redacted]

I believe we should resolve the issues by meeting and talking. I thought about a few alternatives to discuss.

I am open to meet you @ 3PM.
Please let me know if you want to meet.

Regards,
Venkat

Venkat Konda, PhD
Founder/CEO
Konda Technologies Inc.
E-mail: venkat@kondatech.com
Cell # 408-472-3273
Web: www.kondatech.com

On Mon, Jul 9, 2018 at 8:16 AM, geoff tate Flex Logix <geoff@flex-logix.com> wrote:

> Hello Dr. Konda,
>
> Your lawyers are the ones that should be answer your questions below.
>
> I have talked to 2 different execs who had been at FPGA companies you dealt with: both were negative about your technology.
>
> [redacted]
>
> If and when you are ready for a serious discussion let me re-iterate the key terms that we have already told you such a settlement must contain

- Dr. Konda and Kondatech must license all patents worldwide, that are now issued or that issue from any filing already made as of the date of the settlement, to Flex Logix and it's licensees
- Dr. Konda and Kondatech must cease all negative statements about Flex Logix and it's Co-Founders and retract allegations made to UCLA and ISSCC
- In return Flex Logix would pay [redacted]. No equities, no royalties.

The Board has authorized [redacted]. Perhaps I could convince them to consider a little more but you would have to dramatically change your position to make it even worth considering.

Your email indicates a meeting today would be a waste of your time and mine. So I will not be meeting you today at 3pm.

Let me know if/when you are ready for a discussion along the lines outlined above.

Our lawyers are moving ahead with litigation. We'd prefer peace through a reasonable settlement. As we spend more cash on litigation we'll have less motivation to settle.

Geoff Tate, CEO

<FlexLogic Color-01 CROPPED 50 pixels high.jpg>

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Mountain View, California 94040, USA

> On Jul 9, 2018, at 2:28 AM, Venkat Konda <venkat@kondatech.com> wrote:
>
> Dear Geoff,
>
> Look forward to 3PM meeting Monday. As I said I am looking forward to this meeting as one final BUSINESS meeting for an amicable resolution.
>
> However looks like I need to summarize the last couple of months of discussion with Greg. [redacted] told me after last weeks phone conversation with Greg as follows:
>
> 1. If you do not infringe Konda patents why do you want to invalidate Konda patents?
> 2. He wondered in this clear case of infringement/fraud, what is the point of legal expenditure for you?
> 3. So he told me to contact you directly and that is how I left a VM and sent an email. (Two months ago I said several times I wanted to meet you and not your attorney). [redacted] However I am the inventor and the expert of this IP and so as always I will be open and transparent.
>
> [redacted]

[redacted]

It is your choice how much you want to spend on legal fees. As I said before "After the due date May 20, 2018 expired, I was completely prepared not to expect any revenue from your company by not willing to give a license. [redacted]

Look forward to the meeting @ 3PM.

Regards,
Venkat

Venkat Konda, PhD
Founder/CEO
Konda Technologies Inc.
E-mail: venkat@kondatech.com
Cell # 408-472-3273
Web: www.kondatech.com

1. On Sat, Jul 7, 2018 at 6:32 AM, geoff tate Flex Logix <geoff@flex-logix.com> wrote:

> Hello Dr. Konda,
>
> I will meet you 3pm Monday.
>
> To correct you, we do not see value in the Konda patent portfolio. As Greg Stone has told you, and your lawyer [redacted] recently, Flex Logix does not use your technology or infringe your patents.
>
> [redacted]
>
> [redacted].
>
> If you wish to settle, now is the time. I'm willing to listen to a new proposal, if you have one, that addresses the feedback Greg has given you and I have given you. But the meeting will be short if you return to your past themes and proposals.

See you 3pm Monday at Starbucks, 750 Castro, Mountain View.

Geoff Tate, CEO

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Mountain View, California 94040, USA

> On Jul 7, 2018, at 5:37 AM, Venkat Konda <venkat@kondatech.com> wrote:
>
> Dear Geoff,
>
> I will take 3 - 4:30PM slot on Monday July 9 @ the same Starbucks. Sincere thanks for accepting to meet one last time.
>
> Please let us make it an amicable and fruitful business meeting and **ABSOLUTELY** last meeting to reach an amicable resolution.
> You certainly seem to have realized the value of non-exclusive license to all of Konda Patent portfolio with the way you listed it.
> Please come to the meeting to seek license to very valuable IP and to meet hardworking, brilliant inventor who single-handedly invented revolutionary IP/Patents for ~11 years. Similarly I will come to the meeting to give a license to a highly experienced entrepreneur with tremendous track record of building great companies from startup to valuable product selling stage.
> So I promise I will only make fair offer and definitely not exorbitant offers. Similarly I expect great respect towards me with only fair offer from you and no cheap offers.
> As always I also promise to keep factual and only factual statements including on our website and in other communications.
>
> [redacted]
> After the due date May 20, 2018 expired, I was completely prepared not to expect any revenue from your company by not willing to give a license. That is my strong mental makeup and starting point since then. it is your choice whether and how to protect your company and all the stake holders interest in your company.
>
> I only urge both of us to absolutely make this meeting fruitful and final. You and I do not have anytime for silly, meaningless meetings. Otherwise particularly I have to file a compliant immediately as there is no time left for me before 3 year period ends in December and I will signup with litigation attorney I almost finalyzed and it could be a long drawn negative battle with no upside for your company. I am fully prepared and extremely STRONG

WILLED AS ALWAYS to face the consequences of your next steps as well.

Meanwhile I sincerely hope for an amicable resolution and business collaboration by echoing what you said - this meeting to be not-wasteful but path-breaking and highly beneficial for both of our companies. Looking forward...

Regards,
Venkat

Venkat Konda, PhD
Founder/CEO
Konda Technologies Inc.
E-mail: venkat@kondatech.com
Cell # 408-472-3273
Web: www.kondatech.com

On Fri, Jul 6, 2018 at 1:56 PM, geoff tate Flex Logix <geoff@flex-logix.com> wrote:

> Dr. Konda,
>
> As Greg has told you repeatedly, and as he recently told your attorney, our Board has only authorized [redacted] settlement with you. [redacted] This license, of course, needs to extend to any customers or other persons using technology licensed from Flex Logix. If you are interested in a settlement structure in this fashion, I am willing to meet with you. On the other hand, if you continue to seek exorbitant amounts, royalties, or equity, it would be a wasteful expenditure of your time and mine to have a meeting, and I am not interested in doing so.
>
> As Greg has told you, we are currently spending money on legal fees to prepare for litigation that seems inevitable. As we spend more money on those efforts, our willingness to spend on settlement decreases.
>
> If you wish to meet with me Monday July 9, I can meet you 9am-11am or 3-430pm at the same Starbucks we have met at before: 750 Castro Street, Mountain View.
>
> Let me know.
>
> Geoff Tate, CEO
>
> <FlexLogic Color-01 CROPPED 50 pixels high.jpg>
>
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2465 Latham Street, Suite 100
Mountain View, California 94040, USA

> On Jul 5, 2018, at 5:55 PM, Venkat Konda <venkat@kondatech.com> wrote:
>
> Dear Geoff,
>
> I am writing this message to see if we two can meet to reach an amicable resolution. I do not believe attorneys can resolve the issue amicably. So it is in the best interest of both of us, saving money and time, to amicably reach a resolution. This is my last ditch effort before I sign up with a litigation attorney. I am in town till Monday 7/9. Please advise if we can meet anytime before that.
>
> Regards,
> Venkat
>
> Venkat Konda, PhD
> Founder/CEO
> Konda Technologies Inc.
> E-mail: venkat@kondatech.com
> Cell # 408-472-3273
> Web: www.kondatech.com
>
> --
>
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# EXHIBIT 35

Gmail **Venkat Konda <venkat@kondatech.com>**

# Your FPGA 2019 Submission (Number 143)

**PC Chair, FPGA 2019** <fpga2019@softconf.com> Wed, Nov 14, 2018 at 10:52 PM
Reply-To: stephen.neuendorffer@xilinx.com
To: venkat@kondatech.com

Dear venkat konda:

On behalf of the FPGA 2019 Program Committee, I would like to inform you that the following submission has been accepted to appear as a poster at the conference:

Hierarchical FPGA Fabrics using 2D-Benes-BFT-Pyramid Network Layouts with Optimizations

The Program Committee worked very hard to thoroughly review all the submitted papers and to provide feedback to enable you to improve your work. Unfortunately, due to time constraints, not all interesting papers can be presented at the conference in complete form. The poster format allows you a forum to present your work and discuss with members of the community along with an abstract in the published proceedings. However, since your work is not being presented in full form, you still have the opportunity to revise your paper and submit it to another conference. We hope you will take this opportunity to come to the conference and discuss your work.

Instructions to upload your final abstract are at the following site:

https://www.scomminc.com/pp/acmsig/fpga2019.htm

The reviews and comments are attached below.

Congratulations on your fine work. If you have any additional questions, please feel free to get in touch.

Best Regards,
Stephen Neuendorffer, PC Chair, FPGA 2019
FPGA 2019

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================================================================================
FPGA 2019 Reviews for Submission #143
================================================================================

Title: Hierarchical FPGA Fabrics using 2D-Benes-BFT-Pyramid Network Layouts with Optimizations
Authors: venkat konda
================================================================================
                            REVIEWER #1
================================================================================

--------------------------------------------------------------------------------
Reviewer's Scores
--------------------------------------------------------------------------------
[redacted]

Detailed Comments
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[redacted]
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[redacted]

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==========
REVIEWER #2
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Reviewer's Scores
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[redacted]

Detailed Comments
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[redacted]

(2) [redacted]

(3) [redacted]

(4) Similar work has been published before (for example, "Building Efficient, Reconfigurable Hardware using Hierarchical Interconnects" thesis by Wang, Chengcheng) but is not referenced

(5) [redacted]

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REVIEWER #3
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Reviewer's Scores
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[redacted]

[redacted]

Detailed Comments

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[redacted]

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REVIEWER #4

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Reviewer's Scores

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[redacted]

Detailed Comments

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[redacted]

*. [redacted]

[redacted]

*. You should refer to this paper and compare your approach with theirs.
A Multi-Granularity FPGA with Hierarchical Interconnects for Efficient and Flexible Mobile Computing
Cheng C. Wang etc.
ISSCC 2014
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FPGA 2019 - https://www.softconf.com/i/fpga2019

# EXHIBIT 36

H3340238

FILED
In the Office of the Secretary of State
of the State of California
JAN 04 2011

# ARTICLES OF INCORPORATION

I

The name of this corporation is HIERLOGIX INC.

II

The purpose of the corporation is to engage in any lawful act or activity for which a corporation may be organized under the **General Corporation Law** of California other than the banking business, the trust company business or the practice of a profession permitted to be incorporated by the California Corporations Code.

III

The name and address in the State of California of this corporation's initial agent for service of process is:

Name: Chengcheng Wang

Address: 15220 S. Normandie Avenue, Unit 304

City: Gardena State: **CALIFORNIA** Zip: 90247

IV

This corporation is authorized to issue only one class of shares of stock; and the total number of shares, which this corporation is authorized to issue, is ONE HUNDRED THOUSAND (100,000).

Dennis W. Chiu, Incorporator

# State of California
## Secretary of State

**S**

**E-G78343**

**FILED**

In the office of the Secretary of State of the State of California

**Sep - 24 2011**

This Space For Filing Use Only

### Statement of Information
**(Domestic Stock and Agricultural Cooperative Corporations)**

**FEES (Filing and Disclosure): $25.00. If amendment, see instructions.**

**IMPORTANT - READ INSTRUCTIONS BEFORE COMPLETING THIS FORM**

1. **CORPORATE NAME**

C3340238
HIERLOGIX INC.

**Due Date:**

**Complete Addresses for the Following** (Do not abbreviate the name of the city. Items 2 and 3 cannot be P.O. Boxes.)

| | CITY | STATE | ZIP CODE |
|---|---|---|---|
| 2. STREET ADDRESS OF PRINCIPAL EXECUTIVE OFFICE<br>15220 S NORMANDIE AVE UNIT 304 GARDENA CA 90247 | | | |
| 3. STREET ADDRESS OF PRINCIPAL BUSINESS OFFICE IN CALIFORNIA, IF ANY<br>15220 S NORMANDIE AVE UNIT 304 GARDENA CA 90247 | CITY | STATE | ZIP CODE |
| 4. MAILING ADDRESS OF THE CORPORATION, IF DIFFERENT THAN ITEM 2 | CITY | STATE | ZIP CODE |

**Names and Complete Addresses of the Following Officers** (The corporation must list these three officers. A comparable title for the specific officer may be added; however, the preprinted titles on this form must not be altered.)

| | ADDRESS | CITY | STATE | ZIP CODE |
|---|---|---|---|---|
| 5. CHIEF EXECUTIVE OFFICER/<br>CHENGCHENG WANG | 15220 S NORMANDIE AVE UNIT 304 | GARDENA, CA 90247 | | |
| 6. SECRETARY<br>CHENGCHENG WANG | 15220 S NORMANDIE AVE UNIT 304 | GARDENA, CA 90247 | | |
| 7. CHIEF FINANCIAL OFFICER/<br>CHENGCHENG WANG | 15220 S NORMANDIE AVE UNIT 304 | GARDENA CA 90247 | | |

**Names and Complete Addresses of All Directors, Including Directors Who Are Also Officers** (The corporation must have at least one director. Attach additional pages, if necessary.)

| | ADDRESS | CITY | STATE | ZIP CODE |
|---|---|---|---|---|
| 8. NAME<br>CHENGCHENG WANG | 15220 S NORMANDIE AVE UNIT 304 | GARDENA, CA 90247 | | |
| 9. NAME<br>DEJAN MARKOVIC | 715 GAYLEY AVE APT 311 | LOS ANGELES, CA 90024 | | |
| 10. NAME | ADDRESS | CITY | STATE | ZIP CODE |

11. NUMBER OF VACANCIES ON THE BOARD OF DIRECTORS, IF ANY:

**Agent for Service of Process** (If the agent is an individual, the agent must reside in California and Item 13 must be completed with a California street address (a P.O.Box address is not acceptable). If the agent is another corporation, the agent must have on file with the California Secretary of State a certificate pursuant to California Corporations Code section 1505 and Item 13 must be left blank.)

12. NAME OF AGENT FOR SERVICE OF PROCESS

CHENGCHENG WANG

| | CITY | STATE | ZIP CODE |
|---|---|---|---|
| 13. STREET ADDRESS OF AGENT FOR SERVICE OF PROCESS IN CALIFORNIA, **IF AN INDIVIDUAL**<br>15220 S NORMANDIE AVE UNIT 304 GARDENA, CA 90247 | | | |

**Type of Business**

14. DESCRIBE THE TYPE OF BUSINESS OF THE CORPORATION

ENGINEERING - ELECTRICAL

15. BY SUBMITTING THIS STATEMENT OF INFORMATION TO THE CALIFORNIA SECRETARY OF STATE, THE CORPORATION CERTIFIES THE INFORMATION CONTAINED HEREIN, INCLUDING ANY ATTACHMENTS, IS TRUE AND CORRECT.

| 09/24/2011 | CHENGCHENG WANG | PRESIDENT | |
|---|---|---|---|
| DATE | TYPE OR PRINT NAME OF PERSON COMPLETING THE FORM | TITLE | SIGNATURE |

SI-200 C (REV 10/2010)

APPROVED BY SECRETARY OF STATE

# State of California
## Secretary of State

**S**

**Statement of Information**
**(Domestic Stock and Agricultural Cooperative Corporations)**
**FEES (Filing and Disclosure): $25.00.**
**If this is an amendment, see instructions.**
**IMPORTANT - READ INSTRUCTIONS BEFORE COMPLETING THIS FORM**

**E-U28563**
**FILED**

In the office of the Secretary of State of the State of California

**Sep - 25 2013**

This Space For Filing Use Only

1. **CORPORATE NAME**
HIERLOGIX INC.

1299 SAN TOMAS AQUINO RD 118
SAN JOSE CA 95117

2. **CALIFORNIA CORPORATE NUMBER** C3340238

**No Change Statement** ( Not applicable if agent address of record is a P.O. Box address. See instructions.)

3. **If there have been any changes to the information contained in the last Statement of Information filed with the California Secretary of State, or no statement of information has been previously filed, this form must be completed in its entirety.**
☐ If there has been no change in any of the information contained in the last Statement of Information filed with the California Secretary of State, check the box and proceed **to Item 17.**

**Complete Addresses for the Following** (Do not abbreviate the name of the city. Items 4 and 5 cannot be P.O. Boxes.)

| | CITY | STATE | ZIP CODE |
|---|---|---|---|
| 4. STREET ADDRESS OF PRINCIPAL EXECUTIVE OFFICE<br>1299 SAN TOMAS AQUINO RD 118 SAN JOSE CA 95117 | | | |
| 5. STREET ADDRESS OF PRINCIPAL BUSINESS OFFICE IN CALIFORNIA, IF ANY<br>1299 SAN TOMAS AQUINO RD 118 SAN JOSE CA 95117 | CITY | STATE | ZIP CODE |
| 6. MAILING ADDRESS OF CORPORATION, IF DIFFERENT THAN ITEM 4 | CITY | STATE | ZIP CODE |

**Names and Complete Addresses of the Following Officers** (The corporation must list these three officers. A comparable title for the specific officer may be added; however, the preprinted titles on this form must not be altered.)

| | ADDRESS | CITY | STATE | ZIP CODE |
|---|---|---|---|---|
| 7. CHIEF EXECUTIVE OFFICER/<br>DEJAN MARKOVIC | 858 CLARK WAY APT 118 | PALO ALTO | CA | 94304 |
| 8. SECRETARY<br>CHENGCHENG WANG | 1299 SAN TOMAS AQUINO RD APT 118 | SAN JOSE | CA | 95117 |
| 9. CHIEF FINANCIAL OFFICER/<br>CHENGCHENG WANG | 1299 SAN TOMAS AQUINO RD APT 118 | SAN JOSE | CA | 95117 |

**Names and Complete Addresses of All Directors, Including Directors Who Are Also Officers** (The corporation must have at least one director. Attach additional pages, if necessary.)

| | ADDRESS | CITY | STATE | ZIP CODE |
|---|---|---|---|---|
| 10. NAME<br>ROBERT BRODERSEN | 1299 SAN TOMAS AQUINO RD APT 118 | SAN JOSE | CA | 95117 |
| 11. NAME | | | | |
| 12. NAME | | | | |

13. NUMBER OF VACANCIES ON THE BOARD OF DIRECTORS, IF ANY:

**Agent for Service of Process** If the agent is an individual, the agent must reside in California and Item 15 must be completed with a California street address, a P.O.Box address is not acceptable. If the agent is another corporation, the agent must have on file with the California Secretary of S addr certificate pursuant to California Corporations Code section 1505 and Item 15 must be left blank.

14. NAME OF AGENT FOR SERVICE OF PROCESS
CHENGCHENG WANG

| | CITY | STATE | ZIP CODE |
|---|---|---|---|
| 15. STREET ADDRESS OF AGENT FOR SERVICE OF PROCESS IN CALIFORNIA, **IF AN INDIVIDUAL**<br>1299 SAN TOMAS AQUINO RD APT 118 SAN JOSE CA 95117 | | | |

**Type of Business**

16. DESCRIBE THE TYPE OF BUSINESS OF THE CORPORATION
ENGINEERING DESIGN

17. BY SUBMITTING THIS STATEMENT OF INFORMATION TO THE CALIFORNIA SECRETARY OF STATE, THE CORPORATION CERTIFIES THE INFORMATION CONTAINED HEREIN, INCLUDING ANY ATTACHMENTS, IS TRUE AND CORRECT.

| 09/25/2013 | CHENGCHENG WANG | SECRETARY | |
|---|---|---|---|
| DATE | TYPE/PRINT NAME OF PERSON COMPLETING FORM | TITLE | SIGNATURE |

# EXHIBIT 37

GREGORY P. STONE (State Bar No. 78329)
gregory.stone@mto.com
STEVEN M. PERRY (State Bar No. 106154)
steven.perry@mto.com
ELIZABETH A. LAUGHTON (State Bar No. 305800)
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350 South Grand Avenue, 50th Floor
Los Angeles, California 90071-3426
Telephone: (213) 683-9100
Facsimile: (213) 687-3702

Attorneys for Plaintiff
FLEX LOGIX TECHNOLOGIES, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA, SAN JOSE DIVISION

FLEX LOGIX TECHNOLOGIES, INC., a Delaware corporation,

Plaintiff,

vs.

VENKAT KONDA, an individual, and KONDA TECHNOLOGIES, INC., a California corporation,

Defendants.

CASE NO.

**COMPLAINT FOR:**

1. **FALSE ADVERTISING, 15 U.S.C. § 1125(a)(1)(B);**
2. **UNFAIR BUSINESS PRACTICES, CAL. BUS. & PROF. CODE § 17200 *et seq.***

**DEMAND FOR JURY TRIAL**

Flex Logix Technologies, Inc. ("Flex Logix"), a Delaware corporation, alleges:

## PARTIES

1. Plaintiff Flex Logix is a Delaware corporation with its principal place of business in the city of Mountain View, California. Flex Logix is registered to do business in California.

2. Upon information and belief, defendant Venkat Konda ("Konda") resides in San Jose, California.

3. Upon information and belief, defendant Konda Technologies, Inc. ("KondaTech") is a California corporation with its principal place of business in San Jose, California.

4. Upon information and belief, Konda owns and controls KondaTech.

5. Upon information and belief, Konda owns and manages a website with the url *www.kondatech.com*.

## JURISDICTION AND VENUE

6. This court has subject matter jurisdiction over Flex Logix's claims pursuant to 28 U.S.C. § 1331, in that Flex Logix has pled a claim under the Lanham Act, 15 U.S.C. § 1125(a)(1), and the Court has supplemental jurisdiction over Flex Logix's state law claim pursuant to 28 U.S.C. § 1367.

7. This Court has personal jurisdiction over Defendants because: the claims asserted against Defendants arise out of their commission of tortious acts in California; they regularly do or solicit business in California; they engage in persistent courses of conduct in California; and/or they expected or should reasonably have expected that the conduct at issue would have consequences in California.

8. Venue in this district is proper under 28 U.S.C. § 1391 because a substantial part of the events giving rise to the asserted claims took place in this district.

## INTRADISTRICT ASSIGNMENT

9. Pursuant to Local Rule 3-5(b), Flex Logix alleges that assignment to the San Jose Division is proper under Local Rule 3-2(e) because Plaintiff and Defendants have

their principal places of business and/or reside in the San Jose Division, as alleged *supra* at paragraphs 1-3.

**BACKGROUND**

10. Flex Logix was incorporated in 2014. Flex Logix has developed advanced technologies that enable FPGAs (field programmable gate arrays) to be easily embedded into any SoC (system-on-chip). This embedded FPGA technology allows key functions to be optimized or customized after a device is fabricated – even after a device is installed into a system in the field — and has a wide range of applications. Flex Logix provides its customers physical design and logic design files; training and assistance with architectural issues, integration and testing; and licenses covering its intellectual property. Flex Logix has spent years developing and optimizing its technology and has 11 issued patents.

11. KondaTech claims to be an IP licensing company that licenses FPGA Routing Fabric IP and interconnection networks IP in general. KondaTech claims to have been founded in 2007.

12. Beginning in or before March 2018, Konda began to make threats to Flex Logix that if Flex Logix did not pay millions of dollars (and transfer equity) to Konda and/or KondaTech, Konda would communicate false statements of fact regarding Flex Logix and its employees to customers and potential customers of Flex Logix, as well as "all the FGPA vendors." Konda also stated that he was ready to "go to jail or . . . die" over this matter and asked if Plaintiff was ready to do the same. When Flex Logix refused to pay the requested millions of dollars to Defendants, Defendants adopted what Konda called a "coarse [sic] of action" that included making false statements to Flex Logix's customers and potential customers that two of Flex Logix's founders were "fraud people" who had "stolen" Defendants' IP.

13. Defendants have created and are operating a website at kondatech.com. Upon information and belief, this website is generally and widely accessible to the public. Defendants use this website in part to advertise and promote Konda's "FPGA Routing Fabric IP and interconnection networks IP." Defendants' website contains a scroll on the

home page that falsely states that "[f]raudsters Cheng Wang and Dejan Markovic started Flex-Logix with Stolen Interconnect IP from Konda Technologies." Defendants' website also has a section titled: "Fraudsters Wang & Markovic found Flex-logix with stolen IP from Konda." Defendants' website also contains a section titled "Fraudsters Wang Markovic Stole Konda IP," where Defendants falsely accuse two of Flex-Logix's founders of engaging in "research misconduct" involving "falsification, fabrication and plagiarism."

14. The statements by Defendants cited in this Complaint are false and made in bad faith and are likely to deceive a substantial segment of the recipients of Defendants' statements. Konda has specifically stated that "if we do not settle I will turn even nasty on all the people involved in stealing Konda IP and also[]supporting it."

15. The statements by Defendants cited in the Complaint are likely to influence decisions by Plaintiff's customers and potential customers regarding their use of Plaintiff's FPGA architecture.

16. As Defendants know, allegations that a small start-up has "stolen" IP from a competitor are likely to have adverse consequences in terms of customer acceptance, hiring and retention, and potential investments. The false statements by Defendants cited in this Complaint are likely to cause injury to Plaintiff either by directly diverting of sales from Plaintiff to Defendants or other suppliers of FPGA technology, or by lessening the goodwill associated with Flex Logix and its advanced FGPA technology.

## FIRST CLAIM FOR RELIEF

### Violation of Lanham Act, 15 U.S.C. § 1125(a)(1)

17. Plaintiff incorporates by reference the allegations made in paragraphs 1-16, inclusive.

18. Defendants have made false statements of fact regarding Plaintiff, its technology, and its employees to Plaintiff's customers and potential customers. Such false statements have been made in bad faith, for the purpose of influencing those customers and potential customers not to adopt or license Plaintiff's FPGA technology and/or to adopt Defendants' technology.

19. The customers and potential customers who received Defendants' false assertions were likely to be misled and deceived by them.

20. Defendants knew, or reasonably should have known, that their statements were false and/or likely to mislead potential FPGA users.

21. As an actual and proximate result of Defendants' willful and intentional acts, Plaintiff has suffered and is likely to suffer damages in an amount to be determined at trial. Unless Defendants are enjoined, Plaintiff will suffer irreparable harm and damage to its business, reputation, and goodwill.

22. Pursuant to 15 U.S.C. § 1116, Plaintiff is entitled to damages for Defendants' Lanham Act violations; an accounting for profits made by Defendants in connection with this misconduct; and the costs of this action (in no case less than $45,000).

23. Plaintiff is informed and believes, and on that basis alleges, that Defendants' conduct was undertaken willfully and with the intention of causing confusion, mistake or deception, making this an exceptional case entitling Plaintiff to recover additional damages and reasonable attorneys' fees pursuant to 15 U.S.C. § 1117.

## SECOND CLAIM FOR RELIEF

**Violation of Cal. Bus. & Prof. Code § 17200 *et seq.***

24. Plaintiff incorporates by reference paragraphs 1 through 23, inclusive.

25. The acts of Defendants alleged herein, including but not limited to, advertising, constitute unlawful, unfair and fraudulent business practices in violation of Cal. Bus. & Prof. Code §17200, *et seq.*

26. As an actual and proximate result of Defendants' willful and intentional acts, Plaintiff has suffered and is likely to suffer damages in an amount to be determined at trial. Unless Defendants are enjoined, Plaintiff will suffer irreparable harm and damage to its business, reputation, and goodwill.

## PRAYER FOR RELIEF

WHEREAS, Plaintiff asks this Court for judgment as follows:

1. For judgment in favor of Plaintiff on its claims;

2. For actual, pecuniary, special and consequential damages in an amount to be determined at trial, but in no case less than $45,000.

3. For a preliminary and permanent injunction requiring Defendants to retract their false statements of fact regarding Plaintiff and its employees and requiring Defendants to refrain from making those, and substantially similar, false statements in the future.

4. For costs of suit, including pursuant to 15 U.S.C. § 1117;

5. For attorneys' fees and additional damages pursuant to 15 U.S.C. § 1117; and

6. For such other and further relief that the Court deems appropriate.

DATED: July 13, 2018

Respectfully submitted,

MUNGER, TOLLES & OLSON LLP
GREGORY P. STONE
STEVEN M. PERRY
ELIZABETH A. LAUGHTON

By: */s/ Steven M. Perry*
STEVEN M. PERRY

Attorneys for Plaintiff
FLEX LOGIX TECHNOLOGIES, INC.

# EXHIBIT 38

GREGORY P. STONE (State Bar No. 78329)
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Attorneys for Plaintiff
FLEX LOGIX TECHNOLOGIES, INC.

NITOJ P. SINGH (State Bar No. 265005)
DHILLON LAW GROUP INC.
177 Post Street, Suite 700
San Francisco, California 94108
Telephone: (415) 433-1700
Facsimile: (415) 520-6593

Attorneys for Defendants
VENKAT KONDA and
KONDA TECHNOLOGIES, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA, SAN JOSE DIVISION

FLEX LOGIX TECHNOLOGIES, INC., a Delaware corporation,

Plaintiff,

vs.

VENKAT KONDA, an individual, and KONDA TECHNOLOGIES, INC., a California corporation,

Defendants.

CASE NO. 5:18-cv-04222-LHK

**~~[PROPOSED]~~ ORDER CONTINUING THE INITIAL CASE MANAGEMENT CONFERENCE (AND RELATED DEADLINES) FOR SETTLEMENT PURPOSES**

Initial CMC: October 17, 2018
Time: 2:00 p.m.
Ctrm: 8, 4th Floor

Pursuant to the parties' stipulation, and for good cause shown, IT IS HEREBY ORDERED that the Initial Case Management Conference, currently scheduled for October 17, 2018, shall be continued to December 19, 2018 at 2:00 p.m. If the matter does not settle, Defendants shall respond to the Complaint on or before December 10, 2018.

DATED: September 24, 2018

Hon. Lucy H. Koh
United States District Judge

# EXHIBIT 39

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

FLEX LOGIX,

Plaintiff,

v.

VENKAT KONDA, et al.,

Defendants.

Case No. 18-CV-04222-LHK

**ORDER CONTINUING THE INITIAL CASE MANAGEMENT CONFERENCE**

Re: Dkt. No. 21

On December 5, 2018, in light of ongoing settlement negotiations, the parties filed a stipulation requesting to continue the initial case management conference set for December 18, 2018 at 2:00 p.m. to February 6, 2019. ECF No. 21.

The initial case management conference set for December 18, 2018 is CONTINUED to February 27, 2019 at 2:00 p.m. No further continuances will be granted.

**IT IS SO ORDERED.**

Dated: December 6, 2018

Lucy H. Koh

LUCY H. KOH
United States District Judge

# EXHIBIT 40

GREGORY P. STONE (State Bar No. 78329)
gregory.stone@mto.com
STEVEN M. PERRY (State Bar No. 106154)
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Facsimile: (213) 687-3702

Attorneys for Plaintiff
FLEX LOGIX TECHNOLOGIES, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA, SAN JOSE DIVISION

| | |
|---|---|
| FLEX LOGIX TECHNOLOGIES, INC., a Delaware corporation,<br><br>Plaintiff,<br><br>vs.<br><br>VENKAT KONDA, an individual, and KONDA TECHNOLOGIES, INC., a California corporation,<br><br>Defendants. | CASE NO. 5:18-cv-04222-LHK<br><br>**NOTICE OF DISMISSAL OF ACTION WITHOUT PREJUDICE PURSUANT TO RULE 41(a)(1)** |

PLEASE TAKE NOTICE that plaintiff Flex Logix Technologies, Inc. hereby dismisses the above-entitled action without prejudice pursuant to Fed.R.Civ.Pro. 41(a)(1).

DATED: December 10, 2018

MUNGER, TOLLES & OLSON LLP

By: */s/ Steven M. Perry*
STEVEN M. PERRY

Attorneys for Plaintiff
FLEX LOGIX TECHNOLOGIES, INC.

# EXHIBIT 41

Gmail **Venkat Konda <venkat@kondatech.com>**

# Fwd: Confirmation of our understanding

**Ben Singer** <BSinger@singerbea.com> Mon, Dec 10, 2018 at 7:53 PM
To: Evan Budaj <EBudaj@singerbea.com>, "venkat@kondatech.com" <venkat@kondatech.com>, "nsingh@dhillonlaw.com" <nsingh@dhillonlaw.com>

FYI

Begin forwarded message:

**From:** Ben Singer <BSinger@singerbea.com>
**Date:** December 10, 2018 at 10:52:51 PM EST
**To:** "Stone, Gregory" <Gregory.Stone@mto.com>
**Subject: Re: Confirmation of our understanding**

Mr. Stone-

Acknowledged and agreed.

Best,

BLS

On Dec 10, 2018, at 10:50 PM, Stone, Gregory <Gregory.Stone@mto.com> wrote:

> Benjamin,
>
> We have agreed that Flex Logix Technologies, Inc. will dismiss without prejudice its current action so that the parties may continue their settlement discussions without the pressure of case deadlines. If settlement discussions break down and Flex Logix Technologies, Inc. refiles some or all of the claims it has asserted in this action, Dr. Konda and Konda Technologies, Inc. will not seek to recover any of the fees and/or costs they have incurred in connection with the current action. Further, should Dr. Konda and/or Konda Technologies, Inc. wish to initiate any legal claims against Flex Logix Technologies, Inc., they each will first give Flex Logix Technologies, Inc. two business days prior notice so that Flex Logix Technologies, Inc. can refile some or all of its claims and put the parties back in the position they are in presently, where Flex Logix Technologies, Inc. is the plaintiff and Dr. Konda and Konda Technologies, Inc. are defendants. Such notice shall be given to Geoff Tate and to me and shall be in writing.
>
> Please acknowledge your agreement and we will then file the dismissal.
>
> Best regards,

Greg

**Gregory P. Stone | Munger, Tolles & Olson LLP**
350 South Grand Avenue | 50th Floor | Los Angeles, CA 90071
Tel: 213.683.9255 | Fax: 213.683.5155 | Cell: 213.309.5999
gregory.stone@mto.com | www.mto.com

# EXHIBIT 42

Gmail **Venkat Konda <venkat@kondatech.com>**

# FW: Flex Logix/Konda Notice

**Evan Budaj** <EBudaj@singerbea.com> Thu, Dec 13, 2018 at 4:28 PM
To: Venkat Konda <venkat@kondatech.com>
Cc: Ben Singer <BSinger@singerbea.com>, "Nitoj Singh (DhillonLaw)" <nsingh@dhillonlaw.com>

FYI

Thanks,

Evan

**From:** Evan Budaj
**Sent:** Thursday, December 13, 2018 4:28 PM
**To:** 'Gregory.Stone@mto.com' <Gregory.Stone@mto.com>; 'geoff@flex-logix.com' <geoff@flex-logix.com>
**Cc:** Ben Singer <BSinger@singerbea.com>; 'Nitoj Singh (DhillonLaw)' <nsingh@dhillonlaw.com>
**Subject:** Flex Logix/Konda Notice

Greg and Geoff,

Per our discussions, Mr. Konda and Konda Technologies hereby provide notice in order to preserve their rights to file a lawsuit on Monday, December 17, 2018—i.e., two business days from today—regarding the wrongs committed by Flex Logix against Mr. Konda and Konda Technologies that have been the subject of the parties' discussions. Please note that in the interim we intend to continue our good-faith negotiations. We plan to check in with you at least by tomorrow, and to provide notice on the morning of Monday, December 17, 2018 if we intend to file later that day.

Best,

singer bea LLP

**Evan Budaj**

Email: ebudaj@singerbea.com

Web: www.singerbea.com

(628) 400-4125 (direct)

601 Montgomery Street, Suite 1950

San Francisco, California 94111

(415) 500-6080 (main/fax)

# EXHIBIT 43

HARMEET K. DHILLON (SBN: 207873)
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DHILLON LAW GROUP INC.
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San Francisco, California 94108
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Facsimile: (415) 520-6593

*Attorneys for Plaintiff Konda Technologies, Inc.*

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

KONDA TECHNOLOGIES, INC., a California corporation,

Plaintiff,

v.

FLEX LOGIX TECHNOLOGIES, INC.,

Defendant.

CASE NO. 5:18-CV-7581

**COMPLAINT FOR:**

1. **Unfair Business Practices**
2. **Infringement of U.S. Patent No. 8,269,523**
3. **Infringement of U.S. Patent No. 8,898,611**
4. **Infringement of U.S. Patent No. 9,529,958**
5. **Infringement of U.S. Patent No. 10,003,553**
6. **Infringement of U.S. Patent No. 10,050,904**

**JURY TRIAL DEMANDED**

Plaintiff Konda Technologies, Inc. ("Konda Tech"), by and through its undersigned counsel, hereby asserts as follows against Defendant Flex Logix Technologies, Inc. ("Flex Logix"). Upon information and belief, Konda Tech alleges as follows:

## NATURE OF THE ACTION

1. This is a civil action for patent infringement arising under the patent laws of the United States, Title 35 of the United States Code.

2. As set forth in more detail below, Flex Logix has been infringing United States Patent Nos. 8,269,523 (the "'523 patent"); 8,898,611 (the "'611 patent"); 9,529,958 (the "'958 patent"); 10,003,553 (the "'553 patent") and 10,050,904 (the "'904 patent") (collectively, the "patents-in-suit"), and continue to do so through the present date.

## PARTIES

3. Konda Tech is a California corporation with its principle place of business in San Jose, California.

4. Upon information and belief, Flex Logix is a Delaware corporation registered to do business in California, and with its principle place of business in Mountain View, California

## JURISDICTION AND VENUE

5. This Court has subject matter jurisdiction over patent infringement Claims II–VI pursuant to 28 U.S.C. §§ 1331 and 1338(a), and the Court has supplemental jurisdiction over state law Claim I pursuant to 28 U.S.C. § 1367.

6. This Court has personal jurisdiction over Flex Logix because (a) it has committed the acts of patent infringement complained of herein in this State and this District, and/or (b) it has directed its acts of infringement and other unlawful acts complained of herein at this State and this District.

7. This Court has personal jurisdiction over Flex Logix for the additional reason that it has engaged in systematic and continuous contacts with this State and this District by, *inter alia*, regularly conducting and soliciting business in this State and this District, and deriving

substantial revenue from products and/or services provided to persons in this State and this District.

8. Venue is proper in this District under 28 U.S.C. § 1391(b) because a substantial part of the acts complained of herein occurred in this District, Flex Logix transacts business in this District, Flex Logix resides in this District, and/or the property that is the subject of this action is situated in this District.

9. Venue is proper in this District under 28 U.S.C. §§ 1391(c)–(d) and 1400(b) because (i) Flex Logix resides in this District; and (ii) Flex Logix has committed acts of infringement and has a regular and established place of business in this District.

## INTRADISTRICT ASSIGNMENT

10. Pursuant to Local Rule 3-5(b), Konda Tech alleges that assignment to the San Jose Division is proper under Local Rule 3-2(e) because Plaintiff and Defendant have their principal places of business and/or reside in the San Jose Division, as alleged *supra* at paragraphs 3–4.

## FACTUAL BACKGROUND

11. Konda Tech was founded by Dr. Venkat Konda ("Dr. Konda") in 2007. Dr. Konda is a pioneer in field-programmable gate array ("FPGA") routing fabric and interconnection networks technology. Konda Tech is based on Dr. Konda's work, and provides chip and system level interconnect technology solutions. Konda Tech has licensed FPGA interconnect architecture patent rights to two FPGA chip vendors, the first of which has made and sold three generations of chips. Dr. Konda has a Ph.D. in Computer Science and Engineering from the University of Louisville, and has been granted eleven patents in the space.

12. In or around January 2009, Dr. Konda was introduced to Dr. Dejan Markovic ("Dr. Markovic") by Dr. Flavio Bonomi ("Dr. Bonomi"), a VP Head of Advanced Architecture and Research at Cisco Systems, Inc. ("Cisco"). Konda Tech was one of six startups that received an oral offer for funding from Cisco that was later rescinded. Dr. Markovic knew of Cisco's

rescinded offer, and that Konda Tech was still looking for funding, and Dr. Markovic claimed that Konda Tech could receive funding through UCLA's Institute of Technology Advancement ("ITA"). Dr. Markovic was a UCLA professor focused on circuits and embedded systems (which overlaps and compliments with Konda Tech intellectual property), and involved with the ITA. Dr. Markovic was not focused on FPGA work until he met Dr. Konda.

13. Dr. Markovic was interested in Konda Tech's intellectual property ("Konda Tech IP") and suggested that Dr. Konda present before the ITA. Dr. Konda did make such a presentation on October 12, 2009. The presentation was fruitless as the ITA does not provide funding to non-UCLA related entities—a fact that should have been known to Dr. Markovic.

14. Dr. Markovic, enamored with Konda Tech IP, also asked Dr. Konda to give a seminar on the technology to Dr. Markovic's students. Among those in attendance at the October 12, 2009 seminar was Dr. Cheng C. Wang ("Dr. Wang"), a graduate student at the time. Dr. Wang grew similarly interested in Konda Tech IP.

15. In June and July 2010, Dr. Markovic called Dr. Konda, and told him that he wanted to use Konda Tech IP in two different applications for DARPA funding. Dr. Konda advised that he did not then have the time to work with Dr. Markovic. However, both times, Dr. Markovic assured Dr. Konda that he would not have to spend any time on the application, and that he would incorporate the Konda Tech IP into the application from the then published Konda Tech WIPO patents. Dr. Markovic assured Dr. Konda that he would take a license from Konda Tech should the DARPA grant be approved.

16. Attached hereto as Exhibits 1 and 2 are the June 23, 2010 and August 6, 2010 DARPA funding proposals (the "DARPA Proposals") that followed those conversations.

17. Both of the DARPA Proposals make clear that Konda Tech IP was at the heart of what Drs. Markovic and Wang were hoping to accomplish:

> Konda Technologies inventions with regular VLSI layouts for Benes/BFT based hierarchical networks are seminal and subsumes all the other known network topologies such as Clos networks, hypercube networks, cube-connected cycles and pyramid networks, which makes these networks implementable in a FPGA devices

> with regular structures both interconnect distribution-wise and layout-wise which is the key to exploit improved area, power, and performance of FPGA devices. The regularity of Konda hierarchical layout is also the key for its commercializability in System-on-Chip interconnect devices, FPIC devices as well.

Indeed, the proposals state that they "will make use of hierarchically routed and proprietary Konda interconnect architecture." The first DARPA Proposal further estimates that Dr. Konda and Konda Tech would complete 620 task hours of the estimate 1020 task hours for key personnel.

18. Those DARPA Proposals, replete with references to Konda Tech IP, had been rejected. However, Dr. Markovic and Dr. Wang were not dissuaded from continuing to work with Konda Tech IP.

19. In 2010, Dr. Markovic told Dr. Konda over the phone that his students, including Dr. Wang, were implementing Konda Tech IP, specifically the 2D layout, on an FPGA chip. In June 2011, Drs. Markovic and Wang presented a paper at the 2011 VLSI Circuits Symposium titled "A 1.1 GOPS/mQ FPGA Chip with Hierarchical Interconnect Fabric"—based on Konda Tech IP.

20. Dr. Markovic invited Dr. Konda by email in the fall of 2013 to meet him at Stanford University while he was a Visiting Associate Professor. When they met, Dr. Konda inquired whether Dr. Markovic and his students had stopped implementing Konda Tech IP. Dr. Markovic replied yes. During the conversation Dr. Konda also shared the names of customers he was working with to license Konda Tech IP.

21. Between 2011 and 2014, Drs. Markovic and Konda had occasional phone calls, where they spoke about the progress of their respective work, but Dr. Markovic never disclosed that Konda Tech IP was the subject of Dr. Wang's June 2013 Ph.D. dissertation titled, "Building Efficient, Reconfigurable Hardware using Hierarchical Interconnects."

22. Dr. Konda met with Drs. Markovic and Wang at the home of Dr. Bonomi in January 2014. Dr. Bonomi had invited them to his home because he was in the process of forming his own startup, and needed to license Konda Tech IP. Dr. Bonomi was looking for implementation help from Drs. Markovic and Wang. Over the course of their discussions, Drs.

Markovic and Wang stated that they were looking for funding for their separate startup, but when queried, refused to disclose the technological focus of their startup. Cryptically, Dr. Markovic later stated that he *may* need to license Konda Tech IP for their separate startup as well.

23. A couple weeks later, Drs. Markovic and Wang published a paper titled "A Multi-Granularity FPGA with Hierarchical Interconnects for Efficient and Flexible Mobile Computing"—again, based on Konda Tech IP—at the 2014 International Solid State Circuits Conference (the "ISSCC paper"). Though publishing at secondary conferences and journals, Drs. Markovic and Wang never attended or published any papers at the International Symposium on FPGAs held annually in Monterey, California. This is the primary FPGA conference, and one they know Dr. Konda attends every year.

24. The ISSCC paper is attached hereto as Exhibit 3.

25. The ISSCC paper describes and demonstrates technologies that were invented by Dr. Konda, monetized by Konda Tech, and the subject of the patents-in-suit.

26. Drs. Markovic and Wang's conduct make clear that they employed subterfuge and deceit to gain access to Konda Tech IP, develop their fraudulent credibility in the technology through publications based on Konda Tech IP, and then used Konda Tech IP to launch their own company—Flex Logix.

27. Drs. Markovic and Wang ultimately co-founded Flex Logix in February 2014.

28. Dr. Konda only learned of Drs. Markovic and Wang's above-referenced publications, dissertation, and the formation of Flex Logix in December 2015, when advised of the same by Dr. Vaughn Betz, a University of Toronto professor, when he asked if Flex Logix was using Konda Tech IP.

29. Flex Logix touts the ISSCC paper on its website as describing Flex Logix's "new, patented interconnect, XFLX™." http://www.flex-logix.com/fpga-tutorial/.

**FIRST CAUSE OF ACTION**

**Unfair Business Practices**

30. Konda Tech incorporates by reference every allegation contained in each and every one of the above paragraphs, as though set forth fully herein.

31. Flex Logix's patent infringement, and other tortious behavior, as described above and below in the causes of action listed in this Complaint, all constitute unfair and unlawful business practices pursuant to California Business & Professions Code Section 17200 *et seq.*

32. The unlawful conduct described herein resulted in economic harm to Konda Tech.

33. As a direct and proximate result of their acts mentioned herein, Flex Logix has received and continues to receive ill-gotten gains belonging to Konda Tech.

34. Konda Tech is entitled to restitution for its losses in an amount to be determined.

35. Because the conduct alleged herein is ongoing, and there is no indication that Flex Logix will cease its unlawful conduct described herein, Konda Tech requests that this Court enjoin Flex Logix from further violations of California's laws.

**SECOND CAUSE OF ACTION**

**Infringement of Patent No. 8,269,523**

36. Konda Tech incorporates by reference every allegation contained in each and every one of the above paragraphs, as though set forth fully herein.

37. The '523 patent, entitled "VLSI Layouts of Fully Connected Generalized Networks," was duly and lawfully issued on September 18, 2012. A true and correct copy of the '523 patent is attached to this Complaint as Exhibit 4.

38. Konda Tech is the owner of all rights, title, and interest in the '523 patent, including the right to bring this suit for injunctive relief and damages.

39. Konda Tech has the exclusive right to make, use, sell, and offer to sell any product embodying the '523 patent throughout the United States, and to import any product embodying the '523 patent into the United States.

40. Konda Tech has commercially exploited the ’523 patent by licensing the underlying technology to companies who, like Flex Logix, wish to make use of Dr. Konda’s inventions disclosed in the ’523 patent.

41. The ’523 patent is valid and enforceable.

42. Upon information and belief, Flex Logix has had knowledge of Konda, the Konda Tech IP, the ’523 patent, and Konda Tech’s commercial exploitation of the ’523 patent at least as early as the issuance of the ’523 patent.

43. Flex Logix has been aware of the ’523 patent since at least as early as the filing of this Complaint.

44. Flex Logix has infringed, and continues to infringe, literally and/or through the doctrine of equivalents, one or more claims of the ’523 patent, including but not limited to claim 1, pursuant to 35 U.S.C. § 271(a), by making, using, selling, offering to sell, and/or importing within the United States, without authority, certain FPGA devices (“Accused FPGA Devices”).

45. On information and belief, the Accused FPGA Devices, such as an integrated circuit device comprising a plurality of sub-integrated circuit blocks and a routing network. Flex Logix infringed and continues to infringe at least claim 1 of the ’523 patent for at least the following reasons:

46. Flex Logix’s Accused FPGA Devices are integrated circuit devices.

47. On information and belief, Flex Logix’s Accused FPGA Devices have a plurality of sub-integrated circuit blocks and a routing network, and said each plurality of sub-integrated circuit blocks comprising a plurality of inlet links and a plurality of outlet links.

48. On information and belief, Flex Logix’s Accused FPGA Devices with said routing network comprising of a plurality of stages y, in each said sub-integrated circuit block, starting from the lowest stage of 1 to the highest stage of y, where y.gtoreq.1.

49. On information and belief, Flex Logix's Accused FPGA Devices with said routing network comprising a plurality of switches of size d.times.d, where d.gtoreq.2, in each said stage and each said switch of size d.times.d having d inlet links and d outlet links.

50. On information and belief, Flex Logix's Accused FPGA Devices with said plurality of outlet links of said each sub-integrated circuit block are directly connected to said inlet links of said switches of its corresponding said lowest stage of 1, and said plurality of inlet links of said each sub-integrated circuit block are directly connected from said outlet links of said switches of its corresponding said lowest stage of 1.

51. On information and belief, Flex Logix's Accused FPGA Devices with said each sub- integrated circuit block comprising a plurality of forward connecting links connecting from switches in a lower stage to switches in its immediate succeeding higher stage, and also comprising a plurality of backward connecting links connecting from switches in a higher stage to switches in its immediate preceding lower stage.

52. On information and belief, Flex Logix's Accused FPGA Devices with said each sub- integrated circuit block comprising a plurality straight links in said forward connecting links from switches in said each lower stage to switches in its immediate succeeding higher stage and a plurality cross links in said forward connecting links from switches in said each lower stage to switches in its immediate succeeding higher stage, and further comprising a plurality of straight links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage and a plurality of cross links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage.

53. On information and belief, Flex Logix's Accused FPGA Devices with said plurality of sub-integrated circuit blocks arranged in a two-dimensional grid of rows and columns.

54. On information and belief, Flex Logix's Accused FPGA Devices with said all straight links are connecting from switches in each said sub-integrated circuit block are

connecting to switches in the same said sub-integrated circuit block; and said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks which are either placed vertically above or below, or placed horizontally to the left or to the right.

55. On information and belief, Flex Logix's Accused FPGA Devices with each said plurality of sub-integrated circuit blocks comprising same number of said stages and said switches in each said stage, regardless of the size of said two-dimensional grid so that each said plurality of sub- integrated circuit block with its corresponding said stages and said switches in each stage is replicable in both vertical direction or horizontal direction of said two-dimensional grid.

56. To the extent Flex Logix's Accused FPGA Devices, without more, do not directly infringe at least claim 1 of the '523 patent, Flex Logix contributes to infringement of the same under 35 U.S.C. § 271(c) inasmuch as the Infringing Products offered for sale and sold by Flex Logix are each a component of a patented machine or an apparatus used in practicing a patented process, constituting a material part of Konda's invention, knowing the same to be especially made or especially adapted for use in infringement of the '523 patent.

57. Flex Logix actively encourages its customers to use the Accused FPGA Devices in an infringing manner. For example, Flex Logix's website is replete with written directions instructing users on how to use the Accused FPGA Devices in an infringing manner. Flex Logix's website also touts the identities of customers who use the Accused FPGA Devices, including without limitation The Boeing Company, each of whom is a direct infringing inasmuch as they use the Accused FPGA Devices in the infringing manner as instructed by Flex Logix.

58. Upon information and belief, and particularly by way of the detailed documentation instructing users on how to use the Accused FPGA Devices in an infringing manner, Flex Logix has encouraged this infringement with knowledge of the '523 patent and with a specific intent to cause their users to infringe.

59. Flex Logix's acts thus constitute active inducement of patent infringement in violation of 35 U.S.C. § 271(b).

60. Flex Logix will, on information and belief, continue to infringe, induce infringement of, and contribute to the infringement of, the '523 patent unless enjoined.

61. Flex Logix's infringement has irreparably harmed Konda Tech.

62. Flex Logix will, on information and belief, continue to irreparably harm Konda Tech unless enjoined.

63. Pursuant to 35 U.S.C. § 284, Konda Tech is entitled to damages adequate to compensate for the infringement buy in no event less than a reasonable royalty.

64. Flex Logix's infringement of the '523 patent has been willful and deliberate and, pursuant to 35 U.S.C. § 284, Konda Tech is entitled to treble damages.

65. This case is "exceptional" within the meaning of 35 U.S.C. § 285, and Konda Tech is entitled to an award of attorneys' fees.

**THIRD CAUSE OF ACTION**

**Infringement of Patent No. 8,898,611**

66. Konda Tech incorporates by reference every allegation contained in each and every one of the above paragraphs, as though set forth fully herein.

67. The '611 patent, entitled "VLSI Layouts of Fully Connected Generalized and Pyramid Networks with Locality Exploitation," was duly and lawfully issued on November 25, 2014. A true and correct copy of the '611 patent is attached to this Complaint as Exhibit 5.

68. Konda Tech is the owner of all rights, title, and interest in the '611 patent, including the right to bring this suit for injunctive relief and damages.

69. Konda Tech has the exclusive right to make, use, sell, and offer to sell any product embodying the '611 patent throughout the United States, and to import any product embodying the '611 patent into the United States.

70. Konda Tech has commercially exploited the '611 patent by licensing the underlying technology to companies who, like Flex Logix, wish to make use of Dr. Konda's inventions disclosed in the '611 patent.

71. The '611 patent is valid and enforceable.

72. Upon information and belief, Flex Logix has had knowledge of Konda, the Konda Tech IP, the '611 patent, and Konda Tech's commercial exploitation of the '611 patent at least as early as the issuance of the '611 patent.

73. Flex Logix has been aware of the '611 patent since at least as early as the filing of this Complaint.

74. Flex Logix has infringed, and continue to infringe, literally and/or through the doctrine of equivalents, one or more claims of the '611 patent, including but not limited to claim 1, pursuant to 35 U.S.C. § 271(a), by making, using, selling, offering to sell, and/or importing within the United States, without authority, the Accused FPGA devices.

75. On information and belief, Flex Logix's Accused FPGA Devices have an electrical network on an electrical substrate. Flex Logix infringes at least claim 1 of the '611 patent for at least the following reasons:

76. On information and belief, Flex Logix's Accused FPGA Devices have an electrical network on an electrical substrate comprising a plurality of sub-networks corresponding to blocks arranged in a two dimensional layout for a total of $a \times b$ said sub-networks with one side of said layout having the size of $a$ sub-networks and the other side of said layout having the size of $b$ sub-networks where $a \geq 1$ and $b \geq 1$.

77. On information and belief, Flex Logix's Accused FPGA Devices have said electrical network on an electrical substrate comprising at most $N_1$ inlet links and at most $N_2$ outlet links where $N_1 > 1$ and $N_2 > 1$ wherein either $N_2 = N_1 \times p_2$, $N_1 = (a \times b) \times p$, and said each sub-network comprising at most $p$ inlet links and at most $p \times p_2$ outlet links; or

$N_1 = N_2 \times p_1$, $N_2 = (a \times b) \times p$, and said each sub-network comprising at most $p$ outlet links and at most $p \times p_1$ inlet links.

78. On information and belief, Flex Logix's Accused FPGA Devices have said each sub-network comprising at most $y$ stages, starting from the lowest stage of 1 to the highest stage of $y$, where $y \geq 1$.

79. On information and belief, Flex Logix's Accused FPGA Devices have said each stage comprising at least one switch of size $d \times d$, where $d \geq 2$ and each said switch of size $d \times d$ having $d$ incoming links and $d$ outgoing links.

80. On information and belief, Flex Logix's Accused FPGA Devices have said each sub-network may not be comprising the same number of said inlet links and may not be comprising the same number of said outlet links; said each sub-network may not be comprising the same number of said stages; said each stage may not be comprising the same number of switches; and said each switch in said each stage may not be of the same size $d$.

81. On information and belief, Flex Logix's Accused FPGA Devices have said incoming links and said outgoing links in each said switch in said each stage of said each sub-network comprising a plurality of forward connecting links connecting from switches in lower stage to said switches one of succeeding higher stages, and also comprising a plurality of backward connecting links connecting from said switches in higher stage to said switches one of preceding lower stage.

82. On information and belief, Flex Logix's Accused FPGA Devices have said forward connecting links comprising a plurality of straight links connecting from a said switch in a said stage in a said sub-network to a said switch in another stage in the same said sub-network and also comprising a plurality of cross links connecting from a said switch in a said stage in a sub-network to a said switch in another said stage in a different said sub-network.

83. On information and belief, Flex Logix's Accused FPGA Devices have said backward connecting links comprising a plurality of straight links connecting from a said switch

in a said stage in a said sub-network to a said switch in another said stage in the same said sub-network and also comprising a plurality of cross links connecting from a said switch in a said stage in a said sub-network to a said switch in another said stage in a different said sub-network.

84. On information and belief, Flex Logix's Accused FPGA Devices have said all cross links are connecting as either vertical or horizontal links between said switches between each two different said sub-networks, which are either placed vertically above or below, or placed horizontally to the left or to the right.

85. To the extent Flex Logix's Accused FPGA Devices, without more, do not directly infringe at least claim 1 of the '611 patent, Flex Logix contributes to infringement of the same under 35 U.S.C. § 271(c) inasmuch as the Infringing Products offered for sale and sold by Flex Logix are each a component of a patented machine or an apparatus used in practicing a patented process, constituting a material part of Konda's invention, knowing the same to be especially made or especially adapted for use in infringement of the '611 patent.

86. Flex Logix actively encourages its customers to use the Accused FPGA Devices in an infringing manner. For example, Flex Logix's website is replete with written directions instructing users on how to use the Accused FPGA Devices in an infringing manner. Flex Logix's website also touts the identities of customers who use the Accused FPGA Devices, including without limitation The Boeing Company, each of whom is a direct infringing inasmuch as they use the Accused FPGA Devices in the infringing manner as instructed by Flex Logix.

87. Upon information and belief, and particularly by way of the detailed documentation instructing users on how to use the Accused FPGA Devices in an infringing manner, Flex Logix has encouraged this infringement with knowledge of the '611 patent and with a specific intent to cause their users to infringe.

88. Flex Logix's acts thus constitute active inducement of patent infringement in violation of 35 U.S.C. § 271(b).

89. Flex Logix will, on information and belief, continue to infringe, induce infringement of, and contribute to the infringement of, the '611 patent unless enjoined.

90. Flex Logix's infringement has irreparably harmed Konda Tech.

91. Flex Logix will, on information and belief, continue to irreparably harm Konda Tech unless enjoined.

92. Pursuant to 35 U.S.C. § 284, Konda Tech is entitled to damages adequate to compensate for the infringement buy in no event less than a reasonable royalty.

93. Flex Logix's infringement of the '611 patent has been willful and deliberate and, pursuant to 35 U.S.C. § 284, Konda Tech is entitled to treble damages.

94. This case is "exceptional" within the meaning of 35 U.S.C. § 285, and Konda Tech is entitled to an award of attorneys' fees.

**FOURTH CAUSE OF ACTION**

**Infringement of Patent No. 9,529,958**

95. Konda Tech incorporates by reference every allegation contained in each and every one of the above paragraphs, as though set forth fully herein.

96. Konda Tech incorporates all of the above paragraphs as though fully set forth herein.

97. The '958 patent, entitled "VLSI Layouts of Fully Connected Generalized and Pyramid Networks with Locality Exploitation," was duly and lawfully issued on December 27, 2016. A true and correct copy of the '958 patent is attached to this Complaint as Exhibit 6.

98. Konda Tech is the owner of all rights, title, and interest in the '958 patent, including the right to bring this suit for injunctive relief and damages.

99. Konda Tech has the exclusive right to make, use, sell, and offer to sell any product embodying the '958 patent throughout the United States, and to import any product embodying the '958 patent into the United States.

100. Konda Tech has commercially exploited the '958 patent by licensing the underlying technology to companies who, like Flex Logix, wish to make use of Dr. Konda's inventions disclosed in the '958 patent.

101. The '958 patent is valid and enforceable.

102. Upon information and belief, Flex Logix has had knowledge of Konda, the Konda Tech IP, the '958 patent, and Konda Tech's commercial exploitation of the '958 patent at least as early as the issuance of the '958 patent.

103. Flex Logix has been aware of the '958 patent since at least as early as the filing of this Complaint.

104. Flex Logix has infringed, and continue to infringe, literally and/or through the doctrine of equivalents, one or more claims of the '958 patent, including but not limited to claim 1, pursuant to 35 U.S.C. § 271(a), by making, using, selling, offering to sell, and/or importing within the United States, without authority, the Accused FPGA devices.

105. On information and belief, Flex Logix's Accused FPGA Devices, have a two-dimensional layout of hierarchical routing network implemented in a non-transitory medium. Flex Logix infringe at least claim 1 of the '958 patent for at least the following reasons:

106. On information and belief, Flex Logix's Accused FPGA Devices have a total of $a \times b$ blocks with one side of said layout having the size of "$a$" blocks and the other side of said layout having the size of "$b$" blocks where $a \geq 1$ and $b \geq 1$.

107. On information and belief, Flex Logix's Accused FPGA Devices have said routing network comprising a total of $N_1$ inlet links and a total of $N_2$ outlet links and $y$ hierarchical stages where $y \geq 1$, $N_1 > 1$ and $N_2 > 1$ wherein either $N_2 = N_1 \times p_2$, $N_1 = (a \times b) \times p$, and said each block comprising at most $p$ inlet links and at most $p \times p_2$ outlet links; or $N_1 = N_2 \times p_1$, $N_2 = (a \times b) \times p$, and said each block comprising at most $p$ outlet links and at most $p \times p_1$ inlet links, where $p \geq 1$, $p_1 \geq 1$ and $p_2 \geq 1$.

108. On information and belief, Flex Logix's Accused FPGA Devices have said each stage comprising at least one switch of size $d \times d$, where $d \geq 2$ and each said switch of size $d \times d$ having $d$ incoming links and $d$ outgoing links.

109. On information and belief, Flex Logix's Accused FPGA Devices have said each block may not be comprising the same number of said inlet links and may not be comprising the same number of said out links; said each block may not be comprising the same number of said stages; said each stage may not be comprising the same number of switches; and said each switch in said each stage may not be of the same size $d$, Said inlet links directly connected to one or more said incoming links, and said outgoing links directly connected to one or more said outlet links.

110. On information and belief, Flex Logix's Accused FPGA Devices have said incoming links and outgoing links in each switch in said each stage of said each block comprising a plurality of forward connecting links connected from switches in lower stage to switches in the immediate succeeding higher stage, and also comprising a plurality of backward connecting links connected from switches in higher stage to switches in the immediate preceding lower stage.

111. On information and belief, Flex Logix's Accused FPGA Devices have said forward connecting links comprising a plurality of straight links connected from a switch in a stage in a block to a switch in another stage in the same block and also comprising a plurality of cross links connected from a switch in a stage in a block to a switch in another stage in a different block.

112. On information and belief, Flex Logix's Accused FPGA Devices have said backward connecting links comprising a plurality of straight links connected from a switch in a stage in a block to a switch in another stage in the same block and also comprising a plurality of cross links connected from a switch in a stage in a block to a switch in another stage in a different block.

113. On information and belief, Flex Logix's Accused FPGA Devices have said all cross links are connected as either vertical or horizontal links between switches in two different said blocks.

114. To the extent Flex Logix's Accused FPGA Devices, without more, do not directly infringe at least claim 1 of the '958 patent, Flex Logix contributes to infringement of the same under 35 U.S.C. § 271(c) inasmuch as the Infringing Products offered for sale and sold by Flex Logix are each a component of a patented machine or an apparatus used in practicing a patented process, constituting a material part of Konda's invention, knowing the same to be especially made or especially adapted for use in infringement of the '958 patent.

115. Flex Logix actively encourages its customers to use the Accused FPGA Devices in an infringing manner. For example, Flex Logix's website is replete with written directions instructing users on how to use the Accused FPGA Devices in an infringing manner. Flex Logix's website also touts the identities of customers who use the Accused FPGA Devices, including without limitation The Boeing Company, each of whom is a direct infringing inasmuch as they use the Accused FPGA Devices in the infringing manner as instructed by Flex Logix.

116. Upon information and belief, and particularly by way of the detailed documentation instructing users on how to use the Accused FPGA Devices in an infringing manner, Flex Logix has encouraged this infringement with knowledge of the '958 patent and with a specific intent to cause their users to infringe.

117. Flex Logix's acts thus constitute active inducement of patent infringement in violation of 35 U.S.C. § 271(b).

118. Flex Logix will, on information and belief, continue to infringe, induce infringement of, and contribute to the infringement of, the '958 patent unless enjoined.

119. Flex Logix's infringement has irreparably harmed Konda Tech.

120. Flex Logix will, on information and belief, continue to irreparably harm Konda Tech unless enjoined.

121. Pursuant to 35 U.S.C. § 284, Konda Tech is entitled to damages adequate to compensate for the infringement buy in no event less than a reasonable royalty.

122. Flex Logix's infringement of the '958 patent has been willful and deliberate and, pursuant to 35 U.S.C. § 284, Konda Tech is entitled to treble damages.

123. This case is "exceptional" within the meaning of 35 U.S.C. § 285, and Konda Tech is entitled to an award of attorneys' fees.

**FIFTH CAUSE OF ACTION**

**Infringement of Patent No. 10,003,553**

124. Konda Tech incorporates by reference every allegation contained in each and every one of the above paragraphs, as though set forth fully herein.

125. The '553 patent, entitled "Optimization of Multi-stage Hierarchical Networks for Practical Routing Applications," was duly and lawfully issued on June 19, 2018. A true and correct copy of the '553 patent is attached to this Complaint as Exhibit 7.

126. Konda Technologies is the owner of all rights, title, and interest in the '553 patent, including the right to bring this suit for injunctive relief and damages.

127. Konda Tech has the exclusive right to make, use, sell, and offer to sell any product embodying the '553 patent throughout the United States, and to import any product embodying the '553 patent into the United States.

128. Konda Tech has commercially exploited the '553 patent by licensing the underlying technology to companies who, like Flex Logix, wish to make use of Dr. Konda's inventions disclosed in the '553 patent.

129. The '553 patent is valid and enforceable.

130. Upon information and belief, Flex Logix has had knowledge of Konda, the Konda Tech IP, the '553 patent, and Konda Tech's commercial exploitation of the '553 patent at least as early as the issuance of the '553 patent.

131. Flex Logix has been aware of the ’553 patent since at least as early as the filing of this Complaint.

132. Flex Logix has infringed, and continues to infringe, literally and/or through the doctrine of equivalents, one or more claims of the ’553 patent, including but not limited to claim 1, pursuant to 35 U.S.C. § 271(a), by making, using, selling, offering to sell, and/or importing within the United States, without authority, the Accused FPGA Devices.

133. On information and belief, Flex Logix’s Accused FPGA Devices have a network implemented in a non-transitory medium comprising a plurality of subnetworks and a plurality of inlet links and a plurality of outlet links. Flex Logix infringe at least claim 1 of the ’553 patent for at least the following reasons:

134. On information and belief, Flex Logix’s Accused FPGA Devices have a network implemented in a non-transitory medium comprising a plurality of subnetworks and a plurality of inlet links and a plurality of outlet links, said plurality of subnetworks arranged in a two-dimensional grid of rows and columns.

135. On information and belief, Flex Logix’s Accused FPGA Devices have each subnetwork comprising y stages, where y.gtoreq.1; and each stage comprising a switch of size d.sub.i.times.d.sub.0, where d.sub.i.gtoreq.2 and d.sub.0.gtoreq.2 and each switch of size d.sub.i.times.d.sub.0 having d.sub.i incoming links and d.sub.0 outgoing links.

136. On information and belief, Flex Logix’s Accused FPGA Devices have said inlet links are connected to one or more of said incoming links of a said switch of a said stage of a said subnetwork, and said outlet links are connected to one of said outgoing links of a said switch of a said stage of a said subnetwork.

137. On information and belief, Flex Logix’s Accused FPGA Devices have each subnetwork of the plurality of subnetworks may or may not be comprising the same number of said inlet links and may or may not be comprising the same number of said outlet links; each subnetwork of the plurality of subnetworks may or may not be comprising the same number of

said stages; each stage may or may not be comprising the same number of switches; and each switch in each stage may or may not be of the same size, each multiplexer in each stage may or may not be of the same size and Said incoming links and outgoing links in each switch in each stage of each subnetwork comprising a plurality of forward connecting links connected from switches in a stage to switches in another stage in same said subnetwork or another said subnetwork, and also comprising a plurality of backward connecting links connected from switches in a stage to switches in another stage in same subnetwork or another said subnetwork.

138. On information and belief, Flex Logix's Accused FPGA Devices have said forward connecting links comprising zero or more straight links connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in one or more other subnetworks.

139. On information and belief, Flex Logix's Accused FPGA Devices have said backward connecting links comprising zero or more straight links connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork; and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in one or more other subnetworks.

140. To the extent Flex Logix's Accused FPGA Devices, without more, do not directly infringe at least claim 1 of the '553 patent, Flex Logix contributes to infringement of the same under 35 U.S.C. § 271(c) inasmuch as the Infringing Products offered for sale and sold by Flex Logix are each a component of a patented machine or an apparatus used in practicing a patented process, constituting a material part of Konda's invention, knowing the same to be especially made or especially adapted for use in infringement of the '553 patent.

141. Flex Logix actively encourages its customers to use the Accused FPGA Devices in an infringing manner. For example, Flex Logix's website is replete with written directions instructing users on how to use the Accused FPGA Devices in an infringing manner. Flex

Logix's website also touts the identities of customers who use the Accused FPGA Devices, including without limitation The Boeing Company, each of whom is a direct infringing inasmuch as they use the Accused FPGA Devices in the infringing manner as instructed by Flex Logix.

142. Upon information and belief, and particularly by way of the detailed documentation instructing users on how to use the Accused FPGA Devices in an infringing manner, Flex Logix has encouraged this infringement with knowledge of the '553 patent and with a specific intent to cause their users to infringe.

143. Flex Logix's acts thus constitute active inducement of patent infringement in violation of 35 U.S.C. § 271(b).

144. Flex Logix will, on information and belief, continue to infringe, induce infringement of, and contribute to the infringement of, the '553 patent unless enjoined.

145. Flex Logix's infringement has irreparably harmed Konda Tech.

146. Flex Logix will, on information and belief, continue to irreparably harm Konda Tech unless enjoined.

147. Pursuant to 35 U.S.C. § 284, Konda Tech is entitled to damages adequate to compensate for the infringement buy in no event less than a reasonable royalty.

148. Flex Logix's infringement of the '553 patent has been willful and deliberate and, pursuant to 35 U.S.C. § 284, Konda Tech is entitled to treble damages.

149. This case is "exceptional" within the meaning of 35 U.S.C. § 285, and Konda Tech is entitled to an award of attorneys' fees.

**SIXTH CAUSE OF ACTION**

**Infringement of Patent No. 10,050,904**

150. Konda Tech incorporates by reference every allegation contained in each and every one of the above paragraphs, as though set forth fully herein.

151. The ’904 patent, entitled “VLSI Layouts of Fully Connected Generalized and Pyramid Networks with Locality Exploitation,” was duly and lawfully issued on August 14, 2018. A true and correct copy of the ’904 patent is attached to this Complaint as Exhibit 8.

152. Konda Technologies is the owner of all rights, title, and interest in the ’904 patent, including the right to bring this suit for injunctive relief and damages.

153. Konda Tech has the exclusive right to make, use, sell, and offer to sell any product embodying the ’904 patent throughout the United States, and to import any product embodying the ’904 patent into the United States.

154. Konda Tech has commercially exploited the ’904 patent by licensing the underlying technology to companies who, like Flex Logix, wish to make use of Dr. Konda’s inventions disclosed in the ’904 patent.

155. The ’904 patent is valid and enforceable.

156. Upon information and belief, Flex Logix has had knowledge of Konda, the Konda Tech IP, the ’904 patent, and Konda Tech’s commercial exploitation of the ’904 patent at least as early as the issuance of the ’904 patent.

157. Flex Logix has been aware of the ’904 patent since at least as early as the filing of this Complaint.

158. Flex Logix have infringed, and continue to infringe, literally and/or through the doctrine of equivalents, one or more claims of the ’904 patent, including but not limited to claim 1, pursuant to 35 U.S.C. § 271(a), by making, using, selling, offering to sell, and/or importing within the United States, without authority, the Accused FPGA devices.

159. On information and belief, Flex Logix’s Accused FPGA Devices have a programmable integrated circuit device comprising a plurality of programmable logic blocks and a network, and said plurality of programmable logic blocks comprising a plurality of inlet links and a plurality of outlet links; and said network further comprising a plurality of subnetworks and with each subnetwork coupled with at least one of said plurality of

programmable logic blocks; and, said plurality of subnetworks coupled with said plurality of programmable logic blocks arranged in a two-dimensional grid of rows and columns. Flex Logix infringe at least claim 1 of the '904 patent for at least the following reasons:

160. On information and belief, Flex Logix's Accused FPGA Devices have each subnetwork comprising *y* stages, where $y > 1$: and each stage comprising a switch of size $d_i \times d_0$, where $d_i \geq 2$ and $d_o \geq 2$ and each switch of size $d_i \times d_0$ having $d_i$ incoming links and $d_0$ outgoing links.

161. On information and belief, Flex Logix's Accused FPGA Devices have said inlet links are connected to one or more of said incoming links of a said switch of a said stage of a said subnetwork, and said outlet links are connected to one of said outgoing links of a said switch of a said stage of a said subnetwork.

162. On information and belief, Flex Logix's Accused FPGA Devices have each subnetwork of the plurality of subnetworks comprising the same or different number of said inlet links and comprising the same or different number of said outlet links; each subnetwork of the plurality of subnetworks comprising the same or different number of said stages; each stage comprising the same or different number of switches; and each switch in each stage is of the same size or of different size, each multiplexer in each stage is of the same size or of different size.

163. On information and belief, Flex Logix's Accused FPGA Devices have said incoming links and outgoing links in each switch in each stage of each subnetwork comprising a plurality of forward connecting links connected from switches in a stage to switches in another stage in same said subnetwork or another said subnetwork, and also comprising a plurality of backward connecting links connected from switches in a stage to switches in another stage in same subnetwork or another said subnetwork.

164. On information and belief, Flex Logix's Accused FPGA Devices have said forward connecting links comprising zero or more straight links connected from a switch in a

stage in a subnetwork to a switch in another stage in the same subnetwork and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage or same level stage in another subnetwork.

165. On information and belief, Flex Logix's Accused FPGA Devices have said backward connecting links comprising zero or more straight links connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork; and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage or same level stage in another subnetwork.

166. To the extent Flex Logix's Accused FPGA Devices, without more, do not directly infringe at least claim 1 of the '904 patent, Flex Logix contributes to infringement of the same under 35 U.S.C. § 271(c) inasmuch as the Infringing Products offered for sale and sold by Flex Logix are each a component of a patented machine or an apparatus used in practicing a patented process, constituting a material part of Konda's invention, knowing the same to be especially made or especially adapted for use in infringement of the '904 patent.

167. Flex Logix actively encourages its customers to use the Accused FPGA Devices in an infringing manner. For example, Flex Logix's website is replete with written directions instructing users on how to use the Accused FPGA Devices in an infringing manner. Flex Logix's website also touts the identities of customers who use the Accused FPGA Devices, including without limitation The Boeing Company, each of whom is a direct infringing inasmuch as they use the Accused FPGA Devices in the infringing manner as instructed by Flex Logix.

168. Upon information and belief, and particularly by way of the detailed documentation instructing users on how to use the Accused FPGA Devices in an infringing manner, Flex Logix has encouraged this infringement with knowledge of the '904 patent and with a specific intent to cause their users to infringe.

169. Flex Logix's acts thus constitute active inducement of patent infringement in violation of 35 U.S.C. § 271(b).

170. Flex Logix will, on information and belief, continue to infringe, induce infringement of, and contribute to the infringement of, the '904 patent unless enjoined.

171. Flex Logix's infringement has irreparably harmed Konda Tech.

172. Flex Logix will, on information and belief, continue to irreparably harm Konda Tech unless enjoined.

173. Pursuant to 35 U.S.C. § 284, Konda Tech is entitled to damages adequate to compensate for the infringement buy in no event less than a reasonable royalty.

174. Flex Logix's infringement of the '904 patent has been willful and deliberate and, pursuant to 35 U.S.C. § 284, Konda Tech is entitled to treble damages.

175. This case is "exceptional" within the meaning of 35 U.S.C. § 285, and Konda Tech is entitled to an award of attorneys' fees.

## DEMAND FOR JURY TRIAL

Konda Tech hereby demands a trial by jury of all issues so triable under Federal Rule of Civil Procedure 38(b).

## PRAYER FOR RELIEF

WHEREFORE, Konda Tech respectfully requests that this Court:

A. Enter judgment for Konda Tech and against Flex Logix on each of the above claims;

B. Find that United States Patent No. 8,269,523 is valid and enforceable against Flex Logix;

C. Find that Flex Logix has infringed and is infringing United States Patent No. 8,269,523;

D. Permanently enjoin Flex Logix, its officers, agents, servants, employees, and those persons acting in active concert or in participation therewith from infringing United States Patent No. 8,269,523;

E. Award Konda Tech damages sufficient to compensate it for Flex Logix's past and future infringement of United States Patent No. 8,269,523, together with costs and prejudgment interest, pursuant to 35 U.S.C. § 284;

F. Find that United States Patent No. 8,898,611 is valid and enforceable against Flex Logix;

G. Find that Flex Logix has infringed and is infringing United States Patent No. 8,898,611;

H. Permanently enjoin Flex Logix, its officers, agents, servants, employees, and those persons acting in active concert or in participation therewith from infringing United States Patent No. 8,898,611;

I. Award Konda Tech damages sufficient to compensate it for Flex Logix's past and future infringement of United States Patent No. 8,898,611, together with costs and prejudgment interest, pursuant to 35 U.S.C. § 284;

J. Find that United States Patent No. 9,529,958 is valid and enforceable against Flex Logix;

K. Find that Flex Logix has infringed and is infringing United States Patent No. 9,529,958;

L. Permanently enjoin Flex Logix, its officers, agents, servants, employees, and those persons acting in active concert or in participation therewith from infringing United States Patent No. 9,529,958;

M. Award Konda Tech damages sufficient to compensate it for Flex Logix's past and future infringement of United States Patent No. 9,529,958, together with costs and prejudgment interest, pursuant to 35 U.S.C. § 284;

N. Find that United States Patent No. 10,003,553 is valid and enforceable against Flex Logix;

O. Find that Flex Logix has infringed and is infringing United States Patent No. 10,003,553;

P. Permanently enjoin Flex Logix, its officers, agents, servants, employees, and those persons acting in active concert or in participation therewith from infringing United States Patent No. 10,003,553;

Q. Award Konda Tech damages sufficient to compensate it for Flex Logix's past and future infringement of United States Patent No. 10,003,553, together with costs and prejudgment interest, pursuant to 35 U.S.C. § 284;

R. Find that United States Patent No. 10,050,904 is valid and enforceable against Flex Logix;

S. Find that Flex Logix has infringed and is infringing United States Patent No. 10,050,904;

T. Permanently enjoin Flex Logix, its officers, agents, servants, employees, and those persons acting in active concert or in participation therewith from infringing United States Patent No. 10,050,904;

U. Award Konda Tech damages sufficient to compensate it for Flex Logix's past and future infringement of United States Patent No. 10,050,904, together with costs and prejudgment interest, pursuant to 35 U.S.C. § 284;

V. Order an accounting of damages from Flex Logix's infringement;

W. Award Konda Tech enhanced damages, up to and including trebling Konda Tech's damages, pursuant to 35 U.S.C. § 284, for Flex Logix's willful infringement of the patents-in-suit;

X. Award Konda Tech its reasonable attorneys' fees and costs of suit pursuant to 35 U.S.C. § 285 due to the exceptional nature of this case, or as otherwise permitted by law;

Y. Award Konda Tech for all damages legally and/or proximately caused to Konda Tech by Flex Logix as set forth above, including costs and prejudgment interest; and

Z. Award Konda Tech such other or additional relief as the Court deems just and proper.

Date: December 17, 2018

Respectfully submitted,

DHILLON LAW GROUP INC.

By: */s/ Nitoj P. Singh*

Nitoj P. Singh
*Attorneys for Konda Technologies, Inc.*

# EXHIBIT 44

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Attorneys for Defendant
FLEX LOGIX TECHNOLOGIES, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

KONDA TECHNOLOGIES, INC., a California corporation,

Plaintiff,

vs.

FLEX LOGIX TECHNOLOGIES, INC,.

Defendant.

Case No. 5:18-cv-07581-LHK

**NOTICE OF MOTION AND MOTION TO DISMISS COMPLAINT PURSUANT TO FED. R. CIV. P. 12(b)(6) AND TO STRIKE PORTIONS OF COMPLAINT PURSUANT TO FED. R. CIV. P. 12(f); MEMORANDUM OF POINTS AND AUTHORITIES IN SUPPORT THEREOF**

Date: May 9, 2019
Time: 1:30 p.m.
Judge: Lucy H. Koh
Ctrm.: 8, 4th Floor

**NOTICE OF MOTION AND MOTION TO DISMISS AND TO STRIKE**

To Plaintiff Konda Technologies, Inc., and its counsel of record:

PLEASE TAKE NOTICE that on May 9, 2019, at 1:30 p.m., or as soon thereafter as the matter may be heard, in Courtroom No. 8 of the above-captioned Court, located at 4th Floor, 280 South 1st Street, San Jose, CA 95113, Defendant Flex Logix Technologies, Inc. ("Flex Logix") hereby does move the Court for an Order dismissing with prejudice in its entirety Konda Technologies, Inc.'s ("Konda Tech") complaint in this action pursuant to Federal Rule of Civil Procedure 12(b)(6) and/or for an Order striking or dismissing certain portions of Konda's Complaint under Federal Rule of Civil Procedure 12(f) and/or 12(b)(6).

Specifically, Flex Logix moves for an Order dismissing with prejudice:

[1] Konda Tech's Third, Fourth, and Sixth Causes of Action because those Causes of Action fail to state a claim for patent infringement due to the invalidity of each of the patents under 35 U.S.C. § 102.

[2] Konda Tech's Second, Third, Fourth, Fifth, and Sixth Causes of Action because those Causes of Action do not plead facts sufficient to state a plausible claim for patent infringement.

[3] Konda Tech's First Cause of Action for Unfair Business Practices pursuant to California Business & Professions Code Section 17200 et seq. as preempted by federal patent law and as barred by the statute of limitations.

In the event that Konda Tech's complaint is not dismissed in its entirety, Flex Logix also moves for an Order striking and/or dismissing Konda Tech's complaint's references to "fraud" due to the fact that the complaint's references to fraud are immaterial and impertinent with respect to the claims pled and scandalous and in view of the complaint's failure to plead any alleged fraud with particularity.

This motion is based upon this Notice of Motion and Motion; the attached Memorandum of Points and Authorities[1]; all other materials supporting this Motion or the Reply brief filed in support thereof; all pleadings on file in this matter; and any other materials or arguments the Court may receive at or before the hearing on this Motion.

DATED: January 24, 2019

MUNGER, TOLLES & OLSON LLP

By: */s/ Gregory P. Stone*
GREGORY P. STONE

Attorneys for Defendant FLEX LOGIX TECHNOLOGIES, INC.

[1] Defined terms in this Motion are also used in the accompanying Memorandum of Points and Authorities.

**FEDERAL CASES**

**FEDERAL STATUTES**



**STATE STATUTES**



**FEDERAL RULES**

**FEDERAL REGULATIONS**



**OTHER AUTHORITIES**

## MEMORANDUM OF POINTS AND AUTHORITIES

## INTRODUCTION

Konda Tech's complaint alleges that Flex Logix infringes five patents purportedly assigned to Konda Tech, a company founded by Dr. Venkat Konda in 2007. *See* Dkt. 1 (Complaint) at Counts 2-6, ¶ 11. Dr. Konda is the sole named inventor on each of the five asserted patents. *See* Complaint, Exs. 4-8. While the complaint offers few specifics, the complaint alleges that Konda Tech's patents generally relate to "field-programmable gate array ('FPGA') routing fabric" and "interconnection networks technology." *See* Complaint ¶ 11. Konda Tech also brings a state law claim for Unfair Business Practices under California's Unfair Competition law ("UCL") pursuant to California Business & Professions Code Section 17200 et seq. *See* Complaint, Count 1, ¶¶ 30-35.

Konda Tech's complaint fails to state a plausible claim for patent infringement, and its UCL claim is preempted by federal patent law and barred by the applicable statute of limitations. Because Konda Tech's complaint is manifestly deficient in numerous respects, Konda Tech's complaint should be dismissed in its entirety.

First, three of the patents asserted by Konda Tech (specifically, U.S. Patent 8,898,611 ("the '611 patent"); U.S. Patent 9,529,958 ("the '958 patent"); and U.S. Patent 10,050,904 ("the '904 patent")) are invalid in view of one of Konda Tech's *own* prior patent publications.[1] The invalidity of these patents can be straightforwardly determined by a review of Konda Tech's complaint in combination with Konda Tech's own patent applications and patent publications, which are properly judicially noticeable at this stage of the proceedings. In brief, the disclosures of these three patents were made publicly available more than one year prior to the earliest possible priority date for each patent, rendering each of the patents indisputably invalid. There is no subject matter that each of the patents could properly claim that was not publicly disclosed more than one year before each of the patent's earliest possible priority date. Flex Logix submits

[1] Flex Logix contends that each of the five asserted patents is invalid but has limited its motion to three of these patents at this time, because a mere review of the complaint and judicially noticeable materials unequivocally demonstrates the invalidity of those three patents.

this is a circumstance in which this Court may properly dismiss Konda Tech's patent infringement claims based on invalidity of the asserted patents at this stage in the litigation. No further proceedings are necessary in order to permit this Court to reach the conclusion that each of these patents is invalid. There is no reason to delay—this Court can and should dismiss Counts Three, Four, and Six of Konda Tech's complaint due to the invalidity of each of the asserted patents.[2]

Second, Konda Tech makes no attempt to plead a plausible claim for infringement under *Twomby* and *Iqbal* with respect to *any* of the five asserted patents. Among Konda Tech's infringement allegations' numerous deficiencies, Konda Tech fails to identify any accused products, provides no comparison of any allegedly infringing products to the claims of the asserted patents, and relies on mere (and incomplete) recitations of statutory language instead of specific factual allegations. Konda Tech's patent infringement claims are woefully inadequate and should be dismissed.

Third, Konda Tech's UCL claim asserts that "Flex Logix's patent infringement, and other tortious behavior, as described above and below in the causes of action listed in this Complaint, all constitute unfair and unlawful business practices pursuant to California Business & Professions Code Section 17200 *et seq*." Complaint ¶ 31. However, the only "tortious" behavior alleged by Konda Tech in its complaint is patent infringement. Because Konda Tech's UCL claim is based on and coextensive with its allegations of patent infringement, it is preempted by federal patent law, and should be dismissed in its entirety. Moreover, the face of the complaint makes clear that to the extent any of portion of this claim is not preempted by federal patent law, it is barred by the 4-year statute of limitations applicable to such claims.

Finally, Konda Tech's complaint does not purport to state a claim for fraud. Nonetheless, the complaint refers to purported "subterfuge and deceit" by Flex Logix's founders, Drs. Dejan Markovic and Cheng Wang, and references their alleged "fraudulent credibility" in FPGA

[2] Flex Logix has informed Konda Tech's counsel of the clear invalidity of these patents (as well as of the two other asserted patents) and reserves the right to seek relief pursuant to Federal Rule of Civil Procedure 11, a determination that this case is exceptional under 35 U.S.C. § 285, and recovery of its attorneys' fees based on Konda Tech's continued assertion of its patent infringement claims.

technology. Complaint ¶ 26. The complaint's references to fraud are irrelevant to the claims pled and scandalous and in view of the complaint's failure to plead any alleged fraud with particularity. The complaint's references to fraud should be stricken and/or dismissed.

## SUMMARY OF COMPLAINT AND FACTUAL BACKGROUND

Flex Logix provides the following brief summary of Konda Tech's complaint as well as additional factual background based on publicly available patent applications and publications, which this Court may take judicial notice of in considering this motion. *See* Request for Judicial Notice (filed currently herewith) ("RJN"); *see also* Argument Section 1.B, *infra*.

### I. KONDA TECH'S ALLEGATIONS OF INFRINGEMENT OF THE '611 PATENT, THE '958 PATENT, AND THE '904 PATENT

#### A. The Asserted Patents and Their Relationship to Each Other

Konda Tech alleges that Flex Logix infringes the '611 patent, the '958 patent, and the '904 patent. Complaint, Count 3 ('611 patent), Count 4 ('958 patent), Count 6 ('904 patent); Complaint Exs. 5, 6, 8. All three of these patents belong to the same family. The '904 patent is a continuation of the '958 patent, which in turn is a continuation of the '611 patent. *See id.* (Related U.S. Application Data). Because the '958 and '904 patents are continuations of the '611 patent, all three patents must necessarily contain the same disclosures. *See, e.g., Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1321 n.2 (Fed. Cir. 2008) ("[A] continuation contains the same disclosure found in an earlier application."); *Applied Materials, Inc. v. Advanced Semiconductor Materials Am., Inc.*, 98 F.3d 1563, 1579 (Fed. Cir. 1996) ("By definition, a continuation adds no new matter and is akin to an amendment of a pending application.") (Archer, J., *concurring*); MPEP § 201.07 ("A continuation application is an application for the invention(s) disclosed in a prior- filed copending nonprovisional application . . . . The disclosure presented in the continuation must not include any subject matter which would constitute new matter if submitted as an amendment to the parent application.").[3]

[3] Accordingly, while the '958 and '904 patents purport on their face to cross-reference and incorporate by reference additional patent applications in addition to those listed in the '611

Each of the ’611, ’958, and ’904 patents ultimately claims priority to U.S. Provisional Patent Applications 61/252,603 (“the ’603 provisional application”) and 61/252,609 (“the ’609 provisional application”). *See* Complaint Exs. 5, 6, 8 (Related U.S. Application Data). The ’611 patent is characterized as a continuation-in-part with respect to the ’603 and ’609 provisional applications.[4] *See* Complaint Ex. 5 (’611 patent) at 1:8-21. Both the ’603 and ’609 provisional applications were filed on October 16, 2009, which is the earliest priority date possible for each of the ’611, ’958, and ’904 patents. *See* Complaint Exs. 5, 6, 8 (Related U.S. Application Data).

The disclosures of the ’611, ’958, and ’904 patents correspond directly to the two provisional applications to which they claim priority. For example, Figures 1-7 of the ’611, ’958, and ’904 patents (Complaint Exs. 5, 6, 8) match Figures 1-7 of the ’603 provisional (RJN Ex. 2); and Figures 8-10 of the ’611, ’958, and ’904 patents match Figures 1-3 of the ’609 provisional (RJN Ex. 3). The text describing Figures 1-10 of the ’611 ’958, and ’904 patents is also the same as that in the corresponding provisional applications with appropriate updating to reflect different numbering of Figures 8-10 in the ’611 patent, which were Figures 1-3 in the ’609 provisional.

**B. The Publication of the Konda PCT**

International PCT Application No. WO 2008/109756 A1 (“the Konda PCT”) incorporates by reference, among other patent applications, U.S. Provisional Patent Applications 60/984,724 (“the ’724 provisional application”) and 61/018,494 (“the ’494 provisional application”). RJN Ex. 1 (Konda PCT) at 2:18-25. By incorporating the ’724 and ’494 provisional applications by reference, the Konda PCT includes the entirety of the disclosure of those provisional applications. *See Telemac Cellular Corp. v. Topp Telecom, Inc.*, 247 F.3d 1316, 1329 (Fed. Cir. 2001) (“When a document is ‘incorporated by reference’ into a host document, such as a patent, the referenced document becomes effectively part of the host document as if it were explicitly contained therein.” (citation omitted)).

patent, any such incorporation by reference cannot be used to introduce any new matter over and above that contained in the ’611 patent.

[4] This is because Figures 11A1-11A4 of the ’611 patent, and the corresponding description of those Figures, were not included in either of the ’603 and ’609 provisional applications. However, as set forth below, they were included in the Konda PCT.

The Konda PCT was published on September 12, 2008. RJN Ex. 1 (Konda PCT) (noting an "International Publication Date" of September 12, 2008). The publication of the Konda PCT on September 12, 2008, which is more than one year before the October 16, 2009 filing of the '603 and '609 provisional applications (the earliest priority date possible for the '611, '958, and '904 patents), makes the Konda PCT indisputable prior art to each of the '611, '958, and '904 patents under pre-AIA 35 U.S.C. § 102(b) or under AIA 35 U.S.C. § 102(a)(1).[5]

The publication of the Konda PCT included the disclosures of the '724 and '494 provisionals based on their incorporation by reference in the Konda PCT, and made those disclosures public as a matter of law. Specifically, under the regulations governing public availability of patent applications, both of the '724 and '494 provisionals became available to the public upon publication of the Konda PCT.

37 C.F.R. § 1.14 provides, in part, as follows:

> (vi) Unpublished pending applications (including provisional applications) that are **incorporated by reference or otherwise identified**. A copy of the application as originally filed of an **unpublished pending application may be provided to any person**, upon written request and payment of the appropriate fee (§ 1.19(b)), **if the application is incorporated by reference or otherwise identified in** a U.S. patent, a statutory invention registration, a U.S. patent application publication, **an international publication of an international application under PCT Article 21(2)**, or a publication of an international registration under Hague Agreement Article 10(3) of an international design application designating the United States. The Office will not provide access to the paper file of a pending application, except as provided in paragraph (c) or (i) of this section.[6]

(Emphases added). Accordingly, when the Konda PCT (an international publication of an international application under PCT Article 21(2)) published on September 12, 2008, "any person" was entitled to obtain copies of both the '724 and '494 provisional applications from the U.S.

[5] *See* Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284 (2011).

[6] A substantively identical version of this regulation was in effect as of the date of publication of the Konda PCT, September 12, 2008. *See* 37 C.F.R. § 1.14 (2008).

Patent & Trademark Office. And due to their incorporation by reference into the Konda PCT, their contents were effectively contained in the Konda PCT itself.

**C. The Konda PCT Anticipates Each of the '611, '958, and '904 Patents**

A comparison of the '603 and '609 provisionals (to which the '611, '958, and '904 patents ultimately claim priority) and the '724 and '494 provisionals that were included in, and made public by the publication of the Konda PCT, reveals that the '603 and '724 provisional applications are *virtually identical* to each other (*compare* RJN Ex. 2 *with* RJN Ex. 4) and that the '609 and '494 provisional applications are *virtually identical* to each other (*compare* RJN Ex. 3 *with* RJN Ex. 5). The sections pertaining to the "Cross Reference to Related Applications" (and textual references to related applications) have been updated in the later-filed '603 and '609 provisional applications, but all of the figures and text describing the figures are the same between the '603 and '724 provisional applications and the '609 and '494 provisional applications, respectively. The disclosures of certain additional patent applications incorporated by reference in the '611, '958, and '904 patents in the "Cross Reference to Related Applications" sections, which were not included in the provisionals, are also incorporated by reference in the Konda PCT. (*Compare, e.g.*, Complaint Ex. 5 ('611 patent) at 1:5-2:13 *with* RJN Ex. 1 (Konda PCT) at 1:5-2:17).[7]

In other words, the two provisional applications which became public (the '724 and '494 applications) were essentially re-filed more than one year later as the '603 and '609 provisional applications, and then used to provide the disclosure for the patent family containing the '611, '958, and '904 patents now asserted against Flex Logix by Konda Tech. As a result of Konda Tech's actions, the disclosures of the '611, '958, and '904 patents (save the claims) were already

[7] The '611 patent purports to incorporate by reference four patent applications that are not listed in the Konda PCT. *See* Complaint Ex. 5 ('611 patent at 1:5-2:13) ("Cross Reference to Related Applications"). However, each of these additional cited applications claims priority to the applications previously cited in the Konda PCT as follows: U.S. App. 12/530,207 claims priority to U.S. provisionals 60/905,526 and 60/940,383 (Complaint Ex. 5 at 1:22-36); U.S. App. 12/601,273 claims priority to U.S. provisionals 60/940,387 and 60/940,390 (Complaint Ex. 5 at 1:37-50); U.S. App. 12/601,274 claims priority to U.S. provisionals 60/940,391 and 60/940,392 (Complaint Ex. 5 at 1:51-2:3); and U.S. App. 12/601,275 claims priority to U.S. provisional 60/940,394 (Complaint Ex. 5 at 2:4-13).

disclosed in the prior art more than one year prior to the earliest priority date claimed by each of the patents, October 16, 2009, rendering each of these patents invalid. *See* pre-AIA 35 U.S.C. § 102(b) and AIA 35 U.S.C. § 102(a)(1).

The following chart summarizes where in the Konda PCT each of the disclosures of the alleged inventions of the '611, '958, and '904 patents can be found.[8]

| **'611 Patent, '958 Patent, and '904 Patent (earliest priority date October 16, 2009)** | **Konda PCT (published September 12, 2008)** |
|---|---|
| **Figures** | |
| **Figures 1-7** | **Figures 1-7 of '724 Provisional Application (RJN Ex. 4) as incorporated by reference in Konda PCT (RJN Ex. 1)** |
| **Figures 8-10** | **Figures 1-3 of the '494 Provisional Application (RJN Ex. 5) as incorporated by reference in Konda PCT** |
| **Figures 11A1-11A4** | **Figures 4A1-4A4 of Konda PCT** |
| **Detailed Description of the Invention** | |
| **Introductory text**<br>**'611 patent at 7:16-8:46**<br>**'958 patent at 7:63-9:30**<br>**'904 patent at 8:6-9:39** | **'724 Provisional Application at 6:17-9:6 (with docket numbers and references to applications updated) as incorporated by reference** |
| **Description of Figures 1-7**<br>**'611 patent at 8:47-41:4**<br>**'958 patent at 9:31-44:32**<br>**'904 patent at 9:40-44:34** | **'724 Provisional Application at 9:8-61:18 (with docket numbers and references to applications updated) as incorporated by reference** |
| **Description of Figures 8-10**<br>**'611 patent at 41:5-62:3** | **'494 Provisional Application at 7:16-42:2 (with Figure numbers and labels changed appropriately to reflect renumbering and with docket numbers and references to applications updated) as incorporated by** |

[8] *See also* Exhibit 6 to the attached Declaration of Elizabeth A. Laughton, which provides a detailed visual color-coded comparison of the disclosures of the Konda PCT to the representative '611 patent.

| **'611 Patent, '958 Patent, and '904 Patent (earliest priority date October 16, 2009)** | **Konda PCT (published September 12, 2008)** |
|---|---|
| **'958 patent at 44:33-66:61**<br>**'904 patent at 44:35-66:56** | **reference** |
| **Description of Figures 11A1-11A4**<br>**'611 patent at 62:5-64:20**<br>**'958 patent at 66:63-69:16**<br>**'904 patent at 66:58-69:12** | **Konda PCT at 69:1-72:14 (with Figure numbers and labels changed appropriately to reflect renumbering )** |

## II. KONDA TECH'S INFRINGEMENT CLAIMS ARE INADEQUATELY PLED

Konda Tech alleges that Flex Logix infringes five patents purportedly assigned to Konda Tech. *See* Complaint, Counts 2-6. The complaint alleges direct infringement by Flex Logix under 35 U.S.C. § 271(a) as well as induced and contributory infringement under 35 U.S.C. § 271(b) and (c), respectively. The complaint alleges almost no specific facts in support of its infringement claims and instead relies on vague statements and mere legal conclusions.

Konda Tech's complaint does not specify what Flex Logix products are accused of infringing the asserted patents. Rather, it simply states that "certain FPGA devices ('Accused FPGA Devices')" are alleged to infringe. *See* Complaint ¶ 44; *see also, e.g.*, Complaint ¶ 56 (referring to, but nowhere defining, "Infringing Products"). With respect to its allegations of infringement, for each of the patents, the complaint makes *no* attempt to compare the patented claims to any allegedly infringing products. Instead, the complaint recites claim language and states that "[o]n information and belief," they are met by the "Accused FPGA Devices." *See* Complaint, Counts 2-6.[9]

The complaint's induced and contributory infringement allegations are equally unsupported and conclusory. With respect to its induced infringement allegations, for each patent,

[9] At times, the claim language recited is not even the actual claim language from the patent. *Compare, e.g.*, Complaint ¶¶ 48, 49, 135 *with* Complaint Ex. 4 ('523 patent) at claim 1 and Complaint Ex. 7 ('553 patent) at claim 1.

the complaint states that "[f]or example, Flex Logix's website is replete with written directions instructing users on how to use the Accused FPGA Devices in an infringing manner" and references purported "detailed documentation instructing users on how to use the Accused FPGA Devices in an infringing manner." *See, e.g.*, Complaint ¶¶ 57-58 (allegations regarding '523 patent). It provides no additional specificity regarding these alleged "written directions" and "detailed documentation." The rest of Konda Tech's inducement allegations merely recite some (but not all) of the elements of a claim for induced infringement. *See, e.g.*, Complaint ¶¶ 57-59. For alleged contributory infringement, the complaint simply parrots some (but not all) the elements of the statute: "Flex Logix contributes to infringement of the same under 35 U.S.C. § 271(c) inasmuch as the Infringing Products offered for sale and sold by Flex Logix are each a component of a patented machine or an apparatus used in practicing a patented process, constituting a material part of Konda's invention, knowing the same to be especially made or especially adapted for use in infringement of the '523 patent." Complaint ¶ 56 (allegations regarding '523 patent). The complaint provides no factual allegations in support of these contentions.

## III. KONDA TECH'S UNFAIR BUSINESS PRACTICES CLAIM IS BASED ON ALLEGED PATENT INFRINGEMENT

Konda Tech's complaint alleges that Flex Logix founders, Drs. Dejan Markovic and Cheng Wang, "employed subterfuge and deceit to gain access to Konda Tech IP, develop their fraudulent credibility in the technology through publications based on Konda Tech IP, and then used Konda Tech IP to launch their own company—Flex Logix." Complaint ¶ 26. The complaint does not define Konda Tech IP other than to note that "IP" refers to "intellectual property." Complaint ¶ 13. The complaint never specifically identifies any alleged "Konda Tech IP" other than the patents asserted in the complaint. The complaint also alleges that Dr. Markovic stated to Dr. Konda that Dr. Markovic "would incorporate *the Konda Tech IP* into [a grant] application

*from the then published Konda Tech WIPO patents*." Complaint ¶ 15 (emphases added). Thus, the only "Konda Tech IP" referenced in the complaint consists of patents.[10]

The complaint alleges that as of January 2014, Konda was aware that Drs. Wang and Markovic were "looking for funding for their separate startup" (which eventually become Flex Logix) and that Dr. Markovic stated to Dr. Konda in January 2014 that "he *may* need to license Konda Tech IP for [that] separate startup." Complaint ¶ 22 (emphasis original). The complaint alleges that Drs. Markovic and Wang ultimately co-founded Flex Logix in February 2014. Complaint ¶ 27. The complaint does not identify any alleged wrongful conduct by either Drs. Markovic and Wang or by Flex Logix (save its allegations of patent infringement by Flex Logix) allegedly occurring after February 2014.

Konda Tech's complaint articulates the basis for its UCL claim as follows: "Flex Logix's patent infringement, and other tortious behavior, as described above and below in the causes of action listed in this Complaint, all constitute unfair and unlawful business practices pursuant to California Business & Professions Code Section 17200 *et seq*." Complaint ¶ 31. While the complaint references alleged "other tortious behavior," the complaint provides no specificity regarding the nature of said tortious behavior nor does it allege the commission of any torts.

## LEGAL STANDARDS

To survive a Rule 12(b)(6) motion, "a complaint must contain sufficient factual matter, accepted as true, to 'state a claim to relief that is plausible on its face.'" *Ashcroft v. Iqbal*, 556 U.S. 662, 678 (2009) (quoting *Bell Atl. Corp. v. Twombly*, 550 U.S. 544, 570 (2007)). This Court need not "accept any unreasonable inferences or assume the truth of legal conclusions cast in the form of factual allegations." *Brown v. Elec. Arts, Inc.*, 724 F.3d 1235, 1248 (9th Cir. 2013) (citation omitted); *see also In re Gilead Scis. Sec. Litig.*, 536 F.3d 1049, 1055 (9th Cir. 2008)

[10] Patents and patent publications are publicly available. Because Konda Tech does not allege the existence of any protectable intellectual property other than patents, Flex Logix notes that Konda Tech's allegations are illogical since the disclosures in patents and patent publications are available to the public. *See Pfaff v. Wells Elecs., Inc.*, 525 U.S. 55, 63 (1998) ("[T]he patent system represents a carefully crafted bargain that encourages both the creation and the public disclosure of new and useful advances in technology, in return for an exclusive monopoly for a limited period of time.").

("Nor is the court required to accept as true allegations that are merely conclusory, unwarranted deductions of fact, or unreasonable inferences." (citation omitted)). Further, "[t]he court need not . . . accept as true allegations that contradict matters properly subject to judicial notice or by exhibit." *Gilead*, 536 F.3d at 1055.

"[I]n deciding a Rule 12(b)(6) motion, courts may consider facts subject to judicial notice." *City of Royal Oak Ret. Sys. v. Juniper Networks, Inc.*, 880 F. Supp. 2d 1045, 1058 (N.D. Cal. 2012); *Wishnev v. Nw. Mut. Life Ins.*, 162 F. Supp. 3d 930, 935 (N.D. Cal. 2016) (same); *Bullwinkle v. U.S. Bank, Nat'l Ass'n*, No. C13-03281 HRL, 2013 WL 5718451, at *2 (N.D. Cal. Oct. 21, 2013) (same).

Federal Rule of Civil Procedure 12(f) provides that the court "may strike from a pleading an insufficient defense or any redundant, immaterial, impertinent, or scandalous matter." Fed. R. Civ. P. 12(f). "The function of a motion to strike is to avoid the expenditure of time and money that must arise from litigating spurious issues by dispensing with those issues prior to trial." *Colgate v. JUUL Labs, Inc.*, No. 18-CV-02499-WHO, 2018 WL 5619679, at *3 (N.D. Cal. Oct. 30, 2018) (internal citation and quotation omitted). "Immaterial matter is that which has no essential or important relationship to the claim for relief or the defenses being pleaded." *Zep Solar Inc. v. Westinghouse Solar Inc.*, No. C 11-06493 JSW, 2012 WL 1293873, at *1 (N.D. Cal. Apr. 16, 2012) (internal citation and quotation omitted). "Impertinent material consists of statements that do not pertain, or are not necessary, to the issues in question." *Id.* (internal citation and quotation omitted). "Allegations are considered 'scandalous' when they unnecessarily reflect on the moral character of an individual, including allegations that cast a cruelly derogatory light on a party or other person." *Gilbert v. MoneyMutual, LLC*, No. 13-CV-01171-JSW, 2015 WL 12953231, at *1 (N.D. Cal. Aug. 24, 2015) (internal citation and quotation omitted).

## ARGUMENT

### I. THIS COURT SHOULD DISMISS KONDA TECH'S INFRINGEMENT CLAIMS BASED ON THE '611 PATENT, '958 PATENT, AND '904 PATENT BECAUSE THESE PATENTS ARE INDISPUTABLY INVALID

The '611 patent, '958 patent, and '904 patent are indisputably invalid over Konda Tech's own prior patent publication, the Konda PCT. The invalidity of these patents is manifest in view

of the complaint itself and materials attached thereto, and in view of Konda Tech's own prior patent publications and applications. While Flex Logix recognizes that it is a rare situation where invalidity of a patent due to anticipation can be resolved on the pleadings, Flex Logix submits that this is such a case.

**A. This Court May Properly Invalidate the '611 Patent, '958 Patent, and '904 Patent at This Time**

Flex Logix's motion to dismiss is proper because the complaint, the exhibits attached thereto, and materials that are properly the subject of judicial notice clearly demonstrate that the '611 patent, the '958 patent, and the '904 patent are invalid. It is not often the case that the invalidity of a patent is readily apparent at the motion to dismiss stage. However, when invalidity is readily apparent, there is no just reason to delay in reaching such a determination. For example, in *Select Controls v. Am. Elec. Components, Inc.*, the court granted a motion to dismiss a patent infringement claim at the pleading stage because "the Complaint and the exhibits attached thereto reveal unequivocally that the design covered by the [patent-in-suit] was both 'the subject of a commercial offer for sale' and 'ready for patenting' prior to the Critical Date of April 18, 2001." *Select Controls v. American Electronic Components, Inc.*, No. 07 Civ. 1306(DLC), 2008 WL 216612, at *5 (S.D.N.Y. Jan. 22, 2008). The court concluded that "[the patent-in-suit] is therefore invalid as a matter of law . . ., and SCI's Claim I, alleging infringement of the '823 Patent, must be dismissed." *Id.* So too here, the invalidity of the '611 patent, the '958 patent, and the '904 patent is manifest from materials properly considered at the pleading stage and Konda Tech's infringement claims should be dismissed.

**B. This Court May Take Judicial Notice of and Consider Konda Tech's Patent Publications and Applications on a Motion to Dismiss**

Flex Logix requests that in considering its motion, this Court take judicial notice of the Konda Tech patent applications and publications referenced in this motion. *See* RJN (filed concurrently herewith). Here, because Konda Tech's patent applications and publications are documents of which this Court may properly take judicial notice at the motion to dismiss stage, this Court may decide Flex Logix's motion under Rule 12(b)(6). *See id.*; *see also Gorski v. The Gymboree Corp.*, No. 14-CV-01314-LHK, 2014 WL 3533324, at *3 n.1 (N.D. Cal. July 16,

2014). However, if the Court declines to decide Flex Logix' motion under Rule 12(b)(6), Flex Logix respectfully requests that its motion be converted to one for summary judgment under Rule 12(d). Flex Logix submits that there are no material disputed facts regarding the invalidity of the '611 patent, the '958 patent, and the '904 patent in view of the Konda PCT and that Flex Logix is entitled to judgment as a matter of law. *See* Fed. R. Civ. P. 56; *Chestnut v. Juel*, No. C 96-3422 JSB, 1997 WL 68538, at *1 (N.D. Cal. Feb. 12, 1997).

### C. The '611 Patent, '958 Patent, and '904 Patent Are Unquestionably Invalid

As set forth in detail above, *supra*, Background Section I, all of the figures in the '611, '958, and patents and all of the text describing those figures were included in the Konda PCT, which is indisputable prior art to the '611, '958, and '904 patents under pre-AIA 35 U.S.C. § 102(b) or AIA 102(a)(1). Therefore, if the claims in the '611, '958, and '904 patents are supported by the specification of the '611, '958, and '904 patents, the claims are invalid as anticipated by the Konda PCT under pre-AIA 35 U.S.C. § 102(b) or AIA 102(a)(1). Any attempt by Konda Tech to contend that the claims are directed to subject matter that was not previously publicly disclosed would, at a minimum, mean that Konda Tech's claim of priority to the '603 and '609 provisionals is wholly improper. Moreover, any such argument would almost certainly render Konda Tech's patents invalid for a lack of written description, because they claim subject matter that is not disclosed in the supporting patent specification. *See* 35 U.S.C. § 112. Thus, the invalidity of the '611, '958, and '904 patents is readily apparent in view of the patents themselves, which are attached to Konda Tech's complaint, and materials that are judicially noticeable at the motion to dismiss stage. No claim construction is needed to reach such a determination. Nor is any fact or expert discovery needed. The above-cited materials constitute clear and convincing evidence of the invalidity of these patents, and Konda Tech's patent infringement claims based on the '611, '958, and '904 patents should be dismissed because these patents are invalid.

## II. KONDA TECH'S INFRINGEMENT ALLEGATIONS ARE INADEQUATELY PLED AND SHOULD BE DISMISSED

*All* of Konda Tech's infringement claims lack sufficient factual allegations that would give rise to a plausible claim of patent infringement and accordingly must be dismissed. "[T]he rule

that '[t]hreadbare recitals of the elements of a cause of action, supported by mere conclusory statements, do not suffice' appl[ies] in patent cases." *Hitachi Kokusai Elec. Inc. v. ASM Int'l, N.V*, No. 17-CV-06880-BLF, 2018 WL 3537166, at *2 (N.D. Cal. July 23, 2018). "[The] pleading standards under *Iqbal* and *Twombly* apply to allegations of direct and indirect (i.e., induced and contributory) infringement." *Id.* Konda Tech's infringement allegations are conclusory and manifestly lack the required factual specificity.

First, Konda Tech does not identify what products are accused of infringement. The complaint states only that "certain FPGA devices ('Accused FPGA Devices')" are alleged to infringe. *See* Complaint ¶ 44; *see also, e.g.*, Complaint ¶ 56 (referring to, but nowhere defining, "Infringing Products"). "Within the Ninth Circuit, to plead a plausible claim for direct infringement, a plaintiff must identify the accused products with at least minimal specificity." *Avocet Sports Tech., Inc. v. Garmin Int'l, Inc.*, No. C 11-04049 JW, 2012 WL 1030031, at *2 (N.D. Cal. Mar. 22, 2012). Because Konda Tech's complaint provides no specific identification of accused infringing products, its infringement claims should be dismissed. *See, e.g., Lantiq N. Am., Inc. v. Ralink Tech. Corp.*, No. CV 11-00234 EJD, 2011 WL 2600747, at *7 (N.D. Cal. June 30, 2011) ("This Court disagrees with Plaintiffs that the broad categories of products listed in the Complaint put Ralink California on notice as to what it is to defend with respect to Counts I and II. Plaintiffs must provide more specific identification of the products in any given category that are allegedly infringing Plaintiffs' patents."); *Cal. Inst. of Comput. Assisted Surgery, Inc. v. Med-Surgical Servs., Inc.*, No. 10-02042 CW, 2010 WL 3063132, *1–3 (N.D. Cal. Aug. 3, 2010) (granting motion to dismiss complaint because the complaint failed to identify specifically an accused product and how that product allegedly infringed, where complaint generally identified one system); *Avocet*, 2012 WL 1030031, at *2 (similar).

The complaint also makes *no attempt* to compare the patented claims to any allegedly infringing products. The complaint merely parrots the claim language and states that "[o]n information and belief," certain claim elements are met by the (unidentified) "Accused FPGA Devices." *See* Complaint, Counts 2-6. This type of pleading, which is entirely devoid of factual specificity, fails to state a plausible claim for relief. "[A] complaint does not satisfy the standards

of *Twombly* and *Iqbal* where it does not at least contain *factual allegations* that the accused product practices every element of at least one exemplary claim." *Novitaz, Inc. v. inMarket Media, LLC*, No. 16-CV-06795-EJD, 2017 WL 2311407, at *3 (N.D. Cal. May 26, 2017) (emphasis added) (dismissing direct infringement claims as inadequately pled). Konda Tech's claims for infringement should be dismissed for this reason as well. *See, e.g.*, *id.* at *4 ("[A]llegations [which] merely parrot claim language . . . . are not factual allegations, as the claim language is what [plaintiff] must show in order to prove infringement. Instead, they are '[t]hreadbare recitals of the elements of a cause of action, supported by mere conclusory statements,' which 'do not suffice.'" (quoting *Iqbal*, 556 U.S. at 678); *e.Digital Corp. v. iBaby Labs, Inc.*, No. 15-CV-05790-JST, 2016 WL 4427209, at *5 (N.D. Cal. Aug. 22, 2016) (finding complaint failed to state a claim where plaintiff "ha[d] not attempted to map [a] limitation onto any allegations in the [complaint]" and "based on the Court's own independent review, it cannot discern how the [complaint] could be said to plausibly allege this limitation"); *see also L.M. Sessler Excavating & Wrecking, Inc. v. Bette & Cring, LLC*, No. 16-CV-06534-FPG, 2017 WL 4652709, at *4-5 (W.D.N.Y. Oct. 17, 2017) ("Reliance on the patent language alone to describe Defendant's alleged conduct renders Plaintiff's claim a legal conclusion insufficient to meet the pleading standard of *Twombly* and *Iqbal*.").

Konda Tech's inducement allegations are similarly devoid of any factual content that could give rise to a reasonable inference that Flex Logix has induced infringement of any of the asserted patents. The complaint states that "[f]or example, Flex Logix's website is replete with written directions instructing users on how to use the Accused FPGA Devices in an infringing manner" and references purported "detailed documentation instructing users on how to use the Accused FPGA Devices in an infringing manner." *See, e.g.*, Complaint ¶¶ 57-58 (allegations regarding '523 patent). However, the complaint provides no additional specificity regarding these alleged "written directions" and "detailed documentation," nor does it allege how Flex Logix has knowledge that the induced acts constitute patent infringement or how Flex Logix has the specific intent to induce infringement. *See, e.g., Uniloc USA, Inc. v. Apple Inc.*, No. C 18-00359 WHA, 2018 WL 2047553, at *4 (N.D. Cal. May 2, 2018) ("Uniloc's vague and conclusory allegations

that Apple 'intentionally instructs its customers to infringe' using broad categories of materials, coupled with a list of five generic websites, do not amount to *factual* content supporting any reasonable inference that Apple possessed either 'knowledge that the induced acts constitute patent infringement' or 'specific intent to encourage another's infringement.'"); *CAP Co. v. McAfee, Inc.*, No. 14-CV-05068-JD, 2015 WL 3945875, at *5 (N.D. Cal. June 26, 2015) ("CAP's problem is that it fails to allege any statements by McAfee or Symantec at all. CAP makes passing references to 'user manuals guides, and support articles,' without ever saying what those materials contain, which is wholly inadequate for an inference of specific intent."); *Avocet Sports Tech., Inc. v. Garmin Int'l, Inc.*, No. C 11-04049 JW, 2012 WL 2343163, at *4 (N.D. Cal. June 5, 2012) (holding that pleading that giving customers "specific instructions or training" is insufficient to allege induced infringement).

Turning to Konda Tech's allegations of contributory infringement, the complaint simply parrots *some* of the elements of the relevant statute and provides *no* factual allegations. *See, e.g.*, Complaint ¶ 56 (allegations regarding '523 patent). Notably, the complaint does not even attempt to allege that the accused products have no substantial non-infringing uses, a required element of a contributory infringement claim. *See* 35 U.S.C. § 271(c). Again, these allegations are unquestionably inadequate, fail to plausibly allege a claim for contributory infringement, and should be dismissed. *See, e.g.*, *Windy City Innovations, LLC v. Microsoft Corp.*, 193 F. Supp. 3d 1109, 1116–17 (N.D. Cal. 2016) (An allegation tracking the statute "is nothing but a bare conclusion. Accordingly, the Court *Grants* defendant's motion to dismiss the contributory infringement claim.") (internal citation omitted); *Uniloc USA, Inc. v. Logitech, Inc.*, No. 18-CV-01304-LHK, 2018 WL 6025597, at *3 (N.D. Cal. Nov. 17, 2018) ("Uniloc's fleeting reference to the fact that the accused products have no substantial noninfringing uses does not provide the requisite factual basis to support Uniloc's claim, which merely paraphrases the contributory infringement statute."); *Uniloc*, 2018 WL 2047553, at *5 (Contributory infringement allegations

were "merely [a] formulaic recitation of Section 271(c) not entitled to the presumption of truth.").[11]

## III. THIS COURT SHOULD DISMISS KONDA TECH'S UNFAIR BUSINESS PRACTICES CLAIM

Konda Tech's sole non-patent cause of action is in fact a patent infringement claim in disguise. Because Konda Tech's unfair business practices claim under UCL Section 17200 et seq. is preempted by federal patent law, it should be dismissed with prejudice. Further, Konda Tech's complaint itself also demonstrates that the claim is barred by the 4-year statute of limitations. For this reason as well, this claim should be dismissed with prejudice.

### A. Konda Tech's Unfair Business Practices Claim Is Preempted by Federal Patent Law

"Federal patent and copyright laws limit the states' ability to regulate unfair competition." *Summit Mach. Tool Mfg. Corp. v. Victor CNC Sys., Inc.*, 7 F.3d 1434, 1439 (9th Cir. 1993). "According to the Supreme Court, state law is preempted when it enters 'a field of regulation which the patent laws have reserved to Congress.'" *Id.* (quoting *Bonito Boats, Inc. v. Thunder Craft Boats, Inc.*, 489 U.S. 141, 167 (1989)). "[A] violation of federal patent law—without more—cannot serve as the basis of [a Section 17200] claim." *Halton Co. v. Streivor, Inc.*, No. C 10-00655 WHA, 2010 WL 2077203, at *4 (N.D. Cal. May 21, 2010). Instead, "[a] state-law claim must be 'qualitatively different from a copyright or patent infringement claim' or else it is preempted." *Id.* (quoting *Summit Mach Tool*, 7 F.3d at 1439-40).

Courts routinely dismiss state law claims which are premised solely on a violation of federal patent law as preempted by federal law. *See, e.g.*, *Halton*, 2010 WL 2077203, at *4 (dismissing California unfair competition claim under Section 17200 as preempted by federal

[11] Konda Tech's willful infringement claims are similarly devoid of any factual allegations, and should also be dismissed. Konda Tech simply alleges that "Flex Logix's infringement of the '523 patent has been willful and deliberate and, pursuant to 35 U.S.C. § 284, Konda Tech is entitled to treble damages." *See, e.g.*, *Elec. Scripting Prods., Inc. v. HTC Am. Inc.*, No. 17-CV-05806-RS, 2018 WL 1367324, at *7 (N.D. Cal. Mar. 16, 2018) ("ESPI falls woefully short of sufficiently pleading egregious behavior and willfulness. ESPI must provide factual allegations that are specific to HTC's conduct and do not merely recite the elements of the statutory violations, but rather provide factual material that puts HTC on notice of its allegedly unlawful actions.").

patent law); *AntiCancer, Inc. v. CellSight Techs., Inc.*, No. 10CV2515 JLS (RBB), 2012 WL 3018056, at *7-8 (S.D. Cal. July 24, 2012) (dismissing California common law and unfair competition claims which were "predicated on [defendant's] alleged violation of federal patent laws"); *JAT Wheels, Inc. v. DB Motoring Grp., Inc.*, No. CV 14-5097-GW(AGRx), 2016 WL 9453798, at *3 (C.D. Cal. Feb. 11, 2016) ("Because Plaintiff has not alleged any additional tortious conduct that is separate from the patent law cause of action, preemption applies."); *TMC Aerospace, Inc. v. Elbit Sys. of Am. LLC*, No. CV 15-07595-AB (Ex), 2016 WL 3475322, at *8 (C.D. Cal. Jan. 29, 2016) (dismissing quasi-contract claim where "this claim is substantively no different than Plaintiff's patent infringement claim").

The basis for Konda Tech's UCL claim as articulated in the complaint is as follows: "Flex Logix's patent infringement, and other tortious behavior, as described above and below in the causes of action listed in this Complaint, all constitute unfair and unlawful business practices pursuant to California Business & Professions Code Section 17200 *et seq.*" Complaint ¶ 31. To the extent that Konda Tech's claim is based on "Flex Logix's patent infringement," it is clearly preempted under the authority set forth above. Konda Tech's complaint refers to "other tortious behavior" but nowhere does the complaint allege that Flex Logix committed any other purported torts. Thus, Konda Tech's claim is preempted by federal patent law and should be dismissed.

### B. Konda Tech's Unfair Business Practices Claim Is Also Barred by the Statute of Limitations

Further, to the extent not preempted by federal patent law, Konda Tech's unfair business practices claim under the UCL is barred by the statute of limitations. "Claims under the UCL are subject to a four year statute of limitations that begins to run on the date the cause of action accrues." *Zanze v. Snelling Servs., LLC*, 412 F. App'x 994, 996 (9th Cir. 2011); Cal. Bus. & Prof. Code § 17208 ("Any action to enforce any cause of action pursuant to this chapter shall be commenced within four years after the cause of action accrued."). "A statute of limitations defense may be raised by a motion to dismiss if 'the running of the statute is apparent on the face of the complaint.'" *Zanze*, 412 F. App'x at 996 (*quoting Von Saher v. Norton Simon Museum of Art at Pasadena*, 592 F.3d 954, 969 (9th Cir. 2010)).

Save Konda Tech's allegations of patent infringement, all of the alleged wrongs complained of by Konda Tech took place more than four years before Konda Tech filed its complaint in this action on December 17, 2018. Indeed, the complaint does not identify any alleged specific wrongful conduct by Dr. Markovic, Dr. Wang, or by Flex Logix (save its allegations of patent infringement by Flex Logix) allegedly occurring after February 2014. And Konda Tech alleges no facts to support the application of the discovery rule or equitable tolling in the complaint. Accordingly Konda Tech's unfair business practices claim should be dismissed for this reason as well. *See, e.g.*, *Moran v. Wash. Mut. Bank*, No. 12-CV-04974 NC, 2012 WL 12920636, at *5 (N.D. Cal. Nov. 8, 2012) ("As Moran filed his complaint more than six years after the alleged violations, and he asserts no theory of tolling in the complaint or the amended complaint, defendant's motion to dismiss Moran's § 17200 claims is GRANTED WITH PREJUDICE."); *Montes v. U.S. Bank Nat'l Ass'n*, No. CV 10-0022 PSG (Jcx), 2010 WL 11597507, at *3 (C.D. Cal. July 21, 2010) (dismissing § 17200 claim as time-barred where "Plaintiff's allegations involve disclosures that occurred on or before August 27, 2004, when the mortgage was obtained" and "Plaintiff did not file his complaint until December 2, 2009, beyond the four-year statute of limitations for this cause of action").

## IV. THIS COURT SHOULD STRIKE AND/OR DISMISS THE COMPLAINT'S REFERENCES TO FRAUD

Konda Tech's complaint does not include any claims for fraud nor does it allege that Flex Logix engaged in any allegedly fraudulent conduct. However, the complaint does state that "Drs. Markovic and Wang's conduct make clear that they employed *subterfuge and deceit* to gain access to Konda Tech IP, develop their *fraudulent* credibility in the technology through publications based on Konda Tech IP." Complaint ¶ 26 (emphases added). These allegations should be stricken because they are immaterial and impertinent to the claims pled and are scandalous in that they baselessly impugn the character of Drs. Wang and Markovic.

The above-referenced statement in the complaint is not specific to any of the claims pled. However, to the extent that these allegations are somehow construed to refer to one of those claims, they are woefully deficient, and should be dismissed. "[C]laims that 'sound in fraud' or

are 'grounded in fraud . . . must be pled with particularity under FRCP 9(b)." *Halton*, 2010 WL 2077203, at *4; *see also Kearns v. Ford Motor Co.*, 567 F.3d 1120, 1125 (9th Cir. 2009). "To satisfy the rule, a plaintiff must allege the 'who, what, where, when, and how' of the charged misconduct." *Plascencia v. Wachovia Bank*, No. C 10-03552 RS, 2011 WL 249492, at *1 (N.D. Cal. Jan. 26, 2011) (citing *Cooper v. Pickett*, 137 F.3d 616, 627 (9th Cir. 1997)). "The plaintiff must set forth what is false or misleading about a statement, and why it is false." *Vess v. Ciba-Geigy Corp. USA*, 317 F.3d 1097, 1106 (9th Cir. 2003) (internal citation and quotation omitted). "[T]he circumstances constituting the alleged fraud must be specific enough to give defendants notice of the particular misconduct so that they can defend against the charge and not just deny that they have done anything wrong." *Vess v. Ciba–Geigy Corp. U.S.A.*, 317 F.3d 1097, 1106 (9th Cir. 2003). Konda Tech makes no effort to do so in its complaint.

Because Konda Tech does not state a claim for fraud nor attempt to plead fraud with the requisite specificity, Konda Tech's allegations relating to "subterfuge and deceit" and "fraudulent credibility" are irrelevant to the claims at issue and unfairly impugn the character of both Drs. Markovic and Wang, both non-parties to this action. *See Dallas & Lashmi, Inc. v. 7-Eleven, Inc.*, 112 F. Supp. 3d 1048, 1056 (C.D. Cal. 2015) (noting that one of the purposes of Rule 9(b)'s heightened pleading standard is to "protect defendants from unwarranted damage to their reputations"). Konda Tech's complaint's references to "subterfuge and deceit" and "fraudulent credibility" should be stricken. *See, e.g., SecuriMetrics, Inc. v. Hartford Cas. Ins.*, No. C 05-00917 CW, 2005 WL 2463749, at *6 (N.D. Cal. Oct. 4, 2005) (striking portion of affirmative defense that referenced "fraudulent conduct" where "Defendant's seventh affirmative defense includes fraud and thus is subject to fraud's pleading requirement, which it does not fulfill"); *Daniel v. Richards*, No. 13-CV-02426-VC, 2014 WL 2768624, at *3 (N.D. Cal. June 18, 2014) (striking complaint's references to fraud as "irrelevant"); *Siegel v. Lyons*, No. C-95-3588 DLJ, 1996 WL 634206, at *7-8 (N.D. Cal. Sept. 16, 1996) (granting motion to dismiss and/or strike fraud allegations as deficient); *Felix v. State*, No. 1:13-CV-0561 LJO SKO, 2013 WL 3730176, at *11 (E.D. Cal. July 12, 2013) (granting motion to strike fraud allegations where "Plaintiffs'

allegations regarding overtime fraud do not state an independent claim and will only confuse the trier of fact as to the actual basis for Plaintiffs' retaliation claims").

**CONCLUSION**

For the reasons set forth above, Konda Tech's complaint should be dismissed in its entirety.

DATED: January 24, 2019

MUNGER, TOLLES & OLSON LLP

By: */s/ Gregory P. Stone*
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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA, SAN JOSE DIVISION

KONDA TECHNOLOGIES, INC., a California corporation,

Plaintiff,

vs.

FLEX LOGIX TECHNOLOGIES, INC,.

Defendant.

CASE NO. 5:18-cv-07581-LHK

**[PROPOSED] ORDER GRANTING FLEX LOGIX TECHNOLOGIES, INC.'S MOTION TO DISMISS**

Date: May 9, 2019
Time: 1:30 p.m.
Judge: Lucy H. Koh
Ctrm.: 8, 4th Floor

Before this Court is Defendant Flex Logix Technologies, Inc.'s ("Flex Logix") Motion to Dismiss Plaintiff Konda Technologies, Inc.'s complaint. On consideration of the briefs filed in support and opposition thereto, and all other papers on file herein, Flex Logix's Motion is hereby GRANTED. Plaintiff's complaint is DISMISSED in its entirety WITH PREJUDICE.

**IT IS SO ORDERED.**

DATED: _____, 2019

_____
Hon. Lucy H. Koh
United States District Judge

# EXHIBIT 45

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

KONDA TECHNOLOGIES, INC.,

Plaintiff,

v.

FLEX LOGIX TECHNOLOGIES, INC.,

Defendant.

Case No. 18-CV-07581-LHK

**ORDER DENYING MOTION TO DISMISS AND TO STRIKE AS MOOT AND DENYING STIPULATION AS MOOT**

Re: Dkt. Nos. 21, 29

On December 17, 2018, Plaintiff filed a complaint against Defendant. On January 24, 2019, Defendant filed a motion to dismiss and to strike portions of the complaint. ECF No. 21. On March 1, 2019, the Court granted the parties' stipulation to allow Plaintiff to file an amended complaint. ECF No. 30. Therefore, in light of the amended complaint that is to be filed, Defendant's January 24, 2019 motion to dismiss and to strike portions of the complaint is DENIED as moot.

Plaintiff shall file its first amended complaint on March 4, 2019. Defendant shall file its motion to dismiss and/or strike 14 days thereafter. Plaintiff shall have 21 days to respond to the motion to dismiss and/or strike. Defendant shall have 14 days to reply. The parties cannot select

the hearing date for Defendant's intended motion. The parties shall follow the Court's standard procedure of contacting the Courtroom Deputy within 24 hours of filing their motion to request the next available hearing date on the Court's law and motion calendar. The Court DENIES as moot the parties' stipulation to allow the filing of Plaintiff's first amended complaint and extending the briefing schedule on Defendant's anticipated motion to dismiss. ECF No. 29.

The parties shall file their joint case management statement by March 27, 2019. The Court will decide whether to continue the April 3, 2019 case management conference based on the parties' joint case management statement.

**IT IS SO ORDERED.**

Dated: March 1, 2019

Lucy H. Koh

LUCY H. KOH
United States District Judge

# EXHIBIT 46

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

KONDA TECHNOLOGIES, INC., a California corporation,

Plaintiff,

v.

FLEX LOGIX TECHNOLOGIES, INC., a Delaware Corporation, Dejan Markovic, Ph.D., an individual, and Cheng C. Wang, Ph.D., an individual,

Defendants.

CASE NO. 5:18-cv-07581-LHK

**[PROPOSED] FIRST AMENDED COMPLAINT FOR:**

1. **Unfair Business Practices**
2. **Infringement of U.S. Patent No. 8,269,523**
3. **Infringement of U.S. Patent No. 8,898,611**
4. **Infringement of U.S. Patent No. 9,529,958**
5. **Infringement of U.S. Patent No. 10,003,553**
6. **Infringement of U.S. Patent No. 10,050,904**
7. **Fraud - Intentional Misrepresentation**
8. **Fraud – Concealment**
9. **Misappropriation of Trade Secrets**

**JURY TRIAL DEMANDED**

Plaintiff Konda Technologies, Inc. ("Konda Tech" or "Plaintiff"), by and through its undersigned counsel, hereby asserts as follows against Defendants Flex Logix Technologies, Inc. ("Flex Logix"), Dejan Markovic, Ph.D. ("Dr. Markovic"), and Cheng C. Wang, Ph.D. ("Dr. Wang") (collectively, "Defendants"). Konda Tech alleges as follows:

## NATURE OF THE ACTION

1. This is a civil action for patent infringement arising under the patent laws of the United States, Title 35 of the United States Code and pendent causes of action arising from related transactions and occurrences under the laws of the State of California.

2. As set forth in more detail below, Flex Logix has been infringing United States Patent Nos. 8,269,523 (the "'523 patent"); 8,898,611 (the "'611 patent"); 9,529,958 (the "'958 patent"); 10,003,553 (the "'553 patent"), and 10,050,904 (the "'904 patent") (collectively, the "patents-in-suit"), and continues to do so through the present date, and Defendants have committed additional unlawful acts under the law of this State.

## PARTIES

3. Konda Tech is a California corporation with its principal place of business in San Jose, California.

4. Upon information and belief, Flex Logix is a Delaware corporation registered to do business in California, and with its principal place of business in Mountain View, California.

5. Dr. Markovic is a resident of California and conducts business in Mountain View, California.

6. Dr. Wang is a resident of California and conducts business in Mountain View, California.

## JURISDICTION AND VENUE

7. This Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

8. This Court has personal jurisdiction over Flex Logix, Dr. Markovic, and Dr. Wang, because (a) they have committed the acts of patent infringement and other unlawful acts complained of herein in this State and this District, and/or (b) they have directed their acts of infringement and other unlawful acts complained of herein in this State and this District.

9. This Court has personal jurisdiction over the Defendants for the additional reason that

they have engaged in systematic and continuous contacts with this State and this District by, *inter alia*, regularly conducting and soliciting business in this State and this District, and deriving substantial revenue from products and/or services provided to persons in this State and this District.

10. Venue is proper in this District under 28 U.S.C. § 1391(b), because a substantial part of the acts complained of herein occurred in this District, Defendants transact business in this District, Flex Logix resides in this District, and/or the property that is the subject of this action is situated in this District.

11. Venue is proper in this District under 28 U.S.C. §§ 1391(c)–(d) and 1400(b) because (i) Flex Logix resides in this District and has a regular and established place of business in this District; and (ii) Defendants have committed acts of infringement and other unlawful acts in this District.

**INTRADISTRICT ASSIGNMENT**

12. Pursuant to Local Rule 3-5(b), Konda Tech alleges that assignment to the San Jose Division is proper under Local Rule 3-2(e), because Plaintiff and Defendant Flex Logix have their principal places of business and/or reside in the San Jose Division and/or Defendants have committed unlawful acts in the San Jose Division, as alleged *supra* at paragraphs 3–4 and 8.

**FACTUAL BACKGROUND**

13. Konda Tech was founded by Venkat Konda, Ph.D. ("Dr. Konda") in 2007. Dr. Konda is a pioneer in field-programmable gate array ("FPGA") routing fabric and interconnection networks technology. Konda Tech's business is based on Dr. Konda's work, and provides chip and system level interconnect technology solutions. Konda Tech has licensed FPGA interconnect architecture patent rights to two FPGA chip vendors, the first of which has made and sold three generations of chips. Dr. Konda has a Ph.D. in Computer Science and Engineering from the University of Louisville, and has been granted eleven patents in the space.

14. In or around January 2009, Dr. Konda was introduced to Dr. Markovic by Flavio Bonomi, Ph.D. ("Dr. Bonomi"), a VP and Head of Advanced Architecture and Research at Cisco Systems, Inc. ("Cisco"). Konda Tech was one of six startups that received an oral offer for funding from Cisco that was later rescinded. Dr. Markovic knew of Cisco's rescinded offer, and that Konda Tech was still looking for funding, and Dr. Markovic claimed that Konda Tech could receive funding through

UCLA's Institute of Technology Advancement ("ITA"). Dr. Markovic was and is a UCLA professor focused on circuits and embedded systems (which overlaps and compliments with Konda Tech intellectual property), and involved with the ITA. Dr. Markovic was not focused on FPGA work until he met Dr. Konda.

15. Dr. Markovic was interested in Konda Tech's intellectual property ("Konda Tech IP") and suggested that Dr. Konda present before the ITA. Dr. Konda did make such a presentation on October 12, 2009. The presentation was fruitless as the ITA does not provide funding to non-UCLA related entities—a fact that should have been known to Dr. Markovic prior to inviting Dr. Konda to present to the ITA.

16. Dr. Markovic, enamored with Konda Tech IP, also asked Dr. Konda to give a seminar on the technology to Dr. Markovic's students. Among those in attendance at the October 12, 2009 seminar was Dr. Wang, a graduate student and Ph.D. candidate at the time. Dr. Wang subsequently grew similarly interested in the Konda Tech IP.

17. In June and July 2010, Dr. Markovic called Dr. Konda, and told him that he wanted to use Konda Tech IP in two different applications for DARPA funding. Dr. Konda advised that he did not then have the time to work with Dr. Markovic. However, both times, Dr. Markovic assured Dr. Konda that he would not have to spend any time on the applications, and that he would incorporate the Konda Tech IP into the applications from the then published Konda Tech WIPO patent applications. Dr. Markovic assured Dr. Konda that he would help to secure a license from Konda Tech should a DARPA grant be approved.

18. Attached hereto as Exhibits 1 and 2 are the June 23, 2010 and August 6, 2010 DARPA funding proposals (the "DARPA Proposals") that followed those conversations.

19. Both of the DARPA Proposals make clear that Konda Tech IP was at the heart of what Drs. Markovic and Wang were hoping to accomplish:

> Konda Technologies inventions with regular VLSI layouts for Benes/BFT based hierarchical networks are seminal and subsumes all the other known network topologies such as Clos networks, hypercube networks, cube-connected cycles and pyramid networks, which makes these networks implementable in a FPGA devices with regular structures both interconnect distribution-wise and layout-wise which is the key to exploit improved area, power, and performance of FPGA devices. The regularity of Konda hierarchical

> layout is also the key for its commercializability in System-on-Chip interconnect devices, FPIC devices as well.

Indeed, the DARPA Proposals state that they "will make use of hierarchically routed and proprietary Konda interconnect architecture." The first DARPA Proposal further estimates that Dr. Konda and Konda Tech would complete 620 task hours of the estimated 1020 task hours for key personnel.

20. Those DARPA Proposals, replete with references to Konda Tech IP, were rejected. However, Dr. Markovic and Dr. Wang were not dissuaded from continuing to work with Konda Tech IP.

21. In 2010, Dr. Markovic told Dr. Konda over the phone that his students, including Dr. Wang, were implementing Konda Tech IP as an academic project, specifically the 2D layout, on an FPGA chip. In June 2011, unbeknownst to Dr. Konda, Drs. Markovic and Wang presented a paper at the 2011 VLSI Circuits Symposium titled "A 1.1 GOPS/mQ FPGA Chip with Hierarchical Interconnect Fabric"—based on Konda Tech IP.

22. Subsequently, Dr. Markovic invited Dr. Konda by email in the fall of 2013 to meet him at Stanford University while he was a Visiting Associate Professor. When they met, Dr. Konda inquired whether Dr. Markovic and his students had stopped implementing Konda Tech IP as part of his academic work. Dr. Markovic replied yes. During the conversation Dr. Markovic also asked Dr. Konda to share the names of customers he was working with to license Konda Tech IP.

23. Between 2011 and 2014, Drs. Markovic and Konda had occasional phone calls, where they spoke about the progress of their respective work, but Dr. Markovic never disclosed that Konda Tech IP was the subject of Dr. Wang's June 2013 Ph.D. dissertation titled, "Building Efficient, Reconfigurable Hardware using Hierarchical Interconnects."

24. Dr. Konda met with Drs. Markovic and Wang at the home of Dr. Bonomi in January 2014. Dr. Bonomi had invited them to his home because he was in the process of forming his own startup, and needed to license Konda Tech IP. Dr. Bonomi was looking for implementation help from Drs. Markovic and Wang. Over the course of their discussions, Drs. Markovic and Wang stated that they were looking for funding for their separate startup, but when queried, refused to disclose the technological focus of their startup. Cryptically, Dr. Markovic later stated that he *may* need to license

Konda Tech IP for their separate startup as well. Dr. Konda replied that most of the Konda patents were published or granted and suggested Dr. Markovic check them on the web to see if a license was needed and if so to contact Dr. Konda to obtain a license.

25. A couple of weeks later, Drs. Markovic and Wang published a paper titled "A Multi-Granularity FPGA with Hierarchical Interconnects for Efficient and Flexible Mobile Computing"—again, based on Konda Tech IP—at the 2014 International Solid State Circuits Conference (the "ISSCC paper"). Though publishing at secondary conferences and in journals, Drs. Markovic and Wang never attended or published any papers at the International Symposium on FPGAs held annually in Monterey, California. This is the primary FPGA conference, and one they know Dr. Konda attends every year.

26. The ISSCC paper is attached hereto as Exhibit 3.

27. The ISSCC paper describes and demonstrates technologies that were invented by Dr. Konda, monetized by Konda Tech, and the subject matter of the patents-in-suit.

28. Drs. Markovic's and Wang's conduct make clear that they employed subterfuge and deceit to gain access to Konda Tech IP, develop their fraudulent credibility in the technology through publications based on Konda Tech IP, and then used Konda Tech IP to launch their own company—Flex Logix.

29. Drs. Markovic and Wang ultimately co-founded Flex Logix in February 2014.

30. Dr. Konda only learned of Drs. Markovic and Wang's above-referenced publications, dissertation, and the formation of Flex Logix in December 2015, when informed of the same by Dr. Vaughn Betz, a University of Toronto professor, when he asked Dr. Konda if Flex Logix was using Konda Tech IP.

31. Flex Logix touts the ISSCC paper on its website as describing Flex Logix's "new, patented interconnect, XFLX™." *See*, http://www.flex-logix.com/fpga-tutorial/.

**FIRST CAUSE OF ACTION**

**Unfair Business Practices**

32. Konda Tech incorporates by reference every allegation contained in each and every one of the above paragraphs, as though set forth fully herein.

33. Drs. Markovic and Wang and Flex Logix have systematically misappropriated Konda

Tech IP. This has substantially harmed Konda Tech by Defendants competing against Konda Tech using Konda Tech IP.

34. Flex Logix's tortious behavior, as described above and below in the causes of action listed in this Complaint, all constitute unfair and unlawful business practices pursuant to Business & Professions Code Section 17200, *et seq.*

35. The unlawful conduct described herein has resulted in economic harm to Konda Tech.

36. As a direct and proximate result of their acts mentioned herein, Defendants have received and continue to receive ill-gotten gains belonging to Konda Tech.

37. Konda Tech is entitled to restitution for its losses in an amount to be determined.

38. Because the conduct alleged herein is ongoing, and there is no indication that Defendants will cease their unlawful conduct described herein, Konda Tech requests that this Court enjoin Defendants from further violations of California's laws.

**SECOND CAUSE OF ACTION**

**Infringement of U.S. Patent No. 8,269,523**

39. Konda Tech incorporates by reference every allegation contained in each and every one of the above paragraphs, as though set forth fully herein.

40. The '523 patent, entitled "VLSI Layouts of Fully Connected Generalized Networks," was duly and lawfully issued by the United States Patent and Trademark Office ("USPTO") on September 18, 2012. A true and correct copy of the '523 patent is attached to this First Amended Complaint as Exhibit 4.

41. Konda Tech is the owner of all rights, title, and interest in the '523 patent, including the right to bring this suit for injunctive relief and damages.

42. Konda Tech has the exclusive right to make, use, sell, and offer to sell any product embodying the '523 patent throughout the United States, and to import any product embodying the '523 patent into the United States.

43. Konda Tech has commercially exploited the '523 patent by licensing the underlying technology claimed in the '523 patent to companies who, like Flex Logix, wish to make use of Dr. Konda's inventions disclosed in the '523 patent.

44. The ’523 patent is valid and enforceable.

45. Upon information and belief, Flex Logix has had knowledge of Dr. Konda, the Konda Tech IP, the ’523 patent, and Konda Tech’s commercial exploitation of the ’523 patent at least as early as the issuance of the ’523 patent.

46. Flex Logix has been aware of the ’523 patent since at least as early as the filing of the original Complaint.

47. Flex Logix has infringed, and continues to infringe, literally and/or through the doctrine of equivalents, one or more claims of the ’523 patent, including but not limited to claim 1, pursuant to 35 U.S.C. § 271(a), by making, using, selling, offering to sell, and/or importing within the United States, without authority, the EFLX100, EFLX2.5K, EFLX4K, and EFLX150 Gen 2, EFLX4K Gen 2 (“Flex Logix’s Accused Products”). *See* Exhibit 9 for a list of these products.

48. Flex Logix’s Accused Products are integrated circuit devices comprising a plurality of sub-integrated circuit blocks and a routing network. Flex Logix’s manufacture, importation, use, offer for sale, and/or sale infringed and continues to infringe at least claim 1 of the ’523 patent for at least the following reasons:

49. Flex Logix’s Accused Products are eFPGA manufactured as integrated circuit devices. *See* Exhibit 10**,** Figure 2 on page 5 for Flex Logix interconnect architecture.

50. Flex Logix’s Accused Products have a plurality of sub-integrated circuit blocks (LUTs or Reconfigurable Buliding Blocks or RBBs) and a routing network (switch matrices), and said each plurality of sub-integrated circuit blocks comprising a plurality of inlet links and a plurality of outlet links. The EFLX100 (*See* Exhibit 11) consists of 120 LUTs (which are sub-integrated circuit blocks) such that each LUT corresponds to a switch matrix and 120 LUTs arranged in a 2D-grid of 12*10 size. Similarly, the EFLX2.5K is arranged in 50*50 size. The EFLX4K is arranged in 64*64 size. *See* Exhibit 10**,** Figure 2 on page 5 for Flex Logix interconnect architecture. *See* Exhibit 10**,** on page 6 at Figure 3 illustrates the EFLX200K comprises 50 (in a 7 * 7 grid) EFLX4K IP Core. *See* Exhibit 10**,** on page 1, in the first table corresponding to Flex Logix’s interconnect design approach denoted as “Mixed-radix Hierarchical-Mesh”. *See* Exhibit 12**,** same pages 8 – 10 and page 27. *See* Exhibit 13, page 2 and page 4, 7x7 Array of 114, 240 6-LUTs (~183K LUT4s) and 560 22x22 MACs. *See* Exhibit 14 which

describes the EFLX4K IP Core Gen 2 with LUT6 and Global Foundries. *See* Exhibit 9 which discloses all of Flex Logix's Accused Products. Each tile in each of the above Flex Logix's Accused Products infringes, as well as any group of tiles in each of the above Flex Logix's Accused Products infringes this claim. Also, any subset of a tile in each of the above Flex Logix's Accused Products infringes this claim.

51. Flex Logix's Accused Products with said routing network comprising a plurality of stages y, in each said sub-integrated circuit block, starting from the lowest stage of 1 to the highest stage of y, where $y \geq 1$. Each switch matrix of the EFLX100 consists of several stages of mixed radix and each stage implemented by switches. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect. Similarly, each switch matrix in all Flex Logix's Accused Products comprises several stages of mixed radix and each stage implemented by switches.

52. Flex Logix's Accused Products with said routing network comprising a plurality of switches of size $d \times d$, where $d \geq 2$, in each said stage and each said switch of size $d \times d$ having d inlet links and d outlet links. Each switch matrix of the EFLX100 consists of several stages of mixed radix and each stage is implemented by switches of size $d \times d$, where $d \geq 2$. *See* Exhibit 10**,** Figure 2 on page #5 for Flex Logix interconnect architecture. Similarly, each switch matrix in all Flex Logix's Accused Products comprises several stages of mixed radix and each stage implemented by switches.

53. Flex Logix's Accused Products with said plurality of outlet links of said each sub-integrated circuit block are directly connected to said inlet links of said switches of its corresponding said lowest stage of 1, and said plurality of inlet links of said each sub-integrated circuit block are directly connected from said outlet links of said switches of its corresponding said lowest stage of 1. Each switch matrix of the EFLX100 consists of a plurality of outlet links of said each sub-integrated circuit block directly connected to said inlet links of said switches of its corresponding said lowest stage of 1, and said plurality of inlet links of said each sub-integrated circuit block are directly connected from said outlet links of said switches of its corresponding said lowest stage of 1. *See* Exhibit 10**,** Figure 2 on page #5 for Flex Logix interconnect architecture. Similarly, in all Flex Logix's Accused Products.

54. Flex Logix's Accused Products with said each sub-integrated circuit block comprising a plurality of forward connecting links connecting from switches in a lower stage to switches in its immediate succeeding higher stage, and also comprising a plurality of backward connecting links

connecting from switches in a higher stage to switches in its immediate preceding lower stage. Each switch matrix of the EFLX100 consists of a plurality of forward connecting links connecting from switches in a lower stage to switches in its immediate succeeding higher stage, and also comprising a plurality of backward connecting links connecting from switches in a higher stage to switches in its immediate preceding lower stage. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect architecture. Similarly, in all Flex Logix's Accused Products.

55. Flex Logix's Accused Products with said each sub-integrated circuit block comprising a plurality straight links in said forward connecting links from switches in said each lower stage to switches in its immediate succeeding higher stage and a plurality of cross links in said forward connecting links from switches in said each lower stage to switches in its immediate succeeding higher stage, and further comprising a plurality of straight links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage and a plurality of cross links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage. Each switch matrix in the EFLX100 consists of a plurality of straight links in said forward connecting links from switches in said each lower stage to switches in its immediate succeeding higher stage and a plurality of cross links in said forward connecting links from switches in said each lower stage to switches in its immediate succeeding higher stage, and further comprising a plurality of straight links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage and a plurality of cross links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect. Similarly, in all Flex Logix's Accused Products.

56. Flex Logix's Accused Products with said plurality of sub-integrated circuit blocks arranged in a two-dimensional grid of rows and columns. In the EFLX100 said plurality of switch matrices arranged in a two-dimensional grid of rows and columns. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect architecture. Similarly, in all Flex Logix's Accused Products.

57. Flex Logix's Accused Products with said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated

circuit block; and said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks which are either placed vertically above or below, or placed horizontally to the left or to the right. In the EFLX100, said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks which are either placed vertically above or below, or placed horizontally to the left or to the right., *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect architecture. Similarly, in all Flex-Logix Accused Products.

58. Flex Logix's Accused Products with each said plurality of sub-integrated circuit blocks comprising same number of said stages and said switches in each said stage, regardless of the size of said two-dimensional grid so that each said plurality of sub-integrated circuit block with its corresponding said stages and said switches in each stage is replicable in both vertical direction or horizontal direction of said two-dimensional grid. In the EFLX100 each said plurality of sub-integrated circuit blocks comprising same number of said stages and said switches in each said stage, regardless of the size of said two-dimensional grid so that each said plurality of sub-integrated circuit block with its corresponding said stages and said switches in each stage is replicable in both vertical direction or horizontal direction of said two-dimensional grid. See Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect architecture. Similarly, in all Flex Logix's Accused Products.

59. To the extent Flex Logix's Accused Products, without more, do not directly infringe at least claim 1 of the '523 patent, Flex Logix contributes to infringement of the same under 35 U.S.C. § 271(c) inasmuch as the Flex Logix's Accused Products offered for sale and sold by Flex Logix are each a component of a patented machine or an apparatus used in practicing a patented process, constituting a material part of the claimed invention, knowing the same to be especially made or especially adapted for use in infringement of the '523 patent.

60. Flex Logix actively encourages its customers to use Flex Logix's Accused Products in an infringing manner. For example, Flex Logix's website is replete with written directions instructing users on how to use Flex Logix's Accused Products in an infringing manner. Flex Logix's website also touts the identities of customers who use Flex Logix's Accused Products, including without limitation The

Boeing Company, each of whom is a direct infringer inasmuch as they use Flex Logix's Accused Products in the infringing manner as instructed by Flex Logix (*Also See* Exhibits 9-14).

61. Upon information and belief, and particularly by way of the detailed documentation instructing users on how to use Flex Logix's Accused Products in an infringing manner, Flex Logix has encouraged this infringement with knowledge of the '523 patent and with a specific intent to cause their users to infringe.

62. Flex Logix's acts thus constitute active inducement of patent infringement in violation of 35 U.S.C. § 271(b).

63. Flex Logix will continue to infringe, induce infringement of, and contribute to the infringement of, the '523 patent unless enjoined.

64. Flex Logix's infringement has irreparably harmed Konda Tech.

65. Flex Logix will continue to irreparably harm Konda Tech unless enjoined.

66. Pursuant to 35 U.S.C. § 284, Konda Tech is entitled to damages adequate to compensate for the infringement but in no event less than a reasonable royalty.

67. Flex Logix's infringement of the '523 patent has been willful and deliberate and, pursuant to 35 U.S.C. § 284, Konda Tech is entitled to treble damages.

68. This case is "exceptional" within the meaning of 35 U.S.C. § 285, and Konda Tech is entitled to an award of attorneys' fees.

**THIRD CAUSE OF ACTION**

**Infringement of U.S. Patent No. 8,898,611**

69. Konda Tech incorporates by reference every allegation contained in each and every one of the above paragraphs, as though set forth fully herein.

70. The '611 patent, entitled "VLSI Layouts of Fully Connected Generalized and Pyramid Networks with Locality Exploitation," was duly and lawfully issued by the USPTO on November 25, 2014. A true and correct copy of the '611 patent is attached to this First Amended Complaint as Exhibit 5.

71. Konda Tech is the owner of all rights, title, and interest in the '611 patent, including the right to bring this suit for injunctive relief and damages.

72. Konda Tech has the exclusive right to make, use, sell, and offer to sell any product embodying the ’611 patent throughout the United States, and to import any product embodying the ’611 patent into the United States.

73. Konda Tech has commercially exploited the ’611 patent by licensing the underlying technology to companies who, like Flex Logix, wish to make use of Dr. Konda’s inventions disclosed in the ’611 patent.

74. The ’611 patent is valid and enforceable.

75. Upon information and belief, Flex Logix has had knowledge of Dr. Konda, the Konda Tech IP, the ’611 patent, and Konda Tech’s commercial exploitation of the ’611 patent at least as early as the issuance of the ’611 patent.

76. Flex Logix has been aware of the ’611 patent since at least as early as the filing of the original Complaint.

77. Flex Logix has infringed, and continues to infringe, literally and/or through the doctrine of equivalents, one or more claims of the ’611 patent, including but not limited to claim 1, pursuant to 35 U.S.C. § 271(a), by making, using, selling, offering to sell, and/or importing within the United States, without authority, the EFLX100, EFLX2.5K, EFLX4K, EFLX150 Gen 2, and EFLX4K Gen 2 (“Flex Logix’s Accused Products”). *See* Exhibit 9 for a list of these products.

78. Flex Logix’s Accused Products have an electrical network on an electrical substrate. Flex Logix infringes at least claim 1 of the ’611 patent for at least the following reasons:

79. Flex Logix’s Accused Products are eFPGA manufactured as integrated circuit devices. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect architecture.

80. Flex Logix’s Accused Products have an electrical network on an electrical substrate comprising a plurality of sub-networks (switch matrices) corresponding to blocks arranged in a two dimensional layout for a total of $a \times b$ said sub-networks with one side of said layout having the size of $a$ sub-networks and the other side of said layout having the size of $b$ sub-networks where $a \geq 1$ and $b \geq 1$. The EFLX100 (*See* Exhibit 11) consists of 120 LUTs (which are blocks) and 120 LUTs having corresponding switch matrices arranged in a 2D-grid of 12*10 size where a = 12 and b = 10. Similarly, the EFLX2.5K is arranged in 50*50 size where a = 50 and b = 50. The EFLX4K is arranged in 64*64

size where a = 64 and b = 64. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect architecture. *See* Exhibit 10, on page 6 at Figure 3 which illustrates the EFLX200K comprises 50 (in a 7 * 7 grid) EFLX4K IP Core, where a = 448 and b = 448. *See* Exhibit 10, on page 1, in the first table corresponding to Flex Logix's interconnect design approach denoted as "Mixed-radix Hierarchical-Mesh". *See* Exhibit 12, same pages 8 – 10 and page 27. *See* Exhibit 13, page 2 and page 4, 7x7 Array of 114, 240 6-LUTs (~183K LUT4s) and 560 22x22 MACs. *See* Exhibit 14 which describes the EFLX4K IP Core Gen 2 with LUT6 and Global Foundries. *See* Exhibit 9 which discloses all of Flex Logix's Accused Products**.** Each tile in each of the above Flex Logix's Accused Products infringes, as well as any group of tiles in each of the above Flex Logix's Accused Products infringes this claim. Also, any subset of a tile in each of the above Flex Logix's Accused Products infringes this claim.

81. Flex Logix's Accused Products have said electrical network on an electrical substrate comprising at most $N_1$ inlet links and at most $N_2$ outlet links where $N_1 > 1$ and $N_2 > 1$ wherein either $N_2 = N_1 \times p_2$, $N_1 = (a \times b) \times p$, and said each sub-network comprising at most $p$ inlet links and at most $p \times p_2$ outlet links; or $N_1 = N_2 \times p_1$, $N_2 = (a \times b) \times p$, and said each sub-network comprising at most $p$ outlet links and at most $p \times p_1$ inlet links. The EFLX100 consists of inlet and outlet links with a = 10 and b = 10, LUT4 having 4 inputs and 2 outputs, p = 2, $N_1$ = 400 and $N_2$ = 200. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect. Similarly, each switch matrix in all Flex Logix's Accused Products.

82. Flex Logix's Accused Products have said each sub-network comprising at most $y$ stages, starting from the lowest stage of 1 to the highest stage of $y$, where $y \geq 1$. Each switch matrix (sub-network) of the EFLX100 consists of several stages of mixed radix and each stage implemented by switches. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect. Similarly, each switch matrix in all of Flex Logix's Accused Products comprises several stages of mixed radix and each stage implemented by switches.

83. Flex Logix's Accused Products have said each stage comprising at least one switch of size $d \times d$, where $d \geq 2$ and each said switch of size $d \times d$ having $d$ incoming links and $d$ outgoing links. Each stage of each switch matrix of the EFLX100 consists of several stages of mixed radix and each stage is implemented by switches of size $d \times d$, where $d \geq 2$. *See* Exhibit 10**,** Figure 2 on page #5

for Flex Logix interconnect architecture. Similarly, each switch matrix in all of Flex Logix's Accused Products comprises several stages of mixed radix and each stage implemented by switches.

84. Flex Logix's Accused Products have said each sub-network may not be comprising the same number of said inlet links and may not be comprising the same number of said outlet links; said each sub-network may not be comprising the same number of said stages; said each stage may not be comprising the same number of switches; and said each switch in said each stage may not be of the same size $d$ . The EFLX100 consists of LUTs, DSPs, and Block RAM and so have said differences. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect architecture. Similarly, each switch matrix in all of Flex Logix's Accused Products.

85. Flex Logix's Accused Products have said incoming links and said outgoing links in each said switch in said each stage of said each sub-network comprising a plurality of forward connecting links connecting from switches in lower stage to said switches one of succeeding higher stages, and also comprising a plurality of backward connecting links connecting from said switches in higher stage to said switches one of preceding lower stage. The EFLX100 consists of said incoming links and said outgoing links in each said switch in said each stage of said each switch matrix comprising a plurality of forward connecting links connecting from switches in lower stage to said switches one of succeeding higher stages, and also comprising a plurality of backward connecting links connecting from said switches in higher stage to said switches one of preceding lower stage. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect architecture. Similarly, in all of Flex Logix's Accused Products.

86. Flex Logix's Accused Products have said forward connecting links comprising a plurality of straight links connecting from a said switch in a said stage in a said sub-network to a said switch in another stage in the same said sub-network and also comprising a plurality of cross links connecting from a said switch in a said stage in a sub-network to a said switch in another said stage in a different said sub-network. The EFLX100 consists of said forward connecting links comprising a plurality of straight links connecting from a said switch in a said stage in a said switch matrix to a said switch in another stage in the same said switch matrix and also comprising a plurality of cross links connecting from a said switch in a said stage in a switch matrix to a said switch in another said stage in a different said switch matrix. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect architecture.

Similarly, in all of Flex Logix's Accused Products.

87. Flex Logix's Accused Products have said backward connecting links comprising a plurality of straight links connecting from a said switch in a said stage in a said sub-network to a said switch in another said stage in the same said sub-network and also comprising a plurality of cross links connecting from a said switch in a said stage in a said sub-network to a said switch in another said stage in a different said sub-network. The EFLX100 consists of said backward connecting links comprising a plurality of straight links connecting from a said switch in a said stage in a said switch matrix to a said switch in another said stage in the same said switch matrix and also comprising a plurality of cross links connecting from a said switch in a said stage in a said switch matrix to a said switch in another said stage in a different said switch matrix. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect architecture. Similarly, in all of Flex Logix's Accused Products.

88. Flex Logix's Accused Products have said all cross links are connecting as either vertical or horizontal links between said switches between each two different said sub-networks, which are either placed vertically above or below, or placed horizontally to the left or to the right. The EFLX100 consists of all cross links are connecting as either vertical or horizontal links between said switches between each two different said switch matrices, which are either placed vertically above or below, or placed horizontally to the left or to the right. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect architecture. Similarly, in all of Flex Logix's Accused Products.

89. To the extent Flex Logix's Accused Products, without more, do not directly infringe at least claim 1 of the '611 patent, Flex Logix contributes to infringement of the same under 35 U.S.C. § 271(c) inasmuch as Flex Logix's Accused Products offered for sale and sold by Flex Logix are each a component of a patented machine or an apparatus used in practicing a patented process, constituting a material part of the claimed invention, knowing the same to be especially made or especially adapted for use in infringement of the '611 patent.

90. Flex Logix actively encourages its customers to use Flex Logix's Accused Products in an infringing manner. For example, Flex Logix's website is replete with written directions instructing users on how to use Flex Logix's Accused Products in an infringing manner. Flex Logix's website also touts the identities of customers who use Flex Logix's Accused Products, including without limitation The

Boeing Company, each of whom is a direct infringer inasmuch as they use Flex Logix's Accused Products in the infringing manner as instructed by Flex Logix (*Also See* Exhibits 9-14).

91. Upon information and belief, and particularly by way of the detailed documentation instructing users on how to use Flex Logix's Accused Products in an infringing manner, Flex Logix has encouraged this infringement with knowledge of the '611 patent and with a specific intent to cause their users to infringe.

92. Flex Logix's acts thus constitute active inducement of patent infringement in violation of 35 U.S.C. § 271(b).

93. Flex Logix will continue to infringe, induce infringement of, and contribute to the infringement of, the '611 patent unless enjoined.

94. Flex Logix's infringement has irreparably harmed Konda Tech.

95. Flex Logix will continue to irreparably harm Konda Tech unless enjoined.

96. Pursuant to 35 U.S.C. § 284, Konda Tech is entitled to damages adequate to compensate for the infringement but in no event less than a reasonable royalty.

97. Flex Logix's infringement of the '611 patent has been willful and deliberate and, pursuant to 35 U.S.C. § 284, Konda Tech is entitled to treble damages.

98. This case is "exceptional" within the meaning of 35 U.S.C. § 285, and Konda Tech is entitled to an award of attorneys' fees.

**FOURTH CAUSE OF ACTION**

**Infringement of U.S. Patent No. 9,529,958**

99. Konda Tech incorporates by reference every allegation contained in each and every one of the above paragraphs, as though set forth fully herein.

100. The '958 patent, entitled "VLSI Layouts of Fully Connected Generalized and Pyramid Networks with Locality Exploitation," was duly and lawfully issued by the USPTO on December 27, 2016. A true and correct copy of the '958 patent is attached to this First Amended Complaint as Exhibit 6.

101. Konda Tech is the owner of all rights, title, and interest in the '958 patent, including the right to bring this suit for injunctive relief and damages.

102. Konda Tech has the exclusive right to make, use, sell, and offer to sell any product embodying the ’958 patent throughout the United States, and to import any product embodying the ’958 patent into the United States.

103. Konda Tech has commercially exploited the ’958 patent by licensing the underlying technology to companies who, like Flex Logix, wish to make use of Dr. Konda’s inventions disclosed in the ’958 patent.

104. The ’958 patent is valid and enforceable.

105. Upon information and belief, Flex Logix has had knowledge of Dr. Konda, the Konda Tech IP, the ’958 patent, and Konda Tech’s commercial exploitation of the ’958 patent at least as early as the issuance of the ’958 patent.

106. Flex Logix has been aware of the ’958 patent since at least as early as the filing of the original Complaint.

107. Flex Logix has infringed, and continues to infringe, literally and/or through the doctrine of equivalents, one or more claims of the ’958 patent, including but not limited to claim 1, pursuant to 35 U.S.C. § 271(a), by making, using, selling, offering to sell, and/or importing within the United States, without authority, the EFLX100, EFLX2.5K, EFLX4K, EFLX150 Gen 2, and EFLX4K Gen 2 (“Flex Logix’s Accused Products”). *See* Exhibit 9 for a list of these products.

108. Flex Logix’s Accused Products have a two-dimensional layout of hierarchical routing network implemented in a non-transitory medium. Flex Logix infringes at least claim 1 of the ’958 patent for at least the following reasons:

109. Flex Logix’s Accused Products are eFPGA manufactured as integrated circuit devices. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect architecture.

110. Flex Logix’s Accused Products have a total of $a \times b$ blocks with one side of said layout having the size of “$a$” blocks and the other side of said layout having the size of “$b$” blocks where $a \geq 1$and $b \geq 1$. The EFLX100 (*See* Exhibit 11) consists of 120 LUTs (which are blocks) and 120 LUTs arranged in a 2D-grid of 12*10 size where a = 12 and b = 10. Similarly, the EFLX2.5K is arranged in 50*50 size where a = 50 and b = 50. The EFLX4K is arranged in 64*64 size where a = 64 and b = 64. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect architecture. *See* Exhibit 10 on page 6

at Figure 3 which illustrates the EFLX200K comprises 50 (in a 7 * 7 grid) EFLX4K IP Core, where a = 448 and b = 448. *See* Exhibit 10, on page 1, in the first table corresponding to Flex Logix's interconnect design approach denoted as "Mixed-radix Hierarchical-Mesh". *See* Exhibit 12, same pages 8 – 10 and Page 27. *See* Exhibit 13, page 2 and page 4, 7x7 Array of 114, 240 6-LUTs (~183K LUT4s) and 560 22x22 MACs. *See* Exhibit 14 which describes the EFLX4K IP Core Gen 2 with LUT6 and Global Foundries. *See* Exhibit 9 which discloses all of Flex Logix's Accused Products**.** Each tile in each of the above Flex Logix's Accused Products as well as any group of tiles in each of the above Flex Logix's Accused Products infringes this claim. Also, any subset of a tile in each of the above Flex Logix's Accused Products infringes this claim.

111. Flex Logix's Accused Products have said routing network comprising a total of $N_1$ inlet links and a total of $N_2$ outlet links and $y$ hierarchical stages where $y \geq 1$, $N_1 > 1$ and $N_2 > 1$ wherein either $N_2 = N_1 \times p_2$, $N_1 = (a \times b) \times p$, and said each block comprising at most $p$ inlet links and at most $p \times p_2$ outlet links; or $N_1 = N_2 \times p_1$, $N_2 = (a \times b) \times p$, and said each block comprising at most $p$ outlet links and at most $p \times p_1$ inlet links, where $p \geq 1$, $p_1 \geq 1$ and $p_2 \geq 1$. Each switch matrix (sub-network) of the EFLX100 consists of inlet and outlet links with a = 10 and b = 10, LUT4 having 4 inputs and 2 outputs, p = 2, $N_1$ = 400 and $N_2$ = 200. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect. Similarly, each switch matrix in all of Flex Logix's Accused Products.

112. Flex Logix's Accused products have said each stage comprising at least one switch of size $d \times d$, where $d \geq 2$ and each said switch of size $d \times d$ having $d$ incoming links and $d$ outgoing links. The EFLX100 consists of several stages of mixed radix and each stage implemented by switches where $d \geq 2$. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect. Similarly, each switch matrix in all of Flex Logix's Accused Products comprises several stages of mixed radix and each stage implemented by switches.

113. Flex Logix's Accused Products have said each block may not be comprising the same number of said inlet links and may not be comprising the same number of said out links; said each block may not be comprising the same number of said stages; said each stage may not be comprising the same number of switches; and said each switch in said each stage may not be of the same size $d$, said inlet links directly connected to one or more said incoming links, and said outgoing links directly connected

to one or more said outlet links. The EFLX100 consists of LUTs, DSPs, and Block RAM and so have said differences. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect architecture. Similarly, each switch matrix in all of Flex Logix's Accused Products.

114. Flex Logix's Accused Products have said incoming links and outgoing links in each switch in said each stage of said each block comprising a plurality of forward connecting links connected from switches in lower stage to switches in the immediate succeeding higher stage, and also comprising a plurality of backward connecting links connected from switches in higher stage to switches in the immediate preceding lower stage. The EFLX100 consists of said incoming links and outgoing links in each switch in said each stage of said each block comprising a plurality of forward connecting links connected from switches in lower stage to switches in the immediate succeeding higher stage, and also comprising a plurality of backward connecting links connected from switches in higher stage to switches in the immediate preceding lower stage. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect. Similarly, each switch matrix in all of Flex Logix's Accused Products comprises several stages of mixed radix and each stage implemented by switches.

115. Flex Logix's Accused Products have said forward connecting links comprising a plurality of straight links connected from a switch in a stage in a block to a switch in another stage in the same block and also comprising a plurality of cross links connected from a switch in a stage in a block to a switch in another stage in a different block. The EFLX100 consists of said forward connecting links comprising a plurality of straight links connected from a switch in a stage in a block to a switch in another stage in the same block and also comprising a plurality of cross links connected from a switch in a stage in a block to a switch in another stage in a different block. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect. Similarly, each switch matrix in all of Flex Logix's Accused Products comprises several stages of mixed radix and each stage implemented by switches.

116. Flex Logix's Accused Products have said backward connecting links comprising a plurality of straight links connected from a switch in a stage in a block to a switch in another stage in the same block and also comprising a plurality of cross links connected from a switch in a stage in a block to a switch in another stage in a different block. The EFLX100 consists of said backward connecting links comprising a plurality of straight links connected from a switch in a stage in a block to a switch in

another stage in the same block and also comprising a plurality of cross links connected from a switch in a stage in a block to a switch in another stage in a different block. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect. Similarly, each switch matrix in all of Flex Logix's Accused Products comprises several stages of mixed radix and each stage implemented by switches.

117. Flex Logix's Accused Products have said all cross links are connected as either vertical or horizontal links between switches in two different said blocks. The EFLX100 consists of said all cross links are connected as either vertical or horizontal links between switches in two different said blocks. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect. Similarly, each switch matrix in all of Flex Logix's Accused Products comprises several stages of mixed radix and each stage implemented by switches.

118. To the extent Flex Logix's Accused Products, without more, do not directly infringe at least claim 1 of the '958 patent, Flex Logix contributes to infringement of the same under 35 U.S.C. § 271(c) inasmuch as Flex Logix's Accused Products offered for sale and sold by Flex Logix are each a component of a patented machine or an apparatus used in practicing a patented process, constituting a material part of Dr. Konda's invention, knowing the same to be especially made or especially adapted for use in infringement of the '958 patent.

119. Flex Logix actively encourages its customers to use Flex Logix's Accused Products in an infringing manner. For example, Flex Logix's website is replete with written directions instructing users on how to use Flex Logix's Accused Products in an infringing manner. Flex Logix's website also touts the identities of customers who use Flex Logix's Accused Products, including without limitation The Boeing Company, each of whom is a direct infringer inasmuch as they use Flex Logix's Accused Products in the infringing manner as instructed by Flex Logix (*Also See* Exhibits 9-14).

120. Upon information and belief, and particularly by way of the detailed documentation instructing users on how to use Flex Logix's Accused Products in an infringing manner, Flex Logix has encouraged this infringement with knowledge of the '958 patent and with a specific intent to cause their users to infringe.

121. Flex Logix's acts thus constitute active inducement of patent infringement in violation of 35 U.S.C. § 271(b).

122. Flex Logix will continue to infringe, induce infringement of, and contribute to the infringement of, the ’958 patent unless enjoined.

123. Flex Logix’s infringement has irreparably harmed Konda Tech.

124. Flex Logix will continue to irreparably harm Konda Tech unless enjoined.

125. Pursuant to 35 U.S.C. § 284, Konda Tech is entitled to damages adequate to compensate for the infringement but in no event less than a reasonable royalty.

126. Flex Logix’s infringement of the ’958 patent has been willful and deliberate and, pursuant to 35 U.S.C. § 284, Konda Tech is entitled to treble damages.

127. This case is “exceptional” within the meaning of 35 U.S.C. § 285, and Konda Tech is entitled to an award of attorneys’ fees.

**FIFTH CAUSE OF ACTION**

**Infringement of U.S. Patent No. 10,003,553**

128. Konda Tech incorporates by reference every allegation contained in each and every one of the above paragraphs, as though set forth fully herein.

129. The ’553 patent, entitled “Optimization of Multi-stage Hierarchical Networks for Practical Routing Applications,” was duly and lawfully issued by the USPTO on June 19, 2018. A true and correct copy of the ’553 patent is attached to this First Amended Complaint as Exhibit 7.

130. Konda Tech is the owner of all rights, title, and interest in the ’553 patent, including the right to bring this suit for injunctive relief and damages.

131. Konda Tech has the exclusive right to make, use, sell, and offer to sell any product embodying the ’553 patent throughout the United States, and to import any product embodying the ’553 patent into the United States.

132. Konda Tech has commercially exploited the ’553 patent by licensing the underlying technology to companies who, like Flex Logix, wish to make use of Dr. Konda’s inventions disclosed in the ’553 patent.

133. The ’553 patent is valid and enforceable.

134. Upon information and belief, Flex Logix has had knowledge of Dr. Konda, the Konda Tech IP, the ’553 patent, and Konda Tech’s commercial exploitation of the ’553 patent at least as early

as the issuance of the ’553 patent.

135. Flex Logix has been aware of the ’553 patent since at least as early as the filing of the original Complaint.

136. Flex Logix has infringed, and continues to infringe, literally and/or through the doctrine of equivalents, one or more claims of the ’553 patent, including but not limited to claim 1, pursuant to 35 U.S.C. § 271(a), by making, using, selling, offering to sell, and/or importing within the United States, without authority, the EFLX100, EFLX2.5K, EFLX4K, EFLX150 Gen 2, and EFLX4K Gen 2 (“Flex Logix’s Accused Products”). *See* Exhibit 9 for a list of these products.

137. Flex Logix’s Accused Products have a network implemented in a non-transitory medium comprising a plurality of subnetworks and a plurality of inlet links and a plurality of outlet links. Flex Logix infringes at least claim 1 of the ’553 patent for at least the following reasons:

138. Flex Logix’s Accused Products are eFPGA manufactured as integrated circuit devices. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect architecture.

139. Flex Logix’s Accused Products have a network implemented in a non-transitory medium comprising a plurality of subnetworks and a plurality of inlet links and a plurality of outlet links, said plurality of subnetworks arranged in a two-dimensional grid of rows and columns. The EFLX100 (*See* Exhibit 11) consists of 120 LUTs (which are sub-integrated circuit blocks) such that each LUT corresponds to a switch matrix and 120 LUTs arranged in a 2D-grid of 12*10 size. Similarly, the EFLX2.5K is arranged in 50*50 size. The EFLX4K is arranged in 64*64 size. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect architecture. *See* Exhibit 10, on page 6 at Figure 3 illustrates the EFLX200K comprises 50 (in a 7 * 7 grid) EFLX4K IP Core. *See* Exhibit 10, on page 1, in the first table corresponding to Flex Logix’s interconnect design approach denoted as “Mixed-radix Hierarchical-Mesh”. *See* Exhibit 12, same pages 8 – 10 and page 27. *See* Exhibit 13, page 2 and page 4, 7x7 Array of 114, 240 6-LUTs (~183K LUT4s) and 560 22x22 MACs. Refer to Exhibit 14 which describes the EFLX4K IP Core Gen 2 with LUT6 and Global Foundries. *See* Exhibit 9 which discloses all of Flex Logix’s Accused Products**.** Each tile in each of the above Flex Logix’s Accused Products infringes as well as any group of tiles in each of the above Flex Logix’s Accused Products infringes this claim. Also, any subset of a tile in each of the above Flex Logix’s Accused Products infringes this claim.

140. Flex Logix's Accused Products have each subnetwork comprising y stages, where $y \geq 1$; and each stage comprising a switch of size $d_i \times d_0$, where $d_i \geq 2$ and $d_o \geq 2$ and each switch of size $d_i \times d_0$ having $d_i$ incoming links and $d_0$ outgoing links. Each switch matrix (sub-network) of the EFLX100 consists of comprising y stages, where y.gtoreq.1; and each stage comprising a switch of size $d_i \times d_0$, where $d_i \geq 2$ and $d_o \geq 2$ and each switch of size $d_i \times d_0$ having $d_i$ incoming links and $d_0$ outgoing links . *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect. Similarly, each switch matrix in all of Flex Logix's Accused Products.

141. Flex Logix's Accused Products have said inlet links are connected to one or more of said incoming links of a said switch of a said stage of a said subnetwork, and said outlet links are connected to one of said outgoing links of a said switch of a said stage of a said subnetwork. The EFLX100 consists of said inlet links are connected to one or more of said incoming links of a said switch of a said stage of a said subnetwork, and said outlet links are connected to one of said outgoing links of a said switch of a said stage of a said subnetwork. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect. Similarly, each switch matrix in all of Flex Logix's Accused Products.

142. Flex Logix's Accused Products have each subnetwork of the plurality of subnetworks may or may not be comprising the same number of said inlet links and may or may not be comprising the same number of said outlet links; each subnetwork of the plurality of subnetworks may or may not be comprising the same number of said stages; each stage may or may not be comprising the same number of switches; and each switch in each stage may or may not be of the same size, each multiplexer in each stage may or may not be of the same size and said incoming links and outgoing links in each switch in each stage of each subnetwork comprising a plurality of forward connecting links connected from switches in a stage to switches in another stage in same said subnetwork or another said subnetwork, and also comprising a plurality of backward connecting links connected from switches in a stage to switches in another stage in same subnetwork or another said subnetwork. The EFLX100 consists of LUTs, DSPs, and Block RAM and so have said differences. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect architecture. Similarly, each switch matrix in all of Flex Logix's Accused Products.

143. Flex Logix's Accused Products have said forward connecting links comprising zero or

more straight links connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in one or more other subnetworks. The EFLX100 consists of said forward connecting links comprising zero or more straight links connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in one or more other subnetworks. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect. Similarly, each switch matrix in all of Flex Logix's Accused Products.

144. Flex Logix's Accused Products have said backward connecting links comprising zero or more straight links connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork; and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in one or more other subnetworks. The EFLX100 consists of said backward connecting links comprising zero or more straight links connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork; and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in one or more other subnetworks. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect. Similarly, each switch matrix in all of Flex Logix's Accused Products.

145. To the extent Flex Logix's Accused FPGA Devices, without more, do not directly infringe at least claim 1 of the '553 patent, Flex Logix contributes to infringement of the same under 35 U.S.C. § 271(c) inasmuch as the Infringing Products offered for sale and sold by Flex Logix are each a component of a patented machine or an apparatus used in practicing a patented process, constituting a material part of Konda's invention, knowing the same to be especially made or especially adapted for use in infringement of the '553 patent.

146. Flex Logix actively encourages its customers to use the Accused FPGA Devices in an infringing manner. For example, Flex Logix's website is replete with written directions instructing users on how to use the Accused FPGA Devices in an infringing manner. Flex Logix's website also touts the identities of customers who use the Accused FPGA Devices, including without limitation The Boeing Company, each of whom is a direct infringing inasmuch as they use the Accused FPGA Devices in the

infringing manner as instructed by Flex Logix (*Also See* Exhibits 9-14).

147. Upon information and belief, and particularly by way of the detailed documentation instructing users on how to use the Accused FPGA Devices in an infringing manner, Flex Logix has encouraged this infringement with knowledge of the ’553 patent and with a specific intent to cause their users to infringe.

148. Flex Logix’s acts thus constitute active inducement of patent infringement in violation of 35 U.S.C. § 271(b).

149. Flex Logix will continue to infringe, induce infringement of, and contribute to the infringement of, the ’553 patent unless enjoined.

150. Flex Logix’s infringement has irreparably harmed Konda Tech.

151. Flex Logix will continue to irreparably harm Konda Tech unless enjoined.

152. Pursuant to 35 U.S.C. § 284, Konda Tech is entitled to damages adequate to compensate for the infringement but in no event less than a reasonable royalty.

153. Flex Logix’s infringement of the ’553 patent has been willful and deliberate and, pursuant to 35 U.S.C. § 284, Konda Tech is entitled to treble damages.

154. This case is “exceptional” within the meaning of 35 U.S.C. § 285, and Konda Tech is entitled to an award of attorneys’ fees.

**SIXTH CAUSE OF ACTION**

**Infringement of Patent No. 10,050,904**

155. Konda Tech incorporates by reference every allegation contained in each and every one of the above paragraphs, as though set forth fully herein.

156. The ’904 patent, entitled “VLSI Layouts of Fully Connected Generalized and Pyramid Networks with Locality Exploitation,” was duly and lawfully issued on August 14, 2018. A true and correct copy of the ’904 patent is attached to this First Amended Complaint as Exhibit 8.

157. Konda Technologies is the owner of all rights, title, and interest in the ’904 patent, including the right to bring this suit for injunctive relief and damages.

158. Konda Tech has the exclusive right to make, use, sell, and offer to sell any product embodying the ’904 patent throughout the United States, and to import any product embodying the ’904

patent into the United States.

159. Konda Tech has commercially exploited the ’904 patent by licensing the underlying technology to companies who, like Flex Logix, wish to make use of Dr. Konda’s inventions disclosed in the ’904 patent.

160. The ’904 patent is valid and enforceable.

161. Upon information and belief, Flex Logix has had knowledge of Konda, the Konda Tech IP, the ’904 patent, and Konda Tech’s commercial exploitation of the ’904 patent at least as early as the issuance of the ’904 patent.

162. Flex Logix has been aware of the ’904 patent since at least as early as the filing of this Complaint.

163. Flex Logix have infringed, and continue to infringe, literally and/or through the doctrine of equivalents, one or more claims of the ’904 patent, including but not limited to claim 1, pursuant to 35 U.S.C. § 271(a), by making, using, selling, offering to sell, and/or importing within the United States, without authority, the EFLX100, EFLX2.5K, EFLX4K, EFLX150 Gen 2, EFLX4K Gen 2 (“Flex Logix’s Accused Products”). Refer to Exhibit 9 for a list of these products.

164. Flex Logix’s Accused Products infringe at least claim 1 of the ’904 patent for at least the following reasons:

165. Flex Logix’s Accused Products are eFPGA manufactured as integrated circuit devices. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect architecture.

166. Flex Logix’s Accused FPGA Devices have a programmable integrated circuit device comprising a plurality of programmable logic blocks and a network, and said plurality of programmable logic blocks comprising a plurality of inlet links and a plurality of outlet links; and said network further comprising a plurality of subnetworks and with each subnetwork coupled with at least one of said plurality of programmable logic blocks; and, said plurality of subnetworks coupled with said plurality of programmable logic blocks arranged in a two-dimensional grid of rows and columns. EFLX100 (*See* Exhibit 11) consists of 120 LUTs (which are programmable logic blocks) such that each LUT corresponds to a switch matrix and 120 LUTs arranged in a 2D-grid of 12*10 size. Similarly, the EFLX2.5K is arranged in 50*50 size. The EFLX4K is arranged in 64*64 size. *See* Exhibit 10, Figure 2

on page #5 for Flex Logix interconnect architecture. *See* Exhibit 10, on page 6 at Figure 3 illustrates the EFLX200K comprises 50 (in a 7 * 7 grid) EFLX4K IP Core. Refer to Exhibit 10, on page 1, in the first table corresponding to Flex Logix's interconnect design approach denoted as "Mixed-radix Hierarchical-Mesh".." Refer to Exhibit 12, same pages 8 – 10 and Page 27. *See* Exhibit 13, page 2 and page 4, 7x7 Array of 114, 240 6-LUTs (~183K LUT4s) and 560 22x22 MACs. *See* Exhibit 14 which describes the EFLX4K IP Core Gen 2 with LUT6 and Global Foundries. *See* Exhibit 9 which discloses all of Flex Logix's Accused Products**.** Each tile in each of the above Flex Logix's Accused Products infringes as well as any group of tiles in each of the above Flex Logix's Accused Products infringes this claim. Also, any subset of a tile in each of the above Flex Logix's Accused Products infringes this claim.

167. Flex Logix's Accused Products have each subnetwork comprising *y* stages, where $y > 1$; and each stage comprising a switch of size $d_i \times d_0$, where $d_i \geq 2$ and $d_o \geq 2$ and each switch of size $d_i \times d_0$ having $d_i$ incoming links and $d_0$ outgoing links. Each switch matrix (sub-network) of the EFLX100 consists of each subnetwork (switch matrix) comprising *y* stages, where $y > 1$; and each stage comprising a switch of size $d_i \times d_0$, where $d_i \geq 2$ and $d_o \geq 2$ and each switch of size $d_i \times d_0$ having $d_i$ incoming links and $d_0$ outgoing links . *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect. Similarly, each switch matrix in all of Flex Logix's Accused Products.

168. Flex Logix's Accused Products have said inlet links are connected to one or more of said incoming links of a said switch of a said stage of a said subnetwork, and said outlet links are connected to one of said outgoing links of a said switch of a said stage of a said subnetwork. The EFLX100 consists of each subnetwork comprising said inlet links are connected to one or more of said incoming links of a said switch of a said stage of a said subnetwork, and said outlet links are connected to one of said outgoing links of a said switch of a said stage of a said subnetwork. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect. Similarly, each switch matrix in all of Flex Logix's Accused Products.

169. Flex Logix's Accused Products have each subnetwork of the plurality of subnetworks comprising the same or different number of said inlet links and comprising the same or different number of said outlet links; each subnetwork of the plurality of subnetworks comprising the same or different number of said stages; each stage comprising the same or different number of switches; and each switch

in each stage is of the same size or of different size, each multiplexer in each stage is of the same size or of different size. The EFLX100 consists of LUTs, DSPs, and Block RAM and so have said differences. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect architecture. Similarly, each switch matrix in all of Flex Logix's Accused Products.

170. Flex Logix's Accused Products have said incoming links and outgoing links in each switch in each stage of each subnetwork comprising a plurality of forward connecting links connected from switches in a stage to switches in another stage in same said subnetwork or another said subnetwork, and also comprising a plurality of backward connecting links connected from switches in a stage to switches in another stage in same subnetwork or another said subnetwork. The EFLX100 consists of said incoming links and outgoing links in each switch in each stage of each subnetwork comprising a plurality of forward connecting links connected from switches in a stage to switches in another stage in same said subnetwork or another said subnetwork, and also comprising a plurality of backward connecting links connected from switches in a stage to switches in another stage in same subnetwork or another said subnetwork. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect. Similarly, each switch matrix in all of Flex Logix's Accused Products.

171. Flex Logix's Accused Products have said forward connecting links comprising zero or more straight links connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage or same level stage in another subnetwork. The EFLX100 consists of said forward connecting links comprising zero or more straight links connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage or same level stage in another subnetwork. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect. Similarly, each switch matrix in all of Flex Logix's Accused Products.

172. Flex Logix's Accused Products have said backward connecting links comprising zero or more straight links connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork; and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage or same level stage in another subnetwork. The

EFLX100 consists of said backward connecting links comprising zero or more straight links connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork; and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage or same level stage in another subnetwork. *See* Exhibit 10, Figure 2 on page #5 for Flex Logix interconnect. Similarly, each switch matrix in all of Flex Logix's Accused Products.

173. To the extent Flex Logix's Accused Products, without more, do not directly infringe at least claim 1 of the '904 patent, Flex Logix contributes to infringement of the same under 35 U.S.C. § 271(c) inasmuch as Flex Logix's Accused Products offered for sale and sold by Flex Logix are each a component of a patented machine or an apparatus used in practicing a patented process, constituting a material part of Dr. Konda's invention, knowing the same to be especially made or especially adapted for use in infringement of the '904 patent.

174. Flex Logix actively encourages its customers to use Flex Logix's Accused Products in an infringing manner. For example, Flex Logix's website is replete with written directions instructing users on how to use Flex Logix's Accused Products in an infringing manner. Flex Logix's website also touts the identities of customers who use Flex Logix's Accused Products, including without limitation The Boeing Company, each of whom is a direct infringer inasmuch as they use Flex Logix's Accused Products in the infringing manner as instructed by Flex Logix (*Also See* Exhibits 9-14).

175. Upon information and belief, and particularly by way of the detailed documentation instructing users on how to use the Accused FPGA Devices in an infringing manner, Flex Logix has encouraged this infringement with knowledge of the '904 patent and with a specific intent to cause their users to infringe.

176. Flex Logix's acts thus constitute active inducement of patent infringement in violation of 35 U.S.C. § 271(b).

177. Flex Logix will continue to infringe, induce infringement of, and contribute to the infringement of, the '904 patent unless enjoined.

178. Flex Logix's infringement has irreparably harmed Konda Tech.

179. Flex Logix will continue to irreparably harm Konda Tech unless enjoined.

180. Pursuant to 35 U.S.C. § 284, Konda Tech is entitled to damages adequate to compensate for the infringement but in no event less than a reasonable royalty.

181. Flex Logix's infringement of the '904 patent has been willful and deliberate and, pursuant to 35 U.S.C. § 284, Konda Tech is entitled to treble damages.

182. This case is "exceptional" within the meaning of 35 U.S.C. § 285, and Konda Tech is entitled to an award of attorneys' fees.

**SEVENTH CAUSE OF ACTION**

**Fraud – Intentional Misrepresentation**

183. Konda Tech incorporates by reference every allegation contained in each and every one of the above paragraphs, as though set forth fully herein.

184. Dr. Markovic made false representations that harmed Konda Tech.

185. Dr. Markovic represented to Konda Tech that he would assist Konda Tech to secure funding from UCLA/ITA to fund Konda Tech to bring Konda Tech's IP to the market. Dr. Markovic's representation was false.

186. Dr. Markovic knew that the representation was false when he made it because he knew that UCLA/ITA only funds technologies developed within UCLA. Konda Tech and Konda Tech IP has no affiliation or connection to UCLA and does not qualify for funding by UCLA/ITA.

187. Dr. Markovic intended that Konda Tech rely on the misrepresentation.

188. But for that reliance, Konda Tech would not have shared its proprietary and confidential information with Dr. Markovic.

189. Dr. Markovic subsequently contacted Konda Tech pretending that he would help build Konda Tech by implementing Konda Tech's technology by submitting two DARPA proposals with the promise that 1) if the DARPA proposals were granted, he would obtain a license from Konda Tech; and 2) otherwise if the proposals were rejected by DARPA, he would have his student Dr. Wang undertake the chip implementations and would be used for academic purposes only.

190. Beginning at that time and continuing for years, Dr. Markovic inquired about all details of Konda Tech's technology including the disclosures in the patents-in-suit as well as proprietary implementation details, technical know-how, and business know-how and the then customers and

potential customers and Konda Tech's interaction with them. As a result, Dr. Markovic learned about FPGA business models and the know-how of the FPGA industry with respect to interconnect technology and its historical evolution, all based on the premise that he was helping to get Konda Tech funded.

191. Dr. Markovic always represented to Konda Tech that he was helping Konda Tech get funded. Dr. Markovic intended that Konda Tech rely on his telling Dr. Konda that he was helping Konda Tech so that Konda Tech would provide him with Konda Tech's business plan and technical know-how and customer experience information over a period of years based on his intentionally misrepresenting his true intentions.

192. Dr. Markovic used the information provided by Konda Tech to develop FPGA chips which later became the basis Drs. Markovic and Wang to found Flex Logix.

193. By Flex Logix using Konda Tech IP, Flex Logix has deprived Konda Tech of revenue it would otherwise have received.

194. The unlawful conduct described herein has resulted in economic harm to Konda Tech.

195. As a direct and proximate result of their acts mentioned herein, Defendants have received and continue to receive ill-gotten gains belonging to Konda Tech.

196. Konda Tech is entitled to damages for its losses in an amount to be determined.

197. Konda Tech is also entitled to punitive damages.

**EIGHTH CAUSE OF ACTION**

**Fraud – Concealment**

198. Konda Tech incorporates by reference every allegation contained in each and every one of the above paragraphs, as though set forth fully herein.

199. Drs. Markovic and Wang prevented Konda Tech from discovering certain facts and intended to deceive Konda Tech by concealing facts. Dr. Markovic hid the fact that UCLA/ITA would not fund outside technology. Dr. Markovic intentionally hid the fact that his students had started to develop FPGA chips using Konda Tech IP without authorization from Konda Tech. Drs. Markovic and Wang published papers and received awards for those papers without acknowledging that their work was essentially based on the work by Dr. Konda and Konda Tech IP.

200. Drs. Markovic and Wang also started a company, Hier Logic, and subsequently Flex

Logix using Konda Tech IP without disclosing these facts to Konda Tech.

201. Dr. Markovic and Dr. Wang concealed that their aim was to build their own company by misappropriating Konda Tech IP.

202. Konda Tech did not become aware of the concealed facts until on or about December 18, 2015.

203. Had the omitted facts been disclosed to Konda Tech, Konda Tech reasonably would have behaved differently.

204. Konda Tech was harmed by the deprivation to Konda Tech of revenue it would otherwise have received as a result of the facts concealed by Defendants.

205. Dr. Markovic's and Dr. Wang's concealment was a substantial factor in causing harm to Konda Tech.

206. Konda Tech is entitled to damages for its losses in an amount to be determined.

207. Konda Tech is also entitled to punitive damages.

**NINTH CAUSE OF ACTION**

**Misappropriation of Trade Secrets**

208. Konda Tech incorporates by reference every allegation contained in each and every one of the above paragraphs, as though set forth fully herein.

209. Trade Secret as defined in California Civil Code Section 3426.1(d) as:

> "Trade secret" means information, including a formula, pattern, compilation, program, device, method, technique, or process, that:
> (1) Derives independent economic value, actual or potential, from not being generally known to the public or to other persons who can obtain economic value from its disclosure or use; and
> (2) Is the subject of efforts that are reasonable under the circumstances to maintain its secrecy.

210. Konda Tech is the owner of Konda Tech's business plan, details of technology including all implementation details of the disclosures in the patents-in-suit and other technical know-how, business know-how, Konda Tech's FPGA business models, and current and potential customers as well as Konda Tech's interaction with customers and potential customers ("Konda Tech's Trade Secrets").

211. Defendants misappropriated Konda Tech's Trade Secrets. "Misappropriated" means the

improper use of the trade secret.

212. Konda Tech's Trade Secrets had actual or potential independent economic value because they were secret.

213. Konda Tech made reasonable efforts to keep Konda Tech's Trade Secrets secret. All presentations made by Konda Tech included a "Proprietary and Confidential" statement. Additionally, DARPA states that all information submitted by way of the BAA module is considered confidential. See, Exhibit 15 attached hereto.

214. Defendants' misappropriation of Konda Tech's Trade Secrets caused Drs. Markovic and Wang and Flex Logix to be unjustly enriched.

215. Defendants' use of Konda Tech's Trade Secrets was a substantial factor for Defendants to be unjustly enriched.

216. Konda Tech is entitled to damages in an amount to be determined.

217. Konda Tech is also entitled to punitive damages.

**DEMAND FOR JURY TRIAL**

Konda Tech hereby demands a trial by jury of all issues so triable under Federal Rule of Civil Procedure 38(b).

**PRAYER FOR RELIEF**

WHEREFORE, Konda Tech respectfully requests that this Court:

A. Enter judgment for Konda Tech and against Defendants on each of the above claims;

B. Find that United States Patent No. 8,269,523 is valid and enforceable against Flex Logix;

C. Find that Flex Logix has infringed and is infringing United States Patent No. 8,269,523;

D. Permanently enjoin Flex Logix, its officers, agents, servants, employees, and those persons acting in active concert or in participation therewith from infringing United States Patent No. 8,269,523;

E. Award Konda Tech damages sufficient to compensate it for Flex Logix's past and future infringement of United States Patent No. 8,269,523, together with costs and prejudgment interest, pursuant to 35 U.S.C. § 284;

F. Find that United States Patent No. 8,898,611 is valid and enforceable against Flex Logix;

G. Find that Flex Logix has infringed and is infringing United States Patent No. 8,898,611;

H. Permanently enjoin Flex Logix, its officers, agents, servants, employees, and those persons acting in active concert or in participation therewith from infringing United States Patent No. 8,898,611;

I. Award Konda Tech damages sufficient to compensate it for Flex Logix's past and future infringement of United States Patent No. 8,898,611, together with costs and prejudgment interest, pursuant to 35 U.S.C. § 284;

J. Find that United States Patent No. 9,529,958 is valid and enforceable against Flex Logix;

K. Find that Flex Logix has infringed and is infringing United States Patent No. 9,529,958;

L. Permanently enjoin Flex Logix, its officers, agents, servants, employees, and those persons acting in active concert or in participation therewith from infringing United States Patent No. 9,529,958;

M. Award Konda Tech damages sufficient to compensate it for Flex Logix's past and future infringement of United States Patent No. 9,529,958, together with costs and prejudgment interest, pursuant to 35 U.S.C. § 284;

N. Find that United States Patent No. 10,003,553 is valid and enforceable against Flex Logix;

O. Find that Flex Logix has infringed and is infringing United States Patent No. 10,003,553;

P. Permanently enjoin Flex Logix, its officers, agents, servants, employees, and those persons acting in active concert or in participation therewith from infringing United States Patent No. 10,003,553;

Q. Award Konda Tech damages sufficient to compensate it for Flex Logix's past and future infringement of United States Patent No. 10,003,553, together with costs and prejudgment interest, pursuant to 35 U.S.C. § 284;

R. Find that United States Patent No. 10,050,904 is valid and enforceable against Flex Logix;

S. Find that Flex Logix has infringed and is infringing United States Patent No. 10,050,904;

T. Permanently enjoin Flex Logix, its officers, agents, servants, employees, and those

persons acting in active concert or in participation therewith from infringing United States Patent No. 10,050,904;

U. Award Konda Tech damages sufficient to compensate it for Flex Logix's past and future infringement of United States Patent No. 10,050,904, together with costs and prejudgment interest, pursuant to 35 U.S.C. § 284;

V. Order an accounting of damages from Flex Logix's infringement;

W. Award Konda Tech enhanced damages, up to and including trebling Konda Tech's damages, pursuant to 35 U.S.C. § 284, for Flex Logix's willful infringement of the patents-in-suit;

X. Award Konda Tech its reasonable attorneys' fees and costs of suit pursuant to 35 U.S.C. § 285 due to the exceptional nature of this case, or as otherwise permitted by law;

Y. Award Konda Tech for all damages legally and/or proximately caused to Konda Tech by Defendants as set forth above, including costs and prejudgment interest and punitive damages; and

Z. Award Konda Tech such other or additional relief as the Court deems just and proper.

Date: February 21, 2019

Respectfully submitted,

DHILLON LAW GROUP INC.

By: */s/ Nitoj P. Singh*
Nitoj P. Singh
Attorneys for Konda Technologies, Inc.

# EXHIBIT 47

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Attorneys for Defendant
FLEX LOGIX TECHNOLOGIES, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

KONDA TECHNOLOGIES, INC., a California corporation,

Plaintiff,

vs.

FLEX LOGIX TECHNOLOGIES, INC., a Delaware Corporation; DEJAN MARKOVIC, PH.D., an individual; and CHENG C. WANG, PH.D., an individual,

Defendants.

Case No. 5:18-cv-07581-LHK

**FLEX LOGIX TECHNOLOGIES, INC.'S NOTICE OF MOTION AND MOTION TO DISMISS FIRST AMENDED COMPLAINT PURSUANT TO FED. R. CIV. P. 12(b)(6) AND MEMORANDUM OF POINTS AND AUTHORITIES IN SUPPORT THEREOF**

Date: July 11, 2019
Time: 1:30 pm
Judge: Lucy H. Koh
Ctrm.: 8, 4th Floor

**NOTICE OF MOTION AND MOTION TO DISMISS**

To Plaintiff Konda Technologies, Inc., and its counsel of record:

PLEASE TAKE NOTICE that on July 11, 2019, at 1:30 p.m., or as soon thereafter as the matter may be heard, in Courtroom No. 8 of the above-captioned Court, located at 4th Floor, 280 South 1st Street, San Jose, CA 95113, Defendant Flex Logix Technologies, Inc. ("Flex Logix") will, pursuant to Federal Rule of Civil Procedure 12(b)(6), move the Court for an Order dismissing with prejudice all Counts of Konda Technologies, Inc.'s ("Konda Tech") First Amended Complaint in this action that are asserted against Flex Logix.

Specifically, Flex Logix moves for an Order dismissing with prejudice:

[1] Konda Tech's Third, Fourth, and Sixth Causes of Action because those Causes of Action fail to state a claim for patent infringement due to the invalidity of each of the patents under 35 U.S.C. § 102;

[2] Portions of Konda Tech's Second, Third, Fourth, Fifth, and Sixth Causes of Action because those Causes of Action do not plead facts sufficient to state a plausible claim for indirect or willful patent infringement;

[3] Konda Tech's First Cause of Action for Unfair Business Practices pursuant to California Business & Professions Code Section 17200 et seq. as preempted and as barred by the statute of limitations; and

[4] Konda Tech's Ninth Cause of Action for Misappropriation of Trade Secrets as barred by the statute of limitations and for failure to plead the use of reasonable efforts to maintain the secrecy of the alleged trade secrets.

This motion is based upon this Notice of Motion and Motion; the attached Memorandum of Points and Authorities; all other materials supporting this Motion or the Reply brief filed in support thereof; all pleadings on file in this matter; and any other materials or arguments the Court may receive at or before the hearing on this Motion.[1]

[1] Defined terms in this Motion are also used in the accompanying Memorandum of Points and Authorities.

DATED: March 18, 2019

MUNGER, TOLLES & OLSON LLP

By: */s/ Gregory P. Stone*
GREGORY P. STONE

Attorneys for Defendant FLEX LOGIX TECHNOLOGIES, INC.

**FEDERAL CASES**

**FEDERAL STATUTES**

**STATE STATUTES**



**RULES - OTHER**



**FEDERAL REGULATIONS**



**OTHER AUTHORITIES**

## MEMORANDUM OF POINTS AND AUTHORITIES

## I. INTRODUCTION AND SUMMARY OF ARGUMENT

Konda Tech's original complaint in this action was filed on December 17, 2018. Dkt. 1. Flex Logix moved to dismiss that complaint in its entirety. Dkt. 21. In response, Konda Tech sought to amend its complaint. Dkt. 26; Dkt. 28-1. The parties stipulated that Konda Tech could file an amended complaint, and Flex Logix's motion to dismiss was dismissed as moot. Dkt. 30. Konda Tech filed its First Amended Complaint ("FAC") on March 4, 2019. Dkt. 31. Flex Logix now moves to dismiss the seven causes of action asserted against it in the FAC.[1]

### A. The Court Should Dismiss Konda Tech's Patent Claims Against Flex Logix

The FAC alleges that Flex Logix infringes five patents purportedly assigned to Konda Tech, a company founded by Dr. Venkat Konda in 2007. *See* Dkt. 31 (FAC), Counts 2-6, ¶ 13. Dr. Konda is the sole named inventor on each of the five asserted patents. *See id.* Exs. 4-8. The FAC alleges that Konda Tech's patents generally relate to "field-programmable gate array ('FPGA') routing fabric" and "interconnection networks technology." *See id.* ¶ 13.

Konda Tech's patent claims are deficient in numerous respects. First, three of the patents asserted by Konda Tech (specifically, U.S. Patent 8,898,611 ("the '611 patent"); U.S. Patent 9,529,958 ("the '958 patent"); and U.S. Patent 10,050,904 ("the '904 patent")) are invalid in view of one of Konda Tech's *own* prior patent publications. The invalidity of these patents can be straightforwardly determined by a review of Konda Tech's complaint in combination with Konda Tech's own patent applications and patent publications, which are judicially noticeable at this stage. In brief, the disclosures of these three patents were made publicly available more than one year prior to the earliest possible priority date for each patent, rendering each of the patents indisputably invalid. The Court may properly dismiss Konda Tech's patent infringement claims based on invalidity of the asserted patents at this stage because no further proceedings are necessary in order to permit this Court to conclude that each of these patents is invalid.

[1] Konda Tech's FAC purports to add two additional defendants, Dr. Dejan Markovic and Dr. Cheng Wang. These defendants were not served until a few days before the filing of this motion. The present motion is brought solely on behalf of Defendant Flex Logix.

The sole disputed issue is whether the disclosures of the patents were made available to the public under the governing regulation and thus constitute prior art—a pure question of law. There is no reason to delay—this Court can and should dismiss Counts Three, Four, and Six of Konda Tech's complaint due to the invalidity of each of the three patents asserted in those claims.

Second, Konda Tech fails to plead a plausible claim for indirect or willful infringement under *Twomby* and *Iqbal* with respect to *any* of the five asserted patents. Konda Tech's allegations rely on vague generalities and recitations of statutory language instead of specific factual allegations. Konda Tech's indirect and willful patent infringement claims are clearly inadequate and should be dismissed.

### B. The Court Should Dismiss Konda Tech's Non-Patent Claims Against Flex Logix

Third, Konda Tech's misappropriation of trade secrets claim is barred by the statute of limitations. Konda Tech had actual and/or inquiry notice of the alleged misappropriation within the 3-year statute of limitations period for such claims, but elected to wait to file suit until after the limitations period had run. The running of the statute of limitations is manifest from Konda Tech's own complaint and other materials judicially noticeable at this stage. Furthermore, Konda Tech has failed to adequately plead the use of reasonable efforts to maintain the secrecy of its alleged trade secret information. To the contrary, Konda Tech's complaint clearly alleges the voluntary disclosure of any purported trade secrets. Accordingly, the misappropriation claim should be dismissed with prejudice.

Fourth, Konda Tech's UCL claim is predicated solely on the alleged "tortious behavior" otherwise pled in the complaint. FAC ¶ 34. The only "tortious behavior" by Flex Logix that is alleged in the complaint is patent infringement and misappropriation of trade secrets. Because Konda Tech's UCL claim against Flex Logix is based solely on alleged patent infringement or misappropriation of trade secrets, the UCL claim is preempted by federal patent law and by California's statute governing trade secrets claims. The UCL claim is also clearly barred by the applicable statute of limitations.

## II. FACTUAL BACKGROUND

Flex Logix's motion to dismiss is based on Konda Tech's FAC, on publicly available patent applications and publications, and on the February 21, 2019 Declaration of Venkat Konda ("Konda Declaration") filed in this matter (Dkt. 27). The Court may take judicial notice of each of these documents in considering this motion. *See Reyn's Pasta Bella, LLC v. Visa USA, Inc.*, 442 F.3d 741, 746 n.6 (9th Cir. 2006); *see also* Request for Judicial Notice ("RJN") (filed currently herewith).

### A. Konda Tech's Patent Infringement Allegations

Konda Tech alleges that Flex Logix infringes five patents assigned to Konda Tech. *See* FAC, Counts 2-6. The FAC alleges direct infringement by Flex Logix under 35 U.S.C. § 271(a) as well as induced and contributory infringement under 35 U.S.C. § 271(b) and (c), respectively. *Id.*

With respect to Konda Tech's induced infringement allegations, the FAC states that "Flex Logix's website is replete with written directions instructing users on how to use Flex Logix's Accused Products in an infringing manner" and references purported "detailed documentation instructing users on how to use [the] Accused FPGA Devices in an infringing manner." *See, e.g.*, FAC ¶¶ 60-61 (allegations regarding '523 patent). The complaint provides no additional specificity regarding these alleged "written directions" and "detailed documentation."[2] For alleged contributory infringement, the complaint simply parrots portions of the statute and provides no factual allegations in support. *See, e.g., id.* ¶ 59 (allegations regarding '523 patent). Konda Tech includes no specific factual allegations in support of its claims of willful infringement. *See, e.g., id.* ¶ 67 (allegations regarding '523 patent).

### B. The '611 Patent, the '958 Patent, and the '904 Patent and Their Relationship to Each Other

Konda Tech alleges that Flex Logix infringes the '611 patent, the '958 patent, and the '904 patent. FAC, Count 3 ('611 patent), Count 4 ('958 patent), Count 6 ('904 patent); FAC Exs. 5, 6,

8. All three of these patents belong to the same family. The '904 patent is a continuation of the '958 patent, which is a continuation of the '611 patent. *See id.* (Related U.S. Application Data).

Each of the '611, '958, and '904 patents ultimately claims priority to U.S. Provisional Patent Applications 61/252,603 ("the '603 provisional application") and 61/252,609 ("the '609 provisional application"). *See id.* Exs. 5, 6, 8 (Related U.S. Application Data). The '611 patent is characterized as a continuation-in-part with respect to the '603 and '609 provisional applications. *See id.* Ex. 5 ('611 patent) at 1:8-21. Both the '603 and '609 provisional applications were filed on October 16, 2009, which is the earliest priority date possible for each of the '611, '958, and '904 patents. *See id.* Exs. 5, 6, 8 (Related U.S. Application Data).

The disclosures of the '611, '958, and '904 patents correspond directly to the two provisional applications to which they claim priority. For example, Figures 1-7 of the '611, '958, and '904 patents (FAC Exs. 5, 6, 8) match Figures 1-7 of the '603 provisional (RJN Ex. 2); and Figures 8-10 of the '611, '958, and '904 patents match Figures 1-3 of the '609 provisional (RJN Ex. 3). The text describing Figures 1-10 of the '611 '958, and '904 patents is also the same as that in the corresponding provisional applications with appropriate updating to reflect different numbering of Figures 8-10 in the '611 patent, which were Figures 1-3 in the '609 provisional.

**C. Konda Tech's Allegations of Misappropriation of Trade Secrets**

Konda Tech generally alleges that Flex Logix founders, Drs. Dejan Markovic and Cheng Wang, while engaged in research at UCLA, "employed subterfuge and deceit to gain access to Konda Tech IP, develop their fraudulent credibility in the technology through publications based on Konda Tech IP, and then used Konda Tech IP to launch their own company—Flex Logix." FAC ¶ 28. According to the FAC, Dr. Konda began to disclose the allegedly trade secret information to Drs. Markovic and/or Wang (and others) some time in 2009 and ending some time prior to January 2014. *Id.* ¶¶ 15-16, 23-24, 210. Specifically, Konda Tech alleges that Dr. Konda made a presentation on its technology in October 2009 to "UCLA's Institute of Technology Advancement ('ITA')." *Id.* ¶¶ 14-15. Konda Tech alleges that Dr. Markovic falsely represented

[2] Konda Tech also cites to Exhibits 9-14 of the complaint but provides no allegations regarding the

to Konda Tech that the ITA might be able to "fund Konda Tech to bring Konda Tech's IP to the market." *Id.* ¶ 185.[3] Konda Tech also alleges that Dr. Konda gave "a seminar on the technology to Dr. Markovic's students" in October 2009, which Dr. Wang attended. *Id.* ¶ 16. Konda Tech does not allege that any of the individuals in attendance at that presentations had agreed to be subject to any confidentiality restrictions.

Konda Tech also alleges that Dr. Markovic submitted certain proposals to DARPA containing Konda Tech IP. *Id.* ¶¶ 17-18. Konda Tech alleges that Dr. Markovic incorporated the "Konda Tech IP" in the DARPA proposals "from the then published Konda Tech WIPO patent applications." *Id.* ¶ 17.[4] Konda Tech identifies no alleged trade secrets in any DARPA proposals.

The FAC further alleges that as of January 2014, Dr. Konda was aware that Drs. Markovic and Wang either had formed or were in the process of forming a startup company in the FPGA space. Specifically, Konda Tech alleges that in January 2014, Dr. Konda was aware that Drs. Markovic and Wang were "looking for funding for their separate startup" (which eventually become Flex Logix) and that Dr. Markovic stated to Dr. Konda in January 2014 that "he *may* need to license Konda Tech IP for [that] separate startup." *Id.* ¶ 24 (emphasis in original). The FAC alleges that Drs. Markovic and Wang co-founded Flex Logix in February 2014. *Id.* ¶ 29. Konda Tech does not identify any specific wrongful conduct by either Drs. Markovic and Wang or by Flex Logix allegedly occurring after February 2014. Konda Tech suggests that it did not discover the allegedly improper use of "Konda Tech IP" until December 2015. *See id.* ¶¶ 202, 30.

The entirety of Konda Tech's allegations regarding its efforts to maintain the secrecy of its alleged trade secrets are as follows: "Konda Tech made reasonable efforts to keep Konda Tech's Trade Secrets secret. All presentations made by Konda Tech included a "Proprietary and Confidential" statement. Additionally, DARPA states that all information submitted by way of the BAA module is considered confidential. *See*, Exhibit 15 attached hereto." FAC ¶ 213.

import of these materials. *See, e.g.*, FAC ¶¶ 60-62.

[3] In his sworn declaration, Dr. Konda states that he learned that ITA would not provide funding to Konda Tech in October 2009. Konda Decl. (Dkt. 27) ¶ 29.

**LEGAL STANDARDS**

To survive a Rule 12(b)(6) motion, "a complaint must contain sufficient factual matter, accepted as true, to 'state a claim to relief that is plausible on its face.'" *Ashcroft v. Iqbal*, 556 U.S. 662, 678 (2009) (quoting *Bell Atl. Corp. v. Twombly*, 550 U.S. 544, 570 (2007)). This Court need not "accept any unreasonable inferences or assume the truth of legal conclusions cast in the form of factual allegations." *Brown v. Elec. Arts, Inc.*, 724 F.3d 1235, 1248 (9th Cir. 2013) (citation omitted); *see also In re Gilead Scis. Sec. Litig.*, 536 F.3d 1049, 1055 (9th Cir. 2008) ("Nor is the court required to accept as true allegations that are merely conclusory, unwarranted deductions of fact, or unreasonable inferences." (citation omitted)). Further, "[t]he court need not . . . accept as true allegations that contradict matters properly subject to judicial notice or by exhibit." *Gilead*, 536 F.3d at 1055 (citation omitted).

"[I]n deciding a Rule 12(b)(6) motion, courts may consider facts subject to judicial notice." *City of Royal Oak Ret. Sys. v. Juniper Networks, Inc.*, 880 F. Supp. 2d 1045, 1058 (N.D. Cal. 2012). *Accord Wishnev v. Nw. Mut. Life Ins.*, 162 F. Supp. 3d 930, 935 (N.D. Cal. 2016); *Bullwinkle v. U.S. Bank, Nat'l Ass'n*, No. C13-03281 HRL, 2013 WL 5718451, at *2 (N.D. Cal. Oct. 21, 2013). The Court may also "take judicial notice of court filings and other matters of public record." *Reyn's Pasta Bella, LLC*, 442 F.3d at 746 n.6 (affirming dismissal under Rule 12(b)(6)). *Accord Grassi v. Moody's Investor's Servs.*, No. CIV S-09-0543 JAM DAD PS, 2011 WL 3439184, at *8 (E.D. Cal. Aug. 5, 2011), *aff'd*, 540 F. App'x 737 (9th Cir. 2013) (noting that "a court may take judicial notice of its own files and documents filed in other courts" when ruling on a 12(b)(6) motion); *Minor v. FedEx Office & Print Servs., Inc.*, 182 F. Supp. 3d 966, 974 (N.D. Cal. 2016) (holding that "[p]roper subjects of judicial notice include court documents in the public record" as well as "records of administrative agencies"); *Hott v. City of San Jose*, 92 F. Supp. 2d 996, 998 (N.D. Cal. 2000) (taking judicial notice of memoranda filed in related state court case). *See also* RJN (filed concurrently herewith).

[4] The FAC does not specifically define "Konda Tech IP" other than to note that "IP" refers to "intellectual property." FAC ¶ 15.

## ARGUMENT

### I. THIS COURT SHOULD DISMISS KONDA TECH'S INFRINGEMENT CLAIMS BASED ON THE '611 PATENT, '958 PATENT, AND '904 PATENT BECAUSE THESE PATENTS ARE INDISPUTABLY INVALID

The '611 patent, '958 patent, and '904 patent are indisputably invalid over Konda Tech's own prior patent publication, International PCT Application No. WO 2008/109756 A1 ("the Konda PCT"). The invalidity of these patents is manifest in view of the FAC and materials attached thereto, and in view of Konda Tech's own prior patent publications and applications. While Flex Logix recognizes that it is a rare situation where the invalidity of a patent due to anticipation can be resolved on the pleadings, this is such a case.

#### A. The '611, '958, and '904 Patents Contain the Same Disclosures

Because the '958 and '904 patents are continuations of the '611 patent, all three patents must necessarily contain the same disclosures. *See, e.g., Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1321 n.2 (Fed. Cir. 2008) ("[A] continuation contains the same disclosure found in an earlier application."); *Applied Materials, Inc. v. Advanced Semiconductor Materials Am., Inc.*, 98 F.3d 1563, 1579 (Fed. Cir. 1996) (Archer, J., *concurring*) ("By definition, a continuation adds no new matter and is akin to an amendment of a pending application."); MPEP § 201.07 ("The disclosure presented in the continuation must not include any subject matter which would constitute new matter if submitted as an amendment to the parent application.").[5]

#### B. The Publication of the Konda PCT

The Konda PCT incorporates by reference, among other patent applications, U.S. Provisional Patent Applications 60/984,724 ("the '724 provisional application") and 61/018,494 ("the '494 provisional application"). RJN Ex. 1 (Konda PCT) at 2:18-25; *see* Konda Decl. ¶ 22 (Konda admitting that the Konda PCT incorporates by reference the '724 and '494 provisional

[5] Accordingly, while the '958 and '904 patents purport on their face to cross-reference and incorporate by reference additional patent applications in addition to those listed in the '611 patent, any such incorporation by reference cannot be used to introduce any new matter over and above that contained in the '611 patent. In a declaration submitted in response to Flex Logix's motion to dismiss Konda Tech's initial complaint, in which Flex Logix raised the same invalidity

applications). By incorporating the '724 and '494 provisional applications by reference, the Konda PCT includes the entirety of their disclosures. *See Telemac Cellular Corp. v. Topp Telecom, Inc.*, 247 F.3d 1316, 1329 (Fed. Cir. 2001) ("When a document is 'incorporated by reference' into a host document, such as a patent, the referenced document becomes effectively part of the host document as if it were explicitly contained therein."); *see also* MPEP § 2163.07(b).

The Konda PCT was published on September 12, 2008. RJN Ex. 1 (Konda PCT) (noting an "International Publication Date" of September 12, 2008). The publication of the Konda PCT on September 12, 2008, which is more than one year before the October 16, 2009 filing of the '603 and '609 provisional applications (the earliest priority date possible for the '611, '958, and '904 patents), makes the Konda PCT indisputable prior art to each of the '611, '958, and '904 patents under pre-AIA 35 U.S.C. § 102(b) or under AIA 35 U.S.C. § 102(a)(1).[6]

The publication of the Konda PCT included the disclosures of the '724 and '494 provisionals based on their incorporation by reference in the Konda PCT, and made those disclosures public as a matter of law. Specifically, under the regulations governing public availability of patent applications, both of the '724 and '494 provisionals became available to the public upon publication of the Konda PCT.

37 C.F.R. § 1.14 provides, in part, as follows:

> (vi) Unpublished pending applications (including provisional applications) that are **incorporated by reference or otherwise identified**. A copy of the application as originally filed of an **unpublished pending application may be provided to any person**, upon written request and payment of the appropriate fee (§ 1.19(b)), **if the application is incorporated by reference or otherwise identified in** a U.S. patent, a statutory invention registration, a U.S. patent application publication, **an international publication of an international application under PCT Article 21(2)**, or a publication of an international registration under Hague Agreement Article 10(3) of an international design application designating the United States.

arguments presented in this motion, Dr. Konda admitted that "the claims of the '958 and '904 patents do not claim any subject matter of those cross-referenced applications." Konda Decl. ¶ 27.

[6] *See* Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284 (2011).

> The Office will not provide access to the paper file of a pending application, except as provided in paragraph (c) or (i) of this section.[7]

(Emphases added). Accordingly, when the Konda PCT (an international publication of an international application under PCT Article 21(2)) published on September 12, 2008, "any person" was entitled to obtain copies of both the '724 and '494 provisional applications from the U.S. Patent & Trademark Office. And due to their incorporation by reference into the Konda PCT, their contents were effectively contained in the Konda PCT itself.

**C. <u>The Konda PCT Anticipates Each of the '611, '958, and '904 Patents</u>**

A comparison of the '603 and '609 provisionals (to which the '611, '958, and '904 patents ultimately claim priority) and the '724 and '494 provisionals that were included in, and made public by the publication of the Konda PCT, reveals that the '603 and '724 provisional applications are *virtually identical* to each other (*compare* RJN Ex. 2 *with* RJN Ex. 4) and that the '609 and '494 provisional applications are *virtually identical* to each other (*compare* RJN Ex. 3 *with* RJN Ex. 5). The sections pertaining to the "Cross Reference to Related Applications" (and textual references to related applications) have been updated in the later-filed '603 and '609 provisional applications, but all of the figures and text describing the figures are the same between the '603 and '724 provisional applications and the '609 and '494 provisional applications, respectively. The disclosures of additional patent applications incorporated by reference in the '611, '958, and '904 patents in the "Cross Reference to Related Applications" sections, which were not included in the provisionals, are also incorporated by reference in the Konda PCT. (*Compare, e.g.*, FAC Ex. 5 ('611 patent) at 1:5-2:13 *with* RJN Ex. 1 (Konda PCT) at 1:5-2:17).[8]

[7] A substantively identical version of this regulation was in effect as of the date of publication of the Konda PCT, September 12, 2008. *See* 37 C.F.R. § 1.14 (2008).

[8] The '611 patent purports to incorporate by reference four patent applications that are not listed in the Konda PCT. *See* FAC Ex. 5 ('611 patent at 1:5-2:13) ("Cross Reference to Related Applications"). However, each of these additional cited applications claims priority to the applications previously cited in the Konda PCT as follows: U.S. App. 12/530,207 claims priority to U.S. provisionals 60/905,526 and 60/940,383 (FAC Ex. 5 at 1:22-36); U.S. App. 12/601,273 claims priority to U.S. provisionals 60/940,387 and 60/940,390 (FAC Ex. 5 at 1:37-50); U.S. App. 12/601,274 claims priority to U.S. provisionals 60/940,391 and 60/940,392 (FAC Ex. 5 at 1:51-

In other words, the two provisional applications which became public (the '724 and '494 applications) were essentially re-filed more than one year later as the '603 and '609 provisional applications, and then used to provide the disclosure for the patent family containing the '611, '958, and '904 patents now asserted against Flex Logix by Konda Tech. Konda Tech has admitted as much. *See* Dkt. 26 at 8 ("The '724 and '494 provisional applications were refiled as U.S. Provisional Patent Applications 61/252,603 ('the '603 provisional application') and 61/252,609 ('the '609 provisional application'), respectively, on October 16, 2009."). As a result of Konda Tech's actions, the disclosures of the '611, '958, and '904 patents (save the claims) were already disclosed in the prior art more than one year prior to the earliest priority date claimed by each of the patents, October 16, 2009, rendering each of these patents invalid. *See* pre-AIA 35 U.S.C. § 102(b) and AIA 35 U.S.C. § 102(a)(1).

The following chart summarizes where in the Konda PCT each of the disclosures of the alleged inventions of the '611, '958, and '904 patents can be found.[9]

| **'611 Patent, '958 Patent, and '904 Patent (earliest priority date October 16, 2009)** | **Konda PCT (published September 12, 2008)** |
|---|---|
| **Figures** | |
| **Figures 1-7** | **Figures 1-7 of '724 Provisional Application (RJN Ex. 4) as incorporated by reference in Konda PCT (RJN Ex. 1)** |
| **Figures 8-10** | **Figures 1-3 of the '494 Provisional Application (RJN Ex. 5) as incorporated by reference in Konda PCT** |
| **Figures 11A1-11A4** | **Figures 4A1-4A4 of Konda PCT** |
| **Detailed Description of the Invention** | |
| **Introductory text**<br>**'611 patent at 7:16-8:46**<br>**'958 patent at 7:63-9:30**<br>**'904 patent at 8:6-9:39** | **'724 Provisional Application at 6:17-9:6 (with docket numbers and references to applications updated) as incorporated by reference** |

2:3); and U.S. App. 12/601,275 claims priority to U.S. provisional 60/940,394 (FAC Ex. 5 at 2:4-13).

[9] *See also* Exhibit 6 to the attached Declaration of Elizabeth A. Laughton, which provides a detailed visual color-coded comparison of the disclosures of the Konda PCT to the representative '611 patent.

| **'611 Patent, '958 Patent, and '904 Patent (earliest priority date October 16, 2009)** | **Konda PCT (published September 12, 2008)** |
|---|---|
| **Description of Figures 1-7**<br>**'611 patent at 8:47-41:4**<br>**'958 patent at 9:31-44:32**<br>**'904 patent at 9:40-44:34** | **'724 Provisional Application at 9:8-61:18 (with docket numbers and references to applications updated) as incorporated by reference** |
| **Description of Figures 8-10**<br>**'611 patent at 41:5-62:3**<br>**'958 patent at 44:33-66:61**<br>**'904 patent at 44:35-66:56** | **'494 Provisional Application at 7:16-42:2 (with Figure numbers and labels changed appropriately to reflect renumbering and with docket numbers and references to applications updated) as incorporated by reference** |
| **Description of Figures 11A1-11A4**<br>**'611 patent at 62:5-64:20**<br>**'958 patent at 66:63-69:16**<br>**'904 patent at 66:58-69:12** | **Konda PCT at 69:1-72:14 (with Figure numbers and labels changed appropriately to reflect renumbering )** |

In sum, all the disclosures of the '611, '958, and '904 patents (save the claims) were already disclosed in the prior art more than one year prior to the earliest possible priority date, and thus these patents are clearly invalid.

**D. <u>This Court May Properly Invalidate the '611 Patent, '958 Patent, and '904 Patent at this Time</u>**

Flex Logix's motion to dismiss is proper because the complaint, the exhibits attached thereto, and materials that are properly the subject of judicial notice clearly demonstrate that the '611 patent, the '958 patent, and the '904 patent are invalid. It is not often the case that the invalidity of a patent is readily apparent at the motion to dismiss stage. However, when invalidity is readily apparent, there is no just reason to delay in reaching such a determination. For example, in *Select Controls v. American Electronic Components, Inc.*, the court granted a motion to dismiss a patent infringement claim at the pleading stage because "the Complaint and the exhibits attached thereto reveal unequivocally that the design covered by the [patent-in-suit] was both 'the subject of a commercial offer for sale' and 'ready for patenting' prior to the Critical Date of April 18, 2001." No. 07 Civ. 1306(DLC), 2008 WL 216612, at *5 (S.D.N.Y. Jan. 22, 2008). The court concluded that "[the patent-in-suit] is therefore invalid as a matter of law . . ., and SCI's Claim I,

alleging infringement of the '823 Patent, must be dismissed." *Id.* (citation omitted). So too here, the invalidity of the '611 patent, the '958 patent, and the '904 patent is manifest from materials properly considered at the pleading stage and Konda Tech's infringement claims should be dismissed with prejudice.

**E. The '611 Patent, '958 Patent, and '904 Patent Are Unquestionably Invalid**

As set forth in detail above, all of the figures in the '611, '958, and '904 patents and all of the text describing those figures were included in the Konda PCT, which is indisputable prior art to the '611, '958, and '904 patents under pre-AIA 35 U.S.C. § 102(b) or AIA 102(a)(1). Therefore, if the claims in the '611, '958, and '904 patents are supported by the specification of the '611, '958, and '904 patents, the claims are invalid as anticipated by the Konda PCT under pre-AIA 35 U.S.C. § 102(b) or AIA 102(a)(1). Thus, the invalidity of the '611, '958, and '904 patents is readily apparent in view of the patents themselves, which are attached to Konda Tech's complaint, and materials that are judicially noticeable at the motion to dismiss stage. Neither claim construction nor fact or expert discovery is needed to reach such a determination. The above-cited materials constitute clear and convincing evidence of the invalidity of these patents, and Konda Tech's patent infringement claims based on the '611, '958, and '904 patents should be dismissed because these patents are invalid.[10]

In response to Flex Logix's motion to dismiss Konda Tech's original complaint, Dkt. 21, Konda Tech did not dispute any of the facts recited above. *See* Dkt. 26 at 6-9; Konda Decl. ¶¶ 21-28. Instead, Konda Tech's *only* argument in response was that, as a matter of law, the '724 and

[10] Flex Logix requests that in considering its motion, this Court take judicial notice of the Konda Tech patent applications and publications referenced in this motion. *See* RJN (filed concurrently herewith). Because these are documents of which this Court may properly take judicial notice at the motion to dismiss stage, this Court may decide Flex Logix's motion under Rule 12(b)(6). *See id.*; *see also Gorski v. Gymboree Corp.*, No. 14-CV-01314-LHK, 2014 WL 3533324, at *3 n.1 (N.D. Cal. July 16, 2014). However, if the Court declines to decide Flex Logix' motion under Rule 12(b)(6), Flex Logix respectfully requests that its motion be converted to one for summary judgment under Rule 12(d). There are no material disputed facts regarding the invalidity of the '611 '958, and '904 patents in view of the Konda PCT and Flex Logix submits that it is entitled to judgment as a matter of law. *See* Fed. R. Civ. P. 56; *Chestnut v. Juel*, No. C 96-3422 JSB, 1997 WL 68538, at *1 (N.D. Cal. Feb. 12, 1997).

'494 provisional applications did not become available to the public under 37 C.F.R. § 1.14(a)(1)(vi) with the publication of the Konda PCT. Specifically, Konda Tech argued that because 37 C.F.R. § 1.14(a)(1)(vi) states that "[t]he Office will not provide access to the paper file of a pending application, except as provided in paragraph (c) or (i) of this section," a member of the public must be granted permission under 37 C.F.R. § 1.14 (c) or (i) in order to obtain a copy of provisional application as originally filed under 37 C.F.R. § 1.14(a)(1)(vi). Konda Tech argued that because no such permission was ever granted, the '724 and '494 provisional applications were not publicly available during the relevant time, and thus are not prior art. *See* Dkt. 26 at 6-9.

Konda Tech's argument is baseless and relies upon a blatant misreading of the applicable regulation. The regulation clearly states that "any person" "may be provided" a copy of a provisional "***application as originally filed***" under this subsection. 37 C.F.R. § 1.14(a)(1)(vi) (emphasis added). The regulation then goes on to specify that certain permissions are needed to access "***the paper file of a pending application***." *Id.* While a member of the public may require certain permissions to access the entire "paper file," of the application, under the plain language of the regulation, *no permission* is needed to obtain a copy of the "application as originally filed." *See Hyatt v. U.S. Patent & Trademark Office*, 797 F.3d 1374, 1378 (Fed. Cir. 2015) (noting that certain prosecution materials will "become publicly available in the ordinary course of examination" under 37 C.F.R. § 1.14(a)(1)(v) which contains identical language to subsection (vi) regarding access to the "paper file" of an application); *Nomadix, Inc. v. Second Rule LLC*, No. CV-07-01946-DDP (VBKx), 2009 WL 10668158, at *26 (C.D. Cal. Jan. 16, 2009) ("[T]he '497 provisional application, though unpublished, was publicly available at the time the ['399] patent issued . . . ."); *id.* at *19 (where the '399 patent's specification incorporated by reference the '497 provisional application); *Ex Parte Xiaoming Bao & Stephen M. Allen*, No. 2016-006293, 2017 WL 1397726, *4 (P.T.A.B. Mar. 28, 2017) ("When Kovalic [an international application] published in July 2009, the Kovalic Provisional published as well."); *id.* at *5 ("[w]e are . . . unpersuaded that the Kovalic Provisional was unpublished and unavailable"). The '724 and '494 provisional applications are indisputably prior art to the '611, '958, and '904 patents, and the Konda PCT, which incorporates them by reference, renders these patents invalid.

## II. KONDA TECH'S INDIRECT INFRINGEMENT ALLEGATIONS ARE INADEQUATELY PLED AND SHOULD BE DISMISSED

*All* of Konda Tech's indirect or willful patent infringement claims lack the necessary factual allegations for such claims and accordingly must be dismissed. It is settled that "the rule that '[t]hreadbare recitals of the elements of a cause of action, supported by mere conclusory statements, do not suffice' appl[ies] in patent cases." *Hitachi Kokusai Elec. Inc. v. ASM Int'l, N.V*, No. 17-CV-06880-BLF, 2018 WL 3537166, at *2 (N.D. Cal. July 23, 2018). "[The] pleading standards under *Iqbal* and *Twombly* apply to allegations of . . . indirect (i.e., induced and contributory) infringement." *Id.* Konda Tech's indirect infringement allegations are conclusory and manifestly lack the required factual specificity.

Konda Tech's inducement allegations as pled in its FAC remain devoid of any factual content that could give rise to a reasonable inference that Flex Logix has induced infringement of any of the asserted patents. The FAC states that "Flex Logix's website is replete with written directions instructing users on how to use Flex Logix's Accused Products in an infringing manner" and references purported "detailed documentation instructing users on how to use [the] Accused Products in an infringing manner." *See, e.g.*, FAC ¶¶ 60-61 (allegations regarding '523 patent). However, the FAC provides no additional specificity regarding these alleged "written directions" and "detailed documentation," nor does it allege how Flex Logix has knowledge that the induced acts constitute patent infringement or how Flex Logix has the specific intent to induce infringement. Konda Tech also cites to Exhibits 9-14 of the FAC but provides no allegations regarding import of these materials. *See, e.g.*, *Uniloc USA, Inc. v. Apple Inc.*, No. C 18-00359 WHA, 2018 WL 2047553, at *4 (N.D. Cal. May 2, 2018) ("Uniloc's vague and conclusory allegations that Apple 'intentionally instructs its customers to infringe' using broad categories of materials, coupled with a list of five generic websites, do not amount to *factual* content supporting any reasonable inference that Apple possessed either 'knowledge that the induced acts constitute patent infringement' or 'specific intent to encourage another's infringement.'"); *CAP Co. v. McAfee, Inc.*, No. 14-CV-05068-JD, 2015 WL 3945875, at *5 (N.D. Cal. June 26, 2015) ("CAP makes passing references to 'user manuals guides, and support articles,' without ever saying what

those materials contain, which is wholly inadequate for an inference of specific intent."); *Avocet Sports Tech., Inc. v. Garmin Int'l, Inc.*, No. C 11-04049 JW, 2012 WL 2343163, at *4 (N.D. Cal. June 5, 2012) (holding that pleading that giving customers "specific instructions or training" is insufficient to allege induced infringement).

Konda Tech's contributory infringement allegations simply parrot portions of the statute and allege no facts in support. *See, e.g.*, FAC ¶ 59 (allegations regarding '523 patent). These allegations are clearly inadequate, fail to allege a plausible claim for contributory infringement, and should be dismissed. *See, e.g.*, *Windy City Innovations, LLC v. Microsoft Corp.*, 193 F. Supp. 3d 1109, 1116–17 (N.D. Cal. 2016) (An allegation tracking the statute "is nothing but a bare conclusion. Accordingly, the Court *Grants* defendant's motion to dismiss the contributory infringement claim." (emphases & citation omitted)); *Uniloc USA, Inc. v. Logitech, Inc.*, No. 18-CV-01304-LHK, 2018 WL 6025597, at *3 (N.D. Cal. Nov. 17, 2018) ("Uniloc's fleeting reference to the fact that the accused products have no substantial noninfringing uses does not provide the requisite factual basis to support Uniloc's claim, which merely paraphrases the contributory infringement statute."); *Uniloc*, 2018 WL 2047553, at *5 (Contributory infringement allegations were "merely [a] formulaic recitation of Section 271(c) not entitled to the presumption of truth.").[11]

## III. THIS COURT SHOULD DISMISS KONDA TECH'S MISAPPROPRIATION OF TRADE SECRETS CLAIM

Konda Tech's claim of misappropriation of trade secrets is barred by the statute of limitations because, as Dr. Konda's sworn declaration states, Konda Tech knew or reasonably should have known of the alleged misappropriation no later than February 2014, which is more

[11] Konda Tech's willful infringement claims are similarly devoid of any factual allegations, and should also be dismissed. Konda Tech simply alleges that "Flex Logix's infringement of the '523 patent has been willful and deliberate and, pursuant to 35 U.S.C. § 284, Konda Tech is entitled to treble damages." *See, e.g.*, *Elec. Scripting Prods., Inc. v. HTC Am. Inc.*, No. 17-CV-05806-RS, 2018 WL 1367324, at *7 (N.D. Cal. Mar. 16, 2018) ("ESPI falls woefully short of sufficiently pleading egregious behavior and willfulness. ESPI must provide factual allegations that are specific to HTC's conduct and do not merely recite the elements of the statutory violations, but rather provide factual material that puts HTC on notice of its allegedly unlawful actions.").

than three years before Konda Tech filed suit. Further, Konda Tech has failed to allege the use of reasonable efforts to maintain the secrecy of its alleged trade secrets. Konda Tech's misappropriation of trade secrets claim should also be dismissed.

### A. Konda Tech's Claim of Misappropriation of Trade Secrets Is Barred by the Statute of Limitations

Konda Tech's claim for misappropriation of trade secrets should be dismissed because it is barred by the statute of limitations. "A claim may be dismissed under Rule 12(b)(6) on the ground that it is barred by the applicable statute of limitations only when 'the running of the statute is apparent on the face of the complaint.'" *Stanford Hosp. & Clinics v. Guarantee Trust Life Ins. Co.*, No. 5:11–cv–01271 EJD, 2012 WL 694743, at *3 (N.D. Cal. Mar. 1, 2012) (quoting *Von Saher v. Norton Simon Museum of Art*, 592 F.3d 954, 969 (9th Cir. 2010)). Moreover, the phrase "'face of the complaint' includes matters of which judicial notice may be taken." *Sims v. Wholers*, No. CIV S-09-2582 GGH P, 2011 WL 3584455, at *2 (E.D. Cal. Aug. 12, 2011) (granting motion to dismiss on statute of limitations grounds). Here, the untimeliness of Konda Tech's misappropriation of trade secrets claim is readily apparent from a review of the complaint and the Konda Declaration filed in this action.

"An action for misappropriation must be brought within three years after the misappropriation is discovered or by the exercise of reasonable diligence should have been discovered." Cal. Civ. Code § 3426.6. *See Portney v. CIBA Vision Corp.*, No. SACV 07-0854 AG (MLGx), 2008 WL 5505518, at *9 (C.D. Cal. Dec. 24, 2008) (dismissing trade secrets claim because plaintiff "reasonably should have discovered the alleged violations" during the limitations period). As set forth in the chart below, Konda Tech's FAC and the Konda Declaration demonstrate that Konda Tech had either actual or constructive notice of the facts giving rise to its allegations of trade secret misappropriation no later than February of 2014:

| **Allegation in FAC** | **Actual or Constructive Knowledge by Konda Tech** |
|---|---|
| FAC ¶ 185: "Dr. Markovic represented to Konda Tech that he would assist Konda Tech to secure funding from UCLA/ITA to fund Konda Tech to bring Konda Tech's IP | Konda Decl. ¶ 29: "[A]fter I arrived in Los Angeles on October 12, 2009 to present my business plan to UCLA/ITA, Dr. Markovic for the first time said to me that I should not expect |

| Allegation in FAC | Actual or Constructive Knowledge by Konda Tech |
|---|---|
| to the market. Dr. Markovic's representation was false."<br><br>FAC ¶ 199: "Dr. Markovic hid the fact that UCLA/ITA would not fund outside technology." | UCLA/ITA to fund Konda Tech, because UCLA/ITA will not fund technologies built outside UCLA." |
| FAC ¶ 199: "Dr. Markovic intentionally hid the fact that his students had started to develop FPGA chips using Konda Tech IP without authorization from Konda Tech." | Konda Decl. ¶ 32: " In 2010 when Dr. Markovic told me that his students had begun implementing Konda Tech's technology, I told him to stop. Dr. Markovic's answer was, as a university professor, he could implement any publicly available technology including any technology disclosed in patents or patent applications. I told Dr. Markovic that without a license from Konda Tech, I did not agree that he or UCLA had a right to implement Konda Tech's technology."<br><br>FAC ¶ 21: "In 2010, Dr. Markovic told Dr. Konda over the phone that his students, including Dr. Wang, were implementing Konda Tech IP as an academic project, specifically the 2D layout, on an FPGA chip." |
| FAC ¶ 199: "Drs. Markovic and Wang published papers and received awards for those papers without acknowledging that their work was essentially based on the work by Dr. Konda and Konda Tech IP." | FAC ¶ 21: "In June 2011, unbeknownst to Dr. Konda, Drs. Markovic and Wang presented a paper at the 2011 VLSI Circuits Symposium titled 'A 1.1 GOPS/mQ FPGA Chip with Hierarchical Interconnect Fabric'—based on Konda Tech IP."<br><br>FAC ¶ 25: "A couple of weeks later [in January or February of 2014], Drs. Markovic and Wang published a paper titled 'A Multi-Granularity FPGA with Hierarchical Interconnects for Efficient and Flexible Mobile Computing'—again, based on Konda Tech IP—at the 2014 International Solid State Circuits Conference (the 'ISSCC paper')." |
| FAC ¶¶ 200-201: "Drs. Markovic and Wang also started a company, Hier Logic, and subsequently Flex Logix using Konda Tech IP without disclosing these facts to Konda Tech.<br><br>Dr. Markovic and Dr. Wang concealed that their aim was to build their own company by misappropriating Konda Tech IP." | FAC ¶ 24: "Dr. Konda met with Drs. Markovic and Wang at the home of Dr. Bonomi in January 2014. . . . Over the course of their discussions, Drs. Markovic and Wang stated that they were looking for funding for their separate startup, but when queried, refused to disclose the technological focus of their startup. Cryptically, Dr. Markovic later stated that he *may* need to license Konda Tech IP for their separate startup |

| Allegation in FAC | Actual or Constructive Knowledge by Konda Tech |
|---|---|
| FAC ¶ 191: "Dr. Markovic always represented to Konda Tech that he was helping Konda Tech get funded. Dr. Markovic intended that Konda Tech rely on his telling Dr. Konda that he was helping Konda Tech so that Konda Tech would provide him with Konda Tech's business plan and technical know-how and customer experience information over a period of years based on his intentionally misrepresenting his true intentions."<br>FAC ¶ 192: "Dr. Markovic used the information provided by Konda Tech to develop FPGA chips which later became the basis [sic] Drs. Markovic and Wang to found Flex Logix." | as well."<br>Konda Decl. ¶ 34: "[Dr. Markovic] himself said in January 2014 at Dr. Bonomi's house that he may need to take a license from Konda Tech." |

As detailed in the chart above, Konda Tech's FAC and the Konda Declaration make clear that Konda Tech had either actual or inquiry notice of the facts of the allegedly improper use of its IP no later than February of 2014.[12] As of February 2014, Dr. Konda had actual knowledge of Dr. Wang and Dr. Markovic's alleged implementation of Konda Tech IP *and* knew that Drs. Wang and Markovic were in the process of forming a startup in the FPGA space (otherwise there would be no reason why they "may need to take a license from Konda Tech" for that startup).

Rather than investigate at this point, Dr. Konda did nothing. If Dr. Konda had performed ***any*** investigation in February 2014, he would have discovered the publically available 2011 and 2014 papers cited as allegedly evidencing the improper use of Konda Tech's IP. Thus, Konda Tech had actual knowledge or reasonably should have known of all of the alleged wrongdoing no later than February 2014, and yet waited more than three years to file suit. Konda Tech's trade

[12] Also, as the chart makes clear, the allegations in Konda Tech's complaint are at times directly contradicted by Dr. Konda's sworn declaration, and to the extent they do so, they should be disregarded as implausible. *See Benedict v. Hewlett-Packard Co.*, No. 13-CV-00119-LHK, 2014 WL 234218, at *4 (N.D. Cal. Jan. 21, 2014) ("[A] court need not accept as true allegations contradicted by judicially noticeable facts."); *Martinez v. Allstar Fin. Servs., Inc.*, No. CV 14-04661 MMM (MRWx), 2014 WL 12597333, at *8 (C.D. Cal. Oct. 9, 2014) (concluding that "no plausible inference can arise from the conflicting allegations").

secrets claim is thus barred by the statute of limitations. *See, e.g.*, *Arunachalam v. Apple, Inc.*, No. 5:18-CV-01250-EJD, 2018 WL 5023378, at *4 (N.D. Cal. Oct. 16, 2018) (dismissing trade secrets claim because "Plaintiff was or should have been aware of the alleged conduct by Defendants" during the limitations period); *Micrel Inc. v. Monolithic Power Sys., Inc.*, No. C 04-04770 JSW, 2005 WL 6426678, at *6 (N.D. Cal. Dec. 9, 2005) (dismissing trade secrets claim because plaintiff had constructive notice during limitations period); *MedioStream, Inc. v. Microsoft Corp.*, 869 F. Supp. 2d 1095, 1110 (N.D. Cal. 2012) (similar).[13]

### B. Konda Tech Fails to Allege Reasonable Efforts to Maintain the Secrecy of Its Alleged Trade Secrets

Under California law, in order for information to qualify as a trade secret, it must be "the subject of efforts that are reasonable under the circumstances to maintain its secrecy." Cal. Civ. Code § 3426.1(d). Here, Konda Tech merely alleges that "[a]ll presentations made by Konda Tech included a 'Proprietary and Confidential'" statement and "DARPA states that all information submitted by way of the BAA module is considered confidential." FAC ¶ 213.

With respect to the first allegation, regardless of whether Konda Tech labeled any presentations as "Proprietary and Confidential," Konda Tech alleges that Dr. Konda made a presentation on its technology to UCLA's ITA and also gave a "a seminar on the technology to Dr. Markovic's students" including Dr. Wang. *Id.* ¶¶ 15-16. Konda Tech does not allege that any of the individuals in attendance at either of these presentations was subject to any confidentiality restrictions. Because Dr. Konda voluntarily disclosed, absent restriction, any allegedly trade secret information in its "presentations," Konda Tech's first allegation regarding its secrecy measures fails. *See Logtale, Ltd. v. IKOR, Inc.*, No. C 11-5452 CW, 2013 WL 4427254, at *6 (N.D. Cal. Aug. 14, 2013) ("Because IKOR has alleged that it voluntarily granted Logtale or NEWAI access to its proprietary information, leave to amend would be futile. This claim is therefore dismissed with prejudice."). With respect to Konda Tech's second allegation, Konda Tech alleges that Dr. Markovic incorporated the "Konda Tech IP" in the DARPA proposals "from

[13] The result would be the same even if the 4-year statute of limitations for UCL claims were used.

the then published Konda Tech WIPO patent applications." FAC ¶ 17. Accordingly, as pled, there can be no trade secret information in those proposals, rendering any confidentiality associated with those proposals is irrelevant. Konda Tech's misappropriation of trade secrets claim should be dismissed with prejudice for this reason as well.

## IV. THIS COURT SHOULD DISMISS KONDA TECH'S UNFAIR BUSINESS PRACTICES CLAIM

Konda Tech identifies the basis for its UCL claim as follows: "Flex Logix's *tortious behavior*, as described above and below in the causes of action listed in this Complaint, all constitute unfair and unlawful business practices." FAC ¶ 34 (emphasis added). The *only* tortious behavior allegedly committed by Flex Logix that is identified in the FAC is alleged violations of patent law and misappropriation of trade secrets. Accordingly, Konda Tech's UCL claim is preempted. The claim is also barred by the applicable 4-year statute of limitations.

### A. Konda Tech's UCL Claim Is Preempted by Federal Patent Law

"[A] violation of federal patent law—without more—cannot serve as the basis of [a Section 17200] claim." *Halton Co. v. Streivor, Inc.*, No. C 10-00655 WHA, 2010 WL 2077203, at *4 (N.D. Cal. May 21, 2010). Instead, "[a] state-law claim must be 'qualitatively different from a copyright or patent infringement claim' or else it is preempted." *Id.* (quoting *Summit Mach Tool Mfg. Corp. v. Victor CNC Sys., Inc.*, 7 F.3d 1434, 1439-40 (9th Cir. 1993)). Courts routinely dismiss state law claims which are premised solely on a violation of federal patent law as preempted. *See, e.g.*, *Halton*, 2010 WL 2077203, at *4 (dismissing California unfair competition claim under Section 17200 as preempted by federal patent law); *AntiCancer, Inc. v. CellSight Techs., Inc.*, No. 10CV2515 JLS (RBB), 2012 WL 3018056, at *7-8 (S.D. Cal. July 24, 2012) (dismissing California unfair competition claims which were "predicated on [defendant's] alleged violation of federal patent laws"); *JAT Wheels, Inc. v. DB Motoring Grp., Inc.*, No. CV 14-5097-GW(AGRx), 2016 WL 9453798, at *3 (C.D. Cal. Feb. 11, 2016) ("Because Plaintiff has not alleged any additional tortious conduct that is separate from the patent law cause of action, preemption applies."). If and to the extent that Konda Tech's UCL claim is based on alleged patent infringement, it is preempted.

**B. Konda Tech's UCL Claim Is Preempted by CUTSA**

If and to the extent Konda Tech's UCL claim is based on alleged misappropriation of trade secrets, it is also preempted by the California Uniform Trade Secrets Act ("CUTSA"). "Under California law, CUTSA provides the exclusive civil remedy for conduct falling within its terms and supersedes other civil remedies based upon misappropriation of a trade secret. It therefore supersedes claims—including Section 17200 claims—based on the same nucleus of facts as trade secret misappropriation." *Alta Devices, Inc. v. LG Elecs., Inc.*, 343 F. Supp. 3d 868, 888 (N.D. Cal. 2018) (internal quotation and citation omitted) (emphasis omitted) ("The Court agrees with LGE that Alta's UCL claim is preempted to the extent that it is based on trade secret misappropriation."); *NetApp, Inc. v. Nimble Storage, Inc.*, 41 F. Supp. 3d 816, 839 (N.D. Cal. 2014) (same); *see also* Cal. Civ. Code. § 3426.7. Accordingly, because there is no alleged tortious conduct by Flex Logix that could provide the basis for its UCL claim, this claim should be dismissed with prejudice.

**C. Konda Tech's Unfair Business Practices Claim Is Also Barred by the Statute of Limitations**

Konda Tech's UCL claim is also barred by the statute of limitations. "Claims under the UCL are subject to a four year statute of limitations that begins to run on the date the cause of action accrues." *Zanze v. Snelling Servs., LLC*, 412 F. App'x 994, 996 (9th Cir. 2011); Cal. Bus. & Prof. Code § 17208. As set forth above, *see*, Section II.C, *supra*, save Konda Tech's allegations of patent infringement, all of the alleged wrongs complained of by Konda Tech took place more than four years before Konda Tech filed its complaint in this action, and Konda Tech had notice of the alleged wrongs no later than February 2014. Accordingly, Konda Tech's unfair business practices claim should be dismissed for this reason as well. *See, e.g.*, *Moran v. Wash. Mut. Bank*, No. 12-CV-04974 NC, 2012 WL 12920636, at *5 (N.D. Cal. Nov. 8, 2012) ("As Moran filed his complaint more than six years after the alleged violations, and he asserts no theory of tolling in the complaint or the amended complaint, defendant's motion to dismiss Moran's § 17200 claims is GRANTED WITH PREJUDICE."); *Montes v. U.S. Bank Nat'l Ass'n*, No. CV 10-0022 PSG (Jcx), 2010 WL 11597507, at *3 (C.D. Cal. July 21, 2010) (dismissing § 17200 claim as time-barred).

**CONCLUSION**

For the reasons set forth above, Konda Tech's complaint should be dismissed with prejudice with the exception of Konda Tech's allegations of direct patent infringement as pled in Counts 2 and 5.

DATED: March 18, 2019

MUNGER, TOLLES & OLSON LLP

By: */s/ Gregory P. Stone*
GREGORY P. STONE

Attorneys for Defendant FLEX LOGIX TECHNOLOGIES, INC.

# EXHIBIT 48

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Attorneys for Konda Technologies, Inc.

**UNITED STATES DISTRICT COURT**

**NORTHERN DISTRICT OF CALIFORNIA**

**SAN JOSE DIVISION**

KONDA TECHNOLOGIES, INC., a California corporation,

Plaintiff,

v.

FLEX LOGIX TECHNOLOGIES, INC., a Delaware corporation, *et al.*,

Defendants.

Case Number: 5:18-cv-07581-LHK

**NOTICE OF VOLUNTARY DISMISSAL**

Judge: Hon. Lucy H. Koh
Court: 8, 4th Floor

TO THE COURT, ALL PARTIES, AND THEIR COUNSEL OF RECORD:

NOTICE IS HEREBY GIVEN that pursuant to the Federal Rules of Civil Procedure, Rule 41(a), Plaintiff Konda Technologies, Inc. voluntarily dismisses the above-captioned action without prejudice.

Date: April 3, 2019

DHILLON LAW GROUP INC.

By: */s/ Nitoj P. Singh*
Nitoj P. Singh

Attorneys for Konda Technologies, Inc.

# EXHIBIT 49

3650bbb

| S&DC-S/N | Statement and Designation by Foreign Corporation |
|---|---|

To qualify a corporation from another state or country to transact intrastate business in California, fill out this form, and submit for filing along with:

- A **$100** filing fee (for a foreign stock corporation) or **$30** filing fee (for a foreign nonprofit corporation), and
- A certificate of good standing, issued within the last six (6) months by the agency where the corporation was formed. **Note:** If the corporation is a nonprofit, the certificate of good standing also must indicate the corporation is a nonprofit or nonstock corporation.
- A separate, non-refundable **$15** service fee also must be included, if you **drop off** the completed form.

***Important!*** Corporations in California may have to pay a minimum $800 yearly tax to the California Franchise Tax Board. For more information, go to https://www.ftb.ca.gov.

**FILED**
Secretary of State
State of California
**FEB 26 2014**

1CC

This Space For Office Use Only

**For questions about this form, go to** www.sos.ca.gov/business/be/filing-tips.htm.

**Corporate Name** (List the exact name of the corporation, as shown in the certificate of good standing. If the name of the corporation is not available for use in the State of California, the corporation must qualify under an assumed name. E.g., "[list the exact name] which will do business in California as [list the proposed assumed name]." For general corporate name requirements and restrictions in California, go to www.sos.ca.gov/business/be/name-availability.htm.)

① Flex Logix Technologies, Inc.

**Corporate History**

② State or foreign country where this corporation was formed: Delaware

**Service of Process** (List a California resident or an active 1505 corporation in California that agrees to be your agent to accept service of process in case your corporation is sued. You may list any adult who lives in California. You may **not** list your own corporation as the agent. **Do not** list an address if the agent is a 1505 corporation as the address for service of process is already on file.)

③ a. Incorporating Services, Ltd.
*Agent's Name*

b. _____ CA _____
*Agent's Street Address (if agent is not a corporation) - Do not list a P.O. Box* | *City (no abbreviations)* | *State* | *Zip*

The corporation named in Item 1 above irrevocably consents to service of process directed to it upon the agent designated above, and to service of process on the California Secretary of State if that agent or that agent's successor is no longer authorized to act or cannot be found at the address given.

**Corporate Addresses**

④ a. 4 Valley Oak Street | Portola Valley | CA | 94028
*Street Address of Principal Executive Office - Do not list a P.O. Box* | *City (no abbreviations)* | *State* | *Zip*

b. 4 Valley Oak Street | Portola Valley | CA | 94028
*Street Address of Principal Office in California, if any - Do not list a P.O. Box* | *City (no abbreviations)* | *State* | *Zip*

c. _____
*Mailing Address of Principal Executive Office, if different from 4a or 4b* | *City (no abbreviations)* | *State* | *Zip*

**Read and sign below:** This form must be signed by an officer of the foreign corporation.

▶ _____ 25 Feb 2014 | Geoffrey Ross Tate | President & CEO
Sign here | Print your name here | Your business title

| Make check/money order payable to: **Secretary of State** | ***By Mail*** | ***Drop-Off*** |
|---|---|---|
| Upon filing, we will return one (1) uncertified copy of your filed document for free, and will certify the copy upon request and payment of a $5 certification fee. | Secretary of State<br>Business Entities, P.O. Box 944260<br>Sacramento, CA 94244-2600 | Secretary of State<br>1500 11th Street, 3rd Floor<br>Sacramento, CA 95814 |

3650666

# Delaware



*The First State*

I, JEFFREY W. BULLOCK, SECRETARY OF STATE OF THE STATE OF DELAWARE, DO HEREBY CERTIFY "FLEX LOGIX TECHNOLOGIES, INC." IS DULY INCORPORATED UNDER THE LAWS OF THE STATE OF DELAWARE AND IS IN GOOD STANDING AND HAS A LEGAL CORPORATE EXISTENCE SO FAR AS THE RECORDS OF THIS OFFICE SHOW, AS OF THE TWENTY-FIFTH DAY OF FEBRUARY, A.D. 2014.

AND I DO HEREBY FURTHER CERTIFY THAT THE SAID "FLEX LOGIX TECHNOLOGIES, INC." WAS INCORPORATED ON THE NINETEENTH DAY OF FEBRUARY, A.D. 2014.

AND I DO HEREBY FURTHER CERTIFY THAT THE FRANCHISE TAXES HAVE NOT BEEN ASSESSED TO DATE.


Jeffrey W. Bullock, Secretary of State

5484394 8300

AUTHENTICATION: 1161916

140239966

DATE: 02-25-14

You may verify this certificate online at corp.delaware.gov/authver.shtml

F

# State of California
## Secretary of State

## Statement of Information
**(Foreign Corporation)**
**FEES (Filing and Disclosure): $25.00.**
**If this is an amendment, see instructions.**
**IMPORTANT – READ INSTRUCTIONS BEFORE COMPLETING THIS FORM**

1. **CORPORATE NAME**

2. **CALIFORNIA CORPORATE NUMBER**

This Space for Filing Use Only

**No Change Statement** (Not applicable if agent address of record is a P.O. Box address. See instructions.)

3. **If there have been any changes to the information contained in the last Statement of Information filed with the California Secretary of State, or no statement of information has been previously filed, this form must be completed in its entirety.**

☐ If there has been no change in any of the information contained in the last Statement of Information filed with the California Secretary of State, check the box and proceed **to Item 13**.

**Complete Addresses for the Following** (Do not abbreviate the name of the city. Items 4 and 5 cannot be P.O. Boxes.)

| | | | | |
|---|---|---|---|---|
| 4. STREET ADDRESS OF PRINCIPAL EXECUTIVE OFFICE | | CITY | STATE | ZIP CODE |
| 5. STREET ADDRESS OF PRINCIPAL BUSINESS OFFICE IN CALIFORNIA, IF ANY | | CITY | STATE | ZIP CODE |
| 6. MAILING ADDRESS OF THE CORPORATION, IF DIFFERENT THAN ITEM 4 | | CITY | STATE | ZIP CODE |

**Names and Complete Addresses of the Following Officers** (The corporation must list these three officers. A comparable title for the specific officer may be added; however, the preprinted titles on this form must not be altered.)

| | | | | |
|---|---|---|---|---|
| 7. CHIEF EXECUTIVE OFFICER/ | ADDRESS | CITY | STATE | ZIP CODE |
| 8. SECRETARY | ADDRESS | CITY | STATE | ZIP CODE |
| 9. CHIEF FINANCIAL OFFICER/ | ADDRESS | CITY | STATE | ZIP CODE |

**Agent for Service of Process** If the agent is an individual, the agent must reside in California and Item 11 must be completed with a California street address, a P.O. Box address is not acceptable. If the agent is another corporation, the agent must have on file with the California Secretary of State a certificate pursuant to California Corporations Code section 1505 and Item 11 must be left blank.

10. NAME OF AGENT FOR SERVICE OF PROCESS

| | | | |
|---|---|---|---|
| 11. STREET ADDRESS OF AGENT FOR SERVICE OF PROCESS IN CALIFORNIA, **IF AN INDIVIDUAL** | CITY | STATE | ZIP CODE |

**Type of Business**

12. DESCRIBE THE TYPE OF BUSINESS OF THE CORPORATION

13. THE INFORMATION CONTAINED HEREIN IS TRUE AND CORRECT.

| DATE | TYPE/PRINT NAME OF PERSON COMPLETING FORM | TITLE | SIGNATURE |
|---|---|---|---|

SI-350 (REV 01/2013) APPROVED BY SECRETARY OF STATE

# EXHIBIT 50
# Reserved

# EXHIBIT 51

Gmail **Venkat Konda <vkonda@gmail.com>**

# Re: Responses to your most recent email

**Venkat Konda** <vkonda@gmail.com> Tue, Oct 15, 2019 at 11:28 PM
To: "Stone, Gregory" <Gregory.Stone@mto.com>, "Perry, Steven" <Steven.Perry@mto.com>
Cc: Venkat Konda <vkonda@gmail.com>

Dear Mr. Stone, Mr. Perry:

This replies to your email dated October 13, 2019, below. Your contention that I concede that "a multi-tiered protective order will be necessary" is misconceived. Here, we are dealing with your clients' misappropriation of my FPGA Fabric technology including trade secrets. I am not interested in obtaining discovery of your clients' trade secrets, if any. I am confident that my trade secrets can be adequately protected under the Santa Clara County Superior Court stipulated protective order that I emailed to Mr. Perry on September 20, 2019. Please date and sign that stipulated protective order and return it to me without delay.

Insofar as my point that the protective order that you proposed is too restrictive, your tacit objective is that you want to limit my access to information that you will no doubt designate as highly confidential so that I cannot see the information and force me to hire an attorney to fight with you in court to challenge your designations. I wish to avoid such a procedure.

I also view your "Stone-walling" me with respect to my discovery as inappropriate. First, I have four causes of action, only one of which is for misappropriation of my trade secrets. Therefore, you are in any event required to provide responses to all of my discovery requests served on your clients regarding the fraud-misrepresentation, fraud-concealment, and unfair business practices causes of action. Second, attached is a "Confidential" list of my trade secrets that I allege have been misappropriated by your clients, which gives more than adequate particularity of my trade secrets in full compliance with CCP 2019.210. Accordingly, I demand that you proceed with full responses to my outstanding discovery requests by the dates your responses are due.

This also confirms our meet and confer telephone call scheduled for this Friday, October 18, 2019 at 4:30 PM PDT. Please call me at that time on (408) 472-3273.

Very truly yours,

Venkat Konda, Ph.D.

On Sun, Oct 13, 2019 at 9:54 AM Stone, Gregory <Gregory.Stone@mto.com> wrote:

> Dear Dr. Konda,
>
> Although you argue that the second level of protection is not yet necessary, not only do we disagree, but that is not the point. The point, as you appear to concede, is that a multi-tiered protective order will be necessary in this case. The one we have proposed is appropriate and substantively consistent with what you had earlier proposed. It is not unduly restrictive, nor do you offer any basis for your contention that it is. Please sign the proposed Protective Order that we sent you and return it. To the extent it is not appropriate to make use of the higher levels of confidentiality protection, we will not do so, and, to the extent you disagree with our designations, the Protective Order provides for a procedure to challenge those designations.
>
> We will be available for a meet and confer regarding your discovery requests on October 18 at 4:30 pm. Please reserve time on your calendar for that conference.
>
> I do want to remind you, as Mr. Perry explained in his October 7, 8 am, email, which is part of the chain below, that you have not identified the trade secrets that form the basis for your complaint with adequate particularity, have therefore not complied with CCP § 2019.210, and thus there is an automatic stay of all discovery, including third-party discovery

such as the subpoena you served on the UC General Counsel's office. You may want to turn your attention to remedying that deficiency because, until you do, discovery cannot proceed.

Sincerely,

Greg Stone

**Gregory P. Stone** | **Munger, Tolles & Olson LLP**
350 South Grand Avenue | 50th Floor | Los Angeles, CA 90071
Tel: 213.683.9255 | Fax: 213.683.5155 | Cell: 213.309.5999
gregory.stone@mto.com | www.mto.com

**From:** Venkat Konda <vkonda@gmail.com>
**Sent:** Saturday, October 12, 2019 3:45 PM
**To:** Stone, Gregory <Gregory.Stone@mto.com>; Perry, Steven <Steven.Perry@mto.com>
**Cc:** Venkat Konda <vkonda@gmail.com>
**Subject:** Re: Responses to your most recent email

Dear Mr. Stone and Mr. Perry:

I have not received a response from you to my email dated October 8, 2019.

In view of your failure to respond, I have thoroughly and carefully reviewed all of my discovery requests which I have served in this case. Attached is a file with tables which show that all of the discovery requests that I served on your clients are related to liability or damages for all of my four causes of action.

The tables also list each discovery request that I served on your clients showing that the vast majority do not request confidential or highly confidential information. In fact, there are only a few discovery requests which you can argue possibly encompass confidential information. These are identified in the attached tables and would be covered by the model stipulated protective order of the Santa Clara County Superior Court which I emailed to you on September 20, 2019 (22 days ago).

Based on my analysis, there are no discovery requests for "highly confidential" information, because they do not seek information such as Flex Logix's designs or any trade secrets of your clients. Therefore, please sign the stipulated protective order that I emailed to you and provide full responses to all of my discovery requests by the response due date(s), including any information which you contend is confidential and is so marked, which I will agree to treat as confidential for now.

Based on the above, if you still want to meet and confer I will make myself available at 4:30 PM on October 18, 2019. Please let me know if I need to reserve that time on my calendar.

Very truly Yours,

Venkat Konda Ph.D.

On Tue, Oct 8, 2019 at 1:47 PM Venkat Konda <vkonda@gmail.com> wrote:

> Dear Mr. Stone:
>
> Your proposed Alternative Stipulated Protective Order is too restrictive and unacceptable.
>
> Until a protective order can be worked out between us, produce all responses to the discovery requests that you have received by the response due date. If there are any responses that you withhold on the basis of confidential or highly confidential, produce a log indicating what information and documents are begin withheld, with your responses to my discovery requests with an indication of whether being held as confidential or highly confidential.
>
> Very truly Yours,
>
> Venkat Konda Ph.D.
>
> On Tue, Oct 8, 2019 at 10:32 AM Stone, Gregory <Gregory.Stone@mto.com> wrote:
>
> > Dear Dr. Konda,
> >
> > Thank you for understanding that I am attempting to move certain things related to this litigation forward while Mr. Perry is unavailable.
> >
> > The proposed Protective Order that I sent you is substantively consistent with the double level model protective order that you obtained from the San Mateo (not Santa Clara) Superior Court. I would note that the Santa Mateo Superior Court rules explicitly provide that use of either of the two versions of protective order found on that court's website is "not required." Also, the Protective Order I sent you is, in fact, in compliance with Rules 2.550 and 2.551 of the California Rules of Court, as you will see in reviewing Section 14 of the Protective Order. Please sign and return that Protective Order to us without further delay.
> >
> > Sincerely,
> >
> > Greg Stone
> >
> > **Gregory P. Stone | Munger, Tolles & Olson LLP**
> > 350 South Grand Avenue | 50th Floor | Los Angeles, CA 90071

Tel: 213.683.9255 | Fax: 213.683.5155 | Cell: 213.309.5999
gregory.stone@mto.com | www.mto.com

**From:** Venkat Konda <vkonda@gmail.com>
**Sent:** Monday, October 7, 2019 7:20 PM
**To:** Stone, Gregory <Gregory.Stone@mto.com>; Perry, Steven <Steven.Perry@mto.com>
**Cc:** Venkat Konda <vkonda@gmail.com>
**Subject:** Re: Responses to your most recent email

Dear Mr. Stone,

I am surprised that you responded to my email directed to Mr. Perry last night to which you were copied. I have copied you on all the emails to Mr. Perry beginning on September 20, 2019. You have never responded to one of those emails until now. This is further evidence of "game-playing" on your part. You were apparently available to provide the alternative draft stipulated protective order ("ASPO"), that you emailed to me today, at a much earlier time. Instead, Mr. Perry kept saying he was too busy to send an ASPO earlier. Please reply why you didn't send your ASPO sooner.

Regarding the model stipulated protective order ('SPO") that I sent to you on September 20, 2019, if you say you need additional level of confidentiality, the Santa Clara County superior court has specific provisions for that at the following link: http://www.sanmateocourt.org/documents/complex_civil_litigation/spo_double.pdf.

You didn't do that. Therefore your proposed ASPO ignores the California Rules of Court, Rules 2.550 and 2.551.

Please explain why you ignored the California Rules of Court, Rules 2.550 and 2.551. In order to avoid further unjustified delay on your part I look forward to receiving your response immediately.

Very truly yours,

Venkat Konda, Ph.D.

On Mon, Oct 7, 2019 at 4:11 PM Stone, Gregory <Gregory.Stone@mto.com> wrote:

> Dear Dr. Konda,
>
> I am writing to follow up on Mr. Perry's email below. As he noted, the circumstances of this case necessitate some additional protections not provided for in the model protective order that you sought to adapt to this case. Among other important factors that need to be addressed are that your company competes with Flex Logix, you have asserted that you have patents that cover Flex Logix's designs, you are currently prosecuting patents that you might later argue apply to Flex Logix's designs, you are personally handling (representing yourself) two IPRs that challenge the validity of one of your patents, you claim that trade secrets have been

misappropriated by the defendants in this action, and you are proceeding in this action without a lawyer – representing yourself. Taking all of these and other considerations into account, we have drafted a proposed Protective Order that makes use of the model protective order as much as is appropriate, but that adds some additional language used in other protective orders where the circumstances are more similar to what we have here.

Please sign and return a copy of this proposed Protective Order and we will submit it to the Court for its review and approval.

Sincerely,

Greg Stone

**Gregory P. Stone** | **Munger, Tolles & Olson LLP**
350 South Grand Avenue | 50th Floor | Los Angeles, CA 90071
Tel: 213.683.9255 | Fax: 213.683.5155 | Cell: 213.309.5999
gregory.stone@mto.com | www.mto.com

---

**From:** Perry, Steven <Steven.Perry@mto.com>
**Sent:** Monday, October 7, 2019 8:00 AM
**To:** vkonda@gmail.com
**Cc:** Stone, Gregory <Gregory.Stone@mto.com>
**Subject:** Responses to your most recent email

My responses to your most recent comments are set forth below.

1. I hope that you will give us your availabilities on October 17 and 18 for the meet and confer call that I have proposed. We will do our best to work around your available times.

2. We will be providing our revised Protective Order to you in the next few days. As you probably surmised from my September 29 email, we believe that the model protective order is based on an assumption that each side has retained independent counsel who can review discovery materials that are too sensitive or confidential for the clients to review. The model order is not well suited to a trade secret case where the plaintiff is pro se, and he alleges that he or his company is in competition with the defendant. I note that California courts have held that trial courts should be careful to avoid a situation where a plaintiff is in a position to use the discovery process to review or acquire a defendant's confidential information.

3. Indeed, the automatic stay of discovery set out in C.C.P. 2019.210 is in part intended to avoid the situation addressed above, by requiring that the plaintiff identify the trade secrets at issue with particularity before discovery can be commenced. See Perlan, 178 Cal. App. 4th at 1343 (noting that the upfront particularity requirement not only helps the court in determining whether discovery requests are relevant, but it also "prevents plaintiffs from using the discovery process as a means to obtain defendants' trade secrets").

4. As I noted in my earlier email, the general allegations in your complaint (referring, for example, to "layouts" and "FPGA business models" ) are not sufficient to satisfy the requirements set out in C.C.P. section 2019.210. It is settled that in a case like this one, where the alleged trade secrets involve alleged advances in a specialized technical field, the plaintiff must segregate the alleged secrets and describe each of them with a "more exacting level of particularity...to distinguish the alleged trade secrets from matters already known to persons skilled in the field." That is a quote from the Advanced Modular case you cite. Indeed, each of the two cases that you cite, Advanced Modular and Brescia, support the defendants' position on these issues. Brescia involved a pudding recipe. Plaintiff in that case was not allowed to take discovery until after the plaintiff made three different efforts to describe the trade secrets with the necessary particularity. The court of appeal held that the trial court had properly rejected the plaintiff's first two efforts to describe its trade secrets, because the plaintiff had "attempt[ed] to evade a reasonably particularized identification by referring to the generic description in his [complaint]" and to a voluminous pile of documents. Brescia, 172 Cal. App. 4th at 143-153. That fits your current description of the allegedly misappropriated secrets to a "T." The court of appeal in Brescia noted that such "a tactic...can be prevented by requiring a clear, particularized description of the alleged trade secret sufficient to meet the statutory goals" and by recourse to sanctions "given the importance to trade secret litigation of requiring a reasonably particularized identification of the trade secret." As the Brescia court suggests, we of course reserve the right to seek sanctions should you try to pursue discovery in violation of C.C.P. 2019.210.

5. The Advanced Modular case that you cite also does not support your position. In that case, the trade secret plaintiff "refin[ed] and restat[ed] the parameters of its claimed trade secrets" three different times and submitted supporting declarations by independent experts in the particular technical field at issue. 132 Cal. App. 4th 826, 832-34. In contrast, your complaint provides only a general statement that the allegedly misappropriated trade secrets included "implementation details, technical know-how and business know-how." That general description is light years apart from the detailed identification that eventually passed muster in Advanced Modular.

6. The statutory stay of discovery applies to depositions as well as other forms of discovery. Your proposed deposition notices to Dr. Markovic and Dr. Wang would be invalid and ineffective.

7. As previously discussed, we also believe that discovery should be stayed pending the ruling on our demurrer, which is based on the four corners of the complaint and on facts conceded in that complaint. The Mattco case you cite is distinguishable, as the First District noted in Nelson v. Alaska Airlines, Inc., 2013 WL 3224989 (unpublished). The Nelson court explained that the reasoning of Mattco did not apply to a case where defendant's demurrer "raised questions of law to be determined" from the complaint itself. That is the case here and as in Nelson, a discovery stay is appropriate pending the ruling on the demurrer.

Respectfully,

Steven Perry.

On Oct 7, 2019, at 7:09 AM, Venkat Konda <vkonda@gmail.com> wrote:

Dear Mr. Perry:

I hope that your European travels are going well. That said, I am disappointed that you delayed until now to inform me of your intentions.

You indicate in your email that you "will be back in the U.S. in time to prepare and timely serve the defendants' responses to your first group of discovery requests." I demand that the defendants "timely serve" responses to all of my groups of discovery requests as they become due.

Insofar as a protective order is concerned, I sent you the Santa Clara County Superior Court model stipulated protective order ("SPO") on September 20, 2019. I then sent you a reminder on September 25, 2019. You did not respond until September 26, 2019 saying that "you had not had time to go through" it. Now you say that you "will also send you our proposed Protective Order, prior to serving our responses to those discovery requests." Your lack of diligence in responding to the SPO is unacceptable and smacks of "game-playing" on your part.

Insofar as depositions are concerned, your email states that you "will object to the deposition notices described in your e-mail if you serve them, in part because of the California law barring a plaintiff who has asserted trade secret claims from serving or pursuing any discovery requests before the plaintiff has identified with reasonable particularity each separate trade secret at issue. See Code of Civil Procedure, section 2019.210." In the first place, that section specifically provides for such a disclosure of trade secrets "subject to any orders that may be appropriate under Section 3426.5 of the Civil Code." Section 3426.5 states:

> In an action under this title, a court shall preserve the secrecy of an alleged trade secret by reasonable means, which may include granting protective orders in connection with discovery proceedings, holding in-camera hearings, sealing the records of the action, and ordering any person involved in the litigation not to disclose an alleged trade secret without prior court approval.

You threaten: "If necessary, we will file a motion for protective order that asks the court to enforce the relevant code sections. We can address these issues in the meet and confer call on the 17th or 18th." Your refusal to accept the SPO but, instead, delay discovery and the proposed meet-and-confer for a month is unacceptable.

Your dereliction in signing the SPO cannot be used to avoid my right to discovery. The right to discovery does **NOT** depend on the status of the pleadings. In Mattco Forge, Inc. v. Arthur Young & Co. (1990) 223 Cal. App. 3d 1429, 1436 sanctions were upheld for refusal to make discovery because the demurrer was pending. The court will not stay all discovery simply because a party has filed a demurrer or motion to strike. California law permits discovery to proceed while the pleadings develop. (CCP 2025.210(b); 2030.020(b); 2031.020(b); Budget Finance Plan v. Superior Court (1973) 34 Cal. App. 3d 794, 797-798.) Plaintiffs are entitled to discovery to develop their claims. (Union Mut. Life Ins. Co. v. Superior Court (1978) 80 Cal. App. 3d 1, 12. These cases dispel your mistaken belief that: "We also believe that there should be a stay of discovery until the demurrer is heard and decided…." I adamantly refuse to agree to a stay of discovery.

Your email requests that I "confirm that in conformance with section 2019.210, you are withdrawing the discovery you have served to date." You refer to Perlan Therapeutics, Inc. v. Sup. Ct. (2009) 178 Cal. App. 4th 1333, 1343 to require that I do so. I do not agree. See Advanced Modular Sputtering, Inc. v. Superior Court (2005) 132 Cal. App. 4th 826 and Brescia v. Angelin (2209) 172 Cal. App. 4th 133 (2009). The court in the latter case said: "Rather, such an explanation is required only when, given the nature of the alleged secret or the technological field in which it arises the details provided by the claimant to identify the secret

are themselves inadequate to permit the defendant to learn the boundaries of the secret and investigate defenses or to permit the court to understand the designation and fashion discovery. Further, the trade secret designation is to be liberally construed, and reasonable doubts regarding its adequacy are to be resolved in favor of allowing discovery to go forward."

My Complaint states:

> Plaintiff is the owner of Konda Tech's business plan, details of technology including all implementation details of the disclosures in Konda Tech's patents, layouts, specific architectural variations, Konda Tech's FPGA business models, and current and potential customer lists as well as Konda Tech's interaction with customers and potential customers. All these are valuable trade secrets of Konda tech (hereinafter referred to as "Konda Tech's Trade Secrets").

This description meets the requirements described in the Brescia case.

I have business negotiations the week of October 14 extending into the week of October 21 that could conflict with a meet and confer on October 17 or 18. However, I will try to be available for a call on one of those days if you tell me which of those days and what time(s) you are available for a call.

Because you have not said that the defendants are not available for depositions of October 30 and 31, I intend to notice their depositions for those dates.

Very truly yours,

Venkat Konda, Ph.D.

On Thu, Oct 3, 2019 at 7:43 AM Perry, Steven <Steven.Perry@mto.com> wrote:

> Dr. Konda:
>
> I am in Europe and will be back in the U.S. in time to prepare and timely serve the defendants' responses to your first group of discovery requests. We will also send you our proposed Protective Order, prior to serving our responses to those discovery requests, and we will be available to have a meet and confer call with you regarding the parties' proposed orders on October 17 or 18.
>
> You asked about possible depositions this month. We will object to the deposition notices described in your e-mail if you serve them, in part because of the California law barring a plaintiff who has asserted trade secret claims from serving or pursuing any discovery requests before the plaintiff has identified with reasonable particularity each separate trade secret at issue. See Code of Civil Procedure, section 2019.210. Your complaint does not do so. Moreover, the courts require, in a case like this one, that the plaintiff "segregate" each alleged trade secret in narrative form, rather than cross-referencing to other alleged trade secrets or other documents. See Perlan Therapeutics, Inc. v. Sup. Ct

(2009) 178 Cal. App. 4th 1333, 1343. Your complaint does not satisfy this requirement.

Please confirm that in conformance with section 2019.210, you are withdrawing the discovery you have served to date. If necessary, we will file a motion for protective order that asks the court to enforce the relevant code sections. We can address these issues in the meet and confer call on the 17th or 18th.

We also believe that there should be a stay of discovery until the demurrer is heard and decided, given that the demurrer is based on allegations in the complaint itself that make clear that your claims are barred because, inter alia, the applicable statutes of limitations have run and because you lack standing to assert the 17200 claim, as a matter of law. We can address those issues on the 17th or 18th as well.

The above-described objections to discovery extend to written discovery as well as depositions, and we will make those and other objections when we serve our full set of objections. All rights and defenses are reserved.

Respectfully,

Steven Perry

On Sep 30, 2019, at 10:23 PM, Venkat Konda <vkonda@gmail.com> wrote:

> Dear Mr. Perry:
>
> This is in reply to your email yesterday. What exact date are you leaving to go "overseas?" What exact date are you returning from "overseas?"
>
> In your email you referred to "motion practice." What exactly do you mean?
>
> What provisions of the model protective order adopted by the Santa Clara County Superior Court you have issues with?
>
> You didn't respond to the depositions of your clients availability on October 30 and 31. Please confirm their availability on those dates.
>
> Very truly yours,
>
> Venkat Konda, Ph.D

On Sun, Sep 29, 2019 at 3:06 PM Perry, Steven <Steven.Perry@mto.com> wrote:

> I have now reviewed enough of your discovery requests to provide a preliminary response to your email from a few days ago. I will be traveling internationally this week so I may not be able to respond to any further emails immediately.
>
> My request for a meet and confer call after I get back in the US is a good faith effort to reach an agreement that avoids motion practice by either side. Given your email below, I do not have a lot of confidence that we can reach any agreement, but we are required by the court rules to speak with each other. Please provide times on the 17th or 18th that work for you.
>
> I will send you a longer email when I get back to the states, in preparation for the call. All rights reserved at this point (for both sides). I note that none of the discovery requests require a response prior to the dates I have proposed for the call. (Please note that the 20th is not the due date, because it is a Sunday and because of the rules governing electronic service). I also note that the proposed protective order is not workable in a case involving a pro se litigant, particularly a CUTSA case involving a pro se plaintiff who claims to be a competitor of the defendants.
>
> Respectfully,
>
> Steven Perry.
>
> Sent from my iPad
>
> On Sep 27, 2019, at 6:00 AM, Venkat Konda <vkonda@gmail.com> wrote:
>
> > Mr. Perry:
> >
> > I want to be clear:
> >
> > 1. I emailed the stipulated protective order ("SPO") to you on September 20, 2019. Tomorrow, you will have had the SPO for a week to review. I also sent the original SPO to you, signed by me, on the same date (September 20) by United States Postal Service postal mail. You should have received the signed original earlier this week.
> >
> > The SPO is the "model' protective order adopted by the Santa Clara

County Superior Court, in which I sued your clients, for use in all similar cases. Please date and sign the original SPO and mail it to me by United States Postal Service postal mail without delay for filing with the court.

2. As your email acknowledges, I have served discovery requests for which responses are required from your clients by October 20, 2019, as well as additional discovery requests. The responses are crucial to my opposing the demurrer that you filed on behalf of your clients. I demand responses to my discovery requests that I served by the dates required by the California Code of Civil Procedure. Because of the demurrer, I will not grant an extension of time for your clients to respond to my discovery requests.

3. I intend to notice the depositions of your clients for October 30 and 31. Please confirm that these dates are available for their depositions.

4. In view of the above, what is the purpose of your request for a meet-and-confer call on October 17 or 18, 2019?

Very truly yours,

Venkat Konda, Ph.D

On Thu, Sep 26, 2019 at 1:18 PM Perry, Steven <Steven.Perry@mto.com> wrote:

> Dr. Konda:
>
> I have received your various discovery requests and the proposed protective order but have not yet had the time to go through them. I will be traveling overseas for the next few weeks but am taking the materials with me. I would like to set up a meet-and-confer call with you on the 17th or 18th, before the responses are due. Please let me know your availability on those days.
>
> Steven Perry

Sent from my iPad

From: **Venkat Konda** <vkonda@gmail.com>

Date: Wed, Sep 25, 2019 at 2:43 PM

Subject: Fwd: Proposed Protective Order: Dr. Konda lawsuit against Drs. Markovic and Wang - SUPERIOR COURT OF CALIFORNIA, Case No.: 19CV345846

To: <Steven.Perry@mto.com>, <gregory.stone@mto.com>

Cc: Venkat Konda <vkonda@gmail.com>

Mr. Perry:

I trust that you received the court's model protective order that I emailed to you on September 20, 2019 and also the original that I mailed to you by US Postal Service. Please let me know when I can expect a fully signed version from you.

Venkat Konda

**KONDA.2019-10-15 Trade secrets Final.pdf**
226K

# EXHIBIT 52

Gmail

**Venkat Konda <vkonda@gmail.com>**

# Konda Vs. Markovic : OPPOSITION TO DEFENDANTS' NOTICE OF MOTION AND MOTION FOR PROTECTIVE ORDER STAYING DISCOVERY PURSUANT TO CODE OF CIVIL PROCEDURE SECTIONS 2019.210 AND 2017.020-030 AND IN LIGHT OF PENDING DEMURRER

**Venkat Konda** <vkonda@gmail.com> Wed, Jan 15, 2020 at 4:17 PM
To: "Perry, Steven" <Steven.Perry@mto.com>
Cc: "Stone, Gregory" <gregory.stone@mto.com>, "Dyk, Abe" <Abraham.Dyk@mto.com>, Venkat Konda <vkonda@gmail.com>

To be clear once again, I DO object if you provide the declaration of Dr. [redacted] to Drs. Markovic and Wang, and Mr. Tate and/or any one else!

On Wed, Jan 15, 2020 at 7:05 PM Venkat Konda <vkonda@gmail.com> wrote:
> To be clear, I DO object if you provide the declaration of Dr. [redacted] to Drs. Markovic and Wang, and Mr. Tate and/or any one else?
>
> On Wed, Jan 15, 2020 at 7:01 PM Venkat Konda <vkonda@gmail.com> wrote:
> > Then my answer to your question is "NO".
> >
> > On Wed, Jan 15, 2020 at 6:54 PM Perry, Steven <Steven.Perry@mto.com> wrote:
> >
> > > Our position on that issue has not changed.
> > >
> > > **Steven M. Perry | Munger, Tolles & Olson LLP**
> > > 350 South Grand Avenue | Los Angeles, CA 90071
> > > Tel: 213 683 9133 | Fax: 213 683 5133
> > > perrysm@mto.com | www.mto.com
> > >
> > > ****NOTICE****
> > >
> > > *This message is confidential and may contain information that is privileged, attorney work product or otherwise exempt from disclosure under applicable law. It is not intended for transmission to, or receipt by, any unauthorized person. If you have received this message in error, do not read it. Please delete it without copying it, and notify the sender by reply e-mail so that our address record can be corrected. To the extent that this message or any attachment concerns tax matters, it is not intended to be used and cannot be used by a taxpayer for the purpose of avoiding penalties that may be imposed by law. Thank you.*
> > >
> > > **From:** Venkat Konda <vkonda@gmail.com>
> > > **Sent:** Wednesday, January 15, 2020 3:52 PM
> > > **To:** Perry, Steven <Steven.Perry@mto.com>
> > > **Cc:** Stone, Gregory <Gregory.Stone@mto.com>; Dyk, Abe <Abraham.Dyk@mto.com>; Venkat Konda <vkonda@gmail.com>
> > > **Subject:** Re: Konda Vs. Markovic : OPPOSITION TO DEFENDANTS' NOTICE OF MOTION AND MOTION FOR PROTECTIVE ORDER STAYING DISCOVERY PURSUANT TO CODE OF CIVIL PROCEDURE SECTIONS 2019.210 AND 2017.020-030 AND IN LIGHT OF PENDING DEMURRER
> > >
> > > One question: Are your firm and your clients willing to sign the Santa Clara County Superior Court Stipulated Protective Order I sent to you on September 20, 2019?

On Wed, Jan 15, 2020 at 6:39 PM Perry, Steven <Steven.Perry@mto.com> wrote:

> One question for now: do you object if we provide the declaration of Dr. [redacted] to Drs. Markovic and Wang, and Mr. Tate?
>
> **Steven M. Perry | Munger, Tolles & Olson LLP**
> 350 South Grand Avenue | Los Angeles, CA 90071
> Tel: 213 683 9133 | Fax: 213 683 5133
> perrysm@mto.com | www.mto.com
>
> 
>
> **From:** Venkat Konda <vkonda@gmail.com>
> **Sent:** Wednesday, January 15, 2020 3:15 PM
> **To:** Perry, Steven <Steven.Perry@mto.com>; Stone, Gregory <Gregory.Stone@mto.com>; Dyk, Abe <Abraham.Dyk@mto.com>
> **Cc:** Venkat Konda <vkonda@gmail.com>
> **Subject:** Konda Vs. Markovic : OPPOSITION TO DEFENDANTS' NOTICE OF MOTION AND MOTION FOR PROTECTIVE ORDER STAYING DISCOVERY PURSUANT TO CODE OF CIVIL PROCEDURE SECTIONS 2019.210 AND 2017.020-030 AND IN LIGHT OF PENDING DEMURRER
>
> Mr. Perry, Mr. Stone, MR. Dyk:
>
> Please see the attached.
>
> Sincerely,
>
> Venkat Konda Ph.D.

# EXHIBIT 53

# Individual Usage Details

**Device:** VENKAT KONDA | 408.472.3273

**Billing period:** Dec 17, 2019 - Jan 16, 2020
Showing details for Talk usage

| | | | |
|---|---|---|---|
| **Totals for this billing period:** | 381 calls | 2567 minutes | $0.00 |

| Date / Time | | Contact | Location | Call Type | Minutes | Charge ($) |
|---|---|---|---|---|---|---|
| [redacted] | | | | | | |
| 01/15/2020 | 09:48PM | 530.[redacted] | Incoming, CL | SDDV | 5 | 0.00 |
| [redacted] | | | | | | |
| 01/15/2020 | 09:55PM | 530.[redacted] | Incoming, CL | SDDV | 6 | 0.00 |
| [redacted] | | | | | | |
| 01/15/2020 | 10:46PM | 530.[redacted] | Incoming, CL | SDDV | 12 | 0.00 |
| [redacted] | | | | | | |
| 01/16/2020 | 08:48AM | 530.[redacted] | Davis, CA | SDDV | 17 | 0.00 |
| 01/16/2020 | 09:24AM | 530.[redacted] | Davis, CA | SDDV | 11 | 0.00 |
| [redacted] | | | | | | |

# EXHIBIT 54

Gmail

**Venkat Konda <venkat@kondatech.com>**

# Re: Attached Image

[redacted] <[redacted]> Wed, Jan 15, 2020 at 10:32 PM
To: Venkat Konda <venkat@kondatech.com>
Cc: [redacted] <[redacted]>

Dear Venkat,

I would like to withdraw my declaration from this case as upon further thoughts I do not feel confident about the validity of the statements in the declaration.

Thanks,
[redacted]
---
[redacted]
[redacted]
[redacted], Department of Computer Science
University of California, Davis
[redacted]
---

On Jan 14, 2020, at 9:03 AM, [redacted] <[redacted]> wrote:

<2066_001.pdf>