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Commissioner for Patents  
United States Patent and Trademark Office  
P.O. Box 1450  
Alexandria, VA 22313-1450  
www.uspto.gov

Konda Technologies, Inc  
6278 GRAND OAK WAY  
SAN JOSE CA 95135

**MAILED**

**AUG 19 2019**

In re Application of :  
KONDA, Venkat :  
Application No.: 12/601,275 :  
PCT No.: PCT/US08/64605 :  
Int. Filing Date: 22 May 2008 :  
Priority Date: 25 May 2007 :  
Att. Doc. No.: V-0045US :  
For: VLSI LAYOUTS OF FULLY :  
CONNECTED GENERALIZED :  
NETWORKS :

**INTERNATIONAL PATENT LEGAL ADM.**

**DECISION**

Applicant's Petition To Accept Late Payment of the Basic National Fee Under 37 CFR 1.137(a), filed in the above-captioned application on 08 August 2019 is **GRANTED.**

Applicant states that the entire delay in filing the required reply from the due date for the required reply until the filing of a grantable petition was unintentional. The proper response was previously filed on 22 December 2009. The petition fee has been furnished. A terminal disclaimer is not required as the application was filed on or after 08 June 1995. Accordingly, all requirements under 37 CFR 1.137(a) have been satisfied.

/Erin P. Thomson/  
Erin P. Thomson  
Attorney Advisor  
International Patent Legal Administration  
571-272-3292

Application Number: 12/601,275

Art Unit: 2819

Communication Dated: August 8, 2019

***In The United States Patent And Trademark Office***

Application Number: 12/601,275

Application Filed: 11/22/2009

Applicant(s): Venkat Konda

Patent No. 8,269,523

5 Title: VLSI Layouts of Fully Connected Generalized Networks Confirmation No: 6372

Examiner/Art Unit: Vibol Tan / 2819

Priority Date: 5/25/2007

San Jose, 2019 August 8

**PETITION TO ACCPET LATE PAYMENT OF THE BASIC  
10 NATIONAL FEE UNDER 37 CFR 1.137**

Attn: Richard Cole

Office of PCT Legal

Mail Stop PCT

15 Commissioner for Patents

P.O. Box 1450

Alexandria, Virginia, 22313-1450

Dear Sir/Madam:

20 For the above referenced application, please accept the payment of the basic national fee as being unintentionally delayed. The entire delay in filing the basic national fee from the due date for the fee until the filing of a grantable petition under 37 CFR 1.137 was unintentional. A check of \$1000, the small entity fee, for this petition is enclosed.

25 Very respectfully,

/Venkat Konda/

Venkat Konda

6278 Grand Oak Way

San Jose, CA 95135

30 Phone: 408-472-3273

## Electronic Patent Application Fee Transmittal

<b>Application Number:</b>	12601275			
<b>Filing Date:</b>	31-May-2010			
<b>Title of Invention:</b>	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS			
<b>First Named Inventor/Applicant Name:</b>	Venkat Konda			
<b>Filer:</b>	Venkat Konda			
<b>Attorney Docket Number:</b>	V-0045US			
Filed as Small Entity				
<b>Filing Fees for U.S. National Stage under 35 USC 371</b>				
<b>Description</b>	<b>Fee Code</b>	<b>Quantity</b>	<b>Amount</b>	<b>Sub-Total in USD(\$)</b>
<b>Basic Filing:</b>				
<b>Pages:</b>				
<b>Claims:</b>				
<b>Miscellaneous-Filing:</b>				
<b>Petition:</b>				
PET. REVIVE ABANDON APP, DELAY PYMT-RESP	2453	1	1000	1000
<b>Patent-Appeals-and-Interference:</b>				
<b>Post-Allowance-and-Post-Issuance:</b>				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
<b>Extension-of-Time:</b>				
<b>Miscellaneous:</b>				
<b>Total in USD (\$)</b>				<b>1000</b>

## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	36825423
<b>Application Number:</b>	12601275
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	6372
<b>Title of Invention:</b>	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
<b>First Named Inventor/Applicant Name:</b>	Venkat Konda
<b>Customer Number:</b>	38139
<b>Filer:</b>	Venkat Konda
<b>Filer Authorized By:</b>	
<b>Attorney Docket Number:</b>	V-0045US
<b>Receipt Date:</b>	08-AUG-2019
<b>Filing Date:</b>	31-MAY-2010
<b>Time Stamp:</b>	16:32:33
<b>Application Type:</b>	U.S. National Stage under 35 USC 371

### Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$1000
RAM confirmation Number	E201988G34075103
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

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**File Listing:**

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Petition for review by the PCT legal office	PetUnintDelay-V0045US.pdf	75026	no	1
			dc16c6a0f247024d21c0f54128af4f7c5e1ee3a0		

**Warnings:**

**Information:**

2	Fee Worksheet (SB06)	fee-info.pdf	30076	no	2
			f6cb27709e04fa0fb586944ee8732dc11110b06f		

**Warnings:**

**Information:**

<b>Total Files Size (in bytes):</b>	105102
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**This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.**

**New Applications Under 35 U.S.C. 111**

**If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.**

**National Stage of an International Application under 35 U.S.C. 371**

**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**

**New International Application Filed with the USPTO as a Receiving Office**

**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**

Application Number: 12/601,275

Art Unit: 2819

Communication Dated: August 8, 2019

***In The United States Patent And Trademark Office***

Application Number: 12/601,275

Application Filed: 11/22/2009

Applicant(s): Venkat Konda

Patent No. 8,269,523

5 Title: VLSI Layouts of Fully Connected Generalized Networks Confirmation No: 6372

Examiner/Art Unit: Vibol Tan / 2819

Priority Date: 5/25/2007

San Jose, 2019 August 8

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10 NATIONAL FEE UNDER 37 CFR 1.137**

Attn: Richard Cole

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Mail Stop PCT

15 Commissioner for Patents

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Dear Sir/Madam:

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25 Very respectfully,

/Venkat Konda/

Venkat Konda

6278 Grand Oak Way

San Jose, CA 95135

30 Phone: 408-472-3273

## Electronic Patent Application Fee Transmittal

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<b>Title of Invention:</b>	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS			
<b>First Named Inventor/Applicant Name:</b>	Venkat Konda			
<b>Filer:</b>	Venkat Konda			
<b>Attorney Docket Number:</b>	V-0045US			
Filed as Small Entity				
<b>Filing Fees for U.S. National Stage under 35 USC 371</b>				
<b>Description</b>	<b>Fee Code</b>	<b>Quantity</b>	<b>Amount</b>	<b>Sub-Total in USD(\$)</b>
<b>Basic Filing:</b>				
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PET. REVIVE ABANDON APP, DELAY PYMT-RESP	2453	1	1000	1000
<b>Patent-Appeals-and-Interference:</b>				
<b>Post-Allowance-and-Post-Issuance:</b>				



Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
<b>Extension-of-Time:</b>				
<b>Miscellaneous:</b>				
<b>Total in USD (\$)</b>				<b>1000</b>

## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	36824269
<b>Application Number:</b>	12601275
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	6372
<b>Title of Invention:</b>	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
<b>First Named Inventor/Applicant Name:</b>	Venkat Konda
<b>Customer Number:</b>	38139
<b>Filer:</b>	Venkat Konda
<b>Filer Authorized By:</b>	
<b>Attorney Docket Number:</b>	V-0045US
<b>Receipt Date:</b>	08-AUG-2019
<b>Filing Date:</b>	31-MAY-2010
<b>Time Stamp:</b>	15:45:01
<b>Application Type:</b>	U.S. National Stage under 35 USC 371

### Payment information:

Submitted with Payment	no
------------------------	----

### File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Petition for review by the PCT legal office	PetUnintDelay-V0045US.pdf	75026  dc16c6a0f247024d21c0f54128af4f7c5e1ee3a0	no	1

### Warnings:

Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30076	no	2
			b3624d1e735fe33fb3715c72a18b578c53b67b5d		
Warnings:					
Information:					
Total Files Size (in bytes):				105102	
<p><b>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</b></p> <p><b><u>New Applications Under 35 U.S.C. 111</u></b>  <b>If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</b></p> <p><b><u>National Stage of an International Application under 35 U.S.C. 371</u></b>  <b>If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</b></p> <p><b><u>New International Application Filed with the USPTO as a Receiving Office</u></b>  <b>If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</b></p>					

## PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1  
 Stylesheet Version v1.2

EPAS ID: PAT5474857

<b>SUBMISSION TYPE:</b>	NEW ASSIGNMENT
<b>NATURE OF CONVEYANCE:</b>	ASSIGNMENT
<b>CONVEYING PARTY DATA</b>	
<b>Name</b>	<b>Execution Date</b>
KONDA TECHNOLOGIES INC.	04/15/2019
<b>RECEIVING PARTY DATA</b>	
<b>Name:</b>	VENKAT KONDA
<b>Street Address:</b>	6278 GRAND OAK WAY
<b>City:</b>	SAN JOSE
<b>State/Country:</b>	CALIFORNIA
<b>Postal Code:</b>	95135
<b>PROPERTY NUMBERS Total: 2</b>	
<b>Property Type</b>	<b>Number</b>
<b>Patent Number:</b>	8269523
<b>Application Number:</b>	16202067
<b>CORRESPONDENCE DATA</b>	
<b>Fax Number:</b>	(408)238-2478
<i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i>	
<b>Phone:</b>	4084723273
<b>Email:</b>	venkat@kondatech.com
<b>Correspondent Name:</b>	KONDA TECHNOLOGIES INC.
<b>Address Line 1:</b>	6278 GRAND OAK WAY
<b>Address Line 4:</b>	SAN JOSE, CALIFORNIA 95135
<b>NAME OF SUBMITTER:</b>	VENKAT KONDA
<b>SIGNATURE:</b>	/venkat Konda/
<b>DATE SIGNED:</b>	04/15/2019
This document serves as an Oath/Declaration (37 CFR 1.63).	
<b>Total Attachments: 2</b>	
source=Konda-pat-exe#page1.tif	
source=Konda-pat-exe#page2.tif	

## ASSIGNMENT OF PATENTS

WHEREAS, Konda Technologies, Inc., a California corporation, located at 6278 Grand Oak Way, San Jose, CA 95135, hereinafter referred to as "Assignor," is the record owner of the patents described as

- 1) Title: VLSI Layouts of Fully Connected Generalized Networks  
US Patent No.: 8,269,523  
Patent Issue Date: September 18, 2012;
- 2) Title: VLSI Layouts of Fully Connected Generalized Networks  
US Patent Application No.: 16/202,067  
Patent Filing Date: November 27, 2018;

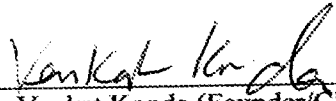
WHEREAS, Konda, Venkat of San Jose, California, having a residence at 6278 Grand Oak Way, San Jose, CA, hereinafter referred to as "ASSIGNEE," wishes to acquire all right, title and interest to and under the patents described above owned by Assignor and in and to any and all improvements to said applications and in any Letters Patent and Registrations which may be granted on the same in the United States or any country throughout the world;

For good and valuable consideration, receipt of which is hereby acknowledged by Assignor, effective 15<sup>th</sup> day of April, 2019, has assigned, and by these presents does assign to Assignee all right, title and interest for the United States and all foreign countries, in and to any and all improvements for the applications described above and in and to said applications and to all utility divisional continuing, substitute, renewal, reissue, and all other patent applications which have been or shall be filed in the United States and all foreign counterparts (including patent, utility model and industrial designs), and in and to any Letters Patent and Registrations which may hereafter be granted on the same in the United States and all countries throughout the world, and to claim the priority from the application as provided by the Paris Convention. The right, title and interest is to be held and enjoyed by Assignee and Assignee's successors and assigns as fully and exclusively as it would have been held and enjoyed by Assignor had this Assignment not been made, for the full term of any Letters Patent and Registrations which may be granted thereon, or of any division, renewal, continuation in whole or in part, substitution, conversion, reissue, prolongation or extension thereof.

Assignor further agrees that they will, without charge to Assignee, but at Assignee's expense, (a) cooperate with Assignee in the prosecution of U.S. Patent applications and foreign counterparts on the applications and any improvements, (b) execute, verify, acknowledge and deliver all such further papers, including patent applications and instruments of transfer, and (c) perform such other acts as Assignee lawfully may request to obtain or maintain Letters Patent and Registrations for the applications and improvements in any and all countries, and to vest title thereto in Assignee, or Assignee's successors and assigns.

IN TESTIMONY WHEREOF, Assignor has signed on the date indicated.

Date: 4/15/2019

By:   
Venkat Konda (Founder/CEO)  
Konda Technologies Inc.  
6278 Grand Oak Way  
San Jose, CA 95135



APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/601,275	09/18/2012	8269523	V-0045US	6372

38139 7590 08/29/2012  
Konda Technologies, Inc  
6278 GRAND OAK WAY  
SAN JOSE, CA 95135

### ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

#### **Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)** (application filed on or after May 29, 2000)

The Patent Term Adjustment is 183 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Venkat Konda, San Jose, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit [SelectUSA.gov](http://SelectUSA.gov).

Change(s) applied  
to document,  
/D.H.P./  
6/29/2012

This application is related to and incorporates by reference in its entirety the US  
 Patent Application <sup>12/601273</sup> ~~Docket No. V-0038US~~ entitled "FULLY CONNECTED  
 GENERALIZED BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned  
 to the same assignee as the current application filed concurrently, the PCT Application  
 5 Serial No. PCT/US08/64603 entitled "FULLY CONNECTED GENERALIZED  
 BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same  
 assignee as the current application, filed May 22, 2008, the U.S. Provisional Patent  
 Application Serial No. 60/940, 387 entitled "FULLY CONNECTED GENERALIZED  
 BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same  
 10 assignee as the current application, filed May 25, 2007, and the U.S. Provisional Patent  
 Application Serial No. 60/940, 390 entitled "FULLY CONNECTED GENERALIZED  
 MULTI-LINK BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to  
 the same assignee as the current application, filed May 25, 2007.

This application is related to and incorporates by reference in its entirety the US  
 Patent Application <sup>12/601274</sup> ~~Docket No. V-0039US~~ entitled "FULLY CONNECTED  
 15 GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda  
 assigned to the same assignee as the current application filed concurrently, the PCT  
 Application Serial No. PCT/US08/64604 entitled "FULLY CONNECTED  
 GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda  
 20 assigned to the same assignee as the current application, filed May 22, 2008, the U.S.  
 Provisional Patent Application Serial No. 60/940, 389 entitled "FULLY CONNECTED  
 GENERALIZED REARRANGEABLY NONBLOCKING MULTI-LINK MULTI-  
 STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current  
 application, filed May 25, 2007, the U.S. Provisional Patent Application Serial No.  
 25 60/940, 391 entitled "FULLY CONNECTED GENERALIZED FOLDED MULTI-  
 STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current  
 application, filed May 25, 2007 and the U.S. Provisional Patent Application Serial No.  
 60/940, 392 entitled "FULLY CONNECTED GENERALIZED STRICTLY  
 NONBLOCKING MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda  
 30 assigned to the same assignee as the current application, filed May 25, 2007.



**PART B - FEE(S) TRANSMITTAL**

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE  
 Commissioner for Patents  
 P.O. Box 1450  
 Alexandria, Virginia 22313-1450  
 or Fax (571) 273-2885**

**INSTRUCTIONS:** This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

**Certificate of Mailing or Transmission**

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/601,275	5/31/2010	Venkat Konda	V-0045US	6372

TITLE OF INVENTION:

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$870	\$300	\$1170	8/17/2012
EXAMINER		ART UNIT	CLASS-SUBCLASS		

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).  
 Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.  
 "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list  
 (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1\_  
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2\_  
 3\_

**3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)**

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: **Konda Technologies Inc.**  
 (B) RESIDENCE: (CITY and STATE OR COUNTRY) **San Jose, CA**

Please check the appropriate assignee category or categories (will not be printed on the patent) :  Individual  Corporation or other private group entity  Government

4a. The following fee(s) are enclosed:  
 Issue Fee  
 Publication Fee (No small entity discount permitted)  
 Advance Order - # of Copies \_

4b. Payment of Fee(s):  
 A check in the amount of the fee(s) is enclosed.  
 Payment by credit card. Form PTO-2038 is attached.  
 The Director is hereby authorized to charge the required fee(s), or credit any overpayment, to Deposit Account Number

**5. Change in Entity Status (from status indicated above)**

a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.  b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above. NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature **/Venkat Konda/** Date **8/15/2012**  
 Typed or printed name **Venkat Konda** Registration No.

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

## Privacy Act Statement

**The Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

## Electronic Patent Application Fee Transmittal

<b>Application Number:</b>	12601275
<b>Filing Date:</b>	31-May-2010
<b>Title of Invention:</b>	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
<b>First Named Inventor/Applicant Name:</b>	Venkat Konda
<b>Filer:</b>	Venkar Konda
<b>Attorney Docket Number:</b>	V-0045US

Filed as Small Entity

### U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
<b>Basic Filing:</b>				
<b>Pages:</b>				
<b>Claims:</b>				
<b>Miscellaneous-Filing:</b>				
Publ. Fee- early, voluntary, or normal	1504	1	300	300
<b>Petition:</b>				
<b>Patent-Appeals-and-Interference:</b>				
<b>Post-Allowance-and-Post-Issuance:</b>				
Utility Appl issue fee	2501	1	870	870

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
<b>Extension-of-Time:</b>				
<b>Miscellaneous:</b>				
<b>Total in USD (\$)</b>				<b>1170</b>

## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	13505897
<b>Application Number:</b>	12601275
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	6372
<b>Title of Invention:</b>	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
<b>First Named Inventor/Applicant Name:</b>	Venkat Konda
<b>Customer Number:</b>	38139
<b>Filer:</b>	Venkar Konda
<b>Filer Authorized By:</b>	
<b>Attorney Docket Number:</b>	V-0045US
<b>Receipt Date:</b>	15-AUG-2012
<b>Filing Date:</b>	31-MAY-2010
<b>Time Stamp:</b>	16:44:45
<b>Application Type:</b>	U.S. National Stage under 35 USC 371

### Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$1170
RAM confirmation Number	3603
Deposit Account	
Authorized User	

### File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1	Issue Fee Payment (PTO-85B)	ptol85b-V0045US.pdf	223614	no	2
			d281677872396a8b938dae41e9e9f2f113d9568		
<b>Warnings:</b>					
<b>Information:</b>					
2	Fee Worksheet (SB06)	fee-info.pdf	31848	no	2
			0d3037333ad300df6fcb48c6df4c5fc1941faee5		
<b>Warnings:</b>					
<b>Information:</b>					
<b>Total Files Size (in bytes):</b>			255462		

**This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.**

**New Applications Under 35 U.S.C. 111**

**If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.**

**National Stage of an International Application under 35 U.S.C. 371**

**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**

**New International Application Filed with the USPTO as a Receiving Office**

**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**



UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

38139 7590 05/17/2012
Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

EXAMINER
TAN, VIBOL
ART UNIT PAPER NUMBER

2819
DATE MAILED: 05/17/2012

Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO.

12/601,275 05/31/2010 Venkat Konda V-0045US 6372
TITLE OF INVENTION: VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS

Table with 7 columns: APPLN. TYPE, SMALL ENTITY, ISSUE FEE DUE, PUBLICATION FEE DUE, PREV. PAID ISSUE FEE, TOTAL FEE(S) DUE, DATE DUE

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.
If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:
A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.
B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:
A. Pay TOTAL FEE(S) DUE shown above, or
B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

**PART B - FEE(S) TRANSMITTAL**

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE  
 Commissioner for Patents  
 P.O. Box 1450  
 Alexandria, Virginia 22313-1450  
 or Fax (571)-273-2885**

**INSTRUCTIONS:** This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

38139 7590 05/17/2012  
**Konda Technologies, Inc**  
 6278 GRAND OAK WAY  
 SAN JOSE, CA 95135

**Certificate of Mailing or Transmission**

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/601,275	05/31/2010	Venkat Konda	V-0045US	6372

TITLE OF INVENTION: VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$870	\$300	\$0	\$1170	08/17/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
TAN, VIBOL	2819	326-041000

<p>1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).</p> <p><input type="checkbox"/> Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.</p> <p><input type="checkbox"/> "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. <b>Use of a Customer Number is required.</b></p>	<p>2. For printing on the patent front page, list</p> <p>(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____</p> <p>(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____</p> <p>3 _____</p>
---	---

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE \_\_\_\_\_ (B) RESIDENCE: (CITY and STATE OR COUNTRY) \_\_\_\_\_

Please check the appropriate assignee category or categories (will not be printed on the patent) :  Individual  Corporation or other private group entity  Government

<p>4a. The following fee(s) are submitted:</p> <p><input type="checkbox"/> Issue Fee</p> <p><input type="checkbox"/> Publication Fee (No small entity discount permitted)</p> <p><input type="checkbox"/> Advance Order - # of Copies _____</p>	<p>4b. Payment of Fee(s); (Please first reapply any previously paid issue fee shown above)</p> <p><input type="checkbox"/> A check is enclosed.</p> <p><input type="checkbox"/> Payment by credit card. Form PTO-2038 is attached.</p> <p><input type="checkbox"/> The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).</p>
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5. Change in Entity Status (from status indicated above)

a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.  b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature \_\_\_\_\_ Date \_\_\_\_\_

Typed or printed name \_\_\_\_\_ Registration No. \_\_\_\_\_

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.





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www.uspto.gov

Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO.
12/601,275 05/31/2010 Venkat Konda V-0045US 6372

38139 7590 05/17/2012
Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

Table with 2 columns: EXAMINER, ART UNIT, PAPER NUMBER
EXAMINER: TAN, VIBOL
ART UNIT: 2819
PAPER NUMBER: (empty)

DATE MAILED: 05/17/2012

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 183 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 183 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

## Privacy Act Statement

**The Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

**Notice of Allowability**

**Application No.**

12/601,275

**Examiner**

Vibol Tan

**Applicant(s)**

KONDA, VENKAT

**Art Unit**

2819

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

- 1.  This communication is responsive to amendment filed 5/8/12.
- 2.  An election was made by the applicant in response to a restriction requirement set forth during the interview on \_\_\_\_\_; the restriction requirement and election have been incorporated into this action.
- 3.  The allowed claim(s) is/are 1 and 3-49.
- 4.  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a)  All    b)  Some\*    c)  None    of the:
    - 1.  Certified copies of the priority documents have been received.
    - 2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_ .
    - 3.  Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has **THREE MONTHS FROM THE "MAILING DATE"** of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

- 5.  A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
  - 6.  CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
    - (a)  including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      - 1)  hereto or 2)  to Paper No./Mail Date \_\_\_\_\_.
    - (b)  including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**
- 7.  DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

- 1.  Notice of References Cited (PTO-892)
- 2.  Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3.  Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date \_\_\_\_\_
- 4.  Examiner's Comment Regarding Requirement for Deposit of Biological Material
- 5.  Notice of Informal Patent Application
- 6.  Interview Summary (PTO-413), Paper No./Mail Date \_\_\_\_\_ .
- 7.  Examiner's Amendment/Comment
- 8.  Examiner's Statement of Reasons for Allowance
- 9.  Other \_\_\_\_\_.

***Allowable Subject Matter***

1. The following is an examiner's statement of reasons for allowance: in combination with other limitations of the claims, the cited prior arts fail to teach said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks which are either placed vertically above or below, or placed horizontally to the left or to the right, each said plurality of sub-integrated circuit blocks comprising same number of said staves and said switches in each said stage, regardless of the size of said two-dimensional grid so that each said plurality of sub-integrated circuit block with its corresponding said stages and said switches in each stage is replicable in both vertical direction or horizontal direction of said two-dimensional grid, as required by amended claim 1.

2. Claims 1 and 3-49 are now in condition for allowance.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571)272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

Art Unit: 2819

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shawki Ismail can be reached on (571) 272-3985. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Vibol Tan/  
Primary Examiner, Art Unit 2819



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BIB DATA SHEET

CONFIRMATION NO. 6372

<b>SERIAL NUMBER</b> 12/601,275	<b>FILING or 371(c) DATE</b> 05/31/2010 <b>RULE</b>	<b>CLASS</b> 326	<b>GROUP ART UNIT</b> 2819	<b>ATTORNEY DOCKET NO.</b> V-0045US	
<b>APPLICANTS</b> Venkat Konda, San Jose, CA;					
** <b>CONTINUING DATA</b> ***** This application is a 371 of PCT/US08/64605 05/22/2008 which claims benefit of 60/940,394 05/25/2007					
** <b>FOREIGN APPLICATIONS</b> *****					
** <b>IF REQUIRED, FOREIGN FILING LICENSE GRANTED</b> ** ** SMALL ENTITY ** 04/08/2010					
Foreign Priority claimed <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No 35 USC 119(a-d) conditions met <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No Verified and Acknowledged <u>/VIBOL TAN/</u> Examiner's Signature	<input type="checkbox"/> Met after Allowance VTan Initials	<b>STATE OR COUNTRY</b> CA	<b>SHEETS DRAWINGS</b> 39	<b>TOTAL CLAIMS</b> 49	<b>INDEPENDENT CLAIMS</b> 1
<b>ADDRESS</b> Konda Technologies, Inc 6278 GRAND OAK WAY SAN JOSE, CA 95135 UNITED STATES					
<b>TITLE</b> VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS					
<b>FILING FEE RECEIVED</b> 1279	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit		

## EAST Search History

## EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S25	35	(US-20080267182-\$ or US-20040114586-\$ or US-20030021267-\$ or US-20030112797-\$ or US-20030053456-\$ or US-20020051447-\$ or US-20020031118-\$ or US-20020031117-\$).did. or (US-8098081-\$ or US-7924052-\$ or US-7468974-\$ or US-7424011-\$ or US-7424010-\$ or US-7397796-\$ or US-7349387-\$ or US-7346049-\$ or US-7130920-\$ or US-6567858-\$ or US-7136380-\$ or US-6456838-\$ or US-6157643-\$ or US-6049542-\$ or US-5856977-\$ or US-5406556-\$ or US-4813038-\$ or US-7139266-\$ or US-7103059-\$ or US-7099314-\$ or US-7065074-\$ or US-7050429-\$ or US-7042873-\$ or US-7031303-\$ or US-7016345-\$ or US-6952418-\$).did. or (US-6201808-\$).did.	US-PGPUB; USPAT	OR	OFF	2012/05/08 15:44
S26	42	konda-venkat.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/05/08 15:44
S27	84	(routing adj network) and (multicast adj connections)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/05/08 15:58
S28	1365	(routing adj network) and (inputs) and (outputs)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/05/08 15:59
S29	229142	(("326") or ("370")).CLAS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/05/08 15:59
S30	693	S28 and S29	US-PGPUB; USPAT; USOCR; FPRS;	OR	OFF	2012/05/08 15:59


			EPO; JPO; DERWENT; IBM_TDB			
S31	380	S30 and links	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/05/08 16:00
S32	1	S30 and (straight adj links) and (vertical adj links) and (horizontal adj links)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/05/08 16:01
S33	1	((straight adj links) and (vertical adj links) and (horizontal adj links)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/05/08 16:02

**EAST Search History (Interference)**

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**5/ 10/ 2012 7:09:30 AM****C:\ Users\ vtan\ Documents\ EAST\ Workspaces\ 12601275.wsp**



<b>Search Notes</b>  	<b>Application/Control No.</b>  12601275	<b>Applicant(s)/Patent Under Reexamination</b>  KONDA, VENKAT
	<b>Examiner</b>  VIBOL TAN	<b>Art Unit</b>  2819


SEARCHED			
Class	Subclass	Date	Examiner
326	38-41	2/2/12	VTan
370	390, 312, 360, 388, 412	2/2/12	VTan

SEARCH NOTES		
Search Notes	Date	Examiner
Inventor search	2/2/12	VTan
search report pct/us2008/064605	2/1/12	VTan
EAST text search	2/2/12	VTan
EAST text update	5/8/12	VTan

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
uspgpub, uspat & upad	text search	5/8/12	VTan

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<b>Index of Claims</b>  	<b>Application/Control No.</b> 12601275	<b>Applicant(s)/Patent Under Reexamination</b> KONDA, VENKAT
	<b>Examiner</b> VIBOL TAN	<b>Art Unit</b> 2819

✓	<b>Rejected</b>
=	<b>Allowed</b>

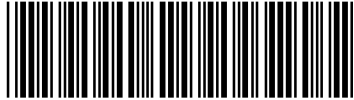
-	<b>Cancelled</b>
÷	<b>Restricted</b>

N	<b>Non-Elected</b>
I	<b>Interference</b>

A	<b>Appeal</b>
O	<b>Objected</b>

Claims renumbered in the same order as presented by applicant
  CPA
  T.D.
  R.1.47

CLAIM		DATE							
Final	Original	05/08/2012							
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<b><i>Index of Claims</i></b>  	<b>Application/Control No.</b> 12601275	<b>Applicant(s)/Patent Under Reexamination</b> KONDA, VENKAT
	<b>Examiner</b> VIBOL TAN	<b>Art Unit</b> 2819

✓	<b>Rejected</b>
=	<b>Allowed</b>

-	<b>Cancelled</b>
÷	<b>Restricted</b>

N	<b>Non-Elected</b>
I	<b>Interference</b>

A	<b>Appeal</b>
O	<b>Objected</b>

Claims renumbered in the same order as presented by applicant
  CPA
  T.D.
  R.1.47

CLAIM		DATE							
Final	Original	05/08/2012							
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	46	=							
	47	=							
	48	=							

*In The United States Patent And Trademark Office*

Application Number: 12/601,275  
Application Filed: 11/22/2009  
5 Applicant(s): Venkat Konda  
Title: VLSI Layouts of Fully Connected Generalized Networks  
Examiner/Art Unit: Vibol Tan / 2819  
International Application Number: PCT/US08/64605  
International Application Filed: 5/22/2008  
10 Priority Date: 5/25/2007

San Jose, 2012 May 8, Tue

**SUPPLEMENTAL AMENDMENT**

(and the response to office letter dated 2/7/2012)

15

Mail Stop Amendment

Commissioner for Patents

P.O. Box 1450

Alexandria, Virginia, 22313-1450

20

Dear Sir/Madam:

In response to the office action mailed 2012 February 7, Applicant has submitted Amendment A on April 30, 2012. In the Amendment A filed on April 30, 2012,

SUPPLEMENTAL AMENDMENT, Contd.

Applicant has made mistakes with the format of the claims and not identifying the cancelled claim. To correct those mistakes, please consider the following Supplemental Amendment.

5 AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

SUPPLEMENTAL AMENDMENT, Contd.

CLAIMS

What is claimed is:

1. (currently amended): An integrated circuit device comprising a plurality of sub-integrated circuit blocks and a routing network, and
- 5 Said each plurality of sub-integrated circuit blocks comprising a plurality of inlet links and a plurality of outlet links; and
- ~~Said routing network interconnects any one of said outlet link of one of said sub-integrated circuit block to one or more said inlet links of one or more of said sub-integrated circuit blocks; and~~
- 10 Said routing network comprising of a plurality of stages  $y$ , in each said sub-integrated circuit block, starting from the lowest stage of 1 to the highest stage of  $y$ , where  $y \geq 1$ ; and
- Said routing network comprising a plurality of switches of size  $d \times d$ , where  $d \geq 2$ , in each said stage and each said switch of size  $d \times d$  having  $d$  inlet links and  $d$
- 15 outlet links; and
- ~~Said each sub-integrated circuit block comprising a plurality of said switches corresponding to each said stage; and~~
- Said plurality of outlet links of said each sub-integrated circuit block are directly connected to said inlet links of said switches of its corresponding said lowest stage of 1, and said plurality of inlet links of said each sub-integrated circuit block are directly
- 20 connected from said outlet links of said switches of its corresponding said lowest stage of 1; and
- Said each sub-integrated circuit block comprising a plurality of forward connecting links connecting from switches in a lower stage to switches in the its
- 25 immediate succeeding higher stage, and also comprising a plurality of backward connecting links connecting from switches in a higher stage to switches in the its immediate preceding lower stage; and

SUPPLEMENTAL AMENDMENT, Contd.

Said each sub-integrated circuit block comprising a plurality straight links in said forward connecting links from switches in said each lower stage to switches in ~~the~~ its immediate succeeding higher stage and a plurality cross links in said forward connecting links from switches in said each lower stage to switches in ~~the~~ its immediate succeeding higher stage, and further comprising a plurality of straight links in said backward connecting links from switches in said each higher stage to switches in ~~the~~ its immediate preceding lower stage and a plurality of cross links in said backward connecting links from switches in said each higher stage to switches in ~~the~~ its immediate preceding lower stage,

10 said plurality of sub-integrated circuit blocks arranged in a two-dimensional grid of rows and columns, and

said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and said all cross links are connecting as either vertical or horizontal links between switches  
15 in two different said sub-integrated circuit blocks which are either placed vertically above or below, or placed horizontally to the left or to the right,

each said plurality of sub-integrated circuit blocks comprising same number of said stages and said switches in each said stage, regardless of the size of said two-dimensional grid so that each said plurality of sub-integrated circuit block with its  
20 corresponding said stages and said switches in each stage is replicable in both vertical direction or horizontal direction of said two-dimensional grid.

2. (cancelled): ~~The integrated circuit device of claim 1, wherein said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and~~  
25 ~~and~~

~~said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks.~~

3. (currently amended): The integrated circuit device of claim 1, ~~wherein said plurality of sub-integrated circuit blocks arranged in a two-dimensional grid~~



SUPPLEMENTAL AMENDMENT, Contd.

said two-dimensional grid of said sub-integrated circuit blocks with their corresponding said stages and said switches in each stage is scalable by any power of 2, and,

for each multiplication of 2 of the size of total said sub-integrated circuit blocks,  
5 by adding one more stage of switches and the layout is placed in hypercube format and also the cross links between said one more stage of switches are connected in hypercube format.

4. (Original): The integrated circuit device of claim 3, wherein said cross links in succeeding stages are connecting as alternative vertical and horizontal links  
10 between switches in said sub-integrated circuit blocks.

5. (Original): The integrated circuit device of claim 4, wherein said cross links from switches in a stage in one of said sub-integrated circuit blocks are connecting to switches in the succeeding stage in another of said sub-integrated circuit blocks so that said cross links are either vertical links or horizontal and vice versa, and hereinafter such  
15 cross links are “shuffle exchange links”).

6. (Original): The integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are substantially of equal length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are substantially  
20 of equal length in the entire said integrated circuit device.

7. (Original): The integrated circuit device of claim 6, wherein the shortest horizontal shuffle exchange links are connecting at the lowest stage and between switches in two nearest neighboring said sub-integrated circuit blocks, and length of the horizontal shuffle exchange links is doubled in each succeeding stage; and the shortest vertical  
25 shuffle exchange links are connecting at the lowest stage and between switches in two nearest neighboring said sub-integrated circuit blocks, and length of the vertical shuffle exchange links is doubled in each succeeding stage.

SUPPLEMENTAL AMENDMENT, Contd.

8. (currently amended): The integrated circuit device of claim 7, wherein  $y \geq (\log_2 N)$ , where  $N > 1$ , so that the length of the horizontal shuffle exchange links in the highest stage is equal to half the size of the horizontal size of said two dimensional grid of sub-integrated circuit blocks and the length of the vertical shuffle exchange links  
5 in the highest stage is equal to half the size of the vertical size of said two dimensional grid of sub-integrated circuit blocks.

9. (Original): The integrated circuit device of claim 8, wherein  $d = 2$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage  
10 in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast Benes network with full bandwidth.

10. (Original): The integrated circuit device of claim 8, wherein  $d = 2$  and there are at least two switches in each said stage in each said sub-integrated circuit block  
15 connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast Benes network and rearrangeably nonblocking for arbitrary fan-out multicast Benes network with full  
bandwidth.

20 11. (Original): The integrated circuit device of claim 8, wherein  $d = 2$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links  
and said routing network is strictly nonblocking for arbitrary fan-out multicast Benes  
25 network with full bandwidth.

12. (currently amended): The integrated circuit device of claim 7, wherein  $y \geq (\log_2 N)$ , where  $N > 1$ , so that the length of the horizontal shuffle exchange links in the highest stage is equal to half the size of the horizontal size of said two dimensional grid of sub-integrated circuit blocks and the length of the vertical shuffle exchange links

SUPPLEMENTAL AMENDMENT, Contd.

in the highest stage is equal to half the size of the vertical size of said two dimensional grid of sub-integrated circuit blocks, and

said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks.

5           13. (Original): The integrated circuit device of claim 12, wherein  $d = 2$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast butterfly fat tree network  
10 with full bandwidth.

          14. (Original): The integrated circuit device of claim 12, wherein  $d = 2$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links  
15 and said routing network is strictly nonblocking for unicast butterfly fat tree network and rearrangeably nonblocking for arbitrary fan-out multicast butterfly fat tree network with full bandwidth.

          15. (Original): The integrated circuit device of claim 12, wherein  $d = 2$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links  
20 and said routing network is strictly nonblocking for arbitrary fan-out multicast butterfly fat tree network with full bandwidth.

          16. (Original): The integrated circuit device of claim 1, wherein said  
25 horizontal and vertical links are implemented on two or more metal layers.

SUPPLEMENTAL AMENDMENT, Contd.

17. (Original): The integrated circuit device of claim 1, wherein said switches comprising active and reprogrammable cross points and said each cross point is programmable by an SRAM cell or a Flash Cell.
18. (Original): The integrated circuit device of claim 1, wherein said sub-  
5 integrated circuit blocks are of equal die size.
19. (Original): The integrated circuit device of claim 16, wherein said sub-integrated circuit blocks are Lookup Tables (hereinafter "LUTs") and said integrated circuit device is a field programmable gate array (FPGA) device or field programmable gate array (FPGA) block embedded in another integrated circuit device.
- 10 20. (Original): The integrated circuit device of claim 16, wherein said sub-integrated circuit blocks are AND or OR gates and said integrated circuit device is a programmable logic device (PLD).
21. (Original): The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks comprising any arbitrary hardware logic or memory circuits.
- 15 22. (Original): The integrated circuit device of claim 1, wherein said switches comprising active one-time programmable cross points and said integrated circuit device is a mask programmable gate array (MPGA) device or a structured ASIC device.
23. (Original): The integrated circuit device of claim 1, wherein said switches comprising passive cross points or just connection of two links or not and said integrated  
20 circuit device is a Application Specific Integrated Circuit (ASIC) device.
24. (Original): The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks further recursively comprise one or more super-sub-integrated circuit blocks and a sub-routing network.
25. (currently amended): The integrated circuit device of claim 5, wherein  
25 said all horizontal shuffle exchange links between switches in any two corresponding said

SUPPLEMENTAL AMENDMENT, Contd.

succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and  $y \geq (\log_2 N)$ , where  $N > 1$ .

26. (Original): The integrated circuit device of claim 25, wherein  $d = 2$  and  
5 there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized multi-stage network with full bandwidth.

10 27. (Original): The integrated circuit device of claim 25, wherein  $d = 2$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized multi-stage  
15 network and rearrangeably nonblocking for arbitrary fan-out multicast generalized multi-stage network with full bandwidth.

28. (Original): The integrated circuit device of claim 25, wherein  $d = 2$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said  
20 stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized multi-stage network with full bandwidth.

29. (currently amended): The integrated circuit device of claim 5, wherein  
25 said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and  $y \geq (\log_2 N)$ , where  $N > 1$ , and

said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks.

SUPPLEMENTAL AMENDMENT, Contd.

30. (Original): The integrated circuit device of claim 29, wherein  $d = 2$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and  
5 said routing network is rearrangeably nonblocking for unicast generalized butterfly fat tree network with full bandwidth.

31. (Original): The integrated circuit device of claim 29, wherein  $d = 2$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said  
10 stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized butterfly fat tree Network and rearrangeably nonblocking for arbitrary fan-out multicast generalized butterfly fat tree network with full bandwidth.

32. (Original): The integrated circuit device of claim 29, wherein  $d = 2$  and  
15 there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized butterfly fat tree network with full bandwidth.

20 33. (Original): The integrated circuit device of claim 1, wherein said straight links connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and  
said cross links are connecting as vertical or horizontal or diagonal links between two different said sub-integrated circuit blocks.

25 34. (Original): The integrated circuit device of claim 8, wherein  $d = 4$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and

SUPPLEMENTAL AMENDMENT, Contd.

said routing network is rearrangeably nonblocking for unicast multi-link Benes network with full bandwidth.

35. (Original): The integrated circuit device of claim 8, wherein  $d = 4$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast multi-link Benes network and rearrangeably nonblocking for arbitrary fan-out multicast multi-link Benes network with full bandwidth.

36. (Original): The integrated circuit device of claim 8, wherein  $d = 4$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast multi-link Benes network with full bandwidth.

37. (Original): The integrated circuit device of claim 12, wherein  $d = 4$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast multi-link butterfly fat tree network with full bandwidth.

38. (Original): The integrated circuit device of claim 12, wherein  $d = 4$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast multi-link butterfly fat tree network and rearrangeably nonblocking for arbitrary fan-out multicast multi-link butterfly fat tree network with full bandwidth.

SUPPLEMENTAL AMENDMENT, Contd.

39. (Original): The integrated circuit device of claim 12, wherein  $d = 4$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links  
5 and said routing network is strictly nonblocking for arbitrary fan-out multicast multi-link butterfly fat tree network with full bandwidth.

40. (currently amended): The integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between  
10 switches in any two corresponding said succeeding stages are of different length and  $y \geq (\log_2 N)$ , where  $N > 1$ .

41. (Original): The integrated circuit device of claim 40, wherein  $d = 4$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage  
15 in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized multi-link multi-stage network with full bandwidth.

42. (Original): The integrated circuit device of claim 40, wherein  $d = 4$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said  
20 stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized multi-link multi-stage network and rearrangeably nonblocking for arbitrary fan-out multicast generalized multi-link multi-stage network with full bandwidth.

43. (Original): The integrated circuit device of claim 40, wherein  $d = 4$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said  
25 stage in each said sub-integrated circuit block connecting said backward connecting links



SUPPLEMENTAL AMENDMENT, Contd.

and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized multi-link multi-stage network with full bandwidth.

44. (currently amended): The integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and  $y \geq (\log_2 N)$ , where  $N > 1$ , and

said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks.

45. (Original): The integrated circuit device of claim 44, wherein  $d = 4$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized multi-link butterfly fat tree network with full bandwidth.

46. (Original): The integrated circuit device of claim 44, wherein  $d = 4$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized multi-link butterfly fat tree Network and rearrangeably nonblocking for arbitrary fan-out multicast generalized multi-link butterfly fat tree network with full bandwidth.

47. (Original): The integrated circuit device of claim 44, wherein  $d = 4$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized multi-link butterfly fat tree network with full bandwidth.

SUPPLEMENTAL AMENDMENT, Contd.

48. (currently amended): The integrated circuit device of claim 1, wherein said plurality of forward connecting links use a plurality of buffers to amplify signals driven through them and said plurality of backward connecting links use a plurality of buffers to amplify signals driven through them; and said buffers can be inverting or non-  
5 inverting buffers.

49. (currently amended): The integrated circuit device of claim 1, wherein said ~~wherein said~~ all switches of size  $d \times d$  are either fully populated or partially populated.

SUPPLEMENTAL AMENDMENT, Contd.

**CONCLUSION**

For all of the above reasons, applicant submits that the Claims are now in proper form, and that the Claims all define patentably over the prior art. Therefore applicant submits that this application is now in condition for allowance, which action he  
5 respectfully solicits.

**Conditional request for Constructive Assistance**

Applicant has amended the claims of this application so that they are proper, definite, and define novel structure which is also unobvious. If, for any reason this application is not believed to be in full condition for allowance, applicant respectfully request the  
10 constructive assistance and suggestions of the Examiner pursuant to M.P.E.P § 2173.02 and § 707.07(j) in order that the undersigned can place this application in allowable condition as soon as possible and without the need for further proceedings.

Very respectfully,

15 /Venkat Konda/

Venkat Konda

Konda Technologies, Inc (USPTO Customer Number: 38139)

6278 Grand Oak Way

San Jose, CA 95135

20 Phone: 408-472-3273

Fax: 408-238-2478

## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	12733551
<b>Application Number:</b>	12601275
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	6372
<b>Title of Invention:</b>	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
<b>First Named Inventor/Applicant Name:</b>	Venkat Konda
<b>Customer Number:</b>	38139
<b>Filer:</b>	Venkar Konda
<b>Filer Authorized By:</b>	
<b>Attorney Docket Number:</b>	V-0045US
<b>Receipt Date:</b>	08-MAY-2012
<b>Filing Date:</b>	31-MAY-2010
<b>Time Stamp:</b>	22:22:15
<b>Application Type:</b>	U.S. National Stage under 35 USC 371

### Payment information:

Submitted with Payment	no
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### File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Supplemental Response or Supplemental Amendment	SuppleAmend-V0045US.pdf	144109 <small>3e7bd4b5740546aeb12e5e0cfd93e5979edc5277</small>	no	15

### Warnings:

### Information:

**This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.**

**New Applications Under 35 U.S.C. 111**

**If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.**

**National Stage of an International Application under 35 U.S.C. 371**

**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**

**New International Application Filed with the USPTO as a Receiving Office**

**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**

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<b>PATENT APPLICATION FEE DETERMINATION RECORD</b> Substitute for Form PTO-875	Application or Docket Number <b>12/601,275</b>	Filing Date <b>05/31/2010</b>	<input type="checkbox"/> To be Mailed
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APPLICATION AS FILED – PART I			OTHER THAN SMALL ENTITY				
	(Column 1)	(Column 2)	SMALL ENTITY <input checked="" type="checkbox"/>	OR			
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)
<input type="checkbox"/> BASIC FEE <small>(37 CFR 1.16(a), (b), or (c))</small>	N/A	N/A	N/A			N/A	
<input type="checkbox"/> SEARCH FEE <small>(37 CFR 1.16(k), (j), or (m))</small>	N/A	N/A	N/A			N/A	
<input type="checkbox"/> EXAMINATION FEE <small>(37 CFR 1.16(o), (p), or (q))</small>	N/A	N/A	N/A			N/A	
TOTAL CLAIMS <small>(37 CFR 1.16(j))</small>	minus 20 =	*	X \$ =		OR	X \$ =	
INDEPENDENT CLAIMS <small>(37 CFR 1.16(h))</small>	minus 3 =	*	X \$ =			X \$ =	
<input type="checkbox"/> APPLICATION SIZE FEE <small>(37 CFR 1.16(s))</small>	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENT <small>(37 CFR 1.16(j))</small>							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II					OTHER THAN SMALL ENTITY				
	(Column 1)	(Column 2)	(Column 3)						
AMENDMENT	05/08/2012	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)
	Total <small>(37 CFR 1.16(i))</small>	* 48	Minus ** 49	= 0	X \$30 =	0	OR	X \$ =	
	Independent <small>(37 CFR 1.16(h))</small>	* 1	Minus *** 3	= 0	X \$125 =	0	OR	X \$ =	
	<input type="checkbox"/> Application Size Fee <small>(37 CFR 1.16(s))</small>								
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <small>(37 CFR 1.16(j))</small>						OR		
					TOTAL ADD'L FEE	0	OR	TOTAL ADD'L FEE	

	(Column 1)	(Column 2)	(Column 3)						
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)
	Total <small>(37 CFR 1.16(i))</small>	*	Minus **	=	X \$ =		OR	X \$ =	
	Independent <small>(37 CFR 1.16(h))</small>	*	Minus ***	=	X \$ =		OR	X \$ =	
	<input type="checkbox"/> Application Size Fee <small>(37 CFR 1.16(s))</small>								
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <small>(37 CFR 1.16(j))</small>						OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

\* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.  
 \*\* If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".  
 \*\*\* If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".  
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:  
 /STELLA LITTLE/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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<b>PATENT APPLICATION FEE DETERMINATION RECORD</b> Substitute for Form PTO-875	Application or Docket Number <b>12/601,275</b>	Filing Date <b>05/31/2010</b>	<input type="checkbox"/> To be Mailed
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APPLICATION AS FILED – PART I			OTHER THAN SMALL ENTITY				
	(Column 1)	(Column 2)	SMALL ENTITY <input checked="" type="checkbox"/>	OR			
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)		RATE (\$)	FEE (\$)
<input type="checkbox"/> BASIC FEE <small>(37 CFR 1.16(a), (b), or (c))</small>	N/A	N/A	N/A		OR	N/A	
<input type="checkbox"/> SEARCH FEE <small>(37 CFR 1.16(k), (j), or (m))</small>	N/A	N/A	N/A		OR	N/A	
<input type="checkbox"/> EXAMINATION FEE <small>(37 CFR 1.16(o), (p), or (q))</small>	N/A	N/A	N/A		OR	N/A	
TOTAL CLAIMS <small>(37 CFR 1.16(j))</small>	minus 20 =	*	X \$ =		OR	X \$ =	
INDEPENDENT CLAIMS <small>(37 CFR 1.16(h))</small>	minus 3 =	*	X \$ =		OR	X \$ =	
<input type="checkbox"/> APPLICATION SIZE FEE <small>(37 CFR 1.16(s))</small>	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				OR		
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENT <small>(37 CFR 1.16(j))</small>					OR		
			TOTAL		OR	TOTAL	

\* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II					OTHER THAN SMALL ENTITY			
	(Column 1)	(Column 2)	(Column 3)					
AMENDMENT	05/08/2012	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 48	Minus ** 49	= 0	X \$30 =	0	OR	X \$ =
	Independent (37 CFR 1.16(h))	* 1	Minus *** 3	= 0	X \$125 =	0	OR	X \$ =
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))						OR	
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						OR	
					TOTAL ADD'L FEE	0	OR	TOTAL ADD'L FEE

	(Column 1)	(Column 2)	(Column 3)					
AMENDMENT	Total (37 CFR 1.16(i))	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)
	*	Minus	**	=	X \$ =		OR	X \$ =
	Independent (37 CFR 1.16(h))	*	Minus	***	X \$ =		OR	X \$ =
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))						OR	
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						OR	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE

\* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.  
 \*\* If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".  
 \*\*\* If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

Legal Instrument Examiner:  
 /TINA M. BELL/

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Table with columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO.
Rows include application details for Venkat Konda, examiner information (TAN, VIBOL), art unit (2819), and mail date (05/01/2012).

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.



<b>Applicant-Initiated Interview Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	12/601,275	KONDA, VENKAT	
	<b>Examiner</b>	<b>Art Unit</b>	
	Vibol Tan	2819	

All participants (applicant, applicant's representative, PTO personnel):

(1) Vibol Tan. (3)\_\_\_\_\_.

(2) Venkat Konda. (4)\_\_\_\_\_.

Date of Interview: 30 April 2012.

Type:  Telephonic  Video Conference  
 Personal [copy given to:  applicant  applicant's representative]

Exhibit shown or demonstration conducted:  Yes  No.  
If Yes, brief description: \_\_\_\_\_.

Issues Discussed 101 112 102 103 Others  
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: 1.

Identification of prior art discussed: 6,940,308 (Wong).

**Substance of Interview**

(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Agreement was reached for the proposed amendment of claim 1 to read as an integrated circuit device comprising a plurality of sub-integrated circuit blocks and a routing network, and Said each plurality of sub-integrated circuit blocks comprising a plurality of inlet links and a plurality of outlet links; and Said routing network comprising of a plurality of stages, in each said sub-integrated circuit block, starting from the lowest stage of 1 to the highest stage of, where; and Said routing network comprising a plurality of switches of size, where, in each said stage and each said switch of size having inlet links and outlet links; and Said plurality of outlet links of said each sub-integrated circuit block are directly connected to said inlet links of said switches of its corresponding said lowest stage of 1, and said plurality of inlet links of said each sub-integrated circuit block are directly connected from said outlet links of said switches of its corresponding said lowest stage of 1; and Said each sub-integrated circuit block comprising a plurality of forward connecting links connecting from switches in a lower stage to switches in the its immediate succeeding higher stage, and also comprising a plurality of backward connecting links connecting from switches in a higher stage to switches in the its immediate preceding lower stage; and Said each sub-integrated circuit block comprising a plurality straight links in said forward connecting links from switches in said each lower stage to switches in the its immediate succeeding higher stage and a plurality cross links in said forward connecting links from switches in said each lower stage to switches in the its immediate succeeding higher stage, and further comprising a plurality of straight links in said backward connecting links from switches in said each higher stage to switches in the its immediate preceding lower stage and a plurality of cross links in said backward connecting links from switches in said each higher stage to switches in the its immediate preceding lower stage, said plurality of sub-integrated circuit blocks arranged in a two-dimensional grid of rows and columns, and said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks which are either placed vertically above or below, or placed horizontally to the left or to the right; and each said plurality of sub-integrated circuit blocks comprising same number of said stages and said switches in each said stage, regardless of the size of said two-dimensional grid so that each said plurality of sub-integrated circuit block with its corresponding said stages and said switches in each stage is replicable in both vertical direction or horizontal direction of said two-dimensional grid.

**Applicant recordation instructions:** The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

**Examiner recordation instructions:** Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

Attachment

/Vibol Tan/ Primary Examiner, Art Unit 2819	
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**Summary of Record of Interview Requirements****Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record**

A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

**Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews**

Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.

All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:

- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:

- 1) A brief description of the nature of any exhibit shown or any demonstration conducted,
- 2) an identification of the claims discussed,
- 3) an identification of the specific prior art discussed,
- 4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
- 5) a brief identification of the general thrust of the principal arguments presented to the examiner,  
(The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
- 6) a general indication of any other pertinent matters discussed, and
- 7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

**Examiner to Check for Accuracy**

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

AMENDMENT A

*In The United States Patent And Trademark Office*

Application Number: 12/601,275  
Application Filed: 11/22/2009  
5 Applicant(s): Venkat Konda  
Title: VLSI Layouts of Fully Connected Generalized Networks  
Examiner/Art Unit: Vibol Tan / 2819  
International Application Number: PCT/US08/64605  
International Application Filed: 5/22/2008  
10 Priority Date: 5/25/2007

San Jose, 2012 Apr 30, Mon

**AMENDMENT A**

(and the response to office letter dated 2/7/2012)

15

Mail Stop Amendment

Commissioner for Patents

P.O. Box 1450

Alexandria, Virginia, 22313-1450

20

Dear Sir/Madam:

In response to the office action mailed 2012 February 7, please consider the following Amendment A.

## AMENDMENT A, Contd.

First Applicant addresses the novelty and unobviousness of the current invention over the prior art, including the U.S. Patent 6,940,308 by Wong and the U.S Patent 7,154,887 by Wu et. al. Applicant also submits that he has reviewed all the other cited references and they do not show the current invention or render it obvious.

5

**I. IN RESPONSE TO CLAIM REJECTIONS – USC 102(b):**

First Applicant submits that the current patent application discloses the VLSI layouts or floor plans of the Benes Network, Butterfly Fat Tree Networks including more generalizations of these networks. The layout is critical to implement these networks in a semiconductor chip which is typically a 2D-plane. As such topologies of the Benes Network and Butterfly Fat Tree networks are known in the prior art and the topologies of the Benes Network and Butterfly Fat Tree networks disclosed in the current invention are the same as in the prior art. However the layouts of these networks are novel.

In addition the layouts disclosed in the current invention include generalized multi-stage networks  $V(N_1, N_2, d, s)$ , generalized folded multi-stage networks  $V_{fold}(N_1, N_2, d, s)$ , generalized butterfly fat tree networks  $V_{bft}(N_1, N_2, d, s)$ , generalized multi-link multi-stage networks  $V_{mlink}(N_1, N_2, d, s)$ , generalized folded multi-link multi-stage networks  $V_{fold-mlink}(N_1, N_2, d, s)$ , generalized multi-link butterfly fat tree networks  $V_{mlink-bft}(N_1, N_2, d, s)$ , and generalized hypercube networks  $V_{hcube}(N_1, N_2, d, s)$  for  $s = 1, 2, 3$  or any number in general.

**The following table addresses the list of items where the current invention is different/superior over column-based layout (or floor plan) disclosed in U.S. Patent 6,940,308 by Wong:**

Item addressed	Solutions in US patent 6,940,308 by Wong	Solutions in Current Application
<b>Layout format</b>	Column-based layout	2D-grid in row-column layout  (Key insight in the disclosure is to arrange the sub-integrated circuits in a hypercube topology)
<b>Fundamental sub-integrated circuit</b>	<p>As disclosed in Fig. 13A, the basic building block of the column-based layout is based on (as mentioned in Col. 13, lines 22-24) “There are two logic cells 81 per switch cell 82, connected in the so called “butterfly pattern”, consistent with the Benes Network topology: ...”.</p> <p>It is clear that column-based layout has the following properties:</p> <ol style="list-style-type: none"> <li>1) Basic building block (or sub-integrated circuit) has cross links connected between switches of two</li> </ol>	<p>As disclosed in Figs. 1C – 1G, the 2D-grid in row-column layout disclosed in the current patent application has no butterfly pattern in the layout. In other words the cross links between switches of two succeeding stages are always connected between two sub-integrated circuits which are placed either horizontally in the same column or vertically in the same row. Also the cross</p>

## AMENDMENT A, Contd.

	<p>succeeding stages with in the same sub-integrated circuit. Otherwise there will not be a butterfly pattern.</p>	<p>links between two succeeding stages are either vertical links (as shown in Figs. 1D &amp; 1F) or horizontal links (as shown in Figs. 1E &amp; 1G).</p>
<p><b>To scale the layout for bigger size of network (or sub-integrated circuits)</b></p>	<p>As disclosed in Fig. 13B, columns are doubled by adding one more stage of switches in both the columns (for example Fig. 13A is replicated to get Fig. 13B and a new stage of switches 83 are added and the cross links between the new stage of switches in the two columns become horizontal links).</p> <ol style="list-style-type: none"> <li>1) It is clear as the network is scaled up, only columns are increasing.</li> <li>2) And the basic building block is the same as that shown in Fig. 13A.</li> </ol>	<p>As disclosed in Fig. 1H, the layout doubles in both columns and rows alternatively, as the size of the network is doubled repeatedly as needed, in hypercube layout format.</p>
<p><b>Industry Applicability or practical use of the layout</b></p> <p>(FPGA vendors typically take the same basic block (consisting of a</p>	<p>The applicant believes column-based layout is impractical for an FPGA vendor to manufacture FPGA devices with different size of basic blocks, as the number of basic blocks in each device determine the size of each</p>	<p>Same basic block can be easily used to manufacture FPGAs of different sizes. (The layout disclosed in the current invention is already adopted by an</p>

## AMENDMENT A, Contd.

<p>certain set of LUTs and registers) and manufacture devices of different sizes of basic blocks (typically called slice, CLB or PLC etc.)</p>	<p>column (as that shown in FIG. 13A) and each device will require a different size of each column to manufacture the devices close to square in size. And hence it is impractical for an FPGA vendor to employ column-based layout.</p>	<p>FPGA vendor namely Quicklogic corporation, located in Sunnyvale, CA).</p>
<p><b>Locality between two neighboring basic blocks either horizontally or vertically</b></p>	<p>From Fig. 13A, it can be seen that for a signal from a logic cell to be routed horizontally to the nearest neighboring column, the signal needs to go through all the stages 82 (whose cross links are connected with in the same column) before connecting out to the logic cell in the basic block of the nearest neighboring column.</p>	<p>For most of the logic cells in this layout, a signal from a logic cell can be routed vertically or horizontally to the nearest neighboring logic cell by passing through one or two stages of switches.</p>



**2. IMPRACTICAL TREE-BASED LAYOUT DISCLOSED IN PATENT 6,940,308 BY WONG:**

1) The tree-based layout disclosed in patent 6,940,308 by Wong is also not practical to implement by an FPGA vendor because:

5           a) From Fig. 14C it is evident that the switches corresponding to the higher stages get pulled into the middle of the layout. For example in Fig. 14C, the switches A4 – P4 are placed in the center or middle of the layout. As the size of the logic cells increase from 16 to bigger sizes, this problem will get even worse as the highest stage switches get pulled into the middle of the layout. The next highest stage switches get pulled into close  
10 to the middle of the layout. Similarly the higher the stage of switches they are placed close to the middle of the layout and the lower the stage of switches they are placed close to the logic cells.

          b) Evidently the logic cells and the switches corresponding to the all the stages for that logic cell cannot be designed as a repeatable basic block and hence this tree-based  
15 layout is not practical to implement by an FPGA vendor.

## II. IN RESPONSE TO CLAIM REJECTIONS – USC 103(a):

### 1. LAYOUT FOR REARRANGEBALY AND STRICLTY NON-BOCKING NETWORKS FOR ARBITRARY FAN-OUT MULTICAST CONNECTIONS:

- 5 1) US patent 7,154,887 by Wu et. al. disclosed a grooming switch based on a rearrangeably non-blocking clos network for arbitrary fan-out multicast traffic. To make 3-stage clos network which is rearrangeably non-blocking for unicast connections, US patent 7,154,887 by Wu et. al. disclosed a rearrangeably non-blocking clos network with 5 stages for arbitrary fan-out multicast traffic by adding 2 more stages.
- 10 2) As disclosed in the “CROSS REFERENCE TO RELATED APPLICATIONS” of the current patent application, by the same applicant, the current patent application also discloses VLSI layouts for:
- a) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-stage networks disclosed in the US Application Serial No. 15 12/530,207 entitled "FULLY CONNECTED GENERALIZED MULTI-STAGE NETWORKS" by the same applicant.
- b) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-stage networks disclosed in the US Application Serial No. 12/601,273 entitled "FULLY CONNECTED GENERALIZED BUTTERFLY FAT 20 TREE NETWORKS" by the same applicant.
- c) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-stage networks disclosed in the US Application Serial No. 12/601,274 entitled "FULLY CONNECTED GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS" by the same applicant.
- 25 **Claims:** Claims 1-3, 8, 12, 25, 29, 40, 44, 48-49 of record are amended and substitute new claims as follows.

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CLAIMS

What is claimed is:

1. (currently amended): An integrated circuit device comprising a plurality of sub-integrated circuit blocks and a routing network, and
  - 5 Said each plurality of sub-integrated circuit blocks comprising a plurality of inlet links and a plurality of outlet links; and
    - ~~Said routing network interconnects any one of said outlet link of one of said sub-integrated circuit block to one or more said inlet links of one or more of said sub-integrated circuit blocks; and~~
    - 10 Said routing network comprising of a plurality of stages  $y$ , in each said sub-integrated circuit block, starting from the lowest stage of 1 to the highest stage of  $y$ , where  $y \geq 1$ ; and
      - Said routing network comprising a plurality of switches of size  $d \times d$ , where  $d \geq 2$ , in each said stage and each said switch of size  $d \times d$  having  $d$  inlet links and  $d$ 
        - 15 outlet links; and
          - ~~Said each sub-integrated circuit block comprising a plurality of said switches corresponding to each said stage; and~~
          - Said plurality of outlet links of said each sub-integrated circuit block are directly connected to said inlet links of said switches of its corresponding said lowest stage of 1,
            - 20 and said plurality of inlet links of said each sub-integrated circuit block are directly connected from said outlet links of said switches of its corresponding said lowest stage of 1; and

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Said each sub-integrated circuit block comprising a plurality straight links in said forward connecting links from switches in said each lower stage to switches in ~~the~~ its immediate succeeding higher stage and a plurality cross links in said forward connecting links from switches in said each lower stage to switches in ~~the~~ its immediate succeeding higher stage, and further comprising a plurality of straight links in said backward connecting links from switches in said each higher stage to switches in ~~the~~ its immediate preceding lower stage and a plurality of cross links in said backward connecting links from switches in said each higher stage to switches in ~~the~~ its immediate preceding lower stage,

10 said plurality of sub-integrated circuit blocks arranged in a two-dimensional grid of rows and columns, and

said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and said all cross links are connecting as either vertical or horizontal links between switches  
15 in two different said sub-integrated circuit blocks which are either placed vertically above or below, or placed horizontally to the left or to the right,

each said plurality of sub-integrated circuit blocks comprising same number of said stages and said switches in each said stage, regardless of the size of said two-dimensional grid so that each said plurality of sub-integrated circuit block with its  
20 corresponding said stages and said switches in each stage is replicable in both vertical direction or horizontal direction of said two-dimensional grid.

2. (currently amended): The integrated circuit device of claim 1, ~~wherein~~  
~~said plurality of sub-integrated circuit blocks arranged in a two-dimensional grid~~  
25 said two-dimensional grid of said sub-integrated circuit blocks with their  
corresponding said stages and said switches in each stage is scalable by any power of 2,  
and,

for each multiplication of 2 of the size of total said sub-integrated circuit blocks,  
by adding one more stage of switches and the layout is placed in hypercube format and

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also the cross links between said one more stage of switches are connected in hypercube format.

3. (Original): The integrated circuit device of claim 2, wherein said cross links in succeeding stages are connecting as alternative vertical and horizontal links  
5 between switches in said sub-integrated circuit blocks.

4. (Original): The integrated circuit device of claim 3, wherein said cross links from switches in a stage in one of said sub-integrated circuit blocks are connecting to switches in the succeeding stage in another of said sub-integrated circuit blocks so that said cross links are either vertical links or horizontal and vice versa, and hereinafter such  
10 cross links are “shuffle exchange links”).

5. (Original): The integrated circuit device of claim 4, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are substantially of equal length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are substantially  
15 of equal length in the entire said integrated circuit device.

6. (Original): The integrated circuit device of claim 5, wherein the shortest horizontal shuffle exchange links are connecting at the lowest stage and between switches in two nearest neighboring said sub-integrated circuit blocks, and length of the horizontal shuffle exchange links is doubled in each succeeding stage; and the shortest vertical  
20 shuffle exchange links are connecting at the lowest stage and between switches in two nearest neighboring said sub-integrated circuit blocks, and length of the vertical shuffle exchange links is doubled in each succeeding stage.

7. (currently amended): The integrated circuit device of claim 6, wherein  $y \geq (\log_2 N)$ , where  $N > 1$ , so that the length of the horizontal shuffle exchange links in  
25 the highest stage is equal to half the size of the horizontal size of said two dimensional grid of sub-integrated circuit blocks and the length of the vertical shuffle exchange links

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in the highest stage is equal to half the size of the vertical size of said two dimensional grid of sub-integrated circuit blocks.

8. (Original): The integrated circuit device of claim 7, wherein  $d = 2$  and there is only one switch in each said stage in each said sub-integrated circuit block  
5 connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast Benes network with full bandwidth.

9. (Original): The integrated circuit device of claim 7, wherein  $d = 2$  and  
10 there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast Benes network and rearrangeably nonblocking for arbitrary fan-out multicast Benes network with full  
15 bandwidth.

10. (Original): The integrated circuit device of claim 7, wherein  $d = 2$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links  
20 and said routing network is strictly nonblocking for arbitrary fan-out multicast Benes network with full bandwidth.

11. (currently amended): The integrated circuit device of claim 6, wherein  $y \geq (\log_2 N)$ , where  $N > 1$ , so that the length of the horizontal shuffle exchange links in the highest stage is equal to half the size of the horizontal size of said two dimensional  
25 grid of sub-integrated circuit blocks and the length of the vertical shuffle exchange links in the highest stage is equal to half the size of the vertical size of said two dimensional grid of sub-integrated circuit blocks, and

said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks.

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12. (Original): The integrated circuit device of claim 11, wherein  $d = 2$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and  
5 said routing network is rearrangeably nonblocking for unicast butterfly fat tree network with full bandwidth.

13. (Original): The integrated circuit device of claim 11, wherein  $d = 2$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said  
10 stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast butterfly fat tree network and rearrangeably nonblocking for arbitrary fan-out multicast butterfly fat tree network with full bandwidth.

14. (Original): The integrated circuit device of claim 11, wherein  $d = 2$  and  
15 there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast butterfly fat tree network with full bandwidth.

20 15. (Original): The integrated circuit device of claim 1, wherein said horizontal and vertical links are implemented on two or more metal layers.

16. (Original): The integrated circuit device of claim 1, wherein said switches comprising active and reprogrammable cross points and said each cross point is programmable by an SRAM cell or a Flash Cell.

25 17. (Original): The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks are of equal die size.

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18. (Original): The integrated circuit device of claim 15, wherein said sub-integrated circuit blocks are Lookup Tables (hereinafter "LUTs") and said integrated circuit device is a field programmable gate array (FPGA) device or field programmable gate array (FPGA) block embedded in another integrated circuit device.
- 5 19. (Original): The integrated circuit device of claim 15, wherein said sub-integrated circuit blocks are AND or OR gates and said integrated circuit device is a programmable logic device (PLD).
20. (Original): The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks comprising any arbitrary hardware logic or memory circuits.
- 10 21. (Original): The integrated circuit device of claim 1, wherein said switches comprising active one-time programmable cross points and said integrated circuit device is a mask programmable gate array (MPGA) device or a structured ASIC device.
22. (Original): The integrated circuit device of claim 1, wherein said switches comprising passive cross points or just connection of two links or not and said integrated  
15 circuit device is a Application Specific Integrated Circuit (ASIC) device.
23. (Original): The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks further recursively comprise one or more super-sub-integrated circuit blocks and a sub-routing network.
24. (currently amended): The integrated circuit device of claim 4, wherein  
20 said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and  
15  $y \geq (\log_2 N)$ , where  $N > 1$ .
- 25 25. (Original): The integrated circuit device of claim 24, wherein  $d = 2$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage



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in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized multi-stage network with full bandwidth.

26. (Original): The integrated circuit device of claim 24, wherein  $d = 2$  and  
5 there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized multi-stage network and rearrangeably nonblocking for arbitrary fan-out multicast generalized multi-  
10 stage network with full bandwidth.

27. (Original): The integrated circuit device of claim 24, wherein  $d = 2$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links  
15 and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized multi-stage network with full bandwidth.

28. (currently amended): The integrated circuit device of claim 4, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between  
20 switches in any two corresponding said succeeding stages are of different length and  $y \geq (\log_2 N)$ , where  $N > 1$ , and

said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks.

29. (Original): The integrated circuit device of claim 28, wherein  $d = 2$  and  
25 there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and

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said routing network is rearrangeably nonblocking for unicast generalized butterfly fat tree network with full bandwidth.

30. (Original): The integrated circuit device of claim 28, wherein  $d = 2$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized butterfly fat tree Network and rearrangeably nonblocking for arbitrary fan-out multicast generalized butterfly fat tree network with full bandwidth.

31. (Original): The integrated circuit device of claim 28, wherein  $d = 2$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized butterfly fat tree network with full bandwidth.

32. (Original): The integrated circuit device of claim 1, wherein said straight links connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and said cross links are connecting as vertical or horizontal or diagonal links between two different said sub-integrated circuit blocks.

33. (Original): The integrated circuit device of claim 7, wherein  $d = 4$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast multi-link Benes network with full bandwidth.

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34. (Original): The integrated circuit device of claim 7, wherein  $d = 4$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast multi-link Benes network and rearrangeably nonblocking for arbitrary fan-out multicast multi-link Benes network with full bandwidth.

35. (Original): The integrated circuit device of claim 7, wherein  $d = 4$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast multi-link Benes network with full bandwidth.

36. (Original): The integrated circuit device of claim 11, wherein  $d = 4$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast multi-link butterfly fat tree network with full bandwidth.

37. (Original): The integrated circuit device of claim 11, wherein  $d = 4$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast multi-link butterfly fat tree network and rearrangeably nonblocking for arbitrary fan-out multicast multi-link butterfly fat tree network with full bandwidth.

38. (Original): The integrated circuit device of claim 11, wherein  $d = 4$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said

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stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast multi-link butterfly fat tree network with full bandwidth.

39. (currently amended): The integrated circuit device of claim 4, wherein  
5 said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and  $y \geq (\log_2 N)$ , where  $N > 1$ .

40. (Original): The integrated circuit device of claim 39, wherein  $d = 4$  and  
10 there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized multi-link multi-stage network with full bandwidth.

41. (Original): The integrated circuit device of claim 39, wherein  $d = 4$  and  
15 there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized multi-link multi-  
20 stage network and rearrangeably nonblocking for arbitrary fan-out multicast generalized multi-link multi-stage network with full bandwidth.

42. (Original): The integrated circuit device of claim 39, wherein  $d = 4$  and  
there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said  
25 stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized multi-link multi-stage network with full bandwidth.

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43. (currently amended): The integrated circuit device of claim 4, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and  
5  $y \geq (\log_2 N)$ , where  $N > 1$ , and

said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks.

44. (Original): The integrated circuit device of claim 43, wherein  $d = 4$  and there is only one switch in each said stage in each said sub-integrated circuit block  
10 connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized multi-link butterfly fat tree network with full bandwidth.

45. (Original): The integrated circuit device of claim 43, wherein  $d = 4$  and  
15 there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized multi-link butterfly fat tree Network and rearrangeably nonblocking for arbitrary fan-out multicast  
20 generalized multi-link butterfly fat tree network with full bandwidth.

46. (Original): The integrated circuit device of claim 43, wherein  $d = 4$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links  
25 and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized multi-link butterfly fat tree network with full bandwidth.

47. (currently amended): The integrated circuit device of claim 1, wherein said plurality of forward connecting links use a plurality of buffers to amplify signals

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driven through them and said plurality of backward connecting links use a plurality of buffers to amplify signals driven through them; and said buffers can be inverting or non-inverting buffers.

48. (currently amended): The integrated circuit device of claim 1, wherein  
5 said ~~wherein said~~ all switches of size  $d \times d$  are either fully populated or partially populated.

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- 1) **The rejection of Claims 1-8, 12, 16-25, 29, 33, 40, 44, and 48-49 under 35 USC 102(b)**

Accordingly applicant submit that the claims do comply with § 102(b) and therefore request withdrawal of this rejection.

- 5 2) **The rejection of Claims 9-11, 13-15, 26-28, 30-32, 34-39, 41-43, and 45-47 under 35 USC 103(a)**

Accordingly applicant submit that the claims do comply with § 103(a) and therefore request withdrawal of this rejection.

10

**CONCLUSION**

For all of the above reasons, applicant submits that the Claims are now in proper form, and that the Claims all define patentably over the prior art. Therefore applicant submits that this application is now in condition for allowance, which action he respectfully solicits.

15

**Conditional request for Constructive Assistance**

Applicant has amended the claims of this application so that they are proper, definite, and define novel structure which is also unobvious. If, for any reason this application is not believed to be in full condition for allowance, applicant respectfully request the constructive assistance and suggestions of the Examiner pursuant to M.P.E.P §  
20 2173.02 and § 707.07(j) in order that the undersigned can place this application in allowable condition as soon as possible and without the need for further proceedings.

Very respectfully,

/Venkat Konda/

25 Venkat Konda

Application Number: 12/601,275 (Venkat Konda)

Art Unit: 2819

AMENDMENT A, Contd.

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## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	12667779
<b>Application Number:</b>	12601275
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	6372
<b>Title of Invention:</b>	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
<b>First Named Inventor/Applicant Name:</b>	Venkat Konda
<b>Customer Number:</b>	38139
<b>Filer:</b>	Venkar Konda
<b>Filer Authorized By:</b>	
<b>Attorney Docket Number:</b>	V-0045US
<b>Receipt Date:</b>	30-APR-2012
<b>Filing Date:</b>	31-MAY-2010
<b>Time Stamp:</b>	18:15:10
<b>Application Type:</b>	U.S. National Stage under 35 USC 371

### Payment information:

Submitted with Payment	no
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### File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	AmendmentA-V0045US.pdf	188498 <small>1ef528eeaf46ce4d077d8e28f40c4a871729bff2</small>	no	21

### Warnings:

### Information:

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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<b>PATENT APPLICATION FEE DETERMINATION RECORD</b> Substitute for Form PTO-875	Application or Docket Number <b>12/601,275</b>	Filing Date <b>05/31/2010</b>	<input type="checkbox"/> To be Mailed
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APPLICATION AS FILED – PART I			OTHER THAN SMALL ENTITY				
	(Column 1)	(Column 2)	SMALL ENTITY <input checked="" type="checkbox"/>	OR			
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)
<input type="checkbox"/> BASIC FEE <small>(37 CFR 1.16(a), (b), or (c))</small>	N/A	N/A	N/A			N/A	
<input type="checkbox"/> SEARCH FEE <small>(37 CFR 1.16(k), (j), or (m))</small>	N/A	N/A	N/A			N/A	
<input type="checkbox"/> EXAMINATION FEE <small>(37 CFR 1.16(o), (p), or (q))</small>	N/A	N/A	N/A			N/A	
TOTAL CLAIMS <small>(37 CFR 1.16(j))</small>	minus 20 =	*	X \$ =		OR	X \$ =	
INDEPENDENT CLAIMS <small>(37 CFR 1.16(h))</small>	minus 3 =	*	X \$ =			X \$ =	
<input type="checkbox"/> APPLICATION SIZE FEE <small>(37 CFR 1.16(s))</small>	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENT <small>(37 CFR 1.16(j))</small>							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II					OTHER THAN SMALL ENTITY				
	(Column 1)	(Column 2)	(Column 3)		SMALL ENTITY	OR			
AMENDMENT	04/30/2012	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)
	Total <small>(37 CFR 1.16(i))</small>	* 48	Minus ** 49	= 0	X \$30 =	0	OR	X \$ =	
	Independent <small>(37 CFR 1.16(h))</small>	* 1	Minus *** 3	= 0	X \$125 =	0	OR	X \$ =	
	<input type="checkbox"/> Application Size Fee <small>(37 CFR 1.16(s))</small>								
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <small>(37 CFR 1.16(j))</small>						OR		
					TOTAL ADD'L FEE	0	OR	TOTAL ADD'L FEE	

	(Column 1)	(Column 2)	(Column 3)						
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)
	Total <small>(37 CFR 1.16(i))</small>	*	Minus **	=	X \$ =		OR	X \$ =	
	Independent <small>(37 CFR 1.16(h))</small>	*	Minus ***	=	X \$ =		OR	X \$ =	
	<input type="checkbox"/> Application Size Fee <small>(37 CFR 1.16(s))</small>								
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <small>(37 CFR 1.16(j))</small>						OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

\* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.  
 \*\* If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".  
 \*\*\* If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".  
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:  
 /ROLITA WIMBUSH/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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<b>Application Data Sheet 37 CFR 1.76</b>		Attorney Docket Number	V-0045US
		Application Number	
Title of Invention	VLSI Layouts of Fully Connected Generalized Networks		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

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**Applicant Information:**

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<b>Applicant Authority</b> <input checked="" type="radio"/> Inventor		<input type="radio"/> Legal Representative under 35 U.S.C. 117		<input type="radio"/> Party of Interest under 35 U.S.C. 118	
<b>Prefix</b>	<b>Given Name</b>	<b>Middle Name</b>	<b>Family Name</b>	<b>Suffix</b>	
	Venkat		Konda		
<b>Residence Information (Select One)</b> <input checked="" type="radio"/> US Residency <input type="radio"/> Non US Residency <input type="radio"/> Active US Military Service					
<b>City</b>	San Jose	<b>State/Province</b>	CA	<b>Country of Residence i</b>	US
<b>Citizenship under 37 CFR 1.41(b) i</b>		US			
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All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the <b>Add</b> button.					<input type="button" value="Add"/>

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<input type="checkbox"/> An Address is being provided for the correspondence Information of this application.			
<b>Customer Number</b>	38139		
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**Application Information:**

<b>Title of the Invention</b>	VLSI Layouts of Fully Connected Generalized Networks		
<b>Attorney Docket Number</b>	V-0045US	<b>Small Entity Status Claimed</b>	<input checked="" type="checkbox"/>
<b>Application Type</b>	Nonprovisional		
<b>Subject Matter</b>	Utility		
<b>Suggested Class (if any)</b>		<b>Sub Class (if any)</b>	
<b>Suggested Technology Center (if any)</b>			
<b>Total Number of Drawing Sheets (if any)</b>	39	<b>Suggested Figure for Publication (if any)</b>	1G

<b>Application Data Sheet 37 CFR 1.76</b>	Attorney Docket Number	V-0045US
	Application Number	
Title of Invention	VLSI Layouts of Fully Connected Generalized Networks	

**Publication Information:**

<input checked="" type="checkbox"/>	Request Early Publication (Fee required at time of Request 37 CFR 1.219)
<input type="checkbox"/>	<b>Request Not to Publish.</b> I hereby request that the attached application not be published under 35 U.S. C. 122(b) and certify that the invention disclosed in the attached application <b>has not and will not</b> be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Customer Number	38139		

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<p>This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.</p>			
Prior Application Status	Expired	<a href="#">Remove</a>	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
<p>Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the <b>Add</b> button.</p>			<a href="#">Add</a>

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Application Number	Country <sup>i</sup>	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
PCT/US08/64605	US	2008-05-22	<input checked="" type="radio"/> Yes <input type="radio"/> No
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<b>Application Data Sheet 37 CFR 1.76</b>	Attorney Docket Number	V-0045US
	Application Number	
Title of Invention	VLSI Layouts of Fully Connected Generalized Networks	

If the Assignee is an Organization check here. <input checked="" type="checkbox"/>			
Organization Name	Konda Technologies Inc.		
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Additional Assignee Data may be generated within this form by selecting the <b>Add</b> button.			<input type="button" value="Add"/>

**Signature:**

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.					
Signature	/Venkat Konda/		Date (YYYY-MM-DD)	2012-04-18	
First Name	Venkat	Last Name	Konda	Registration Number	

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<b>EFS ID:</b>	12576502
<b>Application Number:</b>	12601275
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	6372
<b>Title of Invention:</b>	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
<b>First Named Inventor/Applicant Name:</b>	Venkat Konda
<b>Customer Number:</b>	38139
<b>Filer:</b>	Venkar Konda
<b>Filer Authorized By:</b>	
<b>Attorney Docket Number:</b>	V-0045US
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<b>Filing Date:</b>	31-MAY-2010
<b>Time Stamp:</b>	04:53:51
<b>Application Type:</b>	U.S. National Stage under 35 USC 371

### Payment information:

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### File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	sb0014-V0045US.pdf	1420688 <small>1b1fcd4236336b2fb79c4394e98f66b92e839166</small>	no	4

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/601,275	05/31/2010	Venkat Konda	V-0045US	6372
38139	7590	02/07/2012	EXAMINER	
Konda Technologies, Inc 6278 GRAND OAK WAY SAN JOSE, CA 95135			TAN, VIBOL	
			ART UNIT	PAPER NUMBER
			2819	
			MAIL DATE	DELIVERY MODE
			02/07/2012	PAPER

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**DETAILED ACTION**

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-8, 12, 16-25, 29, 33, 40, 44, and 48-49 are rejected under 35 U.S.C. 102(b) as being anticipated by Wong (U. S. PAT. 6,940,308).

In claim 1, Wong teaches an integrated circuit device comprising a plurality of sub-integrated circuit blocks and a routing network (ASIC; col. 13, lines 4-5), and

Said each plurality of sub-integrated circuit blocks comprising a plurality of inlet links and a plurality of outlet links (input-output pin-pair; Col. 13, Line 25); and

Said routing network interconnects any one of said outlet link of one of said sub-integrated circuit block to one or more said inlet links of one or more of said sub-integrated circuit blocks (peripheral blocks of an integrated circuit; col. 14, line 48); and

Said routing network comprising of a plurality of stages  $y$ , starting from the lowest stage to the highest stage (hierarchical levels; col. 2, lines 7-12); and

Said routing network comprising a plurality of switches of size  $d \times d$ , where  $d \geq 2$ , in each said stage and each said switch of size  $d \times d$  having  $d$  inlet links and  $d$  outlet links (2x2 switch; col. 2, line 27); and

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Said each sub-integrated circuit block comprising a plurality of said switches corresponding to each said stage (switches at first rank of hierarchy; col. 2, lines 34-35; Fig. 3C); and

Said each sub-integrated circuit block comprising a plurality of forward connecting links connecting from switches in lower stage to switches in the immediate succeeding higher stage (col. 2; lines 16-22; see input and output links in Fig. 2B; Fig. 3A), and also comprising a plurality of backward connecting links connecting from switches in higher stage to switches in the immediate preceding lower stage (see upper network and lower network in Fig 3B; see upper and lower in Fig. 3C; inputs and outputs, Fig. 4B); and

Said each sub-integrated circuit block comprising a plurality straight links in said forward connecting links from switches in lower stage to switches in the immediate succeeding higher stage and a plurality cross links in said forward connecting links from switches in lower stage to switches in the immediate succeeding higher stage (pass (straight) mode or cross mode; col. 5, lines 4-13; cross, Fig. 2B; see upper network and lower network in Fig. 3B; see upper and lower in Fig. 3C; inputs and outputs Fig. 4B), and further comprising a plurality of straight links in said backward connecting links from switches in higher stage to switches in the immediate preceding lower stage and a plurality of cross links in said backward connecting links from switches in higher stage to switches in the immediate preceding lower stage (pass (straight) mode or cross mode; col. 5, lines 4-13; cross, Fig. 2B; see upper network and lower network in Fig 3B; see upper and lower in Fig. 3C; inputs and outputs, Fig. 4B).

In claim 2, Wong further teaches the integrated circuit device of claim 1, wherein said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block (Fig. 13A); and

said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks (Fig. 13A).

In claim 3, Wong further teaches the integrated circuit device of claim 2, wherein said plurality of sub-integrated circuit blocks arranged in a two-dimensional grid (width and height dimensions; col. 12, lines 42-51).

In claim 4, Wong further teaches the integrated circuit device of claim 3, wherein said cross links in succeeding stages are connecting as alternative vertical and horizontal links between switches in said sub-integrated circuit blocks (col. 2, lines 7-12; Fig. 10, Fig. 14B).

In claim 5, Wong further teaches the integrated circuit device of claim 4, wherein said cross links from switches in a stage in one of said sub-integrated circuit blocks are connecting to switches in the succeeding stage in another of said sub-integrated circuit blocks so that said cross links are either vertical links or horizontal and vice versa, and hereinafter such cross links are "shuffle exchange links" (rearrangeable interconnection network; col. 1, line 61 - col. 2, Line 6; rearrangeable; col. 4, lines 12-17).

In claim 6, Wong further teaches the integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are substantially of equal length and said vertical shuffle

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exchange links between switches in any two corresponding said succeeding stages are substantially of equal length in the entire said integrated circuit device (original Benes network and every route must travel through all levels, col. 7, lines 26-27; col. 11, lines 23-25).

In claim 7, Wong further teaches the integrated circuit device of claim 6, wherein the shortest horizontal shuffle exchange links are connecting at the lowest stage and between switches in two nearest neighboring said sub-integrated circuit blocks, and length of the horizontal shuffle exchange links is doubled in each succeeding stage (shorter routes; col. 7, lines 26-27; col. 11, lines 23-25); and

the shortest vertical shuffle exchange links are connecting at the lowest stage and between switches in two nearest neighboring said sub-integrated circuit blocks, and length of the vertical shuffle exchange links is doubled in each succeeding stage (length =  $2 * (\log_2 N)$ ; col. 11, lines 23-25).

In claim 8, Wong further teaches the integrated circuit device of claim 7, wherein  $y \geq (\log_2 N)$  so that the length of the horizontal shuffle exchange links in the highest stage is equal to half the size of the horizontal size of said two dimensional grid of sub-integrated circuit blocks and the length of the vertical shuffle exchange links in the highest stage is equal to half the size of the vertical size of said two dimensional grid of sub-integrated circuit blocks (length =  $2 * (\log_2 N)$ ; col. 11, lines 23-25).

In claim 12, Wong further teaches the integrated circuit device of claim 7, wherein  $y \geq (\log_2 N)$  so that the length of the horizontal shuffle exchange links in the highest stage is equal to half the size of the horizontal size of said two dimensional grid

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of sub-integrated circuit blocks and the length of the vertical shuffle exchange links in the highest stage is equal to half the size of the vertical size of said two dimensional grid of sub-integrated circuit blocks (length =  $2 * (\log_2 N)$ ); col. 11, lines 23-25), and said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks (see u-turn links; Figs. 5 and 6B).

In claim 16, Wong further teaches the integrated circuit device of claim 1, wherein said horizontal and vertical links are implemented on two or more metal layers (CMOS integrated circuit; col. 5, lines 22-25).

In claim 17, Wong further the integrated circuit device of claim 1, wherein said switches comprising active and reprogrammable cross points and said each cross point is programmable by an SRAM cell or a Flash Cell (SRAM based FPGA; col. 2, lines 25-26; FPGA, col. 1, lines 14-17).

In claim 18, Wong further teaches the integrated circuit device of claim 1, wherein said sub-integrated circuit blocks are of equal die size (sub-network of equal size; col. 6, lines 10-11).

In claim 19, Wong further teaches the integrated circuit device of claim 16, wherein said sub-integrated circuit blocks are Lookup Tables (hereinafter "LUTs") and said integrated circuit device is a field programmable gate array (FPGA) device or field programmable gate array (FPGA) block embedded in another integrated circuit device (look-up tables; col. 8, line 51; FPGA (Field Programmable Gate Array); col. 1, lines 14-17).



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In claim 20, Wong further teaches the integrated circuit device of claim 16, wherein said sub-integrated circuit blocks are AND or OR gates and said integrated circuit device is a programmable logic device (PLD) ('logic gates'; col. 7, line 36; 'programmable gate arrays'; col. 14, lines 29-31).

In claim 21, Wong further teaches the integrated circuit device of claim 1, wherein said sub-integrated circuit blocks comprising any arbitrary hardware logic or memory circuits (col. 14, lines 44-51).

In claim 22, Wong further teaches the integrated circuit device of claim 1, wherein said switches comprising active one-time programmable cross points and said integrated circuit device is a mask programmable gate array (MPGA) device or a structured ASIC device (MPGA, col. 14, lines 29-31; ASIC, col. 13, lines 4-5).

In claim 23, Wong further teaches the integrated circuit device of claim 1, wherein said switches comprising passive cross points or just connection of two links or not and said integrated circuit device is a Application Specific Integrated Circuit (ASIC) device (logic cells, col. 1, lines 29-31; ASIC, col. 13, lines 4-5).

In claim 24, Wong the integrated circuit device of claim 1, wherein said sub-integrated circuit blocks further recursively comprise one or more super-sub-integrated circuit blocks and a sub-routing network (one or more sub-networks; Col. 6, lines 7-9).

In claim 25, Wong further teaches the integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle

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exchange links between switches in any two corresponding said succeeding stages are of different length and  $y \geq (\log_2 N)$  (length =  $2^{(\log_2 N)}$ ; col. 11, lines 23-25).

In claim 29, Wong further teaches the integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and  $y \geq (\log_2 N)$  (length =  $2^{(\log_2 N)}$ ; col. 11, lines 23-25), and said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks (see u-turn links; Figs. 5 and 6B).

In claim 33, Wong further teaches the integrated circuit device of claim 1, wherein said straight links connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and said cross links are connecting as vertical or horizontal or diagonal links between two different said sub-integrated circuit blocks (see link arrangement in Fig. 3B).

In claim 40, Wong teaches the integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and  $y \geq (\log_2 N)$  (length =  $2^{(\log_2 N)}$ ; col. 11, lines 23-25).

In claim 44, Wong further teaches the integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two

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corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and  $y \geq (\log_2 N)$  (length =  $2 * (\log_2 N)$ ); col. 11, lines 23-25), and said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks (see u-turn links; Figs. 5 and 6B).

In claim 48, Wong further teaches the integrated circuit device of claim 1, wherein said plurality of forward connecting links use a plurality of buffers to amplify signals driven through them and said plurality of backward connecting links use a plurality of buffers to amplify signals driven through them; and said buffers can be inverting or non-inverting buffers (buffers; col. 10, lines 59-64).

In claim 49, Wong further teaches the integrated circuit device of claim 1, wherein said wherein said all switches of size  $d \times d$  are either fully populated or partially populated (populated and depopulated cells; col. 3, lines 34-41).

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 9-11, 13-15, 26-28, 30-32, 34-39, 41-43, and 45-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong in view of Wu et al. (U. S. PAT. 7,154,887), hereinafter Wu.

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In claim 9, Wong discloses a Benes network wherein  $d = 2$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links (col. 2, lines 27-30; 2x2 Benes network; col. 5, lines 26-31); but does not disclose said routing network is rearrangeably nonblocking for unicast Benes network with full bandwidth. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being rearrangeably nonblocking for unicast Benes network with full bandwidth (rearrangeably nonblocking for unicast traffic; col. 2, lines 52-54).

Therefore, it would have been obvious to one ordinarily skilled in the art at the time the invention was made to supplement the teachings of Wong and have routing network being rearrangeably nonblocking for unicast Benes network with full bandwidth, in order to satisfy specific routing requirements.

In claim 10, Wong discloses  $d = 2$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links (8x8 Benes network (each switch has two logic cells that are 2x2, hence 8x8 is 4 switches); col. 2, lines 31-33), but does not disclose said routing network is strictly nonblocking for unicast Benes network and rearrangeably nonblocking for arbitrary fan-out multicast Benes network with full bandwidth. However, in the same field of endeavor, Wu discloses a rearrangeable non-

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blocking switch (Abstract) and a routing network being strictly nonblocking for unicast Benes network (col. 2, lines 9-11; see Fig. 9) and rearrangeably nonblocking for arbitrary fan-out multicast Benes network with full bandwidth (col. 4, lines 6-7; see fanouts, Fig. 7B).

Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be strictly nonblocking for unicast Benes and rearrangeably nonblocking for arbitrary fan-out multicast Benes network with full bandwidth, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 11, Wong discloses  $d = 2$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links ('8x8 Benes network'; col. 2, lines 31-33), but does not disclose said routing network is strictly nonblocking for arbitrary fan-out multicast Benes network with full bandwidth. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network strictly nonblocking for arbitrary fan-out multicast Benes network with full bandwidth (col. 2, lines 8-11; see fanouts, Fig. 7B).

Therefore it would have been obvious to one ordinarily skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be strictly nonblocking for arbitrary fan-out multicast Benes network with full bandwidth, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 13, Wong discloses  $d = 2$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub integrated circuit block connecting said backward connecting links ('8x8 Benes network'; col. 2, lines 31-33) and a muting network being a butterfly fat tree network 7, but does not disclose said routing network is rearrangeably nonblocking for unicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being rearrangeably nonblocking for unicast traffic ('rearrangeably nonblocking for unicast traffic'; col. 2, lines 52-54).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a muting network be rearrangeably nonblocking for unicast traffic, as disclosed by Wu, in order to satisfy specific muting requirements.

In claim 14, Wong discloses wherein  $d = 2$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links ('8x8 Benes network'; col. 2, lines 31-33) and a routing network being a butterfly fat tree network (col. 13, lines 23-24), but does not disclose said routing network is strictly nonblocking for unicast traffic and rearrangeably nonblocking for arbitrary fan-out multicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being strictly nonblocking for unicast traffic (col. 2, lines

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9-11, see Fig. 9) and rearrangeably nonblocking for arbitrary fan-out multicast Benes network with full bandwidth (col. 4, lines 6-7; see 'fanouts', Fig. 7B).

Therefore it would have been obvious to one ordinarily skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be strictly nonblocking for unicast Benes and rearrangeably nonblocking for arbitrary fan-out multicast Benes network with full bandwidth, as disclosed by Wu, in order to satisfy specific muting requirements.

In claim 15, Wong discloses wherein  $d = 2$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links ('8x8 Benes network'; col. 2, Lines 31-33) and a routing network being a butterfly fat tree network with full-bandwidth (col. 13, lines 23-24), but does not disclose said routing network is strictly nonblocking for arbitrary fan-out multicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) wherein a routing network is strictly nonblocking for arbitrary fan-out (col. 2, lines 8-11; see "fanouts", Fig. 7B).

Therefore it would have been obvious to one ordinarily skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be strictly nonblocking for arbitrary fan-out multicast Benes network with full bandwidth, as disclosed by Wu, in order to satisfy specific routing requirements.

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In claim 26, Wong discloses  $d = 2$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub integrated circuit block connecting said backward connecting links and said routing network is generalized with full bandwidth (col. 2, lines 27-30; '2x2 Benes network'; col. 5, lines 26-31; "networks can be generalized"; col. 6, lines 7-9), but does not disclose said routing network is rearrangeably nonblocking for unicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being rearrangeably nonblocking for unicast traffic ('rearrangeably nonblocking for unicast traffic'; col. 2, lines 52-54).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be rearrangeably nonblocking for unicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 27, Wong discloses  $d = 2$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links ('8x8 Benes network' (each switch has two logic cells that are 2x2, hence 8x8 is 4 switches); col. 2, lines 31-33), and said routing network being a generalized network ('networks can be generalized'; col. 6, lines 7-9), but does not disclose said routing network is strictly nonblocking for unicast generalized multi-stage network and rearrangeably nonblocking for arbitrary fan-



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out multicast generalized multi-stage network with full bandwidth. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being rearrangeably nonblocking for arbitrary fan-out multicast multi-stage network with full bandwidth (col. 4, lines 6-7; see 'fanouts', Fig. 7B).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be rearrangeably nonblocking for arbitrary fan-out multicast generalized multi-stage network with full bandwidth, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 28, Wong discloses  $d = 2$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is a generalized routing network ('8x8 Benes network' (each switch has two logic cells that are 2x2, hence 8x8 is 4 switches); col. 2, lines 31-33; 'networks can be generalized'; col. 6, lines 7-9), but does not disclose said routing network is strictly nonblocking for arbitrary fan-out multicast multistage. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network strictly nonblocking for arbitrary fan-out multicast multistage (col. 2, lines 8-11; see 'fanouts', Fig. 7B).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing

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network be strictly nonblocking for arbitrary fan-out multicast multistage network with full bandwidth, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 30, Wong discloses  $d = 2$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub integrated circuit block connecting said backward connecting links and said routing network is a generalized butterfly fat tree network with full bandwidth (col. 2, lines 27-30; '2x2 Benes network'; col. 5, lines 26-31; 'networks can be generalized'; col. 6, lines 7-9; 'butterfly pattern'; col. 13, lines 23-24), but does not disclose said routing network is rearrangeably nonblocking for unicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being rearrangeably nonblocking for unicast traffic ('rearrangeably nonblocking for unicast traffic'; col. 2, lines 52-54).

Therefore it would have been obvious to one ordinarily skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be rearrangeably nonblocking for unicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 31, Wong discloses  $d = 2$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network being a generalized butterfly fat tree network with full-bandwidth ('8x8 Benes network' (each

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switch has two logic cells that are 2x2, hence 8x8 is 4 switches); col. 2, lines 31-33; 'networks can be generalized'; col. 6, lines 7-9; 'butterfly pattern'; col. 13, lines 23-24), but does not disclose said routing network is strictly nonblocking for unicast traffic and rearrangeably nonblocking for arbitrary fan-out multicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being strictly nonblocking for unicast traffic (col. 2, lines 9-11, see Fig. 9) and rearrangeably nonblocking for arbitrary fan-out multicast traffic (col. 4, lines 6-7; see 'fanouts', Fig. 7B).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a muting network be strictly nonblocking for unicast traffic and rearrangeably nonblocking for arbitrary fan-out multicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 32, Wong discloses wherein  $d = 2$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network generalized butterfly fat tree network with full bandwidth ('8x8 Benes network' (each switch has two logic calls that are 2x2, hence 8x8 is 4 switches); col. 2, lines 31-33; 'networks can be generalized'; col. 6, Lines 7-9), but does not disclose said routing network is strictly nonblocking for arbitrary fan-out multicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract)

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and a routing network strictly nonblocking for arbitrary fan-out multicast traffic (col. 2, lines 8-11; see 'fanouts', Fig. 7B).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be strictly nonblocking for arbitrary fan-out multicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 34, Wong discloses  $d = 4$  ('plurality of input terminals and a number of output terminals', claim 1) and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network multi-link Benes network with full bandwidth (col. 2, lines 27-30; '2x2 Benes network'; col. 5, lines 26-31), but does not disclose said routing network is rearrangeably nonblocking for unicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being rearrangeably nonblocking for unicast traffic ('rearrangeably nonblocking for unicast traffic'; col. 2, lines 52-54).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be rearrangeably nonblocking for unicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 35, Wong discloses  $d = 4$  ('plurality of input terminals and a number of output terminals', claim 1) and there are at least two switches in each said stage in each

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said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is a multi-link Benes network ('8x8 Benes network' (each switch has two logic cells that are 2x2, hence 8x8 is 4 switches); col. 2, lines 31-33; col. 6, lines 7-9), but does not disclose said routing network is strictly nonblocking for unicast traffic and rearrangeably nonblocking for arbitrary fan-out multicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being strictly nonblocking for unicast traffic (col. 2, lines 9-11, see Fig. 9) and rearrangeably nonblocking for arbitrary fan-out multicast traffic (col. 4, lines 6-7; see 'fanouts', Fig. 7B).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be strictly nonblocking for unicast traffic and rearrangeably nonblocking for arbitrary fan-out multicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 36, Wong discloses  $d = 4$  ('plurality of input terminals and a number of output terminals', claim 1 ) and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network multi-link Benes network with full bandwidth ('6x8 Benes network' (each switch has two logic cells that are 2x2, hence 8x8 is 4 switches); col. 2, lines 31-33; col. 6, lines 7-9), but does not

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disclose said routing network is strictly nonblocking for arbitrary fan-out multicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being rearrangeably nonblocking for arbitrary fan-out multicast traffic (col. 4, lines 6-7; see 'fanouts', Fig. 7B).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be rearrangeably nonblocking for arbitrary fan-out multicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 37, Wong discloses  $d = 4$  ('plurality of input terminals and a number of output terminals', claim 1) and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is a butterfly fat tree network with full bandwidth (col. 2, lines 27-30; col. 2, lines 31-33; 'butterfly pattern'; col. 13, lines 23-24); but does not disclose said routing network is rearrangeably nonblocking for unicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being rearrangeably nonblocking for unicast traffic ('rearrangeably nonblocking for unicast traffic'; col. 2, lines 52-54).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be rearrangeably nonblocking for unicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

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In claim 38, Wong discloses wherein  $d = 4$  ('plurality of input terminals and a number of output terminals', claim 1) and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links ('8x8 Benes network' (each switch has two logic cells that are 2x2. hence 8x8 is 4 switches); col. 2, lines 31-33; col. 6, lines 7-9) and said routing network is a multi-link butterfly fat tree network (col. 2, lines 27-30; col. 2, lines 31-33; 'butterfly pattern'; col. 13, lines 23-24), but does not disclose said routing network is strictly nonblocking for unicast and rearrangeably nonblocking for arbitrary fan-out multicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being strictly nonblocking for unicast traffic (col. 2, lines 9-11, see Fig. 9) and rearrangeably nonblocking for arbitrary fan-out multicast traffic (col. 4, lines 6-7; see 'fanouts', Fig. 7B).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be strictly nonblocking for unicast traffic and rearrangeably nonblocking for arbitrary fan-out multicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 39, Wong discloses  $d = 4$  ('plurality of input terminals and a number of output terminals', claim 1) and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit

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block connecting said backward connecting links and said routing network is a multi-link butterfly fat tree network with full bandwidth ('8x8 Benes network' (each switch has two logic cells that are 2x2. hence 8x8 is 4 switches; 'butterfly pattern'; col. 13, lines 23-24); col 2, lines 31-33; col. 6, lines 7-9), but does not disclose said routing network is strictly nonblocking for arbitrary fan-out multicast. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network strictly nonblocking for arbitrary fan-out multicast traffic (col. 2, lines 8-11; see 'fanouts', Fig. 7B).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be strictly nonblocking for arbitrary fan-out multicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 41, Wong discloses  $d = 4$  ('plurality of input terminals and a number of output terminals', claim 1) and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links (col. 2, lines 27-30; col. 2, lines 31-33) and said routing network is a generalized multi-link multi-stage network with full bandwidth ('networks can be generalized'; col. 6, lines 7-9), but does not disclose said routing network is rearrangeably nonblocking for unicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network



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being rearrangeably nonblocking for unicast traffic ('rearrangeably nonblocking for unicast traffic'; col. 2, lines 52-54).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be rearrangeably nonblocking for unicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 42, Wong discloses  $d = 4$  ('plurality of input terminals and a number of output terminals', claim 1) and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links ('8x8 Benes network' (each switch has two logic cells that are 2x2, hence 8x8 is 4 switches); col. 2, lines 31-33; col. 6, lines 7-9) and said routing network is a generalized multi-link multi-stage network ('networks can be generalized'; col. 6, lines 7-9), but does not disclose said routing network is strictly nonblocking for unicast and rearrangeably nonblocking for arbitrary fan-out multicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being strictly nonblocking for unicast traffic (col. 2, lines 9-11, see Fig. 9) and rearrangeably nonblocking for arbitrary fan-out multicast traffic (col. 4, lines 6-7; see "fanouts", Fig. 7B).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be strictly nonblocking for unicast traffic and rearrangeably nonblocking for

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arbitrary fan-out multicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 43, Wong discloses  $d = 4$  ('plurality of input terminals and a number of output terminals', claim 1) and there are at least three switches in each said stage in each said sub-integrated circuit connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is a generalized multi-link multistage network with full bandwidth ('8x8 Benes network' (each switch has two logic cells that are 2x2, hence 8x8 is 4 switches); col. 2, lines 31-33; col. 6, lines 7-9; 'networks can be generalized'; col. 6, lines 7-9), but does not disclose said routing network is strictly nonblocking for arbitrary fan-out multicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network strictly nonblocking for arbitrary fan-out multicast traffic (col. 2, lines 8-11; see 'fanouts', Fig. 7B).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be strictly nonblocking for arbitrary fan-out multicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 45, Wong discloses  $d = 4$  ('plurality of input terminals and a number of output terminals', claim 1) and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said

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backward connecting links and said routing network is a generalized multi-link butterfly fat tree network with full bandwidth (col. 2, lines 27-30; col. 2, lines 31-33; 'networks can be generalized'; col. 6, lines 7-9; 'butterfly pattern'; col. 13, lines 23-24), but does not disclose said routing network is rearrangeably nonblocking for unicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network being rearrangeably nonblocking for unicast traffic ('rearrangeably nonblocking for unicast traffic'; col. 2, lines 52-54).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be rearrangeably nonblocking for unicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 46, Wong discloses  $d = 4$  ('plurality of input terminals and a number of output terminals', claim 1) and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network generalized multi-link butterfly fat tree network with full bandwidth ('8x8 Benes network' (each switch has two logic cells that are 2x2, hence 8x8 is 4 switches); col. 2, lines 31-33; col. 6, lines 7-9; 'networks can be generalized'; col. 6, lines 7-9; 'butterfly pattern'; col. 13, lines 23-24), but does not disclose said routing network is strictly nonblocking for unicast traffic and rearrangeably nonblocking for arbitrary fan-out multicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a

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routing network being strictly nonblocking for unicast traffic (col. 2, lines 9-11, see Fig. 9) and rearrangeably nonblocking for arbitrary fan-out multicast traffic (col. 4, lines 6-7; see 'fanouts', Fig. 7B).

Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be strictly nonblocking for unicast traffic and rearrangeably nonblocking for arbitrary fan-out multicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

In claim 47, Wong discloses  $d = 4$  ('plurality of input terminals and a number of output terminals', claim 1) and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is a generalized multilink butterfly fat tree network with full bandwidth ('8x8 Benes network' (each switch has two logic cells that are 2x2, hence 8x8 is 4 switches); col. 2, lines 31-33; col. 6, lines 7-9; networks can be generalized'; col. 6, lines 7-9; 'butterfly pattern'; Col. 13, Lines 23-24), but does not disclose said routing network is strictly nonblocking for arbitrary fan-out multicast traffic. However, in the same field of endeavor, Wu discloses a rearrangeable non-blocking switch (Abstract) and a routing network strictly nonblocking for arbitrary fan-out multicast traffic (col. 2, lines 8-11; see 'fanouts', Fig. 7B).

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Therefore it would have been obvious to one ordinary skilled in the art at the time of the invention was made to supplement the teachings of Wong and have a routing network be strictly nonblocking for arbitrary fan-out multicast traffic, as disclosed by Wu, in order to satisfy specific routing requirements.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571)272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shawki Ismail can be reached on (571) 272-3985. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Vibol Tan/  
Primary Examiner, Art Unit 2819



<b>Notice of References Cited</b>	Application/Control No. 12/601,275	Applicant(s)/Patent Under Reexamination KONDA, VENKAT	
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Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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I	US-			
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*	Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
U	Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)				
V					
W					
X					

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



## EAST Search History

## EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	35	(US-20080267182-\$ or US-20040114586-\$ or US-20030021267-\$ or US-20030112797-\$ or US-20030053456-\$ or US-20020051447-\$ or US-20020031118-\$ or US-20020031117-\$).did. or (US-8098081-\$ or US-7924052-\$ or US-7468974-\$ or US-7424011-\$ or US-7424010-\$ or US-7397796-\$ or US-7349387-\$ or US-7346049-\$ or US-7130920-\$ or US-6567858-\$ or US-7136380-\$ or US-6456838-\$ or US-6157643-\$ or US-6049542-\$ or US-5856977-\$ or US-5406556-\$ or US-4813038-\$ or US-7139266-\$ or US-7103059-\$ or US-7099314-\$ or US-7065074-\$ or US-7050429-\$ or US-7042873-\$ or US-7031303-\$ or US-7016345-\$ or US-6952418-\$).did. or (US-6201808-\$).did.	US-PGPUB; USPAT	OR	OFF	2012/02/02 10:27
S1	2	((("6940308") or ("7154887")).PN.	USPAT; USOCR	OR	OFF	2012/02/01 07:26
S2	3	((("6940308") or ("7154887") or ("20110037498")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/02/01 07:30
S3	81	nonblocking adj multicast	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 08:51
S4	46	non-blocking adj multicast	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 08:51
S5	8	non-blocking adj multi-cast	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 08:52
S6	111	S3 S4 S5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2012/02/02 08:52

			IBM_TDB			
S7	35	S6 and rearrangeably	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 08:53
S8	21	S6 and rearrangeable	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 08:53
S9	39	S7 S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 08:53
S10	2	(routing adj network) same (inlet adj links) same (outlet adj links)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 09:18
S11	173	(routing adj network) same (inputs) same (outputs)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 09:19
S12	223328	((("326") or ("370")).CLAS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 09:22
S13	108	S11 and S12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 09:22
S14	0	(routing adj network) same (inputs) same (outputs) same (higher adj stage) same (lower adj stage)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 09:31
S15	1	(routing adj network) and (inputs) and (outputs) and (higher adj stage) and (lower adj stage)	US-PGPUB; USPAT; USOCR; FPRS;	OR	OFF	2012/02/02 09:31

			EPO; JPO; DERWENT; IBM_TDB			
S16	2	(routing adj network) and (higher adj stage) and (lower adj stage)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 09:31
S17	24	(routing adj network) and (cross adj links)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 09:32
S18	5	(routing adj network) and (cross adj switches)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 09:32
S19	26	S17 S18	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 09:33
S20	882	(routing adj network) and stages	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 09:37
S21	20	(US-20080267182-\$ or US-20040114586-\$ or US-20030021267-\$).did. or (US-8098081-\$ or US-7924052-\$ or US-7468974-\$ or US-7424011-\$ or US-7424010-\$ or US-7397796-\$ or US-7349387-\$ or US-7346049-\$ or US-7130920-\$ or US-6567858-\$ or US-7136380-\$ or US-6456838-\$ or US-6157643-\$ or US-6049542-\$ or US-5856977-\$ or US-5406556-\$ or US-4813038-\$).did.	US-PGPUB; USPAT	OR	OFF	2012/02/02 09:39
S22	41	konda-venkat.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/02/02 09:40
S23	84	(routing adj network) and (multicast adj connections)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	OFF	2012/02/02 09:45


			DERWENT; IBM_TDB		
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**EAST Search History (Interference)**

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**2/ 2/ 2012 10:33:37 AM**

**C:\Users\vtan\Documents\EAST\Workspaces\12601275.wsp**

<b>Search Notes</b>  	<b>Application/Control No.</b>  12601275	<b>Applicant(s)/Patent Under Reexamination</b>  KONDA, VENKAT
	<b>Examiner</b>  VIBOL TAN	<b>Art Unit</b>  2819

SEARCHED			
Class	Subclass	Date	Examiner
326	38-41	2/2/12	VTan
370	390, 312, 360, 388, 412	2/2/12	VTan

SEARCH NOTES		
Search Notes	Date	Examiner
Inventor search	2/2/12	VTan
search report pct/us2008/064605	2/1/12	VTan
EAST text search	2/2/12	VTan

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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www.uspto.gov

Table with 4 columns: APPLICATION NUMBER (12/601,275), FILING OR 371(C) DATE (05/31/2010), FIRST NAMED APPLICANT (Venkat Konda), ATTY. DOCKET NO./TITLE (V-0045US)

CONFIRMATION NO. 6372

PUBLICATION NOTICE

38139
Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135



Title:VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS

Publication No.US-2011-0037498-A1
Publication Date:02/17/2011

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

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Table with 3 columns: U.S. APPLICATION NUMBER NO. (12/601,275), FIRST NAMED APPLICANT (Venkat Konda), ATTY. DOCKET NO. (V-0045US)

38139
Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

Table with 2 columns: INTERNATIONAL APPLICATION NO. (PCT/US08/64605), I.A. FILING DATE (05/22/2008), PRIORITY DATE (05/25/2007)

CONFIRMATION NO. 6372
371 ACCEPTANCE LETTER



Date Mailed: 11/09/2010

NOTICE OF ACCEPTANCE OF APPLICATION UNDER 35 U.S.C 371 AND 37 CFR 1.495

The applicant is hereby advised that the United States Patent and Trademark Office in its capacity as a Designated / Elected Office (37 CFR 1.495), has determined that the above identified international application has met the requirements of 35 U.S.C. 371, and is ACCEPTED for national patentability examination in the United States Patent and Trademark Office.

The United States Application Number assigned to the application is shown above and the relevant dates are:

Table with 2 columns: DATE OF RECEIPT OF 35 U.S.C. 371(c)(1), (c)(2) and (c)(4) REQUIREMENTS (05/31/2010), DATE OF COMPLETION OF ALL 35 U.S.C. 371 REQUIREMENTS (05/31/2010)

A Filing Receipt (PTO-103X) will be issued for the present application in due course. THE DATE APPEARING ON THE FILING RECEIPT AS THE " FILING DATE" IS THE DATE ON WHICH THE LAST OF THE 35 U.S.C. 371 (c)(1), (c)(2) and (c)(4) REQUIREMENTS HAS BEEN RECEIVED IN THE OFFICE. THIS DATE IS SHOWN ABOVE. The filing date of the above identified application is the international filing date of the international application (Article 11(3) and 35 U.S.C. 363). Once the Filing Receipt has been received, send all correspondence to the Group Art Unit designated thereon.

The following items have been received:

- Indication of Small Entity Status
• Copy of the International Application filed on 11/22/2009
• Copy of the International Search Report filed on 11/22/2009
• Oath or Declaration filed on 05/31/2010
• U.S. Basic National Fees filed on 11/22/2009
• Specification filed on 11/22/2009
• Claims filed on 11/22/2009
• Abstracts filed on 11/22/2009
• Drawings filed on 11/22/2009

Applicant is reminded that any communications to the United States Patent and Trademark Office must be mailed to the address given in the heading and include the U.S. application no. shown above (37 CFR 1.5)

NISA F GILCHRIST

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Telephone: (703) 756-1418





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Table with 7 columns: APPLICATION NUMBER, FILING or 371(c) DATE, GRP ART UNIT, FIL FEE REC'D, ATTY. DOCKET NO, TOT CLAIMS, IND CLAIMS. Row 1: 12/601,275, 05/31/2010, 2819, 1279, V-0045US, 49, 1

CONFIRMATION NO. 6372

38139
Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

FILING RECEIPT



Date Mailed: 11/09/2010

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Applicant(s)

Venkat Konda, San Jose, CA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/US08/64605 05/22/2008
which claims benefit of 60/940,394 05/25/2007

Foreign Applications

If Required, Foreign Filing License Granted: 04/08/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is US 12/601,275

Projected Publication Date: 02/17/2011

Non-Publication Request: No

Early Publication Request: No

\*\* SMALL ENTITY \*\*

**Title**

VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS

**Preliminary Class**

326

**PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES**

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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**Title 37, Code of Federal Regulations, 5.11 & 5.15**

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Table with 6 columns: APPLICATION NUMBER, FILING or 371(c) DATE, GRP ART UNIT, FIL FEE REC'D, ATTY. DOCKET NO, TOT CLAIMS, IND CLAIMS. Values: 12/601,275, 05/31/2010, 1279, V-0045US, 49, 1

CONFIRMATION NO. 6372

38139
Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

FILING RECEIPT



Date Mailed: 08/18/2010

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Applicant(s)

Venkat Konda, San Jose, CA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/US08/64605 05/22/2008
which claims benefit of 60/940,394 05/25/2007

Foreign Applications

If Required, Foreign Filing License Granted: 04/08/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is US 12/601,275

Projected Publication Date: 371 Perfected

Non-Publication Request: No

Early Publication Request: No

\*\* SMALL ENTITY \*\*

**Title**

VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS

**Preliminary Class**

**PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES**

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Table with 3 columns: U.S. APPLICATION NUMBER NO. (12/601,275), FIRST NAMED APPLICANT (Venkat Konda), ATTY. DOCKET NO. (V-0045US)

38139
Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

Table with 2 columns: INTERNATIONAL APPLICATION NO. (PCT/US08/64605), I.A. FILING DATE (05/22/2008), PRIORITY DATE (05/25/2007)

CONFIRMATION NO. 6372
371 ACCEPTANCE LETTER



Date Mailed: 08/18/2010

NOTICE OF ACCEPTANCE OF APPLICATION UNDER 35 U.S.C 371 AND 37 CFR 1.495

The applicant is hereby advised that the United States Patent and Trademark Office in its capacity as a Designated / Elected Office (37 CFR 1.495), has determined that the above identified international application has met the requirements of 35 U.S.C. 371, and is ACCEPTED for national patentability examination in the United States Patent and Trademark Office.

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• Copy of the International Search Report filed on 11/22/2009
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• Specification filed on 11/22/2009
• Claims filed on 11/22/2009
• Abstracts filed on 11/22/2009
• Drawings filed on 11/22/2009

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NISA F GILCHRIST

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<p><b>DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)</b></p> <p><input type="checkbox"/> Declaration Submitted With Initial Filing      OR      <input checked="" type="checkbox"/> Declaration Submitted After Initial Filing (surcharge (37 CFR 1.16(f)) required)</p>	Attorney Docket Number	
	First Named Inventor	Venkat Konda
	<i>COMPLETE IF KNOWN</i>	
	Application Number	12/601,275
	Filing Date	11/22/2009
	Art Unit	
Examiner Name		

I hereby declare that: (1) Each inventor's residence, mailing address, and citizenship are as stated below next to their name; and (2) I believe the inventor(s) named below to be the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention titled:

VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS

*(Title of the Invention)*

the application of which

is attached hereto

OR

was filed on (MM/DD/YYYY) 11/22/2009 as United States Application Number or PCT International Application Number 12/601,275 and was amended on (MM/DD/YYYY) \_\_\_\_\_ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified application, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

**Authorization To Permit Access To Application by Participating Offices**

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the above-identified patent application is filed access to the above-identified patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the above-identified patent application is filed to have access to the above-identified patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the above-identified patent application with respect to: 1) the above-identified patent application-as-filed; 2) any foreign application to which the above-identified patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the above-identified patent application; and 3) any U.S. application-as-filed from which benefit is sought in the above-identified patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing the Authorization to Permit Access to Application by Participating Offices.

[Page 1 of 3]

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 21 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

## DECLARATION — Utility or Design Patent Application

### Claim of Foreign Priority Benefits

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached?	
				YES	NO
PCT/US08/64605	USA	5/22/2008	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Additional foreign application number(s) are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

[Page 2 of 3]

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

**DECLARATION — Utility or Design Patent Application**

Direct all correspondence to:	<input checked="" type="checkbox"/>	The address associated with Customer Number:	<input type="text" value="38139"/>	OR	<input type="checkbox"/>	Correspondence address below
Name						
Address						
City			State		Zip	
Country		Telephone		Email		
<b>WARNING:</b>						
<p>Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available. Petitioner/applicant is advised that documents which form the record of a patent application (such as the PTO/SB/01) are placed into the Privacy Act system of records DEPARTMENT OF COMMERCE, COMMERCE-PAT-7, System name: <i>Patent Application Files</i>. Documents not retained in an application file (such as the PTO-2038) are placed into the Privacy Act system of COMMERCE/PAT-TM-10, System name: <i>Deposit Accounts and Electronic Funds Transfer Profiles</i>.</p> <p>I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.</p>						
<b>NAME OF SOLE OR FIRST INVENTOR:</b>			<input type="checkbox"/> A petition has been filed for this unsigned inventor			
Given Name (first and middle [if any])			Family Name or Surname			
Venkat			Konda			
Inventor's Signature				Date		
/Venkat Konda/				5/30/2010		
Residence: City	State	Country	Citizenship			
San Jose	CA	USA	USA			
Mailing Address						
6278 Grand Oak Way						
City	State	Zip	Country			
San Jose	CA	95135	USA			
<input type="checkbox"/> Additional inventors or a legal representative are being named on the _____ supplemental sheet(s) PTO/SB/02A or 02LR attached hereto						

## Electronic Patent Application Fee Transmittal

<b>Application Number:</b>	12601275
<b>Filing Date:</b>	
<b>Title of Invention:</b>	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
<b>First Named Inventor/Applicant Name:</b>	Venkat Konda
<b>Filer:</b>	Venkar Konda
<b>Attorney Docket Number:</b>	V-0045US

Filed as Small Entity

### U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
<b>Basic Filing:</b>				
Natl Stage Search Fee - U.S. was the ISA	2641	1	50	50
Natl Stage Exam Fee - all other cases	2633	1	110	110

**Pages:**

**Claims:**

**Miscellaneous-Filing:**

Oath/decl > 30 mo. from priority date	2617	1	65	65
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**Petition:**

**Patent-Appeals-and-Interference:**

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
<b>Post-Allowance-and-Post-Issuance:</b>				
<b>Extension-of-Time:</b>				
<b>Miscellaneous:</b>				
<b>Total in USD (\$)</b>				<b>225</b>

## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	7714705
<b>Application Number:</b>	12601275
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	6372
<b>Title of Invention:</b>	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
<b>First Named Inventor/Applicant Name:</b>	Venkat Konda
<b>Customer Number:</b>	38139
<b>Filer:</b>	Venkar Konda
<b>Filer Authorized By:</b>	
<b>Attorney Docket Number:</b>	V-0045US
<b>Receipt Date:</b>	31-MAY-2010
<b>Filing Date:</b>	
<b>Time Stamp:</b>	02:44:41
<b>Application Type:</b>	U.S. National Stage under 35 USC 371

### Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$225
RAM confirmation Number	6077
Deposit Account	
Authorized User	

### File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1	Application Data Sheet	sb0001.pdf	813566	no	3
			367e6d42d0fb354656cf1c0bddd5d1c98b7ef69f		

**Warnings:**

**Information:**

This is not an USPTO supplied ADS fillable form

2	Fee Worksheet (PTO-875)	fee-info.pdf	33177	no	2
			4bb705ab794b5cc83faa09fbadf2ba145c30903a		

**Warnings:**

**Information:**

<b>Total Files Size (in bytes):</b>	846743
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**This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.**

**New Applications Under 35 U.S.C. 111**

**If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.**

**National Stage of an International Application under 35 U.S.C. 371**

**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**

**New International Application Filed with the USPTO as a Receiving Office**

**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**

MULTIPLE DEPENDENT CLAIM  
FEE CALCULATION SHEET  
(FOR USE WITH FORM PTO-875)

SERIAL NO.

12-601,275

FILING DATE

APPLICANT(S)

CLAIMS

	AS FILED		AFTER 1 <sup>st</sup> AMENDMENT		AFTER 2 <sup>nd</sup> AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
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TOTAL IND.	1	↓		↓		↓
TOTAL DEP.	48	←		←		←
TOTAL CLAIMS	49					

	AS FILED		AFTER 1 <sup>st</sup> AMENDMENT		AFTER 2 <sup>nd</sup> AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
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100						
TOTAL IND.		↓		↓		↓
TOTAL DEP.		←		←		←
TOTAL CLAIMS						



# PATENT APPLICATION FEE DETERMINATION RECORD

Effective September 30, 2007

Application or Docket Number

12-601,275

## CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
U.S. NATIONAL STAGE FEES		
BASIC FEE	SMALL ENT. = \$155	LARGE ENT. = \$ 310
EXAMINATION FEE	Satisfies PCT Article 33(1)-(4) = \$ 50 / \$ 100	All other situations = \$ 100 / \$ 200
SEARCH FEE	U.S. is ISA = \$ 50 / \$ 100 ALL other countries = \$ 205 / \$ 410	ALL other situations = \$ 255 / \$ 510
FEE FOR EXTRA SPEC. PGS.	107 minus 100 =	7 / 50 = 1
TOTAL CHARGEABLE CLAIMS	49 minus 20 = *	29
INDEPENDENT CLAIMS	1 minus 3 = *	
MULTIPLE DEPENDENT CLAIM PRESENT <input type="checkbox"/>		

SMALL ENTITY TYPE  OR

OTHER THAN SMALL ENTITY

RATE	FEE
BASIC FEE	165
EXAM. FEE	110
SEARCH FEE	50
X\$130	135
X \$ 25 =	754
X \$ 105 =	
\$185	
TOTAL	1214

OR

OR

OR

OR

OR

RATE	FEE
BASIC FEE	
EXAM. FEE	
SEARCH FEE	
X\$260	
X \$ 50 =	
X \$ 210 =	
\$370	
TOTAL	

\* If the difference in column 1 is less than zero, enter "0" in column 2

## CLAIMS AS AMENDED - PART II

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total *	Minus **	=
	Independent *	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>			

SMALL ENTITY OR

OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE
X \$ 25 =	
X\$105	
\$185	
TOTAL ADDIT. FEE	

OR

OR

OR

OR

RATE	ADDITIONAL FEE
X \$ 50 =	
X\$210	
\$370	
TOTAL ADDIT. FEE	

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total *	Minus **	=
	Independent *	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>			

RATE	ADDITIONAL FEE
X \$ 25 =	
X\$105	
\$185	
TOTAL ADDIT. FEE	

OR

OR

OR

OR

RATE	ADDITIONAL FEE
X \$ 50 =	
X\$210	
\$370	
TOTAL ADDIT. FEE	

\* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.  
 \*\* If the "Highest Number Previously Paid For" IN THIS SPACE is less than '20', enter "20".  
 \*\*\* If the "Highest Number Previously Paid For" IN THIS SPACE is less than '3', enter "3".  
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

Table with 3 columns: U.S. APPLICATION NUMBER NO. (12/601,275), FIRST NAMED APPLICANT (Venkat Konda), ATTY. DOCKET NO. (V-0045US)

38139
Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

Table with 2 columns: INTERNATIONAL APPLICATION NO. (PCT/US08/64605), I.A. FILING DATE (05/22/2008), PRIORITY DATE (05/25/2007)

CONFIRMATION NO. 6372
371 FORMALITIES LETTER



Date Mailed: 04/08/2010

NOTIFICATION OF MISSING REQUIREMENTS UNDER 35 U.S.C. 371
IN THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US)

The following items have been submitted by the applicant or the IB to the United States Patent and Trademark Office as a Designated Office (37 CFR 1.494):

- Indication of Small Entity Status
• Priority Document
• Copy of the International Application filed on 11/22/2009
• Copy of the International Search Report filed on 11/22/2009
• Oath or Declaration filed on 11/22/2009
• U.S. Basic National Fees filed on 11/22/2009
• Specification filed on 11/22/2009
• Claims filed on 11/22/2009
• Abstracts filed on 11/22/2009
• Drawings filed on 11/22/2009

The applicant needs to satisfy supplemental fees problems indicated below.

The following items MUST be furnished within the period set forth below in order to complete the requirements for acceptance under 35 U.S.C. 371:

- Oath or declaration of the inventors, in compliance with 37 CFR 1.497(a) and (b), identifying the application by the International application number and international filing date.
• Oath or declaration of the inventors, in compliance with 37 CFR 1.497(a) and (b), identifying the application by the International application number and international filing date. The current oath or declaration does not comply with 37 CFR 1.497(a) and (b) in that it:
• THE PTO/SB/01A OATH REQUIRES AN APPLICATION DATA SHEET.(37 CFR 1.76)
• To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.492(h) of \$65 for a small entity in compliance with 37 CFR 1.27, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fees required for this application is \$225 for a Small Entity:

- \$65 Surcharge.
• The application search fee has not been paid. Applicant must submit \$50 to complete the search fee. Note a surcharge will be required if submitted later than commencement of the national stage (37 CFR 1.492(h)) and the basic national fee was not paid before July 1, 2005.

- The application examination fee has not been paid. Applicant must submit \$110 to complete the examination fee for a small entity in compliance with 37 CFR 1.27. Note a surcharge will be required if submitted later than commencement of the national stage (37 CFR 1.492(h)) and the basic national fee was not paid before July 1, 2005.

**ALL OF THE ITEMS SET FORTH ABOVE MUST BE SUBMITTED WITHIN TWO (2) MONTHS FROM THE DATE OF THIS NOTICE OR BY 32 MONTHS FROM THE PRIORITY DATE FOR THE APPLICATION, WHICHEVER IS LATER. FAILURE TO PROPERLY RESPOND WILL RESULT IN ABANDONMENT.**

The time period set above may be extended by filing a petition and fee for extension of time under the provisions of 37 CFR 1.136(a).

Applicant is reminded that any communications to the United States Patent and Trademark Office must be mailed to the address given in the heading and include the U.S. application no. shown above (37 CFR 1.5)

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.  
<https://portal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html>

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at <http://www.uspto.gov/ebc>.

**If you are not using EFS-Web to submit your reply, you must include a copy of this notice.**

ANITA D JOHNSON

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Telephone: (571) 272-0386

## Electronic Patent Application Fee Transmittal

<b>Application Number:</b>	12601275
<b>Filing Date:</b>	
<b>Title of Invention:</b>	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
<b>First Named Inventor/Applicant Name:</b>	Venkat Konda
<b>Filer:</b>	Venkar Konda
<b>Attorney Docket Number:</b>	V-0045US

Filed as Small Entity

### U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
<b>Basic Filing:</b>				
Basic National Stage Fee	2631	1	165	165
<b>Pages:</b>				
Natl Stage Appl Sz fee per 50 pgs >100	2681	1	135	135
<b>Claims:</b>				
Claims in excess of 20	2615	29	26	754
<b>Miscellaneous-Filing:</b>				
<b>Petition:</b>				
<b>Patent-Appeals-and-Interference:</b>				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
<b>Post-Allowance-and-Post-Issuance:</b>				
<b>Extension-of-Time:</b>				
<b>Miscellaneous:</b>				
<b>Total in USD (\$)</b>				<b>1054</b>

## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	6694837
<b>Application Number:</b>	12601275
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	6372
<b>Title of Invention:</b>	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
<b>First Named Inventor/Applicant Name:</b>	Venkat Konda
<b>Customer Number:</b>	38139
<b>Filer:</b>	Venkar Konda
<b>Filer Authorized By:</b>	
<b>Attorney Docket Number:</b>	V-0045US
<b>Receipt Date:</b>	22-DEC-2009
<b>Filing Date:</b>	
<b>Time Stamp:</b>	19:05:08
<b>Application Type:</b>	U.S. National Stage under 35 USC 371

### Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$1054
RAM confirmation Number	6404
Deposit Account	
Authorized User	

### File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1	Fee Worksheet (PTO-875)	fee-info.pdf	33527 86105945f3d107d6a07e8ca63ed220c3f09331a7	no	2
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**Warnings:**

**Information:**

<b>Total Files Size (in bytes):</b>	33527
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**This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.**

**New Applications Under 35 U.S.C. 111**

**If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.**

**National Stage of an International Application under 35 U.S.C. 371**

**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**

**New International Application Filed with the USPTO as a Receiving Office**

**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**





## Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN  
APPLICATION DATA SHEET (37 CFR 1.76)****Title of  
Invention**

VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS

As the below named inventor(s), I/we declare that:

This declaration is directed to:



The attached application, or



Application No. \_\_\_\_\_ filed on \_\_\_\_\_



As amended on \_\_\_\_\_ (if applicable);

I/we believe that I/we am/are the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought;

I/we have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment specifically referred to above;

I/we acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me/us to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.

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All statements made herein of my/our own knowledge are true, all statements made herein on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and may jeopardize the validity of the application or any patent issuing thereon.

FULL NAME OF INVENTOR(S)

Inventor one: Venkat KondaDate: 11/22/2009Signature: /Venkat Konda/Citizen of: USA

Inventor two: \_\_\_\_\_

Date: \_\_\_\_\_

Signature: \_\_\_\_\_

Citizen of: \_\_\_\_\_

 Additional inventors or a legal representative are being named on \_\_\_\_\_ additional form(s) attached hereto.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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## Electronic Patent Application Fee Transmittal

<b>Application Number:</b>	
<b>Filing Date:</b>	
<b>Title of Invention:</b>	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
<b>First Named Inventor/Applicant Name:</b>	Venkat Konda
<b>Filer:</b>	Venkar Konda
<b>Attorney Docket Number:</b>	V-0045US

Filed as Small Entity

### U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
<b>Basic Filing:</b>				
Basic National Stage Fee	2631	1	165	165
Natl Stage Search - U.S. as IPEA or ISA	2640	1	0	0
<b>Pages:</b>				
Natl Stage Appl Sz fee per 50 pgs >100	2681	1	135	135
<b>Claims:</b>				
Claims in excess of 20	2615	29	26	754
<b>Miscellaneous-Filing:</b>				

<b>Petition:</b>
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Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
<b>Patent-Appeals-and-Interference:</b>				
<b>Post-Allowance-and-Post-Issuance:</b>				
<b>Extension-of-Time:</b>				
<b>Miscellaneous:</b>				
<b>Total in USD (\$)</b>				<b>1054</b>

## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	6501767
<b>Application Number:</b>	12601275
<b>International Application Number:</b>	PCT/US08/64605
<b>Confirmation Number:</b>	6372
<b>Title of Invention:</b>	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
<b>First Named Inventor/Applicant Name:</b>	Venkat Konda
<b>Customer Number:</b>	38139
<b>Filer:</b>	Venkar Konda
<b>Filer Authorized By:</b>	
<b>Attorney Docket Number:</b>	V-0045US
<b>Receipt Date:</b>	22-NOV-2009
<b>Filing Date:</b>	
<b>Time Stamp:</b>	23:28:30
<b>Application Type:</b>	U.S. National Stage under 35 USC 371

### Payment information:

Submitted with Payment	no
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### File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Specification	V-0045US.pdf	299380 <small>debb4d8182a1df928e5922e1c44142090bb a7555</small>	no	69

### Warnings:

### Information:

2	Drawings-only black and white line drawings	V-0045US-FIGs.pdf	581351 9345637693e597fd4d92e2aa679baa691e95ca78	no	39
<b>Warnings:</b>					
<b>Information:</b>					
3	Transmittal of New Application	sb0005_fill.pdf	468829 959ba37f3439c0e68be3c2ba5915c1a196e60d2f	no	2
<b>Warnings:</b>					
<b>Information:</b>					
4	Application Data Sheet	sb0001a.pdf	545678 6fdc91490275bb543e412eafcd318937bc0281	no	2
<b>Warnings:</b>					
<b>Information:</b>					
This is not an USPTO supplied ADS fillable form					
5	Fee Worksheet (PTO-875)	fee-info.pdf	36986 f3996036a9d41e6a4b815016dd7db9f3066caa82	no	2
<b>Warnings:</b>					
<b>Information:</b>					
<b>Total Files Size (in bytes):</b>			1932224		
<p><b>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</b></p> <p><b><u>New Applications Under 35 U.S.C. 111</u></b>  <b>If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</b></p> <p><b><u>National Stage of an International Application under 35 U.S.C. 371</u></b>  <b>If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</b></p> <p><b><u>New International Application Filed with the USPTO as a Receiving Office</u></b>  <b>If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</b></p>					

## VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS

**Venkat Konda**

### 5 CROSS REFERENCE TO RELATED APPLICATIONS

This application is related to and claims priority of the PCT Application Serial No. PCT/US08/64605 entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 22, 2008, and the U.S. Provisional Patent Application  
10 Serial No. 60/940,394 entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

This application is related to and incorporates by reference in its entirety the US Application Serial No. 12/530,207 entitled "FULLY CONNECTED GENERALIZED  
15 MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed September 6, 2009, the PCT Application Serial No. PCT/US08/56064 entitled "FULLY CONNECTED GENERALIZED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application,  
filed March 6, 2008, the U.S. Provisional Patent Application Serial No. 60/905,526  
20 entitled "LARGE SCALE CROSSPOINT REDUCTION WITH NONBLOCKING UNICAST & MULTICAST IN ARBITRARILY LARGE MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed March 6, 2007, and the U.S. Provisional Patent Application Serial No. 60/940,383  
25 entitled "FULLY CONNECTED GENERALIZED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.



This application is related to and incorporates by reference in its entirety the US Patent Application Docket No. V-0038US entitled "FULLY CONNECTED GENERALIZED BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application filed concurrently, the PCT Application  
5 Serial No. PCT/US08/64603 entitled "FULLY CONNECTED GENERALIZED BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 22, 2008, the U.S. Provisional Patent Application Serial No. 60/940, 387 entitled "FULLY CONNECTED GENERALIZED BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same  
10 assignee as the current application, filed May 25, 2007, and the U.S. Provisional Patent Application Serial No. 60/940, 390 entitled "FULLY CONNECTED GENERALIZED MULTI-LINK BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

This application is related to and incorporates by reference in its entirety the US  
15 Patent Application Docket No. V-0039US entitled "FULLY CONNECTED GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application filed concurrently, the PCT Application Serial No. PCT/US08/64604 entitled "FULLY CONNECTED  
20 GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 22, 2008, the U.S. Provisional Patent Application Serial No. 60/940, 389 entitled "FULLY CONNECTED GENERALIZED REARRANGEABLY NONBLOCKING MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current  
25 application, filed May 25, 2007, the U.S. Provisional Patent Application Serial No. 60/940, 391 entitled "FULLY CONNECTED GENERALIZED FOLDED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007 and the U.S. Provisional Patent Application Serial No. 60/940, 392 entitled "FULLY CONNECTED GENERALIZED STRICTLY  
30 NONBLOCKING MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

This application is related to and incorporates by reference in its entirety the U.S. Provisional Patent Application Serial No. 61/252, 603 entitled "VLSI LAYOUTS OF FULLY CONNECTED NETWORKS WITH LOCALITY EXPLOITATION" by Venkat Konda assigned to the same assignee as the current application, filed October 16, 2009.

5 This application is related to and incorporates by reference in its entirety the U.S. Provisional Patent Application Serial No. 61/252, 609 entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED AND PYRAMID NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed October 16, 2009.

## 10 BACKGROUND OF INVENTION

Multi-stage interconnection networks such as Benes networks and butterfly fat tree networks are widely useful in telecommunications, parallel and distributed computing. However VLSI layouts, known in the prior art, of these interconnection networks in an integrated circuit are inefficient and complicated.

15 Other multi-stage interconnection networks including butterfly fat tree networks, Banyan networks, Batcher-Banyan networks, Baseline networks, Delta networks, Omega networks and Flip networks have been widely studied particularly for self routing packet switching applications. Also Benes Networks with radix of two have been widely studied and it is known that Benes Networks of radix two are shown to be built with back to back  
20 baseline networks which are rearrangeably nonblocking for unicast connections.

The most commonly used VLSI layout in an integrated circuit is based on a two-dimensional grid model comprising only horizontal and vertical tracks. An intuitive interconnection network that utilizes two-dimensional grid model is 2D Mesh Network and its variations such as segmented mesh networks. Hence routing networks used in  
25 VLSI layouts are typically 2D mesh networks and its variations. However Mesh Networks require large scale cross points typically with a growth rate of  $O(N^2)$  where N is the number of computing elements, ports, or logic elements depending on the application.

Multi-stage interconnection with a growth rate of  $O(N \times \log N)$  requires significantly small number of cross points. U.S. Patent 6,185,220 entitled “Grid Layouts of Switching and Sorting Networks” granted to Muthukrishnan et al. describes a VLSI layout using existing VLSI grid model for Benes and Butterfly networks. U.S. Patent 5 6,940,308 entitled “Interconnection Network for a Field Programmable Gate Array” granted to Wong describes a VLSI layout where switches belonging to lower stage of Benes Network are layed out close to the logic cells and switches belonging to higher stages are layed out towards the center of the layout.

Due to the inefficient and in some cases impractical VLSI layout of Benes and 10 butterfly fat tree networks on a semiconductor chip, today mesh networks and segmented mesh networks are widely used in the practical applications such as field programmable gate arrays (FPGAs), programmable logic devices (PLDs), and parallel computing interconnects. The prior art VLSI layouts of Benes and butterfly fat tree networks and VLSI layouts of mesh networks and segmented mesh networks require large area to 15 implement the switches on the chip, large number of wires, longer wires, with increased power consumption, increased latency of the signals which effect the maximum clock speed of operation. Some networks may not even be implemented practically on a chip due to the lack of efficient layouts.

## 20 SUMMARY OF INVENTION

When large scale sub-integrated circuit blocks with inlet and outlet links are layed out in an integrated circuit device in a two-dimensional grid arrangement, (for example in an FPGA where the sub-integrated circuit blocks are Lookup Tables) the most intuitive routing network is a network that uses horizontal and vertical links only (the most often 25 used such a network is one of the variations of a 2D Mesh network). A direct embedding of a generalized multi-stage network on to a 2D Mesh network is neither simple nor efficient.

In accordance with the invention, VLSI layouts of generalized multi-stage networks for broadcast, unicast and multicast connections are presented using only

- horizontal and vertical links. The VLSI layouts employ shuffle exchange links where outlet links of cross links from switches in a stage in one sub-integrated circuit block are connected to inlet links of switches in the succeeding stage in another sub-integrated circuit block so that said cross links are either vertical links or horizontal and vice versa.
- 5 In one embodiment the sub-integrated circuit blocks are arranged in a hypercube arrangement in a two-dimensional plane. The VLSI layouts exploit the benefits of significantly lower cross points, lower signal latency, lower power and full connectivity with significantly fast compilation.

- The VLSI layouts presented are applicable to generalized multi-stage networks
- 10  $V(N_1, N_2, d, s)$ , generalized folded multi-stage networks  $V_{fold}(N_1, N_2, d, s)$ , generalized butterfly fat tree networks  $V_{bft}(N_1, N_2, d, s)$ , generalized multi-link multi-stage networks  $V_{mlink}(N_1, N_2, d, s)$ , generalized folded multi-link multi-stage networks  $V_{fold-mlink}(N_1, N_2, d, s)$ , generalized multi-link butterfly fat tree networks  $V_{mlink-bft}(N_1, N_2, d, s)$ , and generalized hypercube networks  $V_{cube}(N_1, N_2, d, s)$  for  $s =$
- 15 1,2,3 or any number in general. The embodiments of VLSI layouts are useful in wide target applications such as FPGAs, CPLDs, pSoCs, ASIC placement and route tools, networking applications, parallel & distributed computing, and reconfigurable computing.

#### BRIEF DESCRIPTION OF DRAWINGS

- 20 FIG. 1A is a diagram 100A of an exemplary symmetrical multi-link multi-stage network  $V_{fold-mlink}(N, d, s)$  having inverse Benes connection topology of nine stages with  $N = 32$ ,  $d = 2$  and  $s=2$ , strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.
- 25 FIG. 1B is a diagram 100B of the equivalent symmetrical folded multi-link multi-stage network  $V_{fold-mlink}(N, d, s)$  of the network 100A shown in FIG. 1A, having inverse Benes connection topology of five stages with  $N = 32$ ,  $d = 2$  and  $s=2$ , strictly nonblocking

network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1C is a diagram 100C layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 1B, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 1D is a diagram 100D layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 1B, in one embodiment, illustrating the connection links ML(1,i) for  $i = [1, 64]$  and ML(8,i) for  $i = [1, 64]$ .

FIG. 1E is a diagram 100E layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 1B, in one embodiment, illustrating the connection links ML(2,i) for  $i = [1, 64]$  and ML(7,i) for  $i = [1, 64]$ .

FIG. 1F is a diagram 100F layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 1B, in one embodiment, illustrating the connection links ML(3,i) for  $i = [1, 64]$  and ML(6,i) for  $i = [1, 64]$ .

FIG. 1G is a diagram 100G layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 1B, in one embodiment, illustrating the connection links ML(4,i) for  $i = [1, 64]$  and ML(5,i) for  $i = [1, 64]$ .

FIG. 1H is a diagram 100H layout of a network  $V_{fold-link}(N, d, s)$  where  $N = 128$ ,  $d = 2$ , and  $s = 2$ , in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 1I is a diagram 100I detailed connections of BLOCK 1\_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing  $V(N, d, s)$  or  $V_{fold}(N, d, s)$ .

FIG. 1J is a diagram 100J detailed connections of BLOCK 1\_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing  $V(N, d, s)$  or  $V_{fold}(N, d, s)$ .

FIG. 1K is a diagram 100K detailed connections of BLOCK 1\_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing  $V(N, d, s)$  or  $V_{fold}(N, d, s)$ .

FIG. 1K1 is a diagram 100M1 detailed connections of BLOCK 1\_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing  $V(N, d, s)$  or  $V_{fold}(N, d, s)$  for  $s = 1$ .

FIG. 1L is a diagram 100L detailed connections of BLOCK 1\_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing  $V(N, d, s)$  or  $V_{fold}(N, d, s)$ .

FIG. 1L1 is a diagram 100L1 detailed connections of BLOCK 1\_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing  $V(N, d, s)$  or  $V_{fold}(N, d, s)$  for  $s = 1$ .

FIG. 2A1 is a diagram 200A1 of an exemplary symmetrical multi-link multi-stage network  $V_{fold-mlink}(N, d, s)$  having inverse Benes connection topology of one stage with  $N = 2$ ,  $d = 2$  and  $s=2$ , strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention. FIG. 2A2 is a diagram 200A2 of the equivalent symmetrical folded multi-link multi-stage network  $V_{fold-mlink}(N, d, s)$  of the network 200A1 shown in FIG. 2A1, having inverse Benes connection topology of one stage with  $N = 2$ ,  $d = 2$  and  $s=2$ , strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention. FIG. 2A3 is a diagram 200A3 layout of the network  $V_{fold-mlink}(N, d, s)$  shown in FIG. 2A2, in one embodiment, illustrating all the connection links.

FIG. 2B1 is a diagram 200B1 of an exemplary symmetrical multi-link multi-stage network  $V_{fold-link}(N, d, s)$  having inverse Benes connection topology of one stage with  $N = 4$ ,  $d = 2$  and  $s=2$ , strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention. FIG. 2B2 is a diagram 200B2 of the equivalent symmetrical folded multi-link multi-stage network  $V_{fold-link}(N, d, s)$  of the network 200B1 shown in FIG. 2B1, having inverse Benes connection topology of one stage with  $N = 4$ ,  $d = 2$  and  $s=2$ , strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention. FIG. 2B3 is a diagram 200B3 layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 2B2, in one embodiment, illustrating the connection links belonging with in each block only. FIG. 2B4 is a diagram 200B4 layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 2B2, in one embodiment, illustrating the connection links ML(1,i) for  $i = [1, 8]$  and ML(2,i) for  $i = [1, 8]$ .

FIG. 2C11 is a diagram 200C11 of an exemplary symmetrical multi-link multi-stage network  $V_{fold-link}(N, d, s)$  having inverse Benes connection topology of one stage with  $N = 8$ ,  $d = 2$  and  $s=2$ , strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention. FIG. 2C12 is a diagram 200C12 of the equivalent symmetrical folded multi-link multi-stage network  $V_{fold-link}(N, d, s)$  of the network 200C11 shown in FIG. 2C11, having inverse Benes connection topology of one stage with  $N = 8$ ,  $d = 2$  and  $s=2$ , strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 2C21 is a diagram 200C21 layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 2C12, in one embodiment, illustrating the connection links belonging with in each block only. FIG. 2C22 is a diagram 200C22 layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 2C12, in one embodiment, illustrating the connection links ML(1,i) for  $i =$

[1, 16] and  $ML(4,i)$  for  $i = [1,16]$ . FIG. 2C23 is a diagram 200C23 layout of the network  $V_{fold-mlink}(N,d,s)$  shown in FIG. 2C12, in one embodiment, illustrating the connection links  $ML(2,i)$  for  $i = [1, 16]$  and  $ML(3,i)$  for  $i = [1,16]$ .

FIG. 2D1 is a diagram 200D1 of an exemplary symmetrical multi-link multi-stage network  $V_{fold-mlink}(N,d,s)$  having inverse Benes connection topology of one stage with  $N = 16$ ,  $d = 2$  and  $s=2$ , strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 2D2 is a diagram 200D2 of the equivalent symmetrical folded multi-link multi-stage network  $V_{fold-mlink}(N,d,s)$  of the network 200D1 shown in FIG. 2D1, having inverse Benes connection topology of one stage with  $N = 16$ ,  $d = 2$  and  $s=2$ , strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 2D3 is a diagram 200D3 layout of the network  $V_{fold-mlink}(N,d,s)$  shown in FIG. 2D2, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 2D4 is a diagram 200D4 layout of the network  $V_{fold-mlink}(N,d,s)$  shown in FIG. 2D2, in one embodiment, illustrating the connection links  $ML(1,i)$  for  $i = [1, 32]$  and  $ML(6,i)$  for  $i = [1,32]$ .

FIG. 2D5 is a diagram 200D5 layout of the network  $V_{fold-mlink}(N,d,s)$  shown in FIG. 2D2, in one embodiment, illustrating the connection links  $ML(2,i)$  for  $i = [1, 32]$  and  $ML(5,i)$  for  $i = [1,32]$ .

FIG. 2D6 is a diagram 200D6 layout of the network  $V_{fold-mlink}(N,d,s)$  shown in FIG. 2D2, in one embodiment, illustrating the connection links  $ML(3,i)$  for  $i = [1, 32]$  and  $ML(4,i)$  for  $i = [1,32]$ .



FIG. 3A is a diagram 300A of an exemplary symmetrical multi-link multi-stage network  $V_{cube}(N,d,s)$  having inverse Benes connection topology of nine stages with  $N = 32$ ,  $d = 2$  and  $s=2$ , strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 3B is a diagram 300B of the equivalent symmetrical folded multi-link multi-stage network  $V_{cube}(N,d,s)$  of the network 300A shown in FIG. 3A, having inverse Benes connection topology of five stages with  $N = 32$ ,  $d = 2$  and  $s=2$ , strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 3C is a diagram 300C layout of the network  $V_{cube}(N,d,s)$  shown in FIG. 3B, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 3D is a diagram 100D layout of the network  $V_{cube}(N,d,s)$  shown in FIG. 3B, in one embodiment, illustrating the connection links  $ML(1,i)$  for  $i = [1, 64]$  and  $ML(8,i)$  for  $i = [1,64]$ .

FIG. 3E is a diagram 300E layout of the network  $V_{cube}(N,d,s)$  shown in FIG. 3B, in one embodiment, illustrating the connection links  $ML(2,i)$  for  $i = [1, 64]$  and  $ML(7,i)$  for  $i = [1,64]$ .

FIG. 3F is a diagram 300F layout of the network  $V_{cube}(N,d,s)$  shown in FIG. 3B, in one embodiment, illustrating the connection links  $ML(3,i)$  for  $i = [1, 64]$  and  $ML(6,i)$  for  $i = [1,64]$ .

FIG. 3G is a diagram 300G layout of the network  $V_{cube}(N,d,s)$  shown in FIG. 3B, in one embodiment, illustrating the connection links  $ML(4,i)$  for  $i = [1, 64]$  and  $ML(5,i)$  for  $i = [1,64]$ .

FIG. 3H is a diagram 300H layout of a network  $V_{\text{hcube}}(N, d, s)$  where  $N = 128$ ,  $d = 2$ , and  $s = 2$ , in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 4A is a diagram 400A layout of the network  $V_{\text{fold-link}}(N, d, s)$  shown in FIG. 1B, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 4B is a diagram 400B layout of the network  $V_{\text{fold-link}}(N, d, s)$  shown in FIG. 1B, in one embodiment, illustrating the connection links  $ML(1,i)$  for  $i = [1, 64]$  and  $ML(8,i)$  for  $i = [1,64]$ .

FIG. 4C is a diagram 400C layout of the network  $V_{\text{fold-link}}(N, d, s)$  shown in FIG. 4C, in one embodiment, illustrating the connection links  $ML(2,i)$  for  $i = [1, 64]$  and  $ML(7,i)$  for  $i = [1,64]$ .

FIG. 4D is a diagram 400D layout of the network  $V_{\text{fold-link}}(N, d, s)$  shown in FIG. 4D, in one embodiment, illustrating the connection links  $ML(3,i)$  for  $i = [1, 64]$  and  $ML(6,i)$  for  $i = [1,64]$ .

FIG. 4E is a diagram 400E layout of the network  $V_{\text{fold-link}}(N, d, s)$  shown in FIG. 4E, in one embodiment, illustrating the connection links  $ML(4,i)$  for  $i = [1, 64]$  and  $ML(5,i)$  for  $i = [1,64]$ .

FIG. 4C1 is a diagram 400C1 layout of the network  $V_{\text{fold-link}}(N, d, s)$  shown in FIG. 1B, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 5A1 is a diagram 500A1 of an exemplary prior art implementation of a two by two switch; FIG. 5A2 is a diagram 500A2 for programmable integrated circuit prior art implementation of the diagram 500A1 of FIG. 5A1; FIG. 5A3 is a diagram 500A3 for one-time programmable integrated circuit prior art implementation of the diagram 500A1

of FIG. 5A1; FIG. 5A4 is a diagram 500A4 for integrated circuit placement and route implementation of the diagram 500A1 of FIG. 5A1.

#### DETAILED DESCRIPTION OF THE INVENTION

5           The present invention is concerned with the VLSI layouts of arbitrarily large switching networks for broadcast, unicast and multicast connections. Particularly switching networks considered in the current invention include: generalized multi-stage networks  $V(N_1, N_2, d, s)$ , generalized folded multi-stage networks  $V_{fold}(N_1, N_2, d, s)$ , generalized butterfly fat tree networks  $V_{bft}(N_1, N_2, d, s)$ , generalized multi-link multi-  
 10 stage networks  $V_{mlink}(N_1, N_2, d, s)$ , generalized folded multi-link multi-stage networks  $V_{fold-mlink}(N_1, N_2, d, s)$ , generalized multi-link butterfly fat tree networks  $V_{mlink-bft}(N_1, N_2, d, s)$ , and generalized hypercube networks  $V_{hcube}(N_1, N_2, d, s)$  for  $s = 1, 2, 3$  or any number in general.

Efficient VLSI layout of networks on a semiconductor chip are very important  
 15 and greatly influence many important design parameters such as the area taken up by the network on the chip, total number of wires, length of the wires, latency of the signals, capacitance and hence the maximum clock speed of operation. Some networks may not even be implemented practically on a chip due to the lack of efficient layouts. The different varieties of multi-stage networks described above have not been implemented  
 20 previously on the semiconductor chips efficiently. For example in Field Programmable Gate Array (FPGA) designs, multi-stage networks described in the current invention have not been successfully implemented primarily due to the lack of efficient VLSI layouts. Current commercial FPGA products such as Xilinx Vertex, Altera's Stratix implement island-style architecture using mesh and segmented mesh routing interconnects using  
 25 either full crossbars or sparse crossbars. These routing interconnects consume large silicon area for crosspoints, long wires, large signal propagation delay and hence consume lot of power.

The current invention discloses the VLSI layouts of numerous types of multi-stage networks which are very efficient. Moreover they can be embedded on to mesh and segmented mesh routing interconnects of current commercial FPGA products. The VLSI layouts disclosed in the current invention are applicable to including the numerous  
 5 generalized multi-stage networks disclosed in the following patent applications, filed concurrently:

1) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-stage networks  $V(N_1, N_2, d, s)$  with numerous connection topologies and the scheduling methods are described in detail in the PCT Application  
 10 Serial No. PCT/US08/56064 that is incorporated by reference above.

2) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized butterfly fat tree networks  $V_{bft}(N_1, N_2, d, s)$  with numerous connection topologies and the scheduling methods are described in detail in PCT Application Serial No. PCT/US08/64603 that is incorporated by reference above.

15 3) Rearrangeably nonblocking for arbitrary fan-out multicast and unicast, and strictly nonblocking for unicast for generalized multi-link multi-stage networks  $V_{mlink}(N_1, N_2, d, s)$  and generalized folded multi-link multi-stage networks  $V_{fold-mlink}(N_1, N_2, d, s)$  with numerous connection topologies and the scheduling methods are described in detail in PCT Application Serial No. PCT/US08/64604 that is  
 20 incorporated by reference above.

4) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-link butterfly fat tree networks  $V_{mlink-bft}(N_1, N_2, d, s)$  with numerous connection topologies and the scheduling methods are described in detail in PCT Application Serial No. PCT/US08/64603 that is incorporated by reference above.

25 5) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized folded multi-stage networks  $V_{fold}(N_1, N_2, d, s)$  with numerous

connection topologies and the scheduling methods are described in detail in PCT Application Serial No. PCT/US08/64604 that is incorporated by reference above.

6) Strictly nonblocking for arbitrary fan-out multicast for generalized multi-link multi-stage networks  $V_{mlink}(N_1, N_2, d, s)$  and generalized folded multi-link multi-stage networks  $V_{fold-mlink}(N_1, N_2, d, s)$  with numerous connection topologies and the scheduling methods are described in detail in PCT Application Serial No. PCT/US08/64604 that is incorporated by reference above.

7) VLSI layouts of numerous types of multi-stage networks with locality exploitation are described in U.S. Provisional Patent Application Serial No. 61/252, 603 that is incorporated by reference above.

8) VLSI layouts of numerous types of multistage pyramid networks are described in U.S. Provisional Patent Application Serial No. 61/252, 609 that is incorporated by reference above.

In addition the layouts of the current invention are also applicable to generalized multi-stage pyramid networks  $V_p(N_1, N_2, d, s)$ , generalized folded multi-stage pyramid networks  $V_{fold-p}(N_1, N_2, d, s)$ , generalized butterfly fat pyramid networks  $V_{bfp}(N_1, N_2, d, s)$ , generalized multi-link multi-stage pyramid networks  $V_{mlink-p}(N_1, N_2, d, s)$ , generalized folded multi-link multi-stage pyramid networks  $V_{fold-mlink-p}(N_1, N_2, d, s)$ , generalized multi-link butterfly fat pyramid networks  $V_{mlink-bfp}(N_1, N_2, d, s)$ , and generalized hypercube networks  $V_{hcube}(N_1, N_2, d, s)$  for  $s = 1, 2, 3$  or any number in general.

**Symmetric RNB generalized multi-link multi-stage network  $V_{mlink}(N_1, N_2, d, s)$  :**

Referring to diagram 100A in FIG. 1A, in one embodiment, an exemplary generalized multi-link multi-stage network  $V_{mlink}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d =$

2; and  $s = 2$  with nine stages of one hundred and forty four switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, 150, 160, 170, 180 and 190 is shown where input stage 110 consists of sixteen, two by four switches IS1-IS16 and output stage 120 consists of sixteen, four by two switches OS1-OS16. And all the middle stages namely the middle stage 130 consists of sixteen, four by four switches MS(1,1) - MS(1,16), middle stage 140 consists of sixteen, four by four switches MS(2,1) - MS(2,16), middle stage 150 consists of sixteen, four by four switches MS(3,1) - MS(3,16), middle stage 160 consists of sixteen, four by four switches MS(4,1) - MS(4,16), middle stage 170 consists of sixteen, four by four switches MS(5,1) - MS(5,16), middle stage 180 consists of sixteen, four by four switches MS(6,1) - MS(6,16), and middle stage 190 consists of sixteen, four by four switches MS(7,1) - MS(7,16).

As disclosed in PCT Application Serial No. PCT/US08/64604 that is incorporated by reference above, such a network can be operated in rearrangeably non-blocking manner for arbitrary fan-out multicast connections and also can be operated in strictly non-blocking manner for unicast connections.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable  $\frac{N}{d}$ , where  $N$  is the total number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by  $\frac{N}{d}$ . The size of each input switch IS1-IS4 can be denoted in general with the notation  $d * 2d$  and each output switch OS1-OS4 can be denoted in general with the notation  $2d * d$ . Likewise, the size of each switch in any of the middle stages can be denoted as  $2d * 2d$ . A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. A symmetric multi-stage network can be represented with the notation  $V_{link}(N, d, s)$ , where  $N$  represents the total number of inlet links of all input switches

(for example the links IL1-IL32),  $d$  represents the inlet links of each input switch or outlet links of each output switch, and  $s$  is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Each of the  $\frac{N}{d}$  input switches IS1 – IS16 are connected to exactly  $d$  switches in middle stage 130 through two links each for a total of  $2 \times d$  links (for example input switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2), and also connected to middle switch MS(1,2) through the links ML(1,3) and ML(1,4)). The middle links which connect switches in the same row in two successive middle stages are called hereinafter straight middle links; and the middle links which connect switches in different rows in two successive middle stages are called hereinafter cross middle links. For example, the middle links ML(1,1) and ML(1,2) connect input switch IS1 and middle switch MS(1,1), so middle links ML(1,1) and ML(1,2) are straight middle links; where as the middle links ML(1,3) and ML(1,4) connect input switch IS1 and middle switch MS(1,2), since input switch IS1 and middle switch MS(1,2) belong to two different rows in diagram 100A of FIG. 1A, middle links ML(1,3) and ML(1,4) are cross middle links.

Each of the  $\frac{N}{d}$  middle switches MS(1,1) – MS(1,16) in the middle stage 130 are connected from exactly  $d$  input switches through two links each for a total of  $2 \times d$  links (for example the links ML(1,1) and ML(1,2) are connected to the middle switch MS(1,1) from input switch IS1, and the links ML(1,7) and ML(1,8) are connected to the middle switch MS(1,1) from input switch IS2) and also are connected to exactly  $d$  switches in middle stage 140 through two links each for a total of  $2 \times d$  links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1), and the links ML(2,3) and ML(2,4) are connected from middle switch MS(1,1) to middle switch MS(2,3)).

Each of the  $\frac{N}{d}$  middle switches MS(2,1) – MS(2,16) in the middle stage 140 are connected from exactly  $d$  input switches through two links each for a total of  $2 \times d$  links

(for example the links  $ML(2,1)$  and  $ML(2,2)$  are connected to the middle switch  $MS(2,1)$  from input switch  $MS(1,1)$ , and the links  $ML(1,11)$  and  $ML(1,12)$  are connected to the middle switch  $MS(2,1)$  from input switch  $MS(1,3)$ ) and also are connected to exactly  $d$  switches in middle stage 150 through two links each for a total of  $2 \times d$  links (for  
 5 example the links  $ML(3,1)$  and  $ML(3,2)$  are connected from middle switch  $MS(2,1)$  to middle switch  $MS(3,1)$ , and the links  $ML(3,3)$  and  $ML(3,4)$  are connected from middle switch  $MS(2,1)$  to middle switch  $MS(3,5)$ ).

Each of the  $\frac{N}{d}$  middle switches  $MS(3,1) - MS(3,16)$  in the middle stage 150 are connected from exactly  $d$  input switches through two links each for a total of  $2 \times d$  links  
 10 (for example the links  $ML(3,1)$  and  $ML(3,2)$  are connected to the middle switch  $MS(3,1)$  from input switch  $MS(2,1)$ , and the links  $ML(2,19)$  and  $ML(2,20)$  are connected to the middle switch  $MS(3,1)$  from input switch  $MS(2,5)$ ) and also are connected to exactly  $d$  switches in middle stage 160 through two links each for a total of  $2 \times d$  links (for example the links  $ML(4,1)$  and  $ML(4,2)$  are connected from middle switch  $MS(3,1)$  to  
 15 middle switch  $MS(4,1)$ , and the links  $ML(4,3)$  and  $ML(4,4)$  are connected from middle switch  $MS(3,1)$  to middle switch  $MS(4,9)$ ).

Each of the  $\frac{N}{d}$  middle switches  $MS(4,1) - MS(4,16)$  in the middle stage 160 are connected from exactly  $d$  input switches through two links each for a total of  $2 \times d$  links  
 (for example the links  $ML(4,1)$  and  $ML(4,2)$  are connected to the middle switch  $MS(4,1)$   
 20 from input switch  $MS(3,1)$ , and the links  $ML(4,35)$  and  $ML(4,36)$  are connected to the middle switch  $MS(4,1)$  from input switch  $MS(3,9)$ ) and also are connected to exactly  $d$  switches in middle stage 170 through two links each for a total of  $2 \times d$  links (for example the links  $ML(5,1)$  and  $ML(5,2)$  are connected from middle switch  $MS(4,1)$  to middle switch  $MS(5,1)$ , and the links  $ML(5,3)$  and  $ML(5,4)$  are connected from middle  
 25 switch  $MS(4,1)$  to middle switch  $MS(5,9)$ ).

Each of the  $\frac{N}{d}$  middle switches  $MS(5,1) - MS(5,16)$  in the middle stage 170 are connected from exactly  $d$  input switches through two links each for a total of  $2 \times d$  links



(for example the links  $ML(5,1)$  and  $ML(5,2)$  are connected to the middle switch  $MS(5,1)$  from input switch  $MS(4,1)$ , and the links  $ML(5,35)$  and  $ML(5,36)$  are connected to the middle switch  $MS(5,1)$  from input switch  $MS(4,9)$ ) and also are connected to exactly  $d$  switches in middle stage 180 through two links each for a total of  $2 \times d$  links (for  
 5 example the links  $ML(6,1)$  and  $ML(6,2)$  are connected from middle switch  $MS(5,1)$  to middle switch  $MS(6,1)$ , and the links  $ML(6,3)$  and  $ML(6,4)$  are connected from middle switch  $MS(5,1)$  to middle switch  $MS(6,5)$ ).

Each of the  $\frac{N}{d}$  middle switches  $MS(6,1) - MS(6,16)$  in the middle stage 180 are connected from exactly  $d$  input switches through two links each for a total of  $2 \times d$  links  
 10 (for example the links  $ML(6,1)$  and  $ML(6,2)$  are connected to the middle switch  $MS(6,1)$  from input switch  $MS(5,1)$ , and the links  $ML(6,19)$  and  $ML(6,20)$  are connected to the middle switch  $MS(6,1)$  from input switch  $MS(5,5)$ ) and also are connected to exactly  $d$  switches in middle stage 190 through two links each for a total of  $2 \times d$  links (for  
 15 example the links  $ML(7,1)$  and  $ML(7,2)$  are connected from middle switch  $MS(6,1)$  to middle switch  $MS(7,1)$ , and the links  $ML(7,3)$  and  $ML(7,4)$  are connected from middle switch  $MS(6,1)$  to middle switch  $MS(7,3)$ ).

Each of the  $\frac{N}{d}$  middle switches  $MS(7,1) - MS(7,16)$  in the middle stage 190 are connected from exactly  $d$  input switches through two links each for a total of  $2 \times d$  links  
 20 (for example the links  $ML(7,1)$  and  $ML(7,2)$  are connected to the middle switch  $MS(7,1)$  from input switch  $MS(6,1)$ , and the links  $ML(7,11)$  and  $ML(7,12)$  are connected to the middle switch  $MS(7,1)$  from input switch  $MS(6,3)$ ) and also are connected to exactly  $d$  switches in middle stage 120 through two links each for a total of  $2 \times d$  links (for  
 25 example the links  $ML(8,1)$  and  $ML(8,2)$  are connected from middle switch  $MS(7,1)$  to middle switch  $MS(8,1)$ , and the links  $ML(8,3)$  and  $ML(8,4)$  are connected from middle switch  $MS(7,1)$  to middle switch  $OS2$ ).

Each of the  $\frac{N}{d}$  middle switches  $OS1 - OS16$  in the middle stage 120 are connected from exactly  $d$  input switches through two links each for a total of  $2 \times d$  links

(for example the links ML(8,1) and ML(8,2) are connected to the output switch OS1 from input switch MS(7,1), and the links ML(8,7) and ML(7,8) are connected to the output switch OS1 from input switch MS(7,2)).

5 Finally the connection topology of the network 100A shown in FIG. 1A is known to be back to back inverse Benes connection topology.

Referring to diagram 100B in FIG. 1B, is a folded version of the multi-link multi-stage network 100A shown in FIG. 1A. The network 100B in FIG. 1B shows input stage 110 and output stage 120 are placed together. That is input switch IS1 and output switch OS1 are placed together, input switch IS2 and output switch OS2 are placed together, and similarly input switch IS16 and output switch OS16 are placed together. All the right going middle links (hereinafter “forward connecting links”) {i.e., inlet links IL1 – IL32 and middle links ML(1,1) - ML(1,64)} correspond to input switches IS1 - IS16, and all the left going middle links (hereinafter “backward connecting links”) {i.e., middle links ML(8,1) - ML(8,64) and outlet links OL1-OL32} correspond to output switches OS1 - OS16.

Middle stage 130 and middle stage 190 are placed together. That is middle switches MS(1,1) and MS(7,1) are placed together, middle switches MS(1,2) and MS(7,2) are placed together, and similarly middle switches MS(1,16) and MS(7,16) are placed together. All the right going middle links {i.e., middle links ML(1,1) - ML(1,64) and middle links ML(2,1) – ML(2,64)} correspond to middle switches MS(1,1) – MS(1,16), and all the left going middle links {i.e., middle links ML(7,1) - ML(7,64) and middle links ML(8,1) and ML(8,64)} correspond to middle switches MS(7,1) – MS(7,16).

Middle stage 140 and middle stage 180 are placed together. That is middle switches MS(2,1) and MS(6,1) are placed together, middle switches MS(2,2) and MS(6,2) are placed together, and similarly middle switches MS(2,16) and MS(6,16) are placed together. All the right going middle links {i.e., middle links ML(2,1) - ML(2,64) and middle links ML(3,1) – ML(3,64)} correspond to middle switches MS(2,1) – MS(2,16), and all the left going middle links {i.e., middle links ML(6,1) - ML(6,64) and

middle links  $ML(7,1)$  and  $ML(7,64)$  correspond to middle switches  $MS(6,1) - MS(6,16)$ .

Middle stage 150 and middle stage 170 are placed together. That is middle switches  $MS(3,1)$  and  $MS(5,1)$  are placed together, middle switches  $MS(3,2)$  and   
 5  $MS(5,2)$  are placed together, and similarly middle switches  $MS(3,16)$  and  $MS(5,16)$  are placed together. All the right going middle links {i.e., middle links  $ML(3,1) - ML(3,64)$  and middle links  $ML(4,1) - ML(4,64)$ } correspond to middle switches  $MS(3,1) - MS(3,16)$ , and all the left going middle links {i.e., middle links  $ML(5,1) - ML(5,64)$  and middle links  $ML(6,1)$  and  $ML(6,64)$ } correspond to middle switches  $MS(5,1) -$    
 10  $MS(5,16)$ .

Middle stage 160 is placed alone. All the right going middle links are the middle links  $ML(4,1) - ML(4,64)$  and all the left going middle links are middle links  $ML(5,1) - ML(5,64)$ .

In one embodiment, in the network 100B of FIG. 1B, the switches that are placed   
 15 together are implemented as separate switches then the network 100B is the generalized folded multi-link multi-stage network  $V_{fold-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$  with nine stages as disclosed in PCT Application Serial No. PCT/US08/64604 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a two by four switch and a four   
 20 by two switch. For example the switch input switch IS1 and output switch OS1 are placed together; so input switch IS1 is implemented as two by four switch with the inlet links IL1 and IL2 being the inputs of the input switch IS1 and middle links  $ML(1,1) - ML(1,4)$  being the outputs of the input switch IS1; and output switch OS1 is implemented as four by two switch with the middle links  $ML(8,1)$ ,  $ML(8,2)$ ,  $ML(8,7)$  and  $ML(8,8)$  being the   
 25 inputs of the output switch OS1 and outlet links OL1 – OL2 being the outputs of the output switch OS1. Similarly in this embodiment of network 100B all the switches that are placed together in each middle stage are implemented as separate switches.

### Hypercube Topology layout schemes:

Referring to layout 100C of FIG. 1C, in one embodiment, there are sixteen blocks namely Block 1\_2, Block 3\_4, Block 5\_6, Block 7\_8, Block 9\_10, Block 11\_12, Block 13\_14, Block 15\_16, Block 17\_18, Block 19\_20, Block 21\_22, Block 23\_24, Block 25\_26, Block 27\_28, Block 29\_30, and Block 31\_32. Each block implements all the switches in one row of the network 100B of FIG. 1B, one of the key aspects of the current invention. For example Block 1\_2 implements the input switch IS1, output Switch OS1, middle switch MS(1,1), middle switch MS(7,1), middle switch MS(2,1), middle switch MS(6,1), middle switch MS(3,1), middle switch MS(5,1), and middle switch MS(4,1).

For the simplification of illustration, Input switch IS1 and output switch OS1 together are denoted as switch 1; Middle switch MS(1,1) and middle switch MS(7,1) together are denoted by switch 2; Middle switch MS(2,1) and middle switch MS(6,1) together are denoted by switch 3; Middle switch MS(3,1) and middle switch MS(5,1) together are denoted by switch 4; Middle switch MS(4,1) is denoted by switch 5.

All the straight middle links are illustrated in layout 100C of FIG. 1C. For example in Block 1\_2, inlet links IL1 – IL2, outlet links OL1 – OL2, middle link ML(1,1), middle link ML(1,2), middle link ML(8,1), middle link ML(8,2), middle link ML(2,1), middle link ML(2,2), middle link ML(7,1), middle link ML(7,2), middle link ML(3,1), middle link ML(3,2), middle link ML(6,1), middle link ML(6,2), middle link ML(4,1), middle link ML(4,2), middle link ML(5,1) and middle link ML(5,2) are illustrated in layout 100C of FIG. 1C.

Even though it is not illustrated in layout 100C of FIG. 1C, in each block, in addition to the switches there may be Configurable Logic Blocks (CLB) or any arbitrary digital circuit (hereinafter “sub-integrated circuit block”) depending on the applications in different embodiments. There are four quadrants in the layout 100C of FIG. 1C namely top-left, bottom-left, top-right and bottom-right quadrants. Top-left quadrant implements Block 1\_2, Block 3\_4, Block 5\_6, and Block 7\_8. Bottom-left quadrant implements Block 9\_10, Block 11\_12, Block 13\_14, and Block 15\_16. Top-right quadrant implements Block 17\_18, Block 19\_20, Block 21\_22, and Block 23\_24. Bottom-right quadrant implements Block 25\_26, Block 27\_28, Block 29\_30, and Block 31\_32. There

are two halves in layout 100C of FIG. 1C namely left-half and right-half. Left-half consists of top-left and bottom-left quadrants. Right-half consists of top-right and bottom-right quadrants.

5 Recursively in each quadrant there are four sub-quadrants. For example in top-left quadrant there are four sub-quadrants namely top-left sub-quadrant, bottom-left sub-quadrant, top-right sub-quadrant and bottom-right sub-quadrant. Top-left sub-quadrant of top-left quadrant implements Block 1\_2. Bottom-left sub-quadrant of top-left quadrant implements Block 3\_4. Top-right sub-quadrant of top-left quadrant implements Block 5\_6. Finally bottom-right sub-quadrant of top-left quadrant implements Block 7\_8.

10 Similarly there are two sub-halves in each quadrant. For example in top-left quadrant there are two sub-halves namely left-sub-half and right-sub-half. Left-sub-half of top-left quadrant implements Block 1\_2 and Block 3\_4. Right-sub-half of top-left quadrant implements Block 5\_6 and Block 7\_8. Finally applicant notes that in each quadrant or half the blocks are arranged as a general binary hypercube. Recursively in larger multi-

15 stage network  $V_{fold-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 > 32$ , the layout in this embodiment in accordance with the current invention, will be such that the super-quadrants will also be arranged in d-ary hypercube manner. (In the embodiment of the layout 100C of FIG. 1C, it is binary hypercube manner since  $d = 2$ , in the network  $V_{fold-link}(N_1, N_2, d, s)$  100B of FIG. 1B).

20 Layout 100D of FIG. 1D illustrates the inter-block links between switches 1 and 2 of each block. For example middle links ML(1,3), ML(1,4), ML(8,7), and ML(8,8) are connected between switch 1 of Block 1\_2 and switch 2 of Block 3\_4. Similarly middle links ML(1,7), ML(1,8), ML(8,3), and ML(8,4) are connected between switch 2 of Block 1\_2 and switch 1 of Block 3\_4. Applicant notes that the inter-block links illustrated in

25 layout 100D of FIG. 1D can be implemented as vertical tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(1,4) and ML(8,8) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(1,4) and ML(8,8) are implemented as a time

30 division multiplexed single track).

Layout 100E of FIG. 1E illustrates the inter-block links between switches 2 and 3 of each block. For example middle links ML(2,3), ML(2,4), ML(7,11), and ML(7,12) are connected between switch 2 of Block 1\_2 and switch 3 of Block 3\_4. Similarly middle links ML(2,11), ML(2,12), ML(7,3), and ML(7,4) are connected between switch 3 of Block 1\_2 and switch 2 of Block 3\_4. Applicant notes that the inter-block links illustrated in layout 100E of FIG. 1E can be implemented as horizontal tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(2,12) and ML(7,4) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(2,12) and ML(7,4) are implemented as a time division multiplexed single track).

Layout 100F of FIG. 1F illustrates the inter-block links between switches 3 and 4 of each block. For example middle links ML(3,3), ML(3,4), ML(6,19), and ML(6,20) are connected between switch 3 of Block 1\_2 and switch 4 of Block 3\_4. Similarly middle links ML(3,19), ML(3,20), ML(6,3), and ML(6,4) are connected between switch 4 of Block 1\_2 and switch 3 of Block 3\_4. Applicant notes that the inter-block links illustrated in layout 100F of FIG. 1F can be implemented as vertical tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(3,4) and ML(6,20) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(3,4) and ML(6,20) are implemented as a time division multiplexed single track).

Layout 100G of FIG. 1G illustrates the inter-block links between switches 4 and 5 of each block. For example middle links ML(4,3), ML(4,4), ML(5,35), and ML(5,36) are connected between switch 4 of Block 1\_2 and switch 5 of Block 3\_4. Similarly middle links ML(4,35), ML(4,36), ML(5,3), and ML(5,4) are connected between switch 5 of Block 1\_2 and switch 4 of Block 3\_4. Applicant notes that the inter-block links illustrated in layout 100G of FIG. 1G can be implemented as horizontal tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(4,4) and ML(5,36) are implemented as two different tracks); or

in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(4,4) and ML(5,36) are implemented as a time division multiplexed single track).

The complete layout for the network 100B of FIG. 1B is given by combining the links in layout diagrams of 100C, 100D, 100E, 100F, and 100G. Applicant notes that in the layout 100C of FIG. 1C, the inter-block links between switch 1 and switch 2 of corresponding blocks are vertical tracks as shown in layout 100D of FIG. 1D; the inter-block links between switch 2 and switch 3 of corresponding blocks are horizontal tracks as shown in layout 100E of FIG. 1E; the inter-block links between switch 3 and switch 4 of corresponding blocks are vertical tracks as shown in layout 100F of FIG. 1F; and finally the inter-block links between switch 4 and switch 5 of corresponding blocks are horizontal tracks as shown in layout 100G of FIG. 1G. The pattern is alternate vertical tracks and horizontal tracks. It continues recursively for larger networks of  $N > 32$  as will be illustrated later.

Some of the key aspects of the current invention are discussed. 1) All the switches in one row of the multi-stage network 100B are implemented in a single block. 2) The blocks are placed in such a way that all the inter-block links are either horizontal tracks or vertical tracks; 3) Since all the inter-block links are either horizontal or vertical tracks, all the inter-block links can be mapped on to island-style architectures in current commercial FPGA's; 4) The length of the longest wire is about half of the width (or length) of the complete layout (For example middle link ML(4,4) is about half the width of the complete layout).

In accordance with the current invention, the layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized folded multi-link multi-stage network  $V_{fold-link}(N_1, N_2, d, s)$  the sub-quadrants, quadrants, and super-quadrants are arranged in d-ary hypercube manner and also the inter-blocks are accordingly connected in d-ary hypercube topology. Even though all the embodiments in the current invention are illustrated for  $N_1 = N_2$ , the embodiments can be extended for  $N_1 \neq N_2$ .

Referring to layout 100H of FIG. 1H, illustrates the extension of layout 100C for the network  $V_{fold-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 128$ ;  $d = 2$ ; and  $s = 2$ . There are four super-quadrants in layout 100H namely top-left super-quadrant, bottom-left super-quadrant, top-right super-quadrant, bottom-right super-quadrant. Total number of blocks in the layout 100H is sixty four. Top-left super-quadrant implements the blocks from block 1\_2 to block 31\_32. Each block in all the super-quadrants has two more switches namely switch 6 and switch 7 in addition to the switches [1-5] illustrated in layout 100C of FIG. 1C. The inter-block link connection topology is the exactly the same between the switches 1 and 2; switches 2 and 3; switches 3 and 4; switches 4 and 5 as it is shown in the layouts of FIG. 1D, FIG. 1E, FIG. 1F, and FIG. 1G respectively.

Bottom-left super-quadrant implements the blocks from block 33\_34 to block 63\_64. Top-right super-quadrant implements the blocks from block 65\_66 to block 95\_96. And bottom-right super-quadrant implements the blocks from block 97\_98 to block 127\_128. In all these three super-quadrants also, the inter-block link connection topology is the exactly the same between the switches 1 and 2; switches 2 and 3; switches 3 and 4; switches 4 and 5 as that of the top-left super-quadrant.

Recursively in accordance with the current invention, the inter-block links connecting the switch 5 and switch 6 will be vertical tracks between the corresponding switches of top-left super-quadrant and bottom-left super-quadrant. And similarly the inter-block links connecting the switch 5 and switch 6 will be vertical tracks between the corresponding switches of top-right super-quadrant and bottom-right super-quadrant. The inter-block links connecting the switch 6 and switch 7 will be horizontal tracks between the corresponding switches of top-left super-quadrant and top-right super-quadrant. And similarly the inter-block links connecting the switch 6 and switch 7 will be horizontal tracks between the corresponding switches of bottom-left super-quadrant and bottom-right super-quadrant.

Referring to diagram 100I of FIG. 1I illustrates a high-level implementation of Block 1\_2 (Each of the other blocks have similar implementation) of the layout 100C of FIG. 1C which represents a generalized folded multi-link multi-stage network



$V_{fold-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$ . Block 1\_2 in 100I illustrates both the intra-block and inter-block links connected to Block 1\_2. The layout diagram 100I corresponds to the embodiment where the switches that are placed together are implemented as separate switches in the network 100B of FIG. 1B. As noted before then  
 5 the network 100B is the generalized folded multi-link multi-stage network  
 $V_{fold-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$  with nine stages as disclosed in PCT Application Serial No. PCT/US08/64604 that is incorporated by reference above.

That is the switches that are placed together in Block 1\_2 as shown in FIG. 1I are  
 10 namely input switch IS1 and output switch OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the switches implemented are input switch IS1 and output switch OS1); middle switch MS(1,1) and middle switch MS(7,1) belonging to switch 2; middle switch MS(2,1) and middle switch MS(6,1) belonging to switch 3; middle switch MS(3,1) and middle switch  
 15 MS(5,1) belonging to switch 4; And middle switch MS(4,1) belonging to switch 5.

Input switch IS1 is implemented as two by four switch with the inlet links IL1 and IL2 being the inputs of the input switch IS1 and middle links ML(1,1) – ML(1,4) being the outputs of the input switch IS1; and output switch OS1 is implemented as four by two switch with the middle links ML(8,1) – ML(8,4) being the inputs of the output switch  
 20 OS1 and outlet links OL1 – OL2 being the outputs of the output switch OS1.

Middle switch MS(1,1) is implemented as four by four switch with the middle links ML(1,1), ML(1,2), ML(1,7) and ML(1,8) being the inputs and middle links ML(2,1) – ML(2,4) being the outputs; and middle switch MS(7,1) is implemented as four by four switch with the middle links ML(7,1), ML(7,2), ML(7,11) and ML(7,12) being the inputs  
 25 and middle links ML(8,1) – ML(8,4) being the outputs. Similarly all the other middle switches are also implemented as four by four switches as illustrated in 100I of FIG. 1I.

Now the VLSI layouts of generalized multi-link multi-stage network  
 $V_{mlink}(N_1, N_2, d, s)$  where  $N_1 = N_2 < 32$ ;  $d = 2$ ;  $s = 2$  and its corresponding version of

folded generalized multi-link multi-stage network  $V_{fold-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 < 32$ ;  $d = 2$ ;  $s = 2$  are discussed. Referring to diagram 200A1 of FIG. 2A1 is generalized multi-link multi-stage network  $V_{link}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 2$ ;  $d = 2$ . Diagram 200A2 of FIG. 2A2 illustrates the corresponding folded generalized multi-link multi-stage network  $V_{fold-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 2$ ;  $d = 2$ , version of the diagram 200A1 of FIG. 2A1. Layout 200A3 of FIG. 2A3 illustrates the VLSI layout of the network 200A2 of FIG. 2A2. There is only one block i.e., Block 1\_2 comprising switch 1. Just like in the layout 100C of FIG. 1C, switch 1 consists of input switch IS1 and output switch OS1.

10 Referring to diagram 200B1 of FIG. 2B1 is generalized multi-link multi-stage network  $V_{link}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 4$ ;  $d = 2$ ;  $s = 2$ . Diagram 200B2 of FIG. 2B2 illustrates the corresponding folded generalized multi-link multi-stage network  $V_{fold-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 4$ ;  $d = 2$ ;  $s = 2$ , version of the diagram 200B1 of FIG. 2B1. Layout 200B3 of FIG. 2B3 illustrates the VLSI layout of the network 200B2 of FIG. 2B2. There are two blocks i.e., Block 1\_2 and Block 3\_4 each comprising switch 1 and switch 2. Switch 1 in each block consists of the corresponding input switch and output switch. For example switch 1 in Block 1\_2 consists of input switch IS1 and output switch OS1. Similarly switch 2 in Block 1\_2 consists of middle switch (1,1). Layout 200B4 of FIG. 2B4 illustrates the inter-block links of the VLSI layout diagram 200B3 of FIG. 2B3. For example middle links ML(1,4) and ML(2,8). It must be noted that all the inter-block links are vertical tracks in this layout. (Alternatively all the inter-blocks can also be implemented as horizontal tracks).

25 Referring to diagram 200C11 of FIG. 2C11 is generalized multi-link multi-stage network  $V_{link}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 8$ ;  $d = 2$ ;  $s = 2$ . Diagram 200C12 of FIG. 2C12 illustrates the corresponding folded generalized multi-link multi-stage network  $V_{fold-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 8$ ;  $d = 2$ ;  $s = 2$ , version of the diagram 200C11 of FIG. 2C11. Layout 200C21 of FIG. 2C21 illustrates the VLSI layout of the network 200C12 of FIG. 2C12. There are four blocks i.e., Block 1\_2, Block 3\_4, Block 5\_6, and Block 7\_8 each comprising switch 1, switch 2 and switch 3. For example switch 1 in

Block 1\_2 consists of input switch IS1 and output switch OS1; Switch 2 in Block 1\_2 consists of MS(1,1) and MS(3,1). Switch 3 in Block 1\_2 consists of MS(2,1).

Layout 200C22 of FIG. 2C22 illustrates the inter-block links between the switch 1 and switch 2 of the VLSI layout diagram 200C21 of FIG. 2C21. For example middle links ML(1,4) and ML(4,8) are connected between Block 1\_2 and Block 3\_4. It must be noted that all the inter-block links between switch 1 and switch 2 of all blocks are vertical tracks in this layout. Layout 200C23 of FIG. 2C23 illustrates the inter-block links between the switch 2 and switch 3 of the VLSI layout diagram 200C21 of FIG. 2C21. For example middle links ML(2,12) and ML(3,4) are connected between Block 1\_2 and Block 5\_6. It must be noted that all the inter-block links between switch 2 and switch 3 of all blocks are horizontal tracks in this layout

Referring to diagram 200D1 of FIG. 2D1 is generalized multi-link multi-stage network  $V_{m-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 16$ ;  $d = 2$ ;  $s = 2$ . Diagram 200D2 of FIG. 2D2 illustrates the corresponding folded generalized multi-link multi-stage network  $V_{fold-m-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 16$ ;  $d = 2$ ;  $s = 2$ , version of the diagram 200D1 of FIG. 2D1. Layout 200D3 of FIG. 2D3 illustrates the VLSI layout of the network 200D2 of FIG. 2D2. There are eight blocks i.e., Block 1\_2, Block 3\_4, Block 5\_6, Block 7\_8, Block 9\_10, Block 11\_12, Block 13\_14 and Block 15\_16 each comprising switch 1, switch 2, switch 3 and switch 4. For example switch 1 in Block 1\_2 consists of input switch IS1 and output switch OS1; Switch 2 in Block 1\_2 consists of MS(1,1) and MS(5,1). Switch 3 in Block 1\_2 consists of MS(2,1) and MS(4,1), and switch 4 in Block 1\_2 consists of MS(3,1).

Layout 200D4 of FIG. 2D4 illustrates the inter-block links between the switch 1 and switch 2 of the VLSI layout diagram 200D3 of FIG. 2D3. For example middle links ML(1,4) and ML(6,8) are connected between Block 1\_2 and Block 3\_4. It must be noted that all the inter-block links between switch 1 and switch 2 of all blocks are vertical tracks in this layout. Layout 200D5 of FIG. 2D5 illustrates the inter-block links between the switch 2 and switch 3 of the VLSI layout diagram 200D3 of FIG. 2D3. For example middle links ML(2,12) and ML(5,4) are connected between Block 1\_2 and Block 5\_6. It

must be noted that all the inter-block links between switch 2 and switch 3 of all blocks are horizontal tracks in this layout. Layout 200D6 of FIG. 2D6 illustrates the inter-block links between the switch 3 and switch 4 of the VLSI layout diagram 200D3 of FIG. 2D3. For example middle links ML(3,4) and ML(4,20) are connected between Block 1\_2 and Block 9\_10. It must be noted that all the inter-block links between switch 3 and switch 4 of all blocks are vertical tracks in this layout.

### **Generalized Multi-link Butterfly Fat Tree Network Embodiment:**

In another embodiment in the network 100B of FIG. 1B, the switches that are placed together are implemented as combined switch then the network 100B is the generalized multi-link butterfly fat tree network  $V_{mlink-bft}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$  with five stages as disclosed in PCT Application Serial No. PCT/US08/64603 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a six by six switch. For example the input switch IS1 and output switch OS1 are placed together; so input switch IS1 and output OS1 are implemented as a six by six switch with the inlet links IL1, IL2, ML(8,1), ML(8,2), ML(8,7) and ML(8,8) being the inputs of the combined switch (denoted as IS1&OS1) and middle links ML(1,1), ML(1,2), ML(1,3), ML(1,4), OL1 and OL2 being the outputs of the combined switch IS1&OS1. Similarly in this embodiment of network 100B all the switches that are placed together are implemented as a combined switch.

Layout diagrams 100C in FIG. 1C, 100D in FIG. 1D, 100E in FIG. 1E, 100F in FIG. 1G are also applicable to generalized multi-link butterfly fat tree network  $V_{mlink-bft}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$  with five stages. The layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized multi-link butterfly fat tree network  $V_{mlink-bft}(N_1, N_2, d, s)$ . Accordingly layout 100H of FIG. 1H is also applicable to generalized multi-link butterfly fat tree network  $V_{mlink-bft}(N_1, N_2, d, s)$ .

Referring to diagram 100J of FIG. 1J illustrates a high-level implementation of Block 1\_2 (Each of the other blocks have similar implementation) of the layout 100C of FIG. 1C which represents a generalized multi-link butterfly fat tree network  $V_{mlink-bft}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$ . Block 1\_2 in 100J illustrates both the intra-block and inter-block links. The layout diagram 100J corresponds to the embodiment where the switches that are placed together are implemented as combined switch in the network 100B of FIG. 1B. As noted before then the network 100B is the generalized multi-link butterfly fat tree network  $V_{mlink-bft}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$  with five stages as disclosed in PCT Application Serial No. PCT/US08/64603 that is incorporated by reference above.

That is the switches that are placed together in Block 1\_2 as shown in FIG. 1J are namely the combined input and output switch IS1&OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the switch implemented is combined input and output switch IS1&OS1); middle switch MS(1,1) belonging to switch 2; middle switch MS(2,1) belonging to switch 3; middle switch MS(3,1) belonging to switch 4; And middle switch MS(4,1) belonging to switch 5.

Combined input and output switch IS1&OS1 is implemented as six by six switch with the inlet links IL1, IL2 and ML(8,1) – ML(8,4) being the inputs and middle links ML(1,1) – ML(1,4), and outlet links OL1 – OL2 being the outputs.

Middle switch MS(1,1) is implemented as eight by eight switch with the middle links ML(1,1), ML(1,2), ML(1,7), ML(1,8), ML(7,1), ML(7,2), ML(7,11) and ML(7,12) being the inputs and middle links ML(2,1) – ML(2,4) and middle links ML(8,1) – ML(8,4) being the outputs. Similarly all the other middle switches are also implemented as eight by eight switches as illustrated in 100J of FIG. 1J. Applicant observes that in middle switch MS(1,1) any one of the right going middle links can be switched to any one of the left going middle links and hereinafter middle switch MS(1,1) provides U-turn links. In general, in the network  $V_{mlink-bft}(N_1, N_2, d, s)$  each input switch, each output switch and each middle switch provides U-turn links.

In another embodiment, middle switch MS(1,1) (or the middle switches in any of the middle stage excepting the root middle stage) of Block 1\_2 of  $V_{\text{mlink-bjt}}(N_1, N_2, d, s)$  can be implemented as a four by eight switch and a four by four switch to save cross points. This is because the left going middle links of these middle switches are never setup to the right going middle links. For example, in middle switch MS(1,1) of Block 1\_2 as shown FIG. 1J, the left going middle links namely ML(7,1), ML(7,2), ML(7,11), and ML(7,12) are never switched to the right going middle links ML(2,1), ML(2,2), ML(2,3), and ML(2,4). And hence to implement MS(1,1) two switches namely: 1) a four by eight switch with the middle links ML(1,1), ML(1,2), ML(1,7), and ML(1,8) as inputs and the middle links ML(2,1), ML(2,2), ML(2,3), ML(2,4), ML(8,1), ML(8,2), ML(8,3), and ML(8,4) as outputs and 2) a four by four switch with the middle links ML(7,1), ML(7,2), ML(7,11), and ML(7,12) as inputs and the middle links ML(8,1), ML(8,2), ML(8,3), and ML(8,4) as outputs are sufficient without loosing any connectivity of the embodiment of MS(1,1) being implemented as an eight by eight switch as described before.)

#### **Generalized multi-stage network Embodiment:**

In one embodiment, in the network 100B of FIG. 1B, the switches that are placed together are implemented as two separate switches in input stage 110 and output stage 120; and as four separate switches in all the middle stages, then the network 100B is the generalized folded multi-stage network  $V_{\text{fold}}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$  with nine stages as disclosed in PCT Application Serial No. PCT/US08/64604 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a two by four switch and a four by two switch respectively. For example the switch input switch IS1 and output switch OS1 are placed together; so input switch IS1 is implemented as two by four switch with the inlet links IL1 and IL2 being the inputs and middle links ML(1,1) – ML(1,4) being the outputs; and output switch OS1 is implemented as four by two switch with the middle links ML(8,1), ML(8,4), ML(8,7) and ML(8,8) being the inputs and outlet links OL1 – OL2 being the outputs.

The switches, corresponding to the middle stages that are placed together are implemented as four two by two switches. For example middle switches MS(1,1), MS(1,17), MS(7,1), and MS(7,17) are placed together; so middle switch MS(1,1) is implemented as two by two switch with middle links ML(1,1) and ML(1,7) being the  
5 inputs and middle links ML(2,1) and ML(2,3) being the outputs; middle switch MS(1,17) is implemented as two by two switch with the middle links ML(1,2) and ML(1,8) being the inputs and middle links ML(2,2) and ML(2,4) being the outputs; middle switch MS(7,1) is implemented as two by two switch with middle links ML(7,1) and ML(7,11) being the inputs and middle links ML(8,1) and ML(8,3) being the outputs; And middle  
10 switch MS(7,17) is implemented as two by two switch with the middle links ML(7,2) and ML(7,12) being the inputs and middle links ML(8,2) and ML(8,4) being the outputs; Similarly in this embodiment of network 100B all the switches that are placed together are implemented as separate switches.

Layout diagrams 100C in FIG. 1C, 100D in FIG. 1D, 100E in FIG. 1E, 100F in  
15 FIG. 1G are also applicable to generalized folded multi-stage network  $V_{fold}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$  with nine stages. The layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized folded multi-stage network  $V_{fold}(N_1, N_2, d, s)$ . Accordingly layout 100H of FIG. 1H is also applicable to generalized folded multi-stage network  $V_{fold}(N_1, N_2, d, s)$ .

20 Referring to diagram 100K of FIG. 1K illustrates a high-level implementation of Block 1\_2 (Each of the other blocks have similar implementation) of the layout 100C of FIG. 1C which represents a generalized folded multi-stage network  $V_{fold}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$ . Block 1\_2 in 100K illustrates both the intra-block and inter-block links. The layout diagram 100K corresponds to the  
25 embodiment where the switches that are placed together are implemented as separate switches in the network 100B of FIG. 1B. As noted before then the network 100B is the generalized folded multi-stage network  $V_{fold}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$  with nine stages as disclosed in PCT Application Serial No. PCT/US08/64604 that is incorporated by reference above.

That is the switches that are placed together in Block 1\_2 as shown in FIG. 1K are namely the input switch IS1 and output switch OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the switches implemented are input switch IS1 and output switch OS1); middle switches  
 5 MS(1,1), MS(1,17), MS(7,1) and MS(7,17) belonging to switch 2; middle switches MS(2,1), MS(2,17), MS(6,1) and MS(6,17) belonging to switch 3; middle switches MS(3,1), MS(3,17), MS(5,1) and MS(5,17) belonging to switch 4; And middle switches MS(4,1), and MS(4,17) belonging to switch 5.

Input switch IS1 and output switch OS1 are placed together; so input switch IS1 is  
 10 implemented as two by four switch with the inlet links IL1 and IL2 being the inputs and middle links ML(1,1) – ML(1,4) being the outputs; and output switch OS1 is implemented as four by two switch with the middle links ML(8,1), ML(8,4), ML(8,7) and ML(8,8) being the inputs and outlet links OL1 – OL2 being the outputs.

Middle switches MS(1,1), MS(1,17), MS(7,1), and MS(7,17) are placed together;  
 15 so middle switch MS(1,1) is implemented as two by two switch with middle links ML(1,1) and ML(1,7) being the inputs and middle links ML(2,1) and ML(2,3) being the outputs; middle switch MS(1,17) is implemented as two by two switch with the middle links ML(1,2) and ML(1,8) being the inputs and middle links ML(2,2) and ML(2,4) being the outputs; middle switch MS(7,1) is implemented as two by two switch with middle  
 20 links ML(7,1) and ML(7,11) being the inputs and middle links ML(8,1) and ML(8,3) being the outputs; And middle switch MS(7,17) is implemented as two by two switch with the middle links ML(7,2) and ML(7,12) being the inputs and middle links ML(8,2) and ML(8,4) being the outputs. Similarly all the other middle switches are also implemented as two by two switches as illustrated in 100K of FIG. 1K.

## 25 **Generalized multi-stage network Embodiment with S = 1:**

In one embodiment, in the network 100B of FIG. 1B (where it is implemented with  $s = 1$ ), the switches that are placed together are implemented as two separate switches in input stage 110 and output stage 120; and as two separate switches in all the middle stages, then the network 100B is the generalized folded multi-stage network



$V_{fold}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 1$  with nine stages as disclosed in PCT Application Serial No. PCT/US08/64604 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a two by two switch and a two by two switch. For example the switch  
 5 input switch IS1 and output switch OS1 are placed together; so input switch IS1 is implemented as two by two switch with the inlet links IL1 and IL2 being the inputs and middle links ML(1,1) – ML(1,2) being the outputs; and output switch OS1 is implemented as two by two switch with the middle links ML(8,1) and ML(8,3) being the inputs and outlet links OL1 – OL2 being the outputs.

10 The switches, corresponding to the middle stages that are placed together are implemented as two, two by two switches. For example middle switches MS(1,1) and MS(7,1) are placed together; so middle switch MS(1,1) is implemented as two by two switch with middle links ML(1,1) and ML(1,3) being the inputs and middle links ML(2,1) and ML(2,2) being the outputs; middle switch MS(7,1) is implemented as two  
 15 by two switch with middle links ML(7,1) and ML(7,5) being the inputs and middle links ML(8,1) and ML(8,2) being the outputs; Similarly in this embodiment of network 100B all the switches that are placed together are implemented as two separate switches.

Layout diagrams 100C in FIG. 1C, 100D in FIG. 1D, 100E in FIG. 1E, 100F in FIG. 1G are also applicable to generalized folded multi-stage network  
 20  $V_{fold}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 1$  with nine stages. The layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized folded multi-stage network  $V_{fold}(N_1, N_2, d, s)$ . Accordingly layout 100H of FIG. 1H is also applicable to generalized folded multi-stage network  $V_{fold}(N_1, N_2, d, s)$ .

Referring to diagram 100K1 of FIG. 1K1 illustrates a high-level implementation  
 25 of Block 1\_2 (Each of the other blocks have similar implementation) for the layout 100C of FIG. 1C when  $s = 1$  which represents a generalized folded multi-stage network  $V_{fold}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 1$  (All the double links are replaced by single links when  $s = 1$ ). Block 1\_2 in 100K1 illustrates both the intra-block and inter-

block links. The layout diagram 100K1 corresponds to the embodiment where the switches that are placed together are implemented as separate switches in the network 100B of FIG. 1B when  $s = 1$ . As noted before then the network 100B is the generalized folded multi-stage network  $V_{fold}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 1$  with  
 5 nine stages as disclosed in PCT Application Serial No. PCT/US08/64604 that is incorporated by reference above.

That is the switches that are placed together in Block 1\_2 as shown in FIG. 1K1 are namely the input switch IS1 and output switch OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the  
 10 switches implemented are input switch IS1 and output switch OS1); middle switches MS(1,1) and MS(7,1) belonging to switch 2; middle switches MS(2,1) and MS(6,1) belonging to switch 3; middle switches MS(3,1) and MS(5,1) belonging to switch 4; And middle switch MS(4,1) belonging to switch 5.

Input switch IS1 and output switch OS1 are placed together; so input switch IS1 is  
 15 implemented as two by two switch with the inlet links IL1 and IL2 being the inputs and middle links ML(1,1) – ML(1,2) being the outputs; and output switch OS1 is implemented as two by two switch with the middle links ML(8,1) and ML(8,3) being the inputs and outlet links OL1 – OL2 being the outputs.

Middle switches MS(1,1) and MS(7,1) are placed together; so middle switch  
 20 MS(1,1) is implemented as two by two switch with middle links ML(1,1) and ML(1,3) being the inputs and middle links ML(2,1) and ML(2,2) being the outputs; And middle switch MS(7,1) is implemented as two by two switch with middle links ML(7,1) and ML(7,5) being the inputs and middle links ML(8,1) and ML(8,2) being the outputs. Similarly all the other middle switches are also implemented as two by two switches as  
 25 illustrated in 100K1 of FIG. 1K1.

### **Generalized Butterfly Fat Tree Network Embodiment:**

In another embodiment in the network 100B of FIG. 1B, the switches that are placed together are implemented as two combined switches then the network 100B is the

generalized butterfly fat tree network  $V_{bft}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$  with five stages as disclosed in PCT Application Serial No. PCT/US08/64603 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a six by six switch. For example the  
 5 input switch IS1 and output switch OS1 are placed together; so input output switch IS1&OS1 are implemented as a six by six switch with the inlet links IL1, IL2, ML(8,1), ML(8,2), ML(8,7) and ML(8,8) being the inputs of the combined switch (denoted as IS1&OS1) and middle links ML(1,1), ML(1,2), ML(1,3), ML(1,4), OL1 and OL2 being the outputs of the combined switch IS1&OS1.

10 The switches, corresponding to the middle stages that are placed together are implemented as two four by four switches. For example middle switches MS(1,1) and MS(1,17) are placed together; so middle switch MS(1,1) is implemented as four by four switch with middle links ML(1,1), ML(1,7), ML(7,1) and ML(7,11) being the inputs and middle links ML(2,1), ML(2,3), ML(8,1) and ML(8,3) being the outputs; middle switch  
 15 MS(1,17) is implemented as four by four switch with the middle links ML(1,2), ML(1,8), ML(7,2) and ML(7,12) being the inputs and middle links ML(2,2), ML(2,4), ML(8,2) and ML(8,4) being the outputs. Similarly in this embodiment of network 100B all the switches that are placed together are implemented as a two combined switches.

Layout diagrams 100C in FIG. 1C, 100D in FIG. 1D, 100E in FIG. 1E, 100F in  
 20 FIG. 1G are also applicable to generalized butterfly fat tree network  $V_{bft}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$  with five stages. The layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized butterfly fat tree network  $V_{bft}(N_1, N_2, d, s)$ . Accordingly layout 100H of FIG. 1H is also applicable to generalized butterfly fat tree network  $V_{bft}(N_1, N_2, d, s)$ .

25 Referring to diagram 100L of FIG. 1L illustrates a high-level implementation of Block 1\_2 (Each of the other blocks have similar implementation) of the layout 100C of FIG. 1C which represents a generalized butterfly fat tree network  $V_{bft}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$ . Block 1\_2 in 100L illustrates both the intra-block and

inter-block links. The layout diagram 100L corresponds to the embodiment where the switches that are placed together are implemented as two combined switches in the network 100B of FIG. 1B. As noted before then the network 100B is the generalized butterfly fat tree network  $V_{bft}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$  with  
 5 five stages as disclosed in PCT Application Serial No. PCT/US08/64603 that is incorporated by reference above.

That is the switches that are placed together in Block 1\_2 as shown in FIG. 1L are namely the combined input and output switch IS1&OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the  
 10 switch implemented is combined input and output switch IS1&OS1); middle switch MS(1,1) and MS(1,17) belonging to switch 2; middle switch MS(2,1) and MS(2,17) belonging to switch 3; middle switch MS(3,1) and MS(3,17) belonging to switch 4; And middle switch MS(4,1) belonging to switch 5.

Combined input and output switch IS1&OS1 is implemented as six by six switch  
 15 with the inlet links IL1, IL2, ML(8,1), ML(8,2), ML(8,7) and ML(8,8) being the inputs and middle links ML(1,1) – ML(1,4) and outlet links OL1 – OL2 being the outputs.

Middle switch MS(1,1) is implemented as four by four switch with middle links ML(1,1), ML(1,7), ML(7,1) and ML(7,11) being the inputs and middle links ML(2,1), ML(2,3), ML(8,1) and ML(8,3) being the outputs; And middle switch MS(1,17) is  
 20 implemented as four by four switch with the middle links ML(1,2), ML(1,8), ML(7,2) and ML(7,12) being the inputs and middle links ML(2,2), ML(2,4), ML(8,2) and ML(8,4) being the outputs. Similarly all the other middle switches are also implemented as two four by four switches as illustrated in 100L of FIG. 1L. Applicant observes that in middle switch MS(1,1) any one of the right going middle links can be switched to any one of the  
 25 left going middle links and hereinafter middle switch MS(1,1) provides U-turn links. In general, in the network  $V_{bft}(N_1, N_2, d, s)$  each input switch, each output switch and each middle switch provides U-turn links.

In another embodiment, middle switch MS(1,1) (or the middle switches in any of the middle stage excepting the root middle stage) of Block 1\_2 of  $V_{bf}(N_1, N_2, d, s)$  can be implemented as a two by four switch and a two by two switch to save cross points. This is because the left going middle links of these middle switches are never setup to the right going middle links. For example, in middle switch MS(1,1) of Block 1\_2 as shown FIG. 1L, the left going middle links namely ML(7,1) and ML(7,11) are never switched to the right going middle links ML(2,1) and ML(2,3). And hence to implement MS(1,1) two switches namely: 1) a two by four switch with the middle links ML(1,1) and ML(1,7) as inputs and the middle links ML(2,1), ML(2,3), ML(8,1), and ML(8,3) as outputs and 2) a two by two switch with the middle links ML(7,1) and ML(7,11) as inputs and the middle links ML(8,1) and ML(8,3) as outputs are sufficient without losing any connectivity of the embodiment of MS(1,1) being implemented as an eight by eight switch as described before.)

#### 15 **Generalized Butterfly Fat Tree Network Embodiment with S = 1:**

In one embodiment, in the network 100B of FIG. 1B (where it is implemented with  $s = 1$ ), the switches that are placed together are implemented as a combined switch in input stage 110 and output stage 120; and as a combined switch in all the middle stages, then the network 100B is the generalized butterfly fat tree network  $V_{bf}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 1$  with five stages as disclosed in PCT Application Serial No. PCT/US08/64603 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a four by four switch. For example the switch input switch IS1 and output switch OS1 are placed together; so input and output switch IS1&OS1 is implemented as four by four switch with the inlet links IL1, IL2, ML(8,1) and ML(8,3) being the inputs and middle links ML(1,1) – ML(1,2) and outlet links OL1 – OL2 being the outputs

The switches, corresponding to the middle stages that are placed together are implemented as a four by four switch. For example middle switches MS(1,1) is

implemented as four by four switch with middle links ML(1,1), ML(1,3), ML(7,1) and ML(7,5) being the inputs and middle links ML(2,1), ML(2,2), ML(8,1) and ML(8,2) being the outputs..

Layout diagrams 100C in FIG. 1C, 100D in FIG. 1D, 100E in FIG. 1E, 100F in  
 5 FIG. 1G are also applicable to generalized butterfly fat tree network  
 $V_{bft}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 1$  with five stages. The layout 100C  
 in FIG. 1C can be recursively extended for any arbitrarily large generalized butterfly fat  
 tree network  $V_{bft}(N_1, N_2, d, s)$ . Accordingly layout 100H of FIG. 1H is also applicable to  
 generalized butterfly fat tree network  $V_{bft}(N_1, N_2, d, s)$ .

10 Referring to diagram 100L1 of FIG. 1L1 illustrates a high-level implementation of  
 Block 1\_2 (Each of the other blocks have similar implementation) for the layout 100C of  
 FIG. 1C when  $s = 1$  which represents a generalized butterfly fat tree network  
 $V_{bft}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 1$  (All the double links are replaced  
 by single links when  $s = 1$ ). Block 1\_2 in 100K1 illustrates both the intra-block and inter-  
 15 block links. The layout diagram 100L1 corresponds to the embodiment where the  
 switches that are placed together are implemented as a combined switch in the network  
 100B of FIG. 1B when  $s = 1$ . As noted before then the network 100B is the generalized  
 butterfly fat tree network  $V_{bft}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 1$  with  
 nine stages as disclosed in PCT Application Serial No. PCT/US08/64603 that is  
 20 incorporated by reference above.

That is the switches that are placed together in Block 1\_2 as shown in FIG. 1L1  
 are namely the input and output switch IS1&OS1 belonging to switch 1, illustrated by  
 dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the  
 switches implemented are input switch IS1 and output switch OS1); middle switch  
 25 MS(1,1) belonging to switch 2; middle switch MS(2,1) belonging to switch 3; middle  
 switch MS(3,1) belonging to switch 4; And middle switch MS(4,1) belonging to switch 5.

Input and output switch IS1&OS1 are placed together; so input and output switch  
 IS1&OS1 is implemented as four by four switch with the inlet links IL1, IL2, ML(8,1)

and ML(8,3) being the inputs and middle links ML(1,1) – ML(1,2) and outlet links OL1 – OL2 being the outputs.

Middle switch MS(1,1) is implemented as four by four switch with middle links ML(1,1), ML(1,3), ML(7,1) and ML(7,5) being the inputs and middle links ML(2,1), ML(2,2), ML(8,1) and ML(8,2) being the outputs. Similarly all the other middle switches are also implemented as four by four switches as illustrated in 100L1 of FIG. 1L1.

In another embodiment, middle switch MS(1,1) (or the middle switches in any of the middle stage excepting the root middle stage) of Block 1\_2 of  $V_{m\text{link-}bft}(N_1, N_2, d, s)$  can be implemented as a two by four switch and a two by two switch to save cross points. This is because the left going middle links of these middle switches are never setup to the right going middle links. For example, in middle switch MS(1,1) of Block 1\_2 as shown FIG. 1L1, the left going middle links namely ML(7,1) and ML(7,5) are never switched to the right going middle links ML(2,1) and ML(2,2). And hence to implement MS(1,1) two switches namely: 1) a two by four switch with the middle links ML(1,1) and ML(1,3) as inputs and the middle links ML(2,1), ML(2,2), ML(8,1), and ML(8,2) as outputs and 2) a two by two switch with the middle links ML(7,1) and ML(7,5) as inputs and the middle links ML(8,1) and ML(8,2) as outputs are sufficient without losing any connectivity of the embodiment of MS(1,1) being implemented as an eight by eight switch as described before.)

20

### **Hypercube-like Topology layout schemes:**

Referring to diagram 300A in FIG. 3A, in one embodiment, an exemplary generalized multi-link multi-stage network  $V_{m\text{link}}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$  with nine stages of one hundred and forty four switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, 150, 170, 170, 180 and 190 is shown where input stage 110

25

consists of sixteen, two by four switches IS1-IS16 and output stage 120 consists of sixteen, four by two switches OS1-OS16.

As disclosed in PCT Application Serial No. PCT/US08/64604 that is incorporated by reference above, such a network can be operated in rearrangeably non-blocking manner for arbitrary fan-out multicast connections and also can be operated in strictly non-blocking manner for unicast connections.

The diagram 300A in FIG. 3A is exactly the same as the diagram 100A in FIG. 1A excepting the connection links between middle stage 150 and middle stage 160 as well as between middle stage 160 and middle stage 170.

Each of the  $\frac{N}{d}$  middle switches are connected to exactly  $d$  switches in middle stage 160 through two links each for a total of  $2 \times d$  links (for example the links ML(4,1) and ML(4,2) are connected from middle switch MS(3,1) to middle switch MS(4,1), and the links ML(4,3) and ML(4,4) are connected from middle switch MS(3,1) to middle switch MS(4,15)).

Each of the  $\frac{N}{d}$  middle switches MS(4,1) – MS(4,16) in the middle stage 160 are connected from exactly  $d$  input switches through two links each for a total of  $2 \times d$  links (for example the links ML(4,1) and ML(4,2) are connected to the middle switch MS(4,1) from input switch MS(3,1), and the links ML(4,59) and ML(4,60) are connected to the middle switch MS(4,1) from input switch MS(3,15)) and also are connected to exactly  $d$  switches in middle stage 170 through two links each for a total of  $2 \times d$  links (for example the links ML(5,1) and ML(5,2) are connected from middle switch MS(4,1) to middle switch MS(5,1), and the links ML(5,3) and ML(5,4) are connected from middle switch MS(4,1) to middle switch MS(5,15)).

Each of the  $\frac{N}{d}$  middle switches MS(5,1) – MS(5,16) in the middle stage 170 are connected from exactly  $d$  input switches through two links each for a total of  $2 \times d$  links (for example the links ML(5,1) and ML(5,2) are connected to the middle switch MS(5,1)



from input switch MS(4,1), and the links ML(5,59) and ML(5,60) are connected to the middle switch MS(5,1) from input switch MS(4,15)).

Finally the connection topology of the network 100A shown in FIG. 1A is also basically back to back inverse Benes connection topology but with a slight variation. All the cross middle links from middle switches MS(3,1) - MS(3,8) connect to middle switches MS(4,9) - MS(4,16) and all the cross middle links from middle switches MS(3,9) - MS(3,16) connect to middle switches MS(4,1) - MS(4,8). Applicant makes a key observation that there are many combinations of connections possible using this property. The difference in the connection topology between diagram 100A of FIG. 1A and diagram 300A of FIG. 3A is that the connections formed by cross middle links between middle stage 150 and middle stage 160 are made of two different combinations otherwise both the diagrams 100A and 300A implement back to back inverse Benes connection topology. Since these networks implement back to back inverse Benes topologies since there is difference in the connections of cross middle links between middle stage 150 and middle stage 160, the same difference in the connections of cross middle links between 160 and middle stage 170 occurs.

Referring to diagram 300B in FIG. 3B, is a folded version of the multi-link multi-stage network 300A shown in FIG. 3A. The network 300B in FIG. 3B shows input stage 110 and output stage 120 are placed together. That is input switch IS1 and output switch OS1 are placed together, input switch IS2 and output switch OS2 are placed together, and similarly input switch IS16 and output switch OS16 are placed together. All the right going middle links {i.e., inlet links IL1 - IL32 and middle links ML(1,1) - ML(1,64)} correspond to input switches IS1 - IS16, and all the left going middle links {i.e., middle links ML(7,1) - ML(7,64) and outlet links OL1-OL32} correspond to output switches OS1 - OS16.

Just the same way there is difference in the connection topology between diagram 100A of FIG. 1A and diagram 300A of FIG. 3A in the way the connections are formed by cross middle links between middle stage 150 and middle stage 160 and also between middle stage 160 and middle stage 170, the exact similar difference is there between the diagram 100B of FIG. 1B and the diagram 300B of FIG. 3B, i.e., in the way the

connections are formed by cross middle links between middle stage 150 and middle stage 160 and also between middle stage 160 and middle stage 170.

In one embodiment, in the network 300B of FIG. 3B, the switches that are placed together are implemented as separate switches then the network 300B is the generalized  
 5 folded multi-link multi-stage network  $V_{fold-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$  with nine stages as disclosed in PCT Application Serial No. PCT/US08/64604 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a two by four switch and a four by two switch. For example the switch input switch IS1 and output switch OS1 are placed  
 10 together; so input switch IS1 is implemented as two by four switch with the inlet links IL1 and IL2 being the inputs of the input switch IS1 and middle links ML(1,1) – ML(1,4) being the outputs of the input switch IS1; and output switch OS1 is implemented as four by two switch with the middle links ML(8,1), ML(8,2), ML(8,7) and ML(8,8) being the inputs of the output switch OS1 and outlet links OL1 – OL2 being the outputs of the  
 15 output switch OS1. Similarly in this embodiment of network 300B all the switches that are placed together are implemented as separate switches.

Referring to layout 300C of FIG. 3C, in one embodiment, there are sixteen blocks namely Block 1\_2, Block 3\_4, Block 5\_6, Block 7\_8, Block 9\_10, Block 11\_12, Block 13\_14, Block 15\_16, Block 17\_18, Block 19\_20, Block 21\_22, Block 23\_24, Block  
 20 25\_26, Block 27\_28, Block 29\_30, and Block 31\_32. Each block implements all the switches in one row of the network 300B of FIG. 3B, one of the key aspects of the current invention. For example Block 1\_2 implements the input switch IS1, output Switch OS1, middle switch MS(1,1), middle switch MS(7,1), middle switch MS(2,1), middle switch MS(6,1), middle switch MS(3,1), middle switch MS(5,1), and middle switch MS(4,1).  
 25 For the simplification of illustration, Input switch IS1 and output switch OS1 together are denoted as switch 1; Middle switch MS(1,1) and middle switch MS(7,1) together are denoted by switch 2; Middle switch MS(2,1) and middle switch MS(6,1) together are denoted by switch 3; Middle switch MS(3,1) and middle switch MS(5,1) together are denoted by switch 4; And middle switch MS(4,1) is denoted by switch 5.

All the straight middle links are illustrated in layout 300C of FIG. 3C. For example in Block 1\_2, inlet links IL1 – IL2, outlet links OL1 – OL2, middle link ML(1,1), middle link ML(1,2), middle link ML(8,1), middle link ML(8,2), middle link ML(2,1), middle link ML(2,2), middle link ML(7,1), middle link ML(7,2), middle link  
 5 ML(3,1), middle link ML(3,2), middle link ML(6,1), middle link ML(6,2), middle link ML(4,1), middle link ML(4,2), middle link ML(5,1) and middle link ML(5,2) are illustrated in layout 300C of FIG. 3C.

Even though it is not illustrated in layout 300C of FIG. 3C, in each block, in addition to the switches there may be Configurable Logic Blocks (CLB) or any arbitrary  
 10 digital circuit or sub-integrated circuit block depending on the applications in different embodiments. There are four quadrants in the layout 300C of FIG. 3C namely top-left, bottom-left, top-right and bottom-right quadrants. Top-left quadrant implements Block 1\_2, Block 3\_4, Block 5\_6, and Block 7\_8. Bottom-left quadrant implements Block 9\_10, Block 11\_12, Block 13\_14, and Block 15\_16. Top-right quadrant implements  
 15 Block 25\_26, Block 27\_28, Block 29\_30, and Block 31\_32. Bottom-right quadrant implements Block 17\_18, Block 19\_20, Block 21\_22, and Block 23\_24. There are two halves in layout 300C of FIG. 3C namely left-half and right-half. Left-half consists of top-left and bottom-left quadrants. Right-half consists of top-right and bottom-right quadrants.

20 Recursively in each quadrant there are four sub-quadrants. For example in top-left quadrant there are four sub-quadrants namely top-left sub-quadrant, bottom-left sub-quadrant, top-right sub-quadrant and bottom-right sub-quadrant. Top-left sub-quadrant of top-left quadrant implements Block 1\_2. Bottom-left sub-quadrant of top-left quadrant implements Block 3\_4. Top-right sub-quadrant of top-left quadrant implements Block  
 25 7\_8. Finally bottom-right sub-quadrant of top-left quadrant implements Block 5\_6. Similarly there are two sub-halves in each quadrant. For example in top-left quadrant there are two sub-halves namely left-sub-half and right-sub-half. Left-sub-half of top-left quadrant implements Block 1\_2 and Block 3\_4. Right-sub-half of top-left quadrant implements Block 7\_8 and Block 5\_6. Recursively in larger multi-stage network  
 30  $V_{fold-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 > 32$ , the layout in this embodiment in accordance

with the current invention, will be such that the super-quadrants will also be arranged in a similar manner.

Layout 300D of FIG. 3D illustrates the inter-block links (in the layout 300C of FIG. 3C all the cross middle links are inter-block links) between switches 1 and 2 of each block. For example middle links ML(1,3), ML(1,4), ML(8,7), and ML(8,8) are connected between switch 1 of Block 1\_2 and switch 2 of Block 3\_4. Similarly middle links ML(1,7), ML(1,8), ML(8,3), and ML(8,4) are connected between switch 2 of Block 1\_2 and switch 1 of Block 3\_4. Applicant notes that the inter-block links illustrated in layout 100D of FIG. 1D can be implemented as vertical tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(1,4) and ML(8,8) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(1,4) and ML(8,8) are implemented as a time division multiplexed single track).

Layout 300E of FIG. 3E illustrates the inter-block links between switches 2 and 3 of each block. For example middle links ML(2,3), ML(2,4), ML(7,11), and ML(7,12) are connected between switch 2 of Block 1\_2 and switch 3 of Block 3\_4. Similarly middle links ML(2,11), ML(2,12), ML(7,3), and ML(7,4) are connected between switch 3 of Block 1\_2 and switch 2 of Block 3\_4. Applicant notes that the inter-block links illustrated in layout 300E of FIG. 3E can be implemented as diagonal tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(2,12) and ML(7,4) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(2,12) and ML(7,4) are implemented as a time division multiplexed single track).

Layout 300F of FIG. 3F illustrates the inter-block links between switches 3 and 4 of each block. For example middle links ML(3,3), ML(3,4), ML(6,19), and ML(6,20) are connected between switch 3 of Block 1\_2 and switch 4 of Block 3\_4. Similarly middle links ML(3,19), ML(3,20), ML(6,3), and ML(6,4) are connected between switch 4 of Block 1\_2 and switch 3 of Block 3\_4. Applicant notes that the inter-block links illustrated

in layout 300F of FIG. 3F can be implemented as vertical tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(3,4) and ML(6,20) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(3,4) and ML(6,20) are implemented as a time division multiplexed single track).

Layout 300G of FIG. 3G illustrates the inter-block links between switches 4 and 5 of each block. For example middle links ML(4,3), ML(4,4), ML(5,35), and ML(5,36) are connected between switch 4 of Block 1\_2 and switch 5 of Block 3\_4. Similarly middle links ML(4,35), ML(4,36), ML(5,3), and ML(5,4) are connected between switch 5 of Block 1\_2 and switch 4 of Block 3\_4. Applicant notes that the inter-block links illustrated in layout 300G of FIG. 3G can be implemented as horizontal tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(4,4) and ML(5,36) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(4,4) and ML(5,36) are implemented as a time division multiplexed single track).

The complete layout for the network 300B of FIG. 3B is given by combining the links in layout diagrams of 300C, 300D, 300E, 300F, and 300G. Applicant notes that in the layout 300C of FIG. 3C, the inter-block links between switch 1 and switch 2 are vertical tracks as shown in layout 300D of FIG. 3D; the inter-block links between switch 2 and switch 3 are horizontal tracks as shown in layout 300E of FIG. 3E; the inter-block links between switch 3 and switch 4 are vertical tracks as shown in layout 300F of FIG. 3F; and finally the inter-block links between switch 4 and switch 5 are horizontal tracks as shown in layout 300G of FIG. 3G. The pattern is either vertical tracks, horizontal tracks or diagonal tracks. It continues recursively for larger networks of  $N > 32$  as will be illustrated later.

Some of the key aspects of the current invention related to layout diagram 300C of IFG. 3C are noted. 1) All the switches in one row of the multi-stage network 300B are implemented in a single block. 2) The blocks are placed in such a way that all the inter-

block links are either horizontal tracks, vertical tracks or diagonal tracks; 3) The length of the longest wire is about half of the width (or length) of the complete layout (For example middle link ML(4,4) is about half the width of the complete layout.);

The layout 300C in FIG. 3C can be recursively extended for any arbitrarily large  
 5 generalized folded multi-link multi-stage network  $V_{fold-link}(N_1, N_2, d, s)$ . Referring to layout 300H of FIG. 3H, illustrates the extension of layout 300C for the network  $V_{fold-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 128$ ;  $d = 2$ ; and  $s = 2$ . There are four super-quadrants in layout 300H namely top-left super-quadrant, bottom-left super-quadrant, top-right super-quadrant, bottom-right super-quadrant. Total number of blocks in the  
 10 layout 300H is sixty four. Top-left super-quadrant implements the blocks from block 1\_2 to block 31\_32. Each block in all the super-quadrants has two more switches namely switch 6 and switch 7 in addition to the switches [1-5] illustrated in layout 300C of FIG. 3C. The inter-block link connection topology is the exactly the same between the switches 1 and 2; switches 2 and 3; switches 3 and 4; switches 4 and 5 as it is shown in  
 15 the layouts of FIG. 3D, FIG. 3E, FIG. 3F, and FIG. 3G respectively.

Bottom-left super-quadrant implements the blocks from block 33\_34 to block 63\_64. Top-right super-quadrant implements the blocks from block 65\_66 to block 95\_96. And bottom-right super-quadrant implements the blocks from block 97\_98 to block 127\_128. In all these three super-quadrants also, the inter-block link connection  
 20 topology is the exactly the same between the switches 1 and 2; switches 2 and 3; switches 3 and 4; switches 4 and 5 as that of the top-left super-quadrant.

Recursively in accordance with the current invention, the inter-block links connecting the switch 5 and switch 6 will be vertical tracks between the corresponding switches of top-left super-quadrant and bottom-left super-quadrant. And similarly the  
 25 inter-block links connecting the switch 5 and switch 6 will be vertical tracks between the corresponding switches of top-right super-quadrant and bottom-right super-quadrant. The inter-block links connecting the switch 6 and switch 7 will be horizontal tracks between the corresponding switches of top-left super-quadrant and top-right super-quadrant. And similarly the inter-block links connecting the switch 6 and switch 7 will be horizontal

tracks between the corresponding switches of bottom-left super-quadrant and bottom-right super-quadrant.

### Ring Topology layout schemes:

5           Layout diagram 400C of FIG. 4C is another embodiment for the generalized folded multi-link multi-stage network  $V_{fold-link}(N_1, N_2, d, s)$  diagram 100B in FIG. 1B.

Referring to layout 400C of FIG. 4C, there are sixteen blocks namely Block 1\_2, Block 3\_4, Block 5\_6, Block 7\_8, Block 9\_10, Block 11\_12, Block 13\_14, Block 15\_16, Block 17\_18, Block 19\_20, Block 21\_22, Block 23\_24, Block 25\_26, Block 27\_28,  
 10 Block 29\_30, and Block 31\_32. Each block implements all the switches in one row of the network 100B of FIG. 1B, one of the key aspects of the current invention. For example Block 1\_2 implements the input switch IS1, output Switch OS1, middle switch MS(1,1), middle switch MS(7,1), middle switch MS(2,1), middle switch MS(6,1), middle switch MS(3,1), middle switch MS(5,1), and middle switch MS(4,1). For the simplification of  
 15 illustration, Input switch IS1 and output switch OS1 together are denoted as switch 1; Middle switch MS(1,1) and middle switch MS(7,1) together are denoted by switch 2; Middle switch MS(2,1) and middle switch MS(6,1) together are denoted by switch 3; Middle switch MS(3,1) and middle switch MS(5,1) together are denoted by switch 4; And middle switch MS(4,1) is denoted by switch 5.

20           All the straight middle links are illustrated in layout 400C of FIG. 4C. For example in Block 1\_2, inlet links IL1 – IL2, outlet links OL1 – OL2, middle link ML(1,1), middle link ML(1,2), middle link ML(8,1), middle link ML(8,2), middle link ML(2,1), middle link ML(2,2), middle link ML(7,1), middle link ML(7,2), middle link ML(3,1), middle link ML(3,2), middle link ML(6,1), middle link ML(6,2), middle link  
 25 ML(4,1), middle link ML(4,2), middle link ML(5,1) and middle link ML(5,2) are illustrated in layout 400C of FIG. 4C.

Even though it is not illustrated in layout 400C of FIG. 4C, in each block, in addition to the switches there may be Configurable Logic Blocks (CLB) or any arbitrary

digital circuit or sub-integrated circuit block depending on the applications in different embodiments. The topology of the layout 400C in FIG. 4C is a ring. For each of the neighboring rows in diagram 100B of FIG. 1B the corresponding blocks are also physically neighbors in layout diagram 400C of FIG. 4C. In addition the topmost row is also logically considered as neighbor to the bottommost row. For example Block 1\_2 (implementing the switches belonging to a row in diagram 100B of FIG. 1B) has Block 3\_4 as neighbor since Block 3\_4 implements the switches in its neighboring row. Similarly Block 1\_2 also has Block 31\_32 as neighbor since Block 1\_2 implements topmost row of switches and Block 31\_32 implements bottommost row of switches in diagram 100B of FIG. 1B. The ring layout scheme illustrated in 400C of FIG. 4C can be generalized for a large multi-stage network  $V_{fold-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 > 32$ , in accordance with the current invention.

Layout 400B of FIG. 4B illustrates the inter-block links (in the layout 400A of FIG. 4A all the cross middle links are inter-block links) between switches 1 and 2 of each block. For example middle links ML(1,3), ML(1,4), ML(8,7), and ML(8,8) are connected between switch 1 of Block 1\_2 and switch 2 of Block 3\_4. Similarly middle links ML(1,7), ML(1,8), ML(8,3), and ML(8,4) are connected between switch 2 of Block 1\_2 and switch 1 of Block 3\_4. Applicant notes that the inter-block links illustrated in layout 400B of FIG. 4B are implemented as vertical tracks or horizontal tracks or diagonal tracks. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(1,4) and ML(8,8) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(1,4) and ML(8,8) are implemented as a time division multiplexed single track).

Layout 400C of FIG. 4C illustrates the inter-block links between switches 2 and 3 of each block. For example middle links ML(2,3), ML(2,4), ML(7,11), and ML(7,12) are connected between switch 2 of Block 1\_2 and switch 3 of Block 3\_4. Similarly middle links ML(2,11), ML(2,12), ML(7,3), and ML(7,4) are connected between switch 3 of Block 1\_2 and switch 2 of Block 3\_4. Applicant notes that the inter-block links illustrated in layout 400C of FIG. 4C are implemented as vertical tracks or horizontal tracks or



diagonal tracks. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(2,12) and ML(7,4) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(2,12) and ML(7,4) are implemented as a time division multiplexed single track).

Layout 400D of FIG. 4D illustrates the inter-block links between switches 3 and 4 of each block. For example middle links ML(3,3), ML(3,4), ML(6,19), and ML(6,20) are connected between switch 3 of Block 1\_2 and switch 4 of Block 3\_4. Similarly middle links ML(3,19), ML(3,20), ML(6,3), and ML(6,4) are connected between switch 4 of Block 1\_2 and switch 3 of Block 3\_4. Applicant notes that the inter-block links illustrated in layout 400D of FIG. 4D are implemented as vertical tracks or horizontal tracks or diagonal tracks. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(3,4) and ML(6,20) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(3,4) and ML(6,20) are implemented as a time division multiplexed single track).

Layout 400E of FIG. 4E illustrates the inter-block links between switches 4 and 5 of each block. For example middle links ML(4,3), ML(4,4), ML(5,35), and ML(5,36) are connected between switch 4 of Block 1\_2 and switch 5 of Block 3\_4. Similarly middle links ML(4,35), ML(4,36), ML(5,3), and ML(5,4) are connected between switch 5 of Block 1\_2 and switch 4 of Block 3\_4. Applicant notes that the inter-block links illustrated in layout 400E of FIG. 4E are implemented as vertical tracks or horizontal tracks or diagonal tracks. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(4,4) and ML(5,36) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(4,4) and ML(5,36) are implemented as a time division multiplexed single track).

The complete layout for the network 100B of FIG. 1B is given by combining the links in layout diagrams of 400A, 400B, 400C, 400D, and 400E.

Some of the key aspects of the current invention related to layout diagram 400A of FIG. 4A are noted. 1) All the switches in one row of the multi-stage network 100B are implemented in a single block. 2) The blocks are placed in such a way that all the inter-block links are either horizontal tracks, vertical tracks or diagonal tracks; 3) Length of the different wires between the same two middle stages is not the same. However it gives an opportunity to implement the most connected circuits to place and route through the blocks which have shorter wires.

Layout diagram 400C1 of FIG. 4C1 is another embodiment for the generalized folded multi-link multi-stage network  $V_{fold-link}(N_1, N_2, d, s)$  diagram 100B in FIG. 1B. Referring to layout 400C1 of FIG. 4C1, there are sixteen blocks namely Block 1\_2, Block 3\_4, Block 5\_6, Block 7\_8, Block 9\_10, Block 11\_12, Block 13\_14, Block 15\_16, Block 17\_18, Block 19\_20, Block 21\_22, Block 23\_24, Block 25\_26, Block 27\_28, Block 29\_30, and Block 31\_32. Each block implements all the switches in one row of the network 100B of FIG. 1B, one of the key aspects of the current invention. For example Block 1\_2 implements the input switch IS1, output Switch OS1, middle switch MS(1,1), middle switch MS(7,1), middle switch MS(2,1), middle switch MS(6,1), middle switch MS(3,1), middle switch MS(5,1), and middle switch MS(4,1). For the simplification of illustration, Input switch IS1 and output switch OS1 together are denoted as switch 1; Middle switch MS(1,1) and middle switch MS(7,1) together are denoted by switch 2; Middle switch MS(2,1) and middle switch MS(6,1) together are denoted by switch 3; Middle switch MS(3,1) and middle switch MS(5,1) together are denoted by switch 4; And middle switch MS(4,1) is denoted by switch 5.

All the straight middle links are illustrated in layout 400C1 of FIG. 4C1. For example in Block 1\_2, inlet links IL1 – IL2, outlet links OL1 – OL2, middle link ML(1,1), middle link ML(1,2), middle link ML(8,1), middle link ML(8,2), middle link ML(2,1), middle link ML(2,2), middle link ML(7,1), middle link ML(7,2), middle link ML(3,1), middle link ML(3,2), middle link ML(6,1), middle link ML(6,2), middle link ML(4,1), middle link ML(4,2), middle link ML(5,1) and middle link ML(5,2) are illustrated in layout 400C1 of FIG. 4C1.

Even though it is not illustrated in layout 400C1 of FIG. 4C1, in each block, in addition to the switches there may be Configurable Logic Blocks (CLB) or any arbitrary digital circuit or sub-integrated circuit block depending on the applications in different embodiments. The topology of the layout 400C1 in FIG. 4C1 is another embodiment of ring layout topology. For each of the neighboring rows in diagram 100B of FIG. 1B the corresponding blocks are also physically neighbors in layout diagram 400C of FIG. 4C. In addition the topmost row is also logically considered as neighbor to the bottommost row. For example Block 1\_2 (implementing the switches belonging to a row in diagram 100B of FIG. 1B) has Block 3\_4 as neighbor since Block 3\_4 implements the switches in its neighboring row. Similarly Block 1\_2 also has Block 31\_32 as neighbor since Block 1\_2 implements topmost row of switches and Block 31\_32 implements bottommost row of switches in diagram 100B of FIG. 1B. The ring layout scheme illustrated in 400C of FIG. 4C can be generalized for a large multi-stage network  $V_{fold-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 > 32$ , in accordance with the current invention.

All the layout embodiments disclosed in the current invention are applicable to generalized multi-stage networks  $V(N_1, N_2, d, s)$ , generalized folded multi-stage networks  $V_{fold}(N_1, N_2, d, s)$ , generalized butterfly fat tree networks  $V_{bft}(N_1, N_2, d, s)$ , generalized multi-link multi-stage networks  $V_{mlink}(N_1, N_2, d, s)$ , generalized folded multi-link multi-stage networks  $V_{fold-link}(N_1, N_2, d, s)$ , generalized multi-link butterfly fat tree networks  $V_{mlink-bft}(N_1, N_2, d, s)$ , and generalized hypercube networks  $V_{hcube}(N_1, N_2, d, s)$  for  $s = 1, 2, 3$  or any number in general, and for both  $N_1 = N_2 = N$  and  $N_1 \neq N_2$ , and  $d$  is any integer.

Conversely applicant makes another important observation that generalized hypercube networks  $V_{hcube}(N_1, N_2, d, s)$  are implemented with the layout topology being the hypercube topology shown in layout 100C of FIG. 1C with large scale cross point reduction as any one of the networks described in the current invention namely: generalized multi-stage networks  $V(N_1, N_2, d, s)$ , generalized folded multi-stage networks  $V_{fold}(N_1, N_2, d, s)$ , generalized butterfly fat tree networks  $V_{bft}(N_1, N_2, d, s)$ ,

generalized multi-link multi-stage networks  $V_{mlink}(N_1, N_2, d, s)$ , generalized folded multi-link multi-stage networks  $V_{fold-mlink}(N_1, N_2, d, s)$ , generalized multi-link butterfly fat tree networks  $V_{mlink-bft}(N_1, N_2, d, s)$  for  $s = 1, 2, 3$  or any number in general, and for both  $N_1 = N_2 = N$  and  $N_1 \neq N_2$ , and  $d$  is any integer.

5

### **Applications Embodiments:**

All the embodiments disclosed in the current invention are useful in many varieties of applications. FIG. 5A1 illustrates the diagram of 500A1 which is a typical two by two switch with two inlet links namely IL1 and IL2, and two outlet links namely OL1 and OL2. The two by two switch also implements four crosspoints namely CP(1,1), CP(1,2), CP(2,1) and CP(2,2) as illustrated in FIG. 5A1. For example the diagram of 500A1 may be the implementation of middle switch MS(1,1) of the diagram 100K of FIG. 1K where inlet link IL1 of diagram 500A1 corresponds to middle link ML(1,1) of diagram 100K, inlet link IL2 of diagram 500A1 corresponds to middle link ML(1,7) of diagram 100K, outlet link OL1 of diagram 500A1 corresponds to middle link ML(2,1) of diagram 100K, outlet link OL2 of diagram 500A1 corresponds to middle link ML(2,3) of diagram 100K.

### **1) Programmable Integrated Circuit Embodiments:**

All the embodiments disclosed in the current invention are useful in programmable integrated circuit applications. FIG. 5A2 illustrates the detailed diagram 500A2 for the implementation of the diagram 500A1 in programmable integrated circuit embodiments. Each crosspoint is implemented by a transistor coupled between the corresponding inlet link and outlet link, and a programmable cell in programmable integrated circuit embodiments. Specifically crosspoint CP(1,1) is implemented by transistor C(1,1) coupled between inlet link IL1 and outlet link OL1, and programmable cell P(1,1); crosspoint CP(1,2) is implemented by transistor C(1,2) coupled between inlet

link IL1 and outlet link OL2, and programmable cell P(1,2); crosspoint CP(2,1) is implemented by transistor C(2,1) coupled between inlet link IL2 and outlet link OL1, and programmable cell P(2,1); and crosspoint CP(2,2) is implemented by transistor C(2,2) coupled between inlet link IL2 and outlet link OL2, and programmable cell P(2,2).

5           If the programmable cell is programmed ON, the corresponding transistor couples the corresponding inlet link and outlet link. If the programmable cell is programmed OFF, the corresponding inlet link and outlet link are not connected. For example if the programmable cell P(1,1) is programmed ON, the corresponding transistor C(1,1) couples the corresponding inlet link IL1 and outlet link OL1. If the programmable cell P(1,1) is  
10 programmed OFF, the corresponding inlet link IL1 and outlet link OL1 are not connected. In volatile programmable integrated circuit embodiments the programmable cell may be an SRAM (Static Random Address Memory) cell. In non-volatile programmable integrated circuit embodiments the programmable cell may be a Flash memory cell. Also the programmable integrated circuit embodiments may implement  
15 field programmable logic arrays (FPGA) devices, or programmable Logic devices (PLD), or Application Specific Integrated Circuits (ASIC) embedded with programmable logic circuits or 3D-FPGAs.

FIG. 5A2 also illustrates a buffer B1 on inlet link IL2. The signals driven along inlet link IL2 are amplified by buffer B1. Buffer B1 can be inverting or non-inverting  
20 buffer. Buffers such as B1 are used to amplify the signal in links which are usually long.

## 2) One-time Programmable Integrated Circuit Embodiments:

All the embodiments disclosed in the current invention are useful in one-time programmable integrated circuit applications. FIG. 5A3 illustrates the detailed diagram 500A3 for the implementation of the diagram 500A1 in one-time programmable  
25 integrated circuit embodiments. Each crosspoint is implemented by a via coupled between the corresponding inlet link and outlet link in one-time programmable integrated circuit embodiments. Specifically crosspoint CP(1,1) is implemented by via V(1,1) coupled between inlet link IL1 and outlet link OL1; crosspoint CP(1,2) is implemented by via V(1,2) coupled between inlet link IL1 and outlet link OL2; crosspoint CP(2,1) is

implemented by via V(2,1) coupled between inlet link IL2 and outlet link OL1; and crosspoint CP(2,2) is implemented by via V(2,2) coupled between inlet link IL2 and outlet link OL2.

If the via is programmed ON, the corresponding inlet link and outlet link are permanently connected which is denoted by thick circle at the intersection of inlet link and outlet link. If the via is programmed OFF, the corresponding inlet link and outlet link are not connected which is denoted by the absence of thick circle at the intersection of inlet link and outlet link. For example in the diagram 500A3 the via V(1,1) is programmed ON, and the corresponding inlet link IL1 and outlet link OL1 are connected as denoted by thick circle at the intersection of inlet link IL1 and outlet link OL1; the via V(2,2) is programmed ON, and the corresponding inlet link IL2 and outlet link OL2 are connected as denoted by thick circle at the intersection of inlet link IL2 and outlet link OL2; the via V(1,2) is programmed OFF, and the corresponding inlet link IL1 and outlet link OL2 are not connected as denoted by the absence of thick circle at the intersection of inlet link IL1 and outlet link OL2; the via V(2,1) is programmed OFF, and the corresponding inlet link IL2 and outlet link OL1 are not connected as denoted by the absence of thick circle at the intersection of inlet link IL2 and outlet link OL1. One-time programmable integrated circuit embodiments may be anti-fuse based programmable integrated circuit devices or mask programmable structured ASIC devices.

### 3) Integrated Circuit Placement and Route Embodiments:

All the embodiments disclosed in the current invention are useful in Integrated Circuit Placement and Route applications, for example in ASIC backend Placement and Route tools. FIG. 5A4 illustrates the detailed diagram 500A4 for the implementation of the diagram 500A1 in Integrated Circuit Placement and Route embodiments. In an integrated circuit since the connections are known a-priori, the switch and crosspoints are actually virtual. However the concept of virtual switch and virtual crosspoint using the embodiments disclosed in the current invention reduces the number of required wires, wire length needed to connect the inputs and outputs of different netlists and the time required by the tool for placement and route of netlists in the integrated circuit.

Each virtual crosspoint is used to either to hardwire or provide no connectivity between the corresponding inlet link and outlet link. Specifically crosspoint CP(1,1) is implemented by direct connect point DCP(1,1) to hardwire (i.e., to permanently connect) inlet link IL1 and outlet link OL1 which is denoted by the thick circle at the intersection of inlet link IL1 and outlet link OL1; crosspoint CP(2,2) is implemented by direct connect point DCP(2,2) to hardwire inlet link IL2 and outlet link OL2 which is denoted by the thick circle at the intersection of inlet link IL2 and outlet link OL2. The diagram 500A4 does not show direct connect point DCP(1,2) and direct connect point DCP(1,3) since they are not needed and in the hardware implementation they are eliminated.

Alternatively inlet link IL1 needs to be connected to outlet link OL1 and inlet link IL1 does not need to be connected to outlet link OL2. Also inlet link IL2 needs to be connected to outlet link OL2 and inlet link IL2 does not need to be connected to outlet link OL1. Furthermore in the example of the diagram 500A4, there is no need to drive the signal of inlet link IL1 horizontally beyond outlet link OL1 and hence the inlet link IL1 is not even extended horizontally until the outlet link OL2. Also the absence of direct connect point DCP(2,1) illustrates there is no need to connect inlet link IL2 and outlet link OL1.

In summary in integrated circuit placement and route tools, the concept of virtual switches and virtual cross points is used during the implementation of the placement & routing algorithmically in software, however during the hardware implementation cross points in the cross state are implemented as hardwired connections between the corresponding inlet link and outlet link, and in the bar state are implemented as no connection between inlet link and outlet link.

### 3) More Application Embodiments:

All the embodiments disclosed in the current invention are also useful in the design of SoC interconnects, Field programmable interconnect chips, parallel computer systems and in time-space-time switches.

Numerous modifications and adaptations of the embodiments, implementations, and examples described herein will be apparent to the skilled artisan in view of the disclosure.



CLAIMS

What is claimed is:

1. An integrated circuit device comprising a plurality of sub-integrated circuit blocks and a routing network, and
- 5 Said each plurality of sub-integrated circuit blocks comprising a plurality of inlet links and a plurality of outlet links; and  
Said routing network interconnects any one of said outlet link of one of said sub-integrated circuit block to one or more said inlet links of one or more of said sub-integrated circuit blocks; and
- 10 Said routing network comprising of a plurality of stages  $y$ , starting from the lowest stage to the highest stage; and  
Said routing network comprising a plurality of switches of size  $d \times d$ , where  $d \geq 2$ , in each said stage and each said switch of size  $d \times d$  having  $d$  inlet links and  $d$  outlet links; and
- 15 Said each sub-integrated circuit block comprising a plurality of said switches corresponding to each said stage; and  
Said each sub-integrated circuit block comprising a plurality of forward connecting links connecting from switches in lower stage to switches in the immediate succeeding higher stage, and also comprising a plurality of backward connecting links
- 20 connecting from switches in higher stage to switches in the immediate preceding lower stage; and  
Said each sub-integrated circuit block comprising a plurality straight links in said forward connecting links from switches in lower stage to switches in the immediate succeeding higher stage and a plurality cross links in said forward connecting links from
- 25 switches in lower stage to switches in the immediate succeeding higher stage, and further comprising a plurality of straight links in said backward connecting links from switches

in higher stage to switches in the immediate preceding lower stage and a plurality of cross links in said backward connecting links from switches in higher stage to switches in the immediate preceding lower stage.

2. The integrated circuit device of claim 1, wherein said all straight links are  
5 connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and

said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks.

3. The integrated circuit device of claim 2, wherein said plurality of sub-  
10 integrated circuit blocks arranged in a two-dimensional grid.

4. The integrated circuit device of claim 3, wherein said cross links in succeeding stages are connecting as alternative vertical and horizontal links between switches in said sub-integrated circuit blocks.

5. The integrated circuit device of claim 4, wherein said cross links from  
15 switches in a stage in one of said sub-integrated circuit blocks are connecting to switches in the succeeding stage in another of said sub-integrated circuit blocks so that said cross links are either vertical links or horizontal and vice versa, and hereinafter such cross links are “shuffle exchange links”).

6. The integrated circuit device of claim 5, wherein said all horizontal shuffle  
20 exchange links between switches in any two corresponding said succeeding stages are substantially of equal length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are substantially of equal length in the entire said integrated circuit device.

7. The integrated circuit device of claim 6, wherein the shortest horizontal  
25 shuffle exchange links are connecting at the lowest stage and between switches in two

nearest neighboring said sub-integrated circuit blocks, and length of the horizontal shuffle exchange links is doubled in each succeeding stage; and the shortest vertical shuffle exchange links are connecting at the lowest stage and between switches in two nearest neighboring said sub-integrated circuit blocks, and length of the vertical shuffle exchange  
5 links is doubled in each succeeding stage.

8. The integrated circuit device of claim 7, wherein  $y \geq (\log_2 N)$  so that the length of the horizontal shuffle exchange links in the highest stage is equal to half the size of the horizontal size of said two dimensional grid of sub-integrated circuit blocks and the length of the vertical shuffle exchange links in the highest stage is equal to half the size of  
10 the vertical size of said two dimensional grid of sub-integrated circuit blocks.

9. The integrated circuit device of claim 8, wherein  $d = 2$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing  
15 network is rearrangeably nonblocking for unicast Benes network with full bandwidth.

10. The integrated circuit device of claim 8, wherein  $d = 2$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said  
20 routing network is strictly nonblocking for unicast Benes network and rearrangeably nonblocking for arbitrary fan-out multicast Benes network with full bandwidth.

11. The integrated circuit device of claim 8, wherein  $d = 2$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in  
25 each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast Benes network with full bandwidth.

12. The integrated circuit device of claim 7, wherein  $y \geq (\log_2 N)$  so that the length of the horizontal shuffle exchange links in the highest stage is equal to half the size of the horizontal size of said two dimensional grid of sub-integrated circuit blocks and the length of the vertical shuffle exchange links in the highest stage is equal to half the size of the vertical size of said two dimensional grid of sub-integrated circuit blocks, and  
5 said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks.

13. The integrated circuit device of claim 12, wherein  $d = 2$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said  
10 forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast butterfly fat tree network with full bandwidth.

14. The integrated circuit device of claim 12, wherein  $d = 2$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting  
15 said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast butterfly fat tree network and rearrangeably nonblocking for arbitrary fan-out multicast butterfly fat tree network with  
20 full bandwidth.

15. The integrated circuit device of claim 12, wherein  $d = 2$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting  
said forward connecting links and there are at least three switches in each said stage in  
each said sub-integrated circuit block connecting said backward connecting links and said  
25 routing network is strictly nonblocking for arbitrary fan-out multicast butterfly fat tree network with full bandwidth.

16. The integrated circuit device of claim 1, wherein said horizontal and vertical links are implemented on two or more metal layers.
17. The integrated circuit device of claim 1, wherein said switches comprising active and reprogrammable cross points and said each cross point is programmable by an SRAM cell or a Flash Cell.
18. The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks are of equal die size.
19. The integrated circuit device of claim 16, wherein said sub-integrated circuit blocks are Lookup Tables (hereinafter "LUTs") and said integrated circuit device is a field programmable gate array (FPGA) device or field programmable gate array (FPGA) block embedded in another integrated circuit device.
20. The integrated circuit device of claim 16, wherein said sub-integrated circuit blocks are AND or OR gates and said integrated circuit device is a programmable logic device (PLD).
21. The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks comprising any arbitrary hardware logic or memory circuits.
22. The integrated circuit device of claim 1, wherein said switches comprising active one-time programmable cross points and said integrated circuit device is a mask programmable gate array (MPGA) device or a structured ASIC device.
23. The integrated circuit device of claim 1, wherein said switches comprising passive cross points or just connection of two links or not and said integrated circuit device is a Application Specific Integrated Circuit (ASIC) device.
24. The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks further recursively comprise one or more super-sub-integrated circuit blocks and a sub-routing network.

25. The integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and  $y \geq (\log_2 N)$ .
- 5 26. The integrated circuit device of claim 25, wherein  $d = 2$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized multi-stage network with  
10 full bandwidth.
27. The integrated circuit device of claim 25, wherein  $d = 2$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in  
15 each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized multi-stage network and rearrangeably nonblocking for arbitrary fan-out multicast generalized multi-stage network with full bandwidth.
28. The integrated circuit device of claim 25, wherein  $d = 2$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting  
20 said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized multi-stage network with full bandwidth.
29. The integrated circuit device of claim 5, wherein said all horizontal shuffle  
25 exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and  $y \geq (\log_2 N)$ , and

said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks.

30. The integrated circuit device of claim 29, wherein  $d = 2$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized butterfly fat tree network with full bandwidth.

31. The integrated circuit device of claim 29, wherein  $d = 2$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized butterfly fat tree Network and rearrangeably nonblocking for arbitrary fan-out multicast generalized butterfly fat tree network with full bandwidth.

32. The integrated circuit device of claim 29, wherein  $d = 2$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized butterfly fat tree network with full bandwidth.

33. The integrated circuit device of claim 1, wherein said straight links connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and said cross links are connecting as vertical or horizontal or diagonal links between two different said sub-integrated circuit blocks.

34. The integrated circuit device of claim 8, wherein  $d = 4$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast multi-link Benes network with full bandwidth.

35. The integrated circuit device of claim 8, wherein  $d = 4$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast multi-link Benes network and rearrangeably nonblocking for arbitrary fan-out multicast multi-link Benes network with full bandwidth.

36. The integrated circuit device of claim 8, wherein  $d = 4$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast multi-link Benes network with full bandwidth.

37. The integrated circuit device of claim 12, wherein  $d = 4$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast multi-link butterfly fat tree network with full bandwidth.

38. The integrated circuit device of claim 12, wherein  $d = 4$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in



each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast multi-link butterfly fat tree network and rearrangeably nonblocking for arbitrary fan-out multicast multi-link butterfly fat tree network with full bandwidth.

5           39.     The integrated circuit device of claim 12, wherein  $d = 4$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast multi-link butterfly fat tree network with full bandwidth.

10           40.     The integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and  $y \geq (\log_2 N)$ .

15           41.     The integrated circuit device of claim 40, wherein  $d = 4$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized multi-link multi-stage network with full bandwidth.

20           42.     The integrated circuit device of claim 40, wherein  $d = 4$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized multi-link multi-stage network and rearrangeably nonblocking for arbitrary fan-out multicast generalized multi-link multi-stage network with full bandwidth.

43. The integrated circuit device of claim 40, wherein  $d = 4$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said  
 5 routing network is strictly nonblocking for arbitrary fan-out multicast generalized multi-link multi-stage network with full bandwidth.

44. The integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two  
 10 corresponding said succeeding stages are of different length and  $y \geq (\log_2 N)$ , and said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks.

45. The integrated circuit device of claim 44, wherein  $d = 4$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said  
 15 forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized multi-link butterfly fat tree network with full bandwidth.

46. The integrated circuit device of claim 44, wherein  $d = 4$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting  
 20 said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized multi-link butterfly fat tree Network and rearrangeably nonblocking for arbitrary fan-out multicast generalized multi-link  
 25 butterfly fat tree network with full bandwidth.

47. The integrated circuit device of claim 44, wherein  $d = 4$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting

said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized multi-link butterfly fat tree network with full bandwidth.

5           48.     The integrated circuit device of claim 1, wherein said plurality of forward connecting links use a plurality of buffers to amplify signals driven through them and said plurality of backward connecting links use a plurality of buffers to amplify signals driven through them; and said buffers can be inverting or non-inverting buffers.

              49.     The integrated circuit device of claim 1, wherein said all  
10 switches of size  $d \times d$  are either fully populated or partially populated.

## VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS

**Venkat Konda**

### ABSTRACT OF DISCLOSURE

In accordance with the invention, VLSI layouts of generalized multi-stage  
 5 networks for broadcast, unicast and multicast connections are presented using only  
 horizontal and vertical links. The VLSI layouts employ shuffle exchange links where  
 outlet links of cross links from switches in a stage in one sub-integrated circuit block are  
 connected to inlet links of switches in the succeeding stage in another sub-integrated  
 circuit block so that said cross links are either vertical links or horizontal and vice versa.  
 10 In one embodiment the sub-integrated circuit blocks are arranged in a hypercube  
 arrangement in a two-dimensional plane. The VLSI layouts exploit the benefits of  
 significantly lower cross points, lower signal latency, lower power and full connectivity  
 with significantly fast compilation.

The VLSI layouts presented are applicable to generalized multi-stage networks  
 15  $V(N_1, N_2, d, s)$ , generalized folded multi-stage networks  $V_{fold}(N_1, N_2, d, s)$ , generalized  
 butterfly fat tree networks  $V_{bft}(N_1, N_2, d, s)$ , generalized multi-link multi-stage networks  
 $V_{mlink}(N_1, N_2, d, s)$ , generalized folded multi-link multi-stage networks  
 $V_{fold-mlink}(N_1, N_2, d, s)$ , generalized multi-link butterfly fat tree networks  
 $V_{mlink-bft}(N_1, N_2, d, s)$ , and generalized hypercube networks  $V_{hcube}(N_1, N_2, d, s)$  for  $s =$   
 20 1,2,3 or any number in general. The embodiments of VLSI layouts are useful in wide  
 target applications such as FPGAs, CPLDs, pSoCs, ASIC placement and route tools,  
 networking applications, parallel & distributed computing, and reconfigurable computing.

FIG. 1A

100A

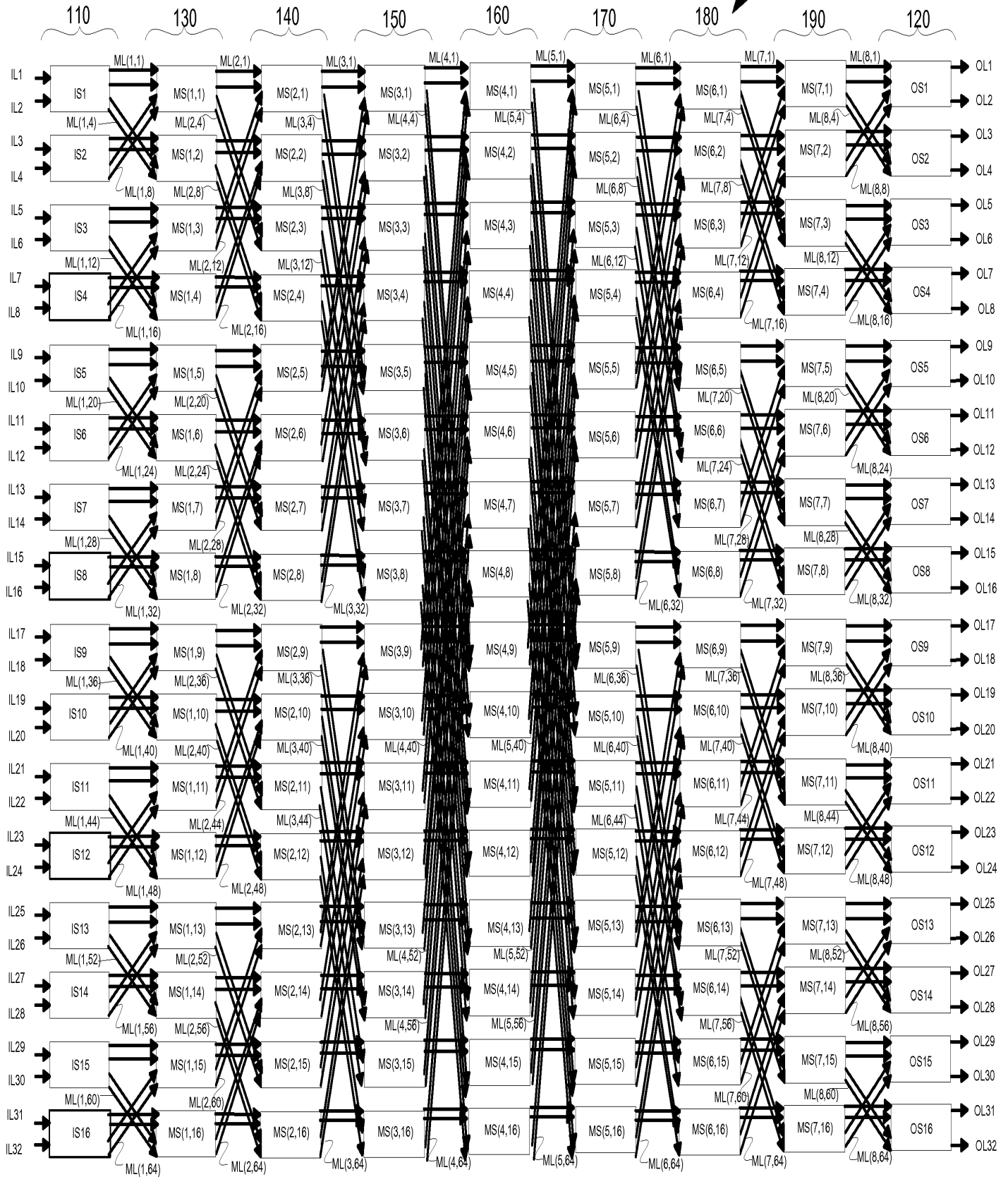


FIG. 1B

100B

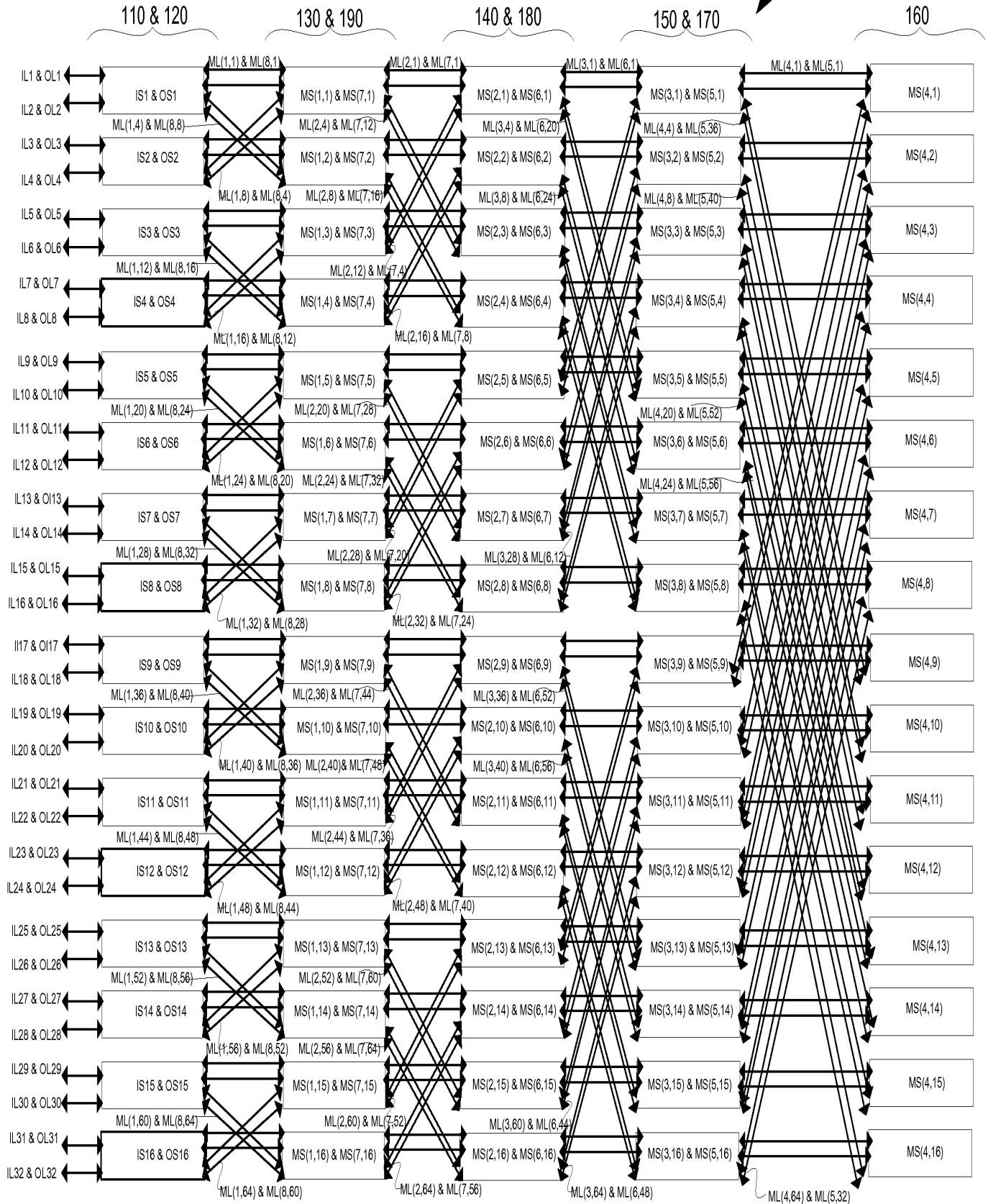
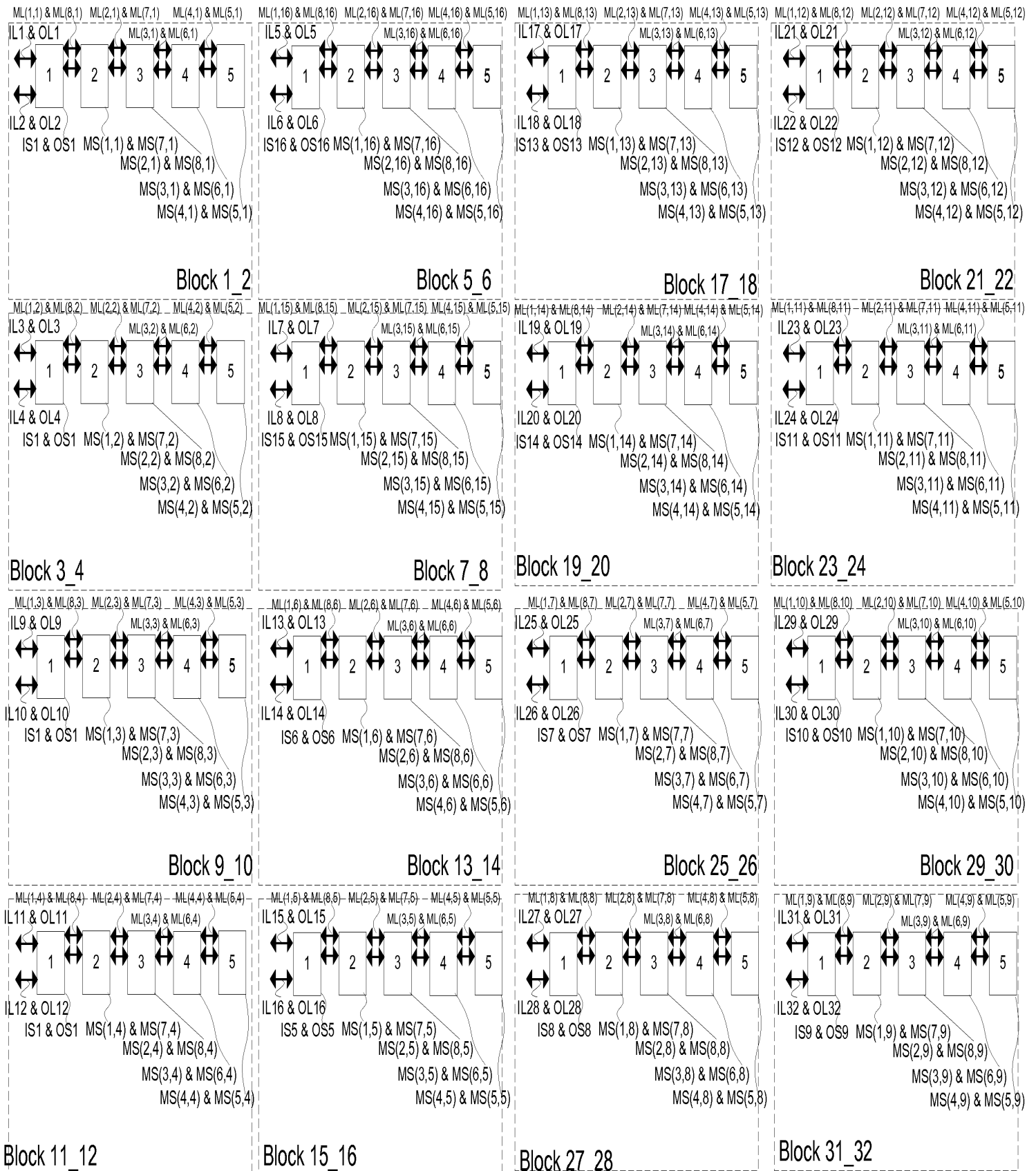




FIG. 1C



100D

FIG. 1D

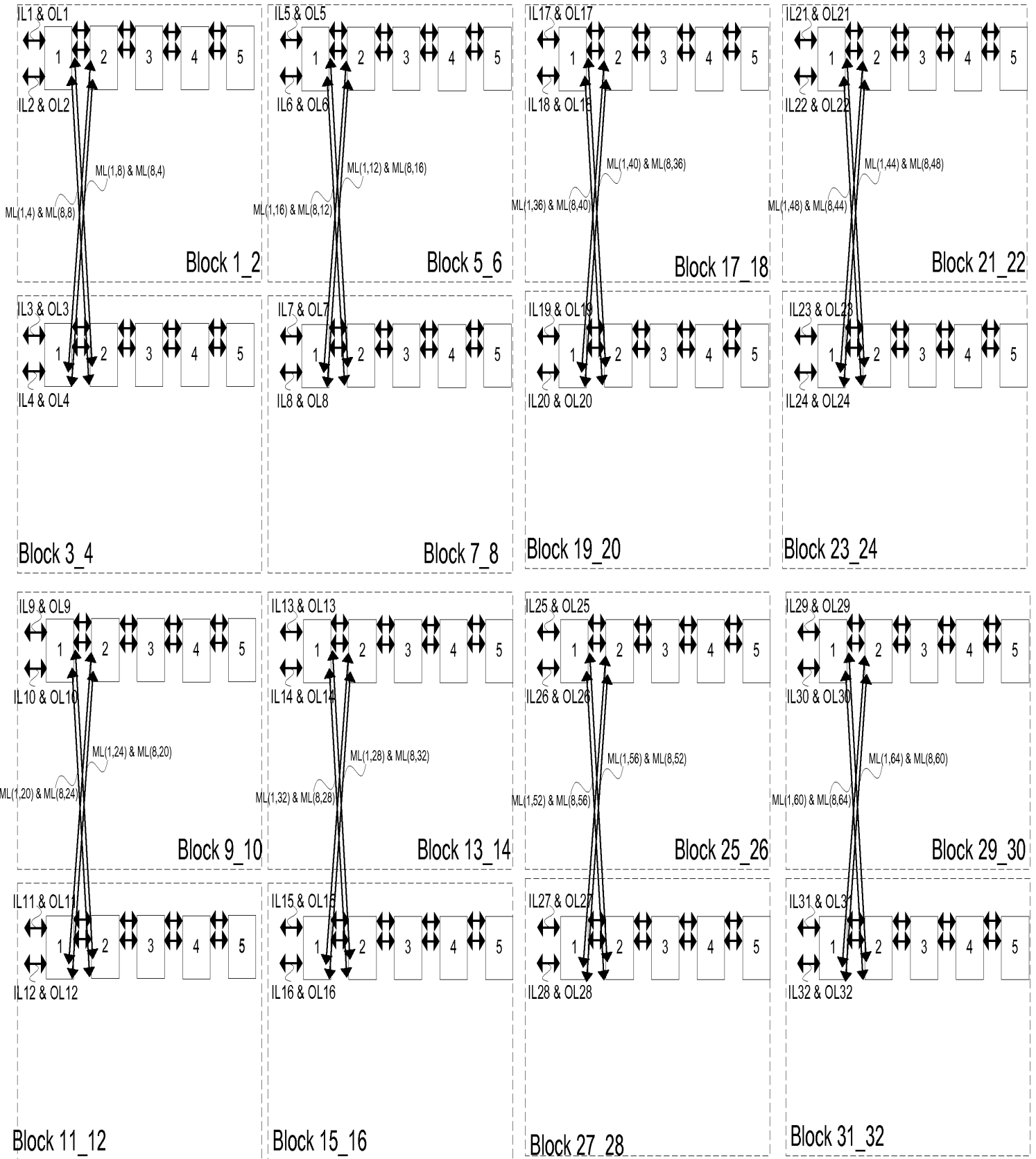




FIG. 1E

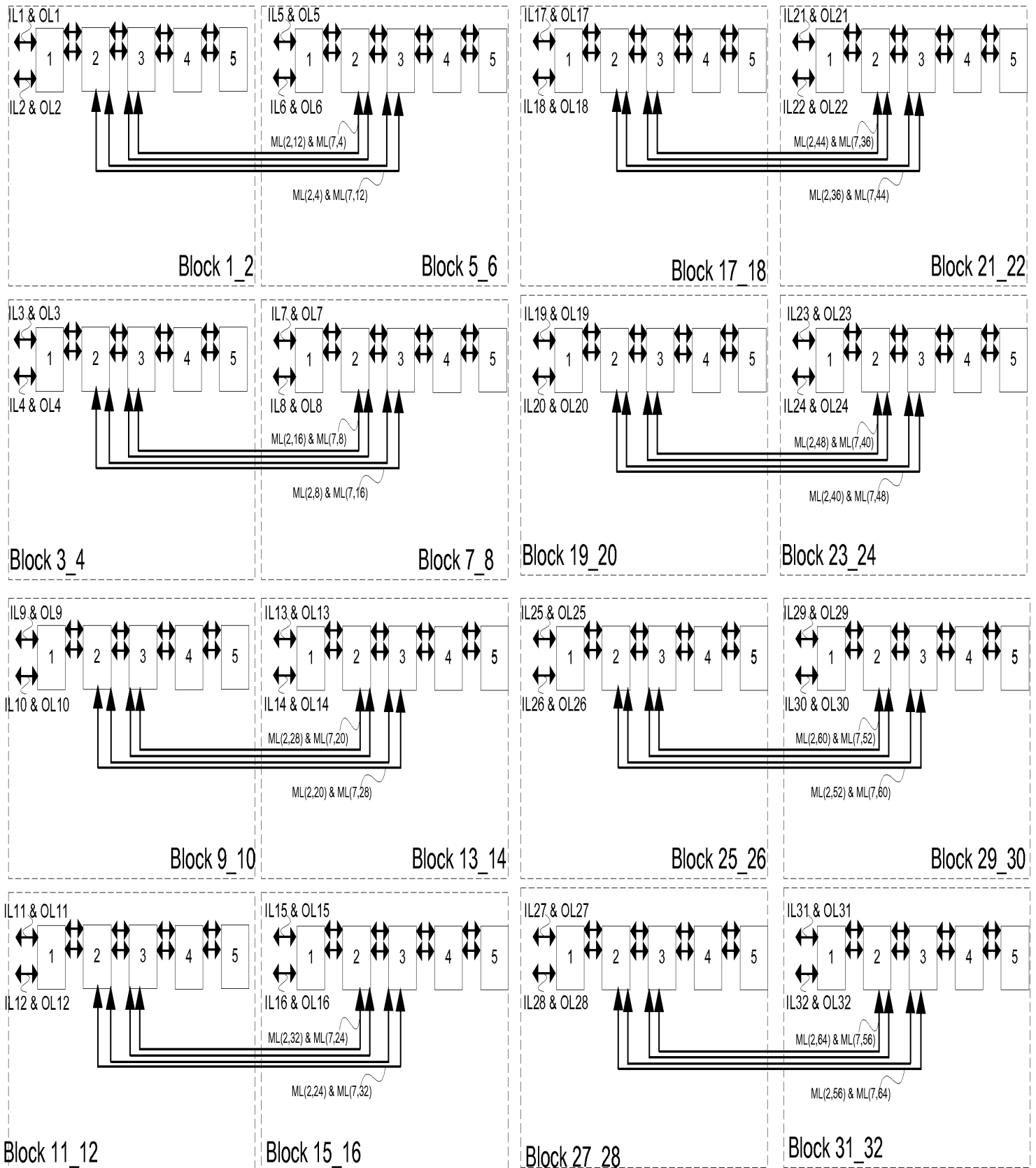


FIG. 1F

100F

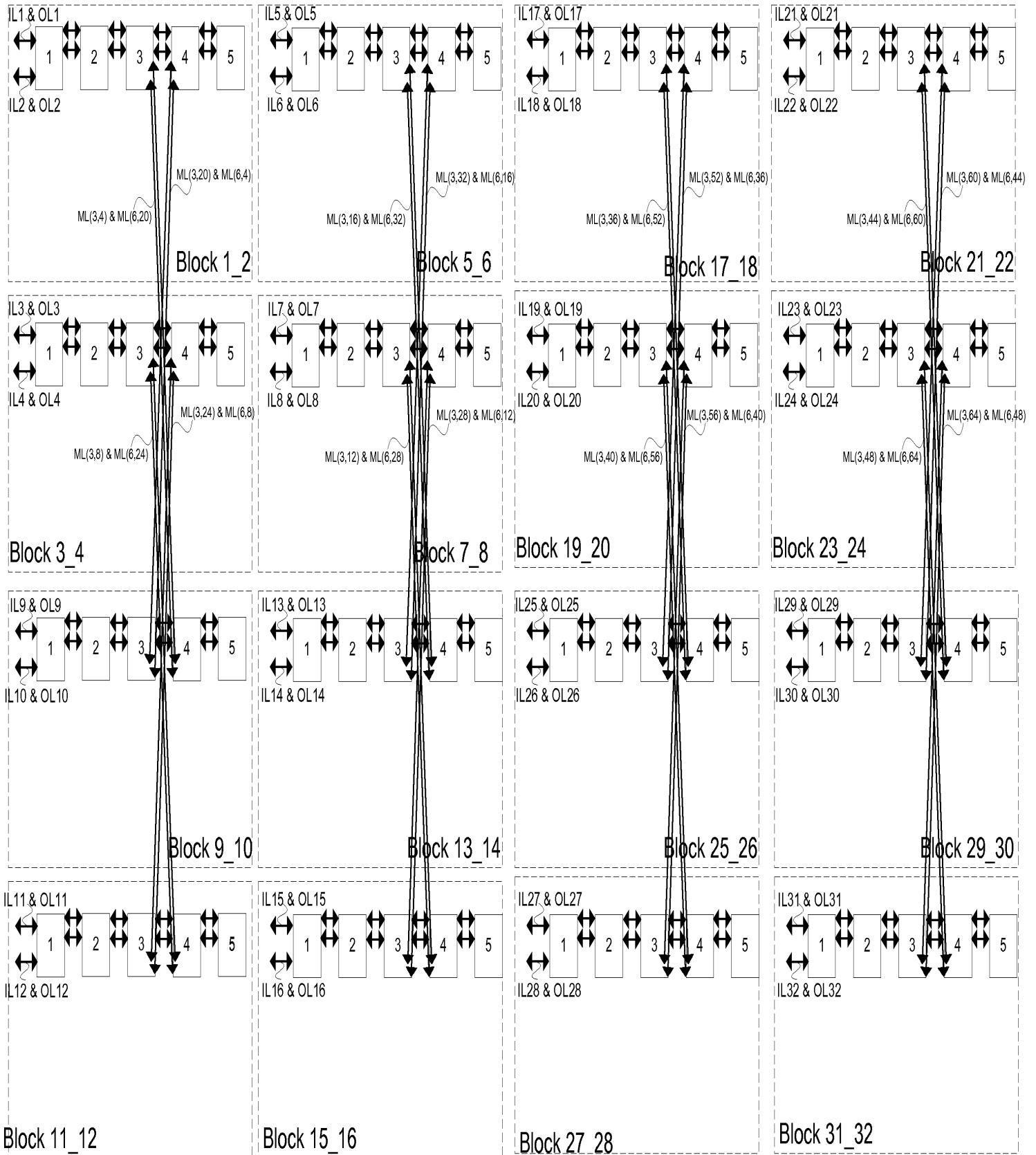
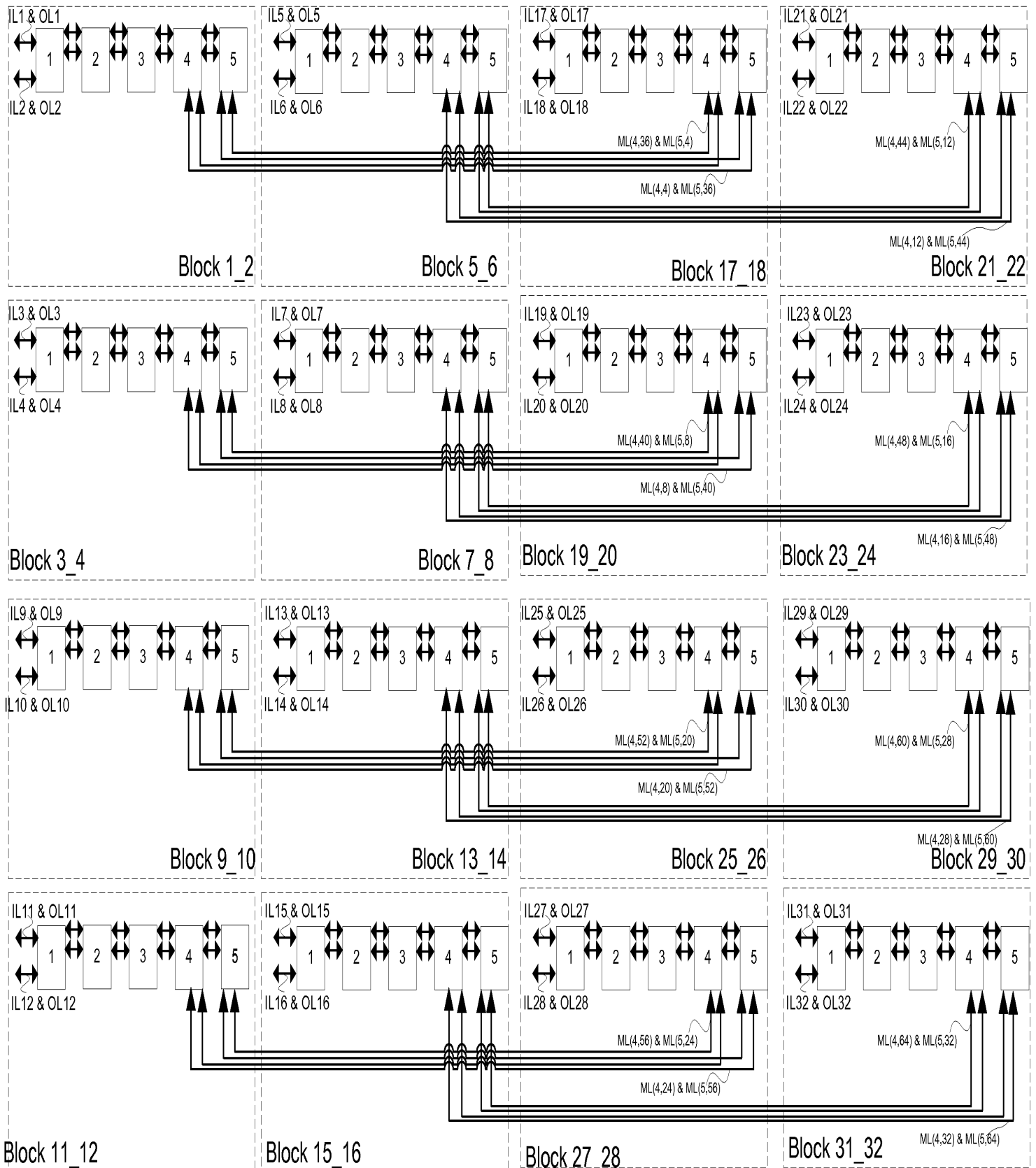


FIG. 1G

100G



100H

FIG. 1H

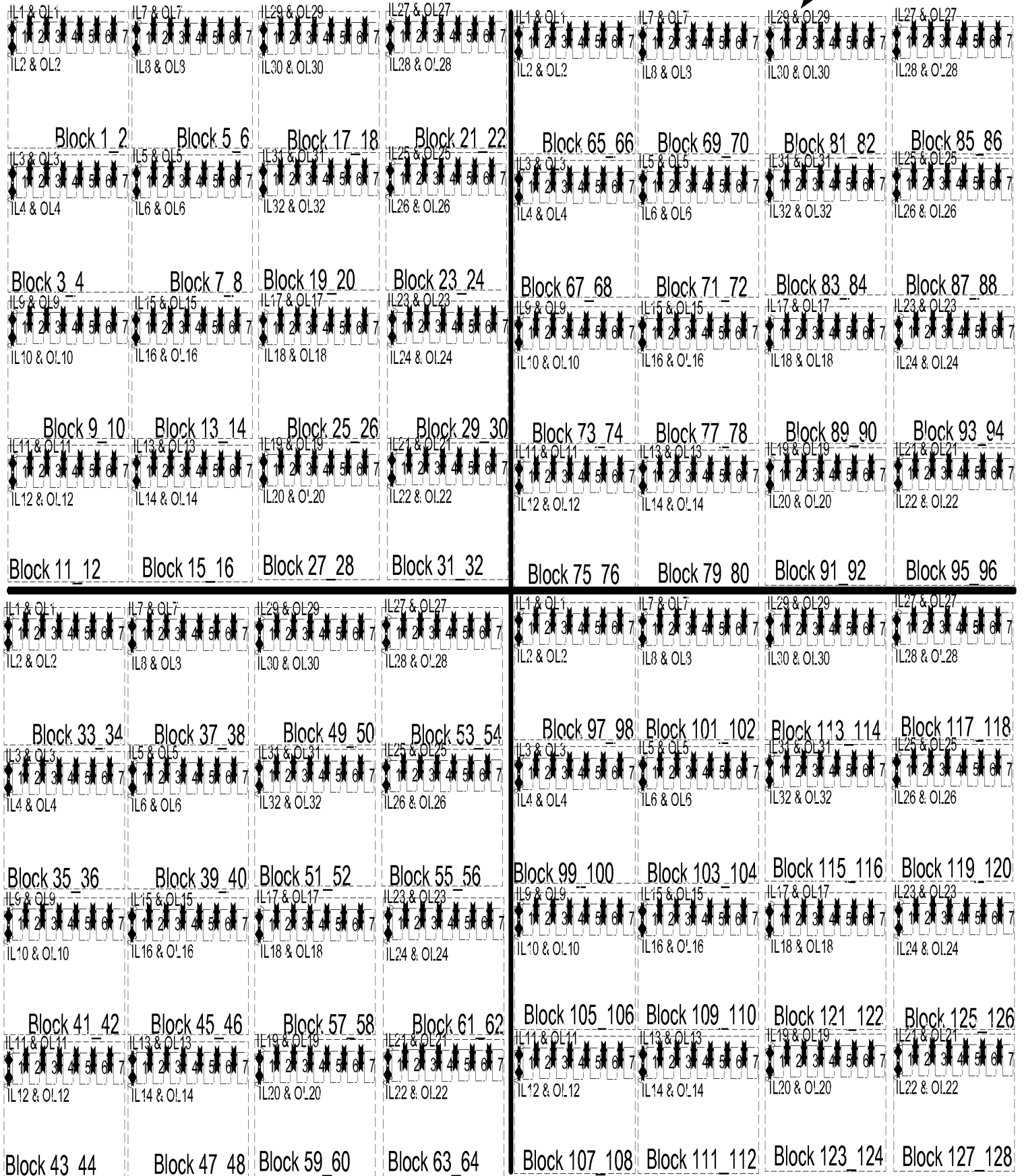


FIG. 11

1001

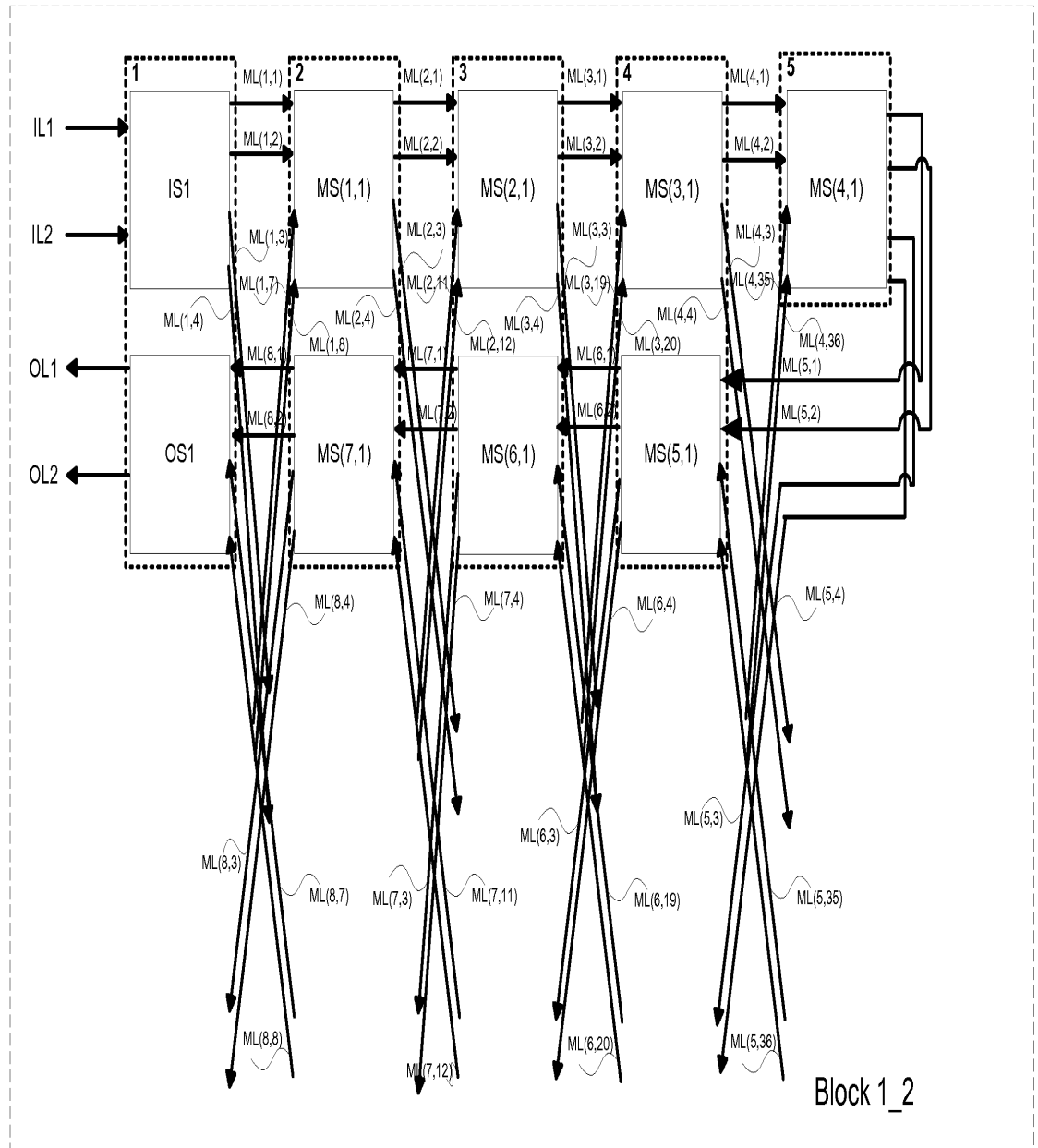


FIG. 1J

100J

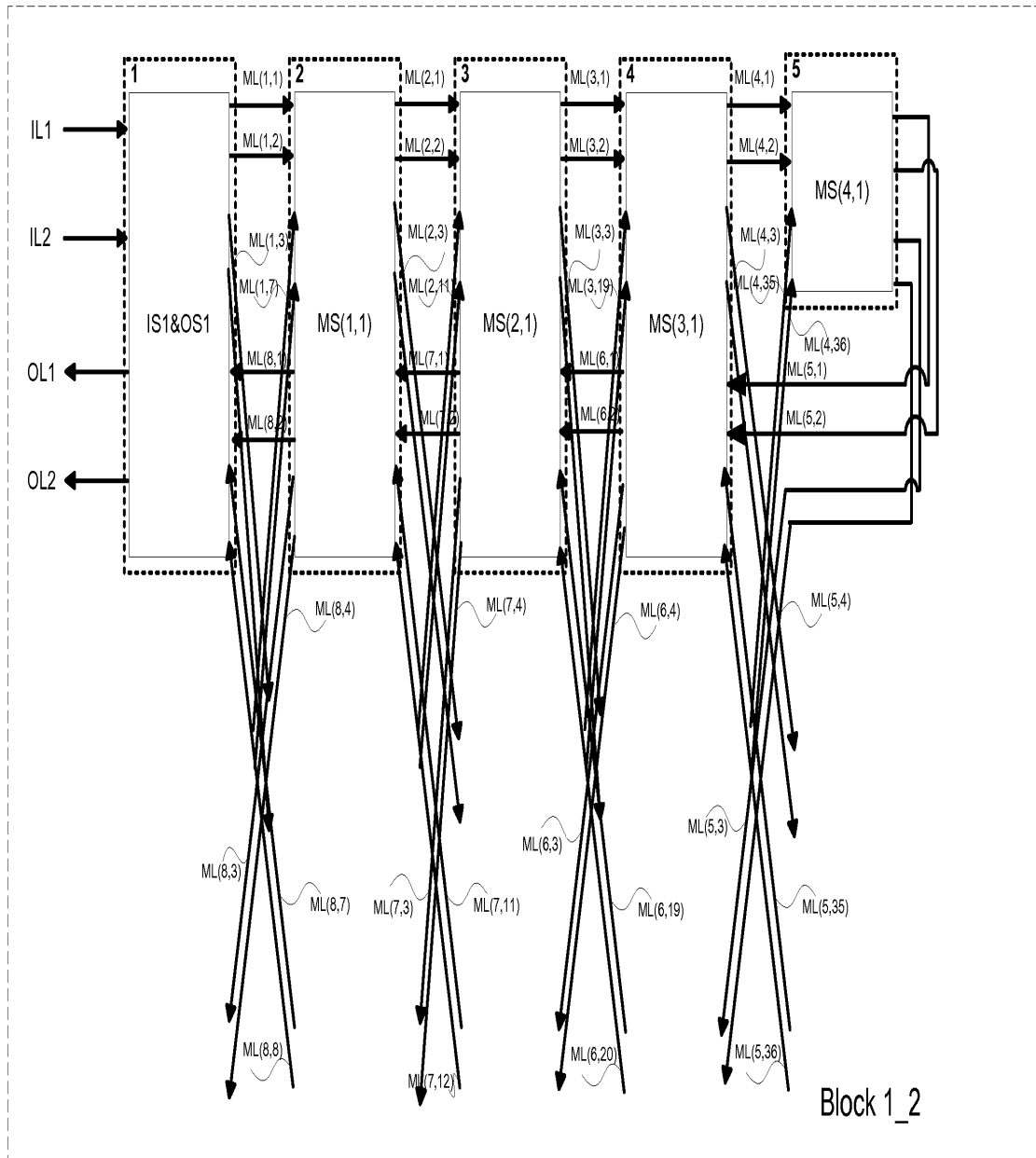


FIG. 1K

100K

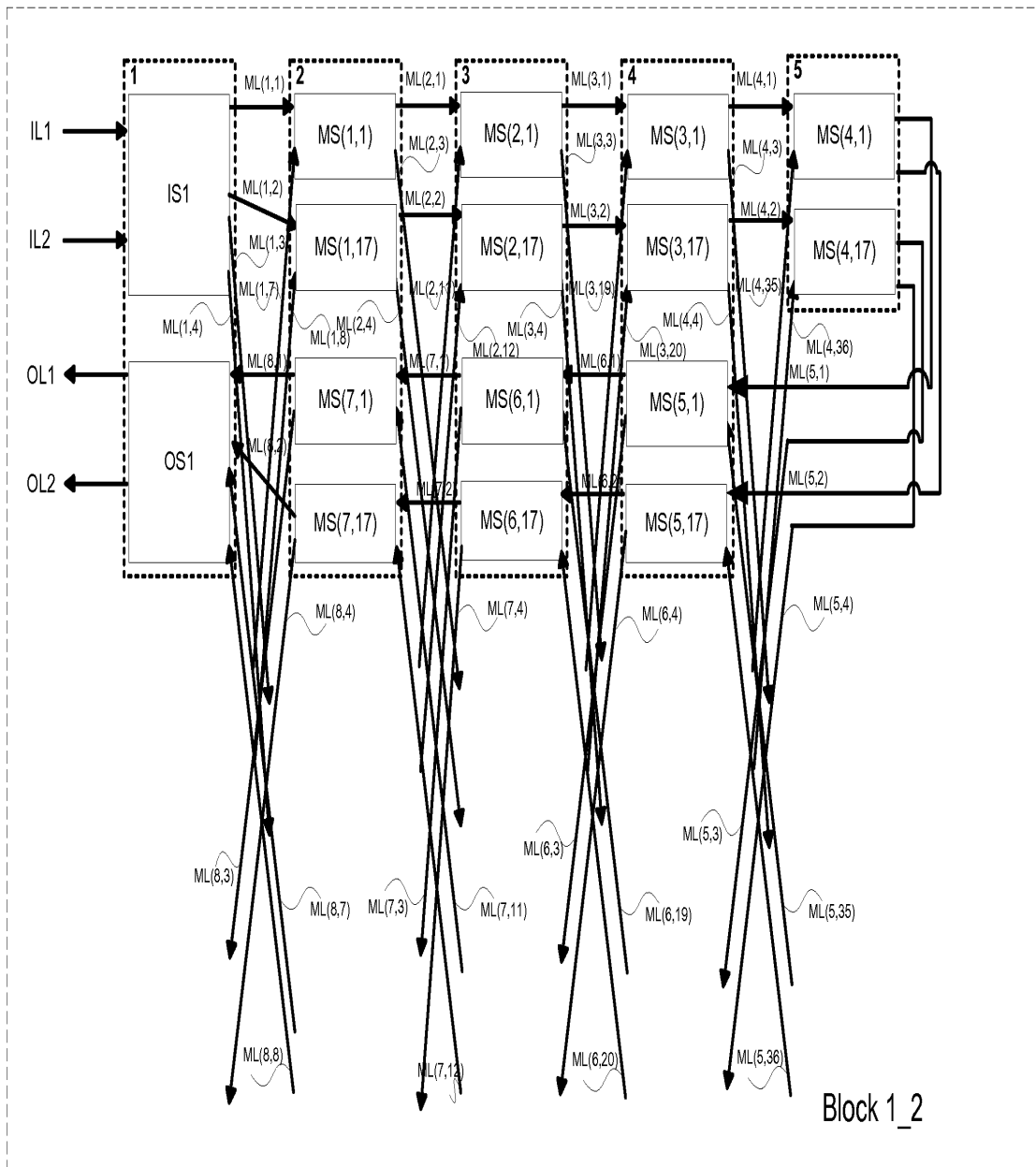


FIG. 1K1

100K1  
↙

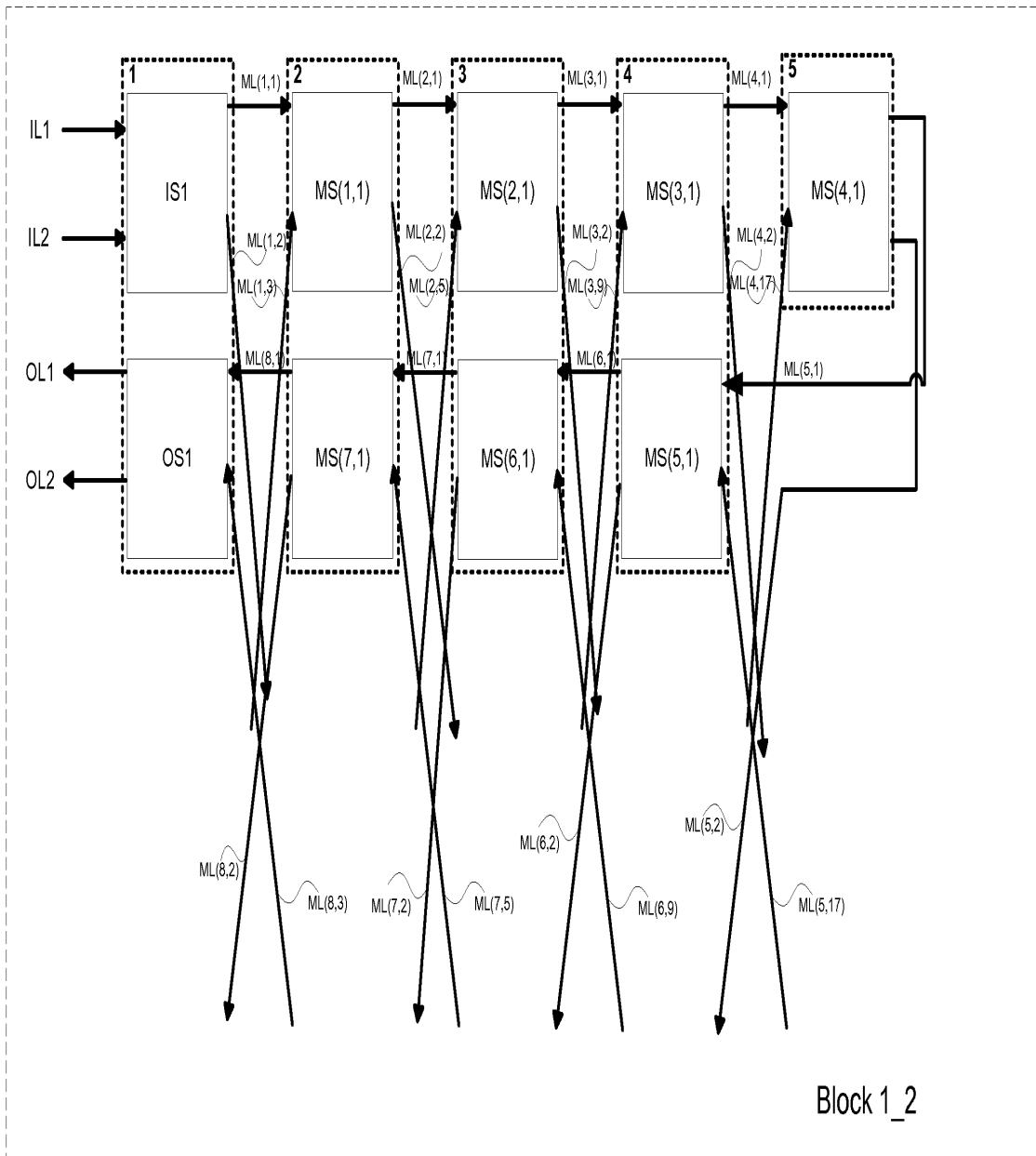




FIG. 1L

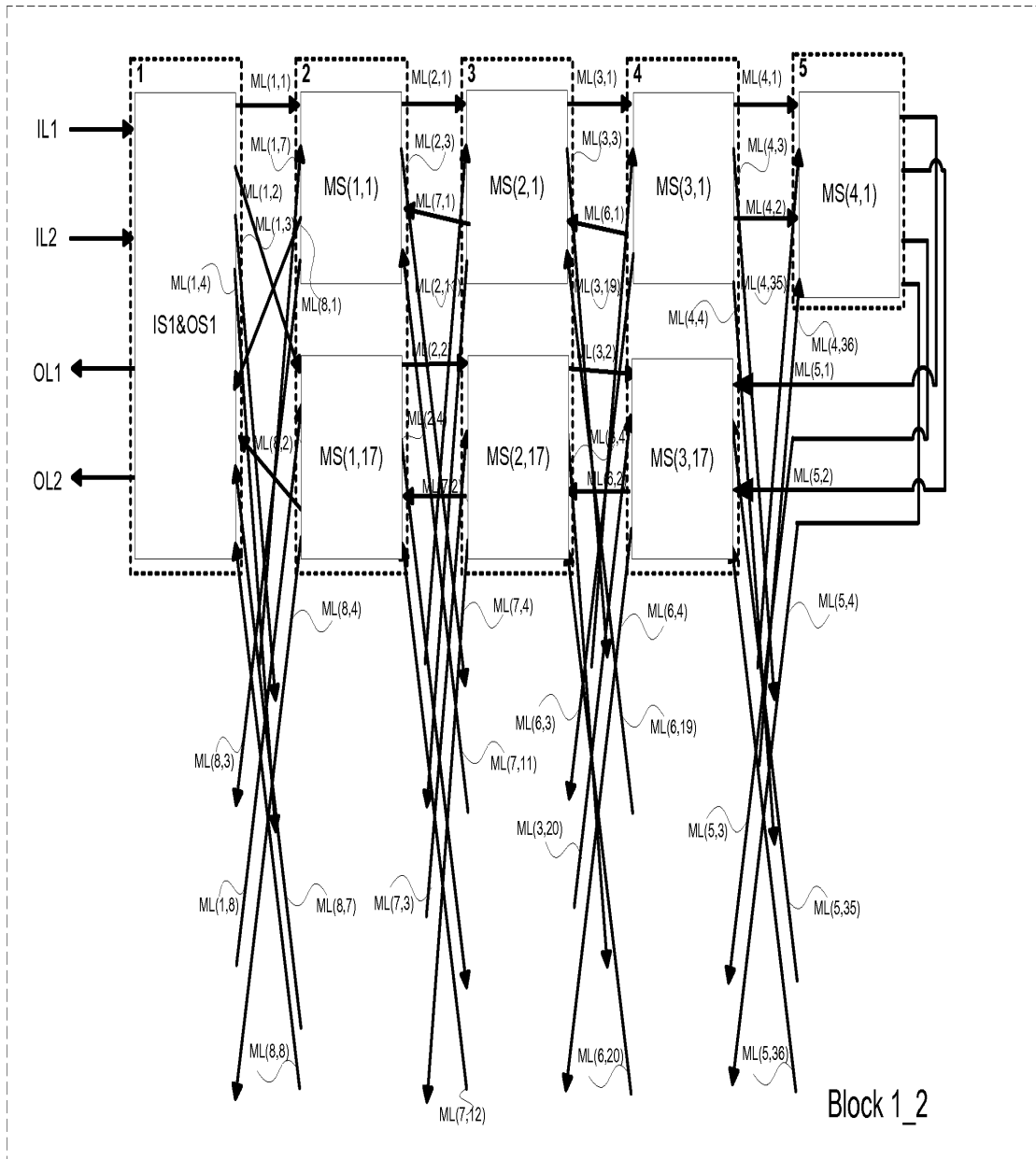


FIG. 1L1

100L1  
↙

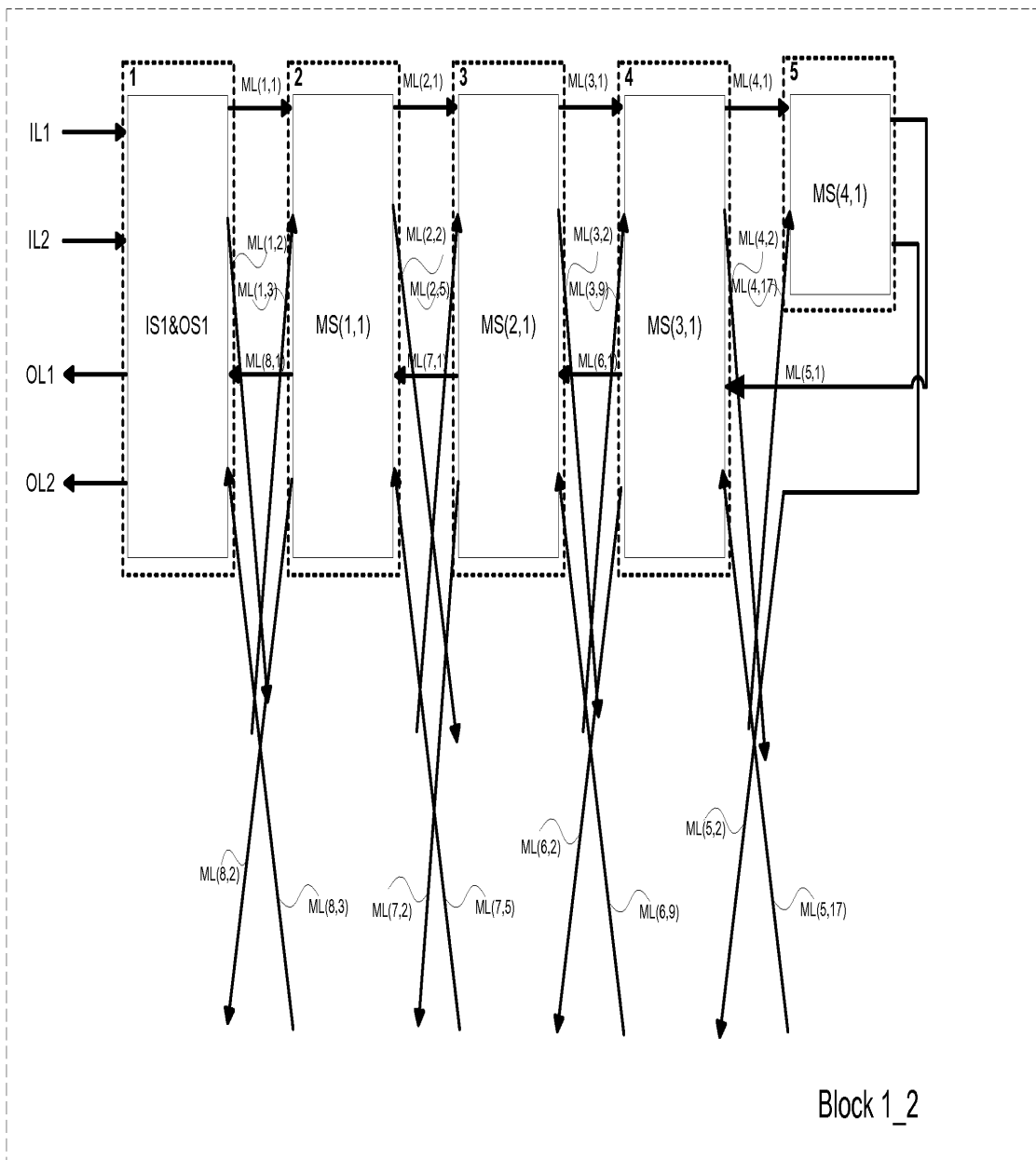


FIG. 2A1

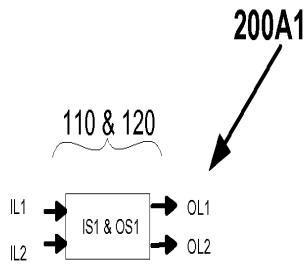


FIG. 2A2

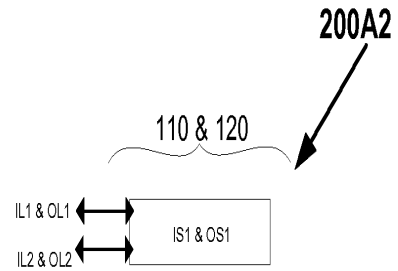


FIG. 2A3

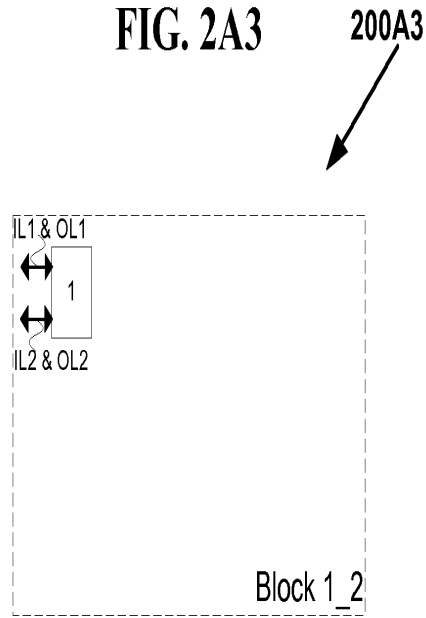


FIG. 2B1

200B1

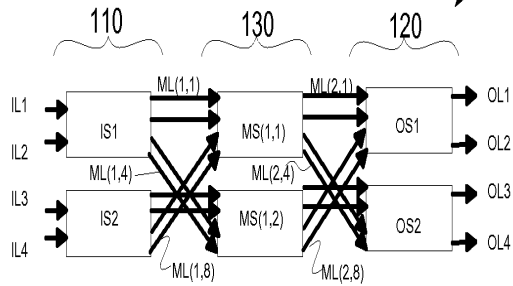


FIG. 2B2

200B2

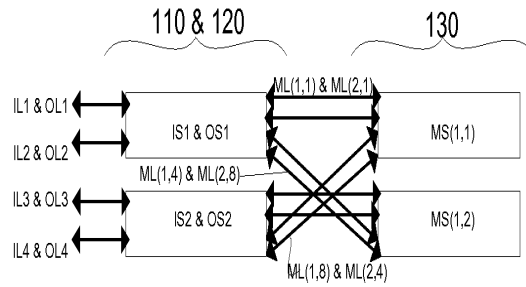


FIG. 2B3

200B3

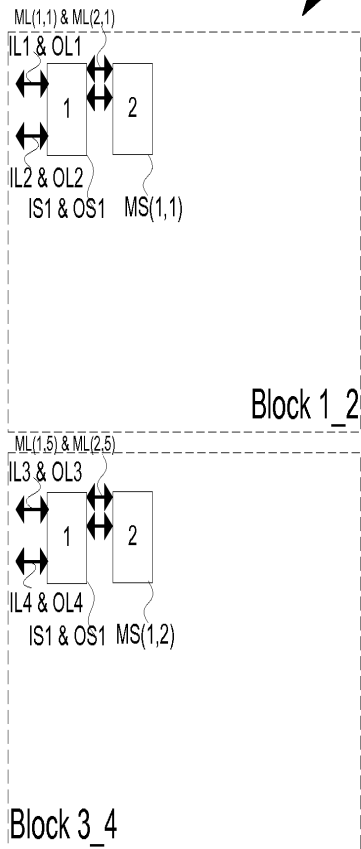


FIG. 2B4

200B4

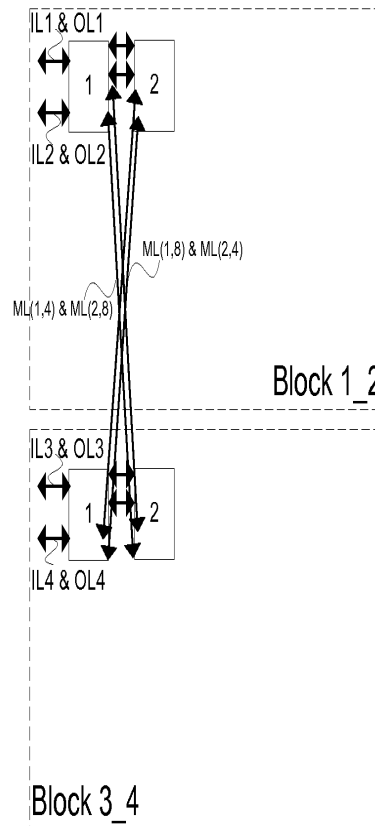


FIG. 2C11

200C11

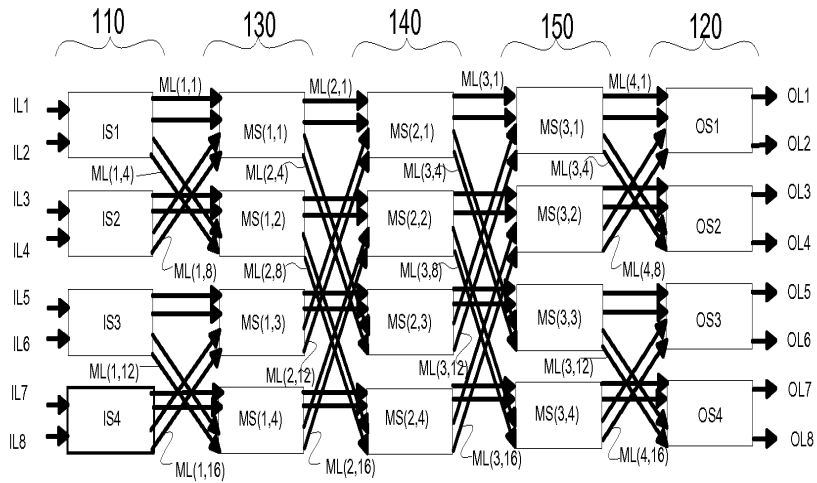


FIG. 2C12

200C12

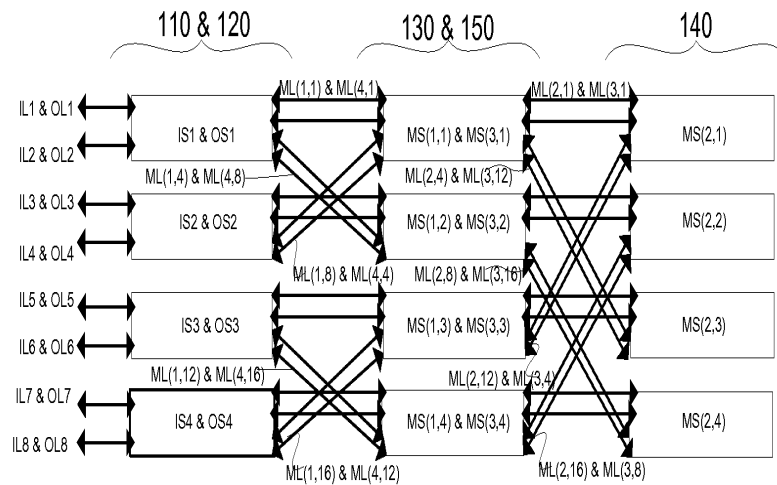
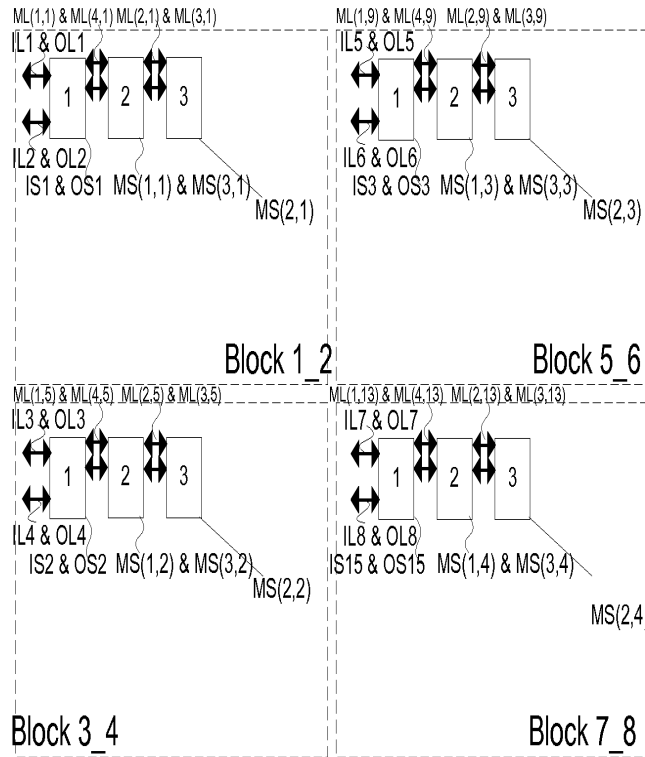
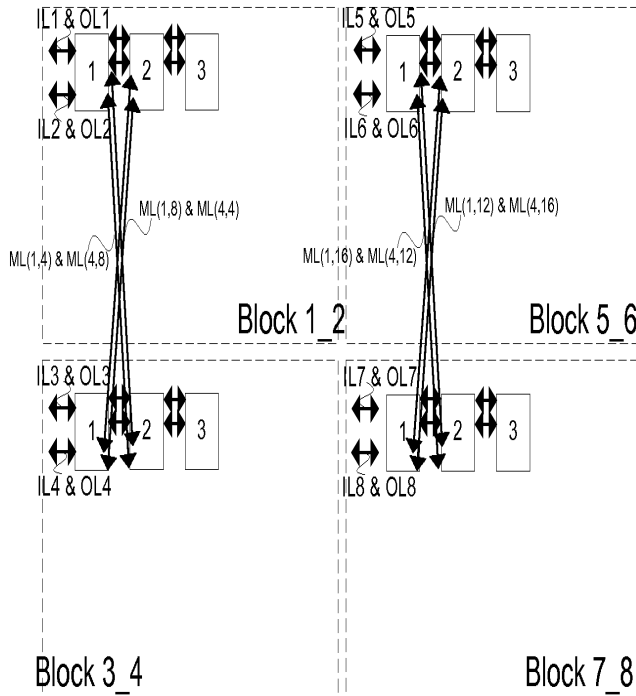


FIG. 2C21



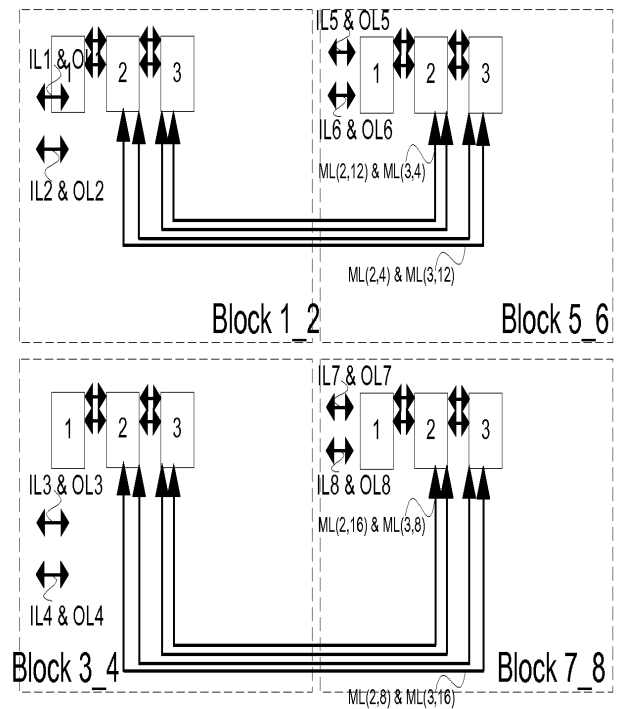
200C21

FIG. 2C22



200C22

FIG. 2C23



200C23

FIG. 2D1

200D1

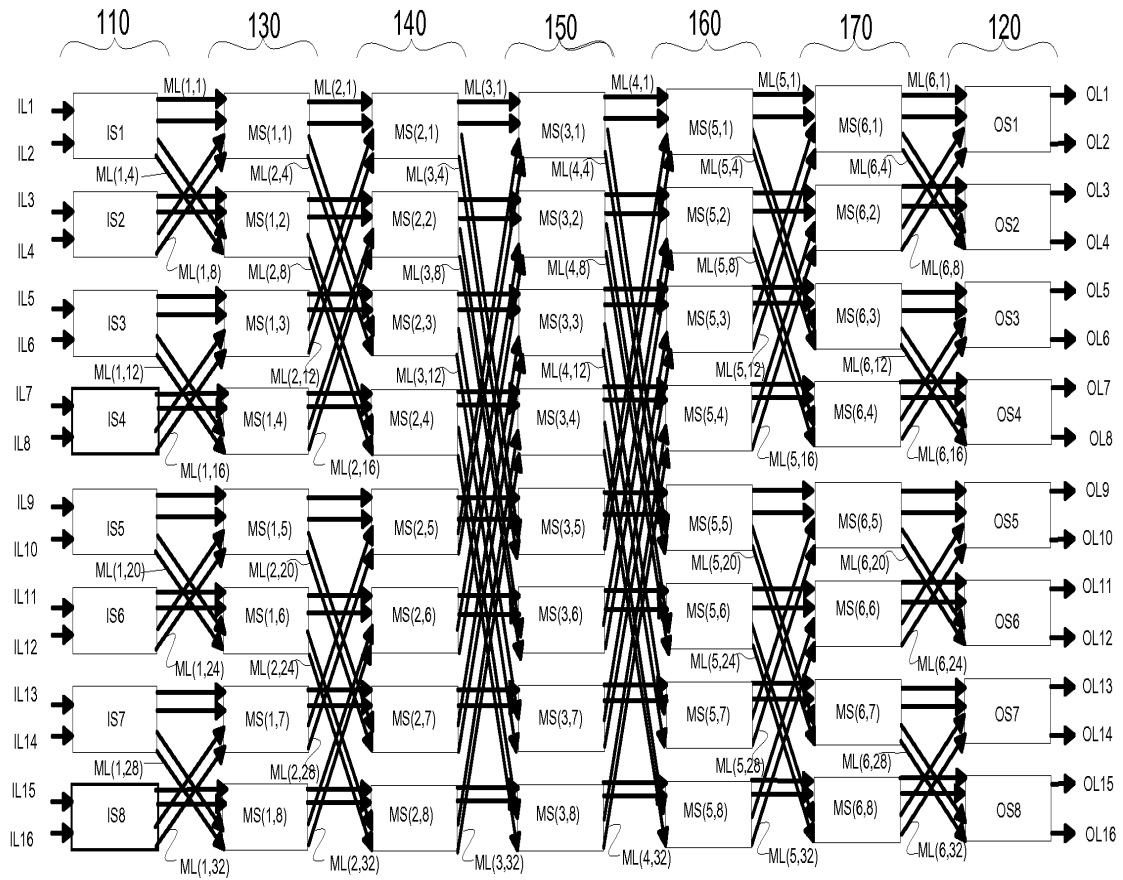


FIG. 2D2

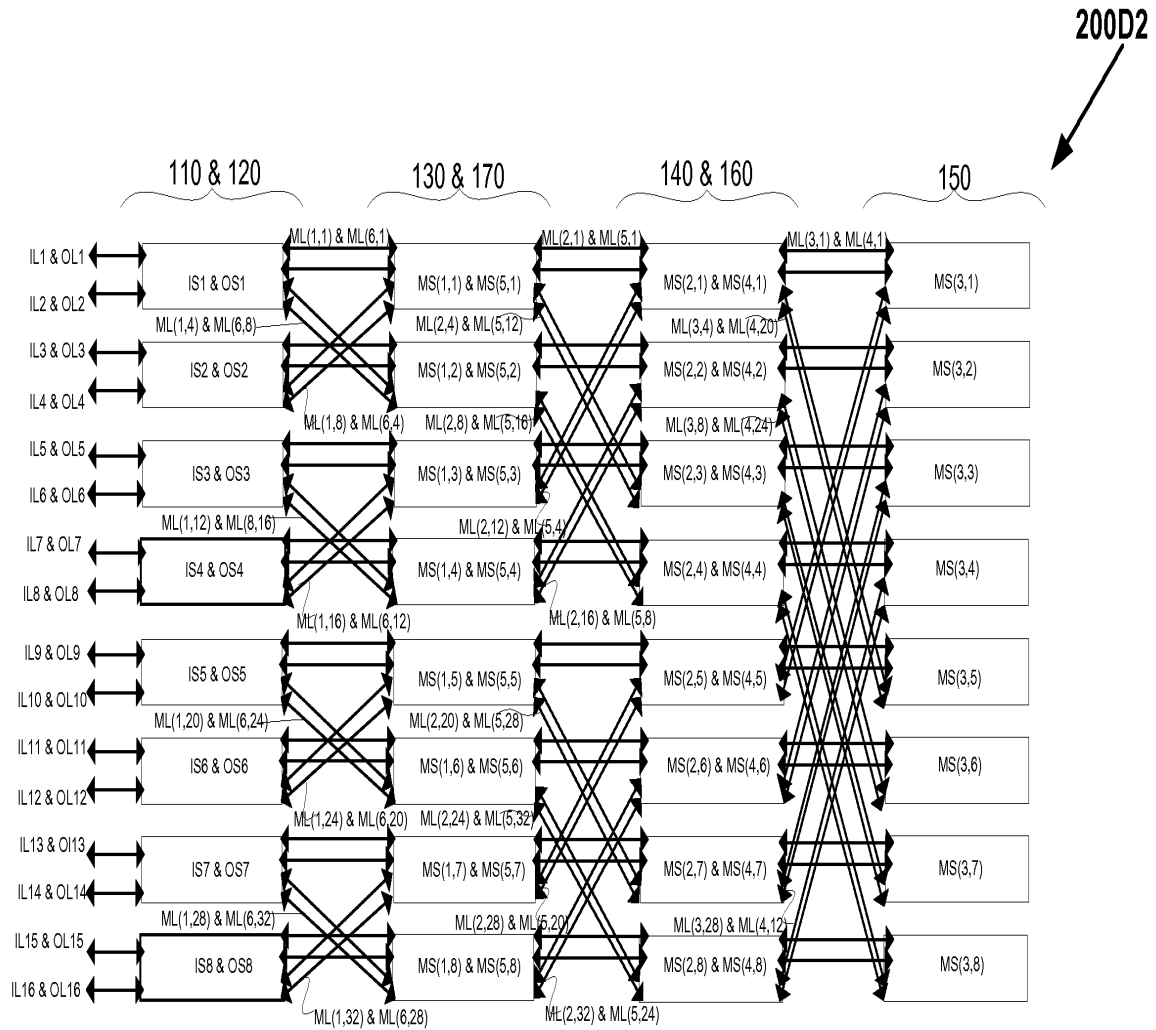




FIG. 2D3

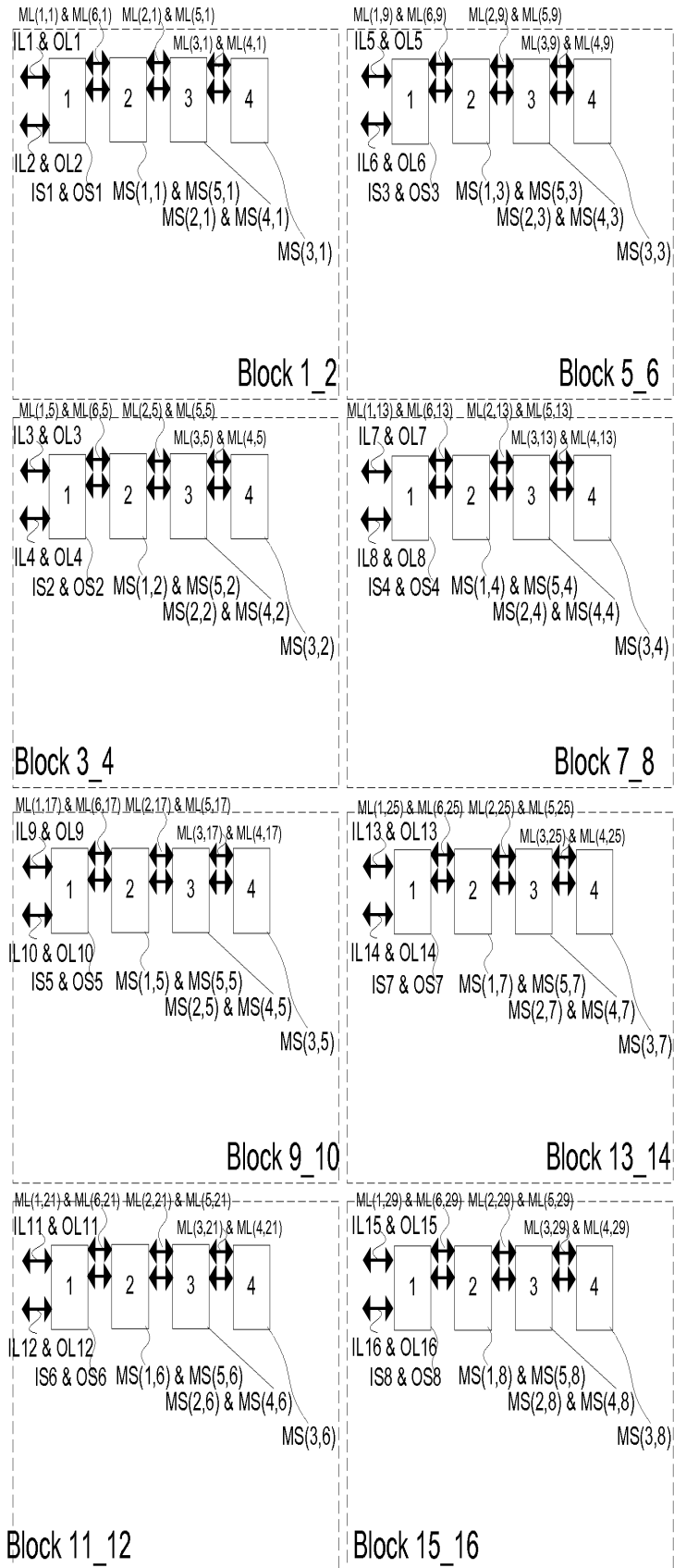
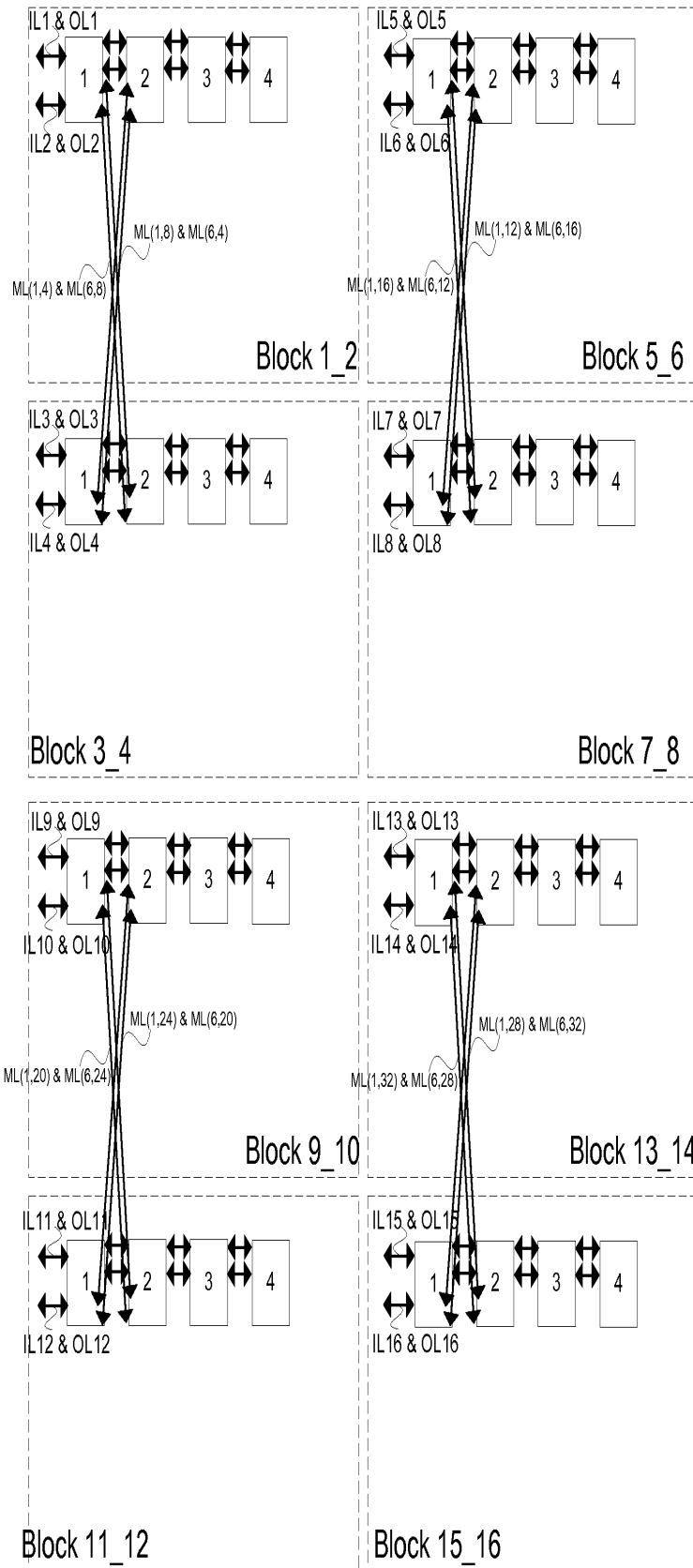


FIG. 2D4



200D5

FIG. 2D5

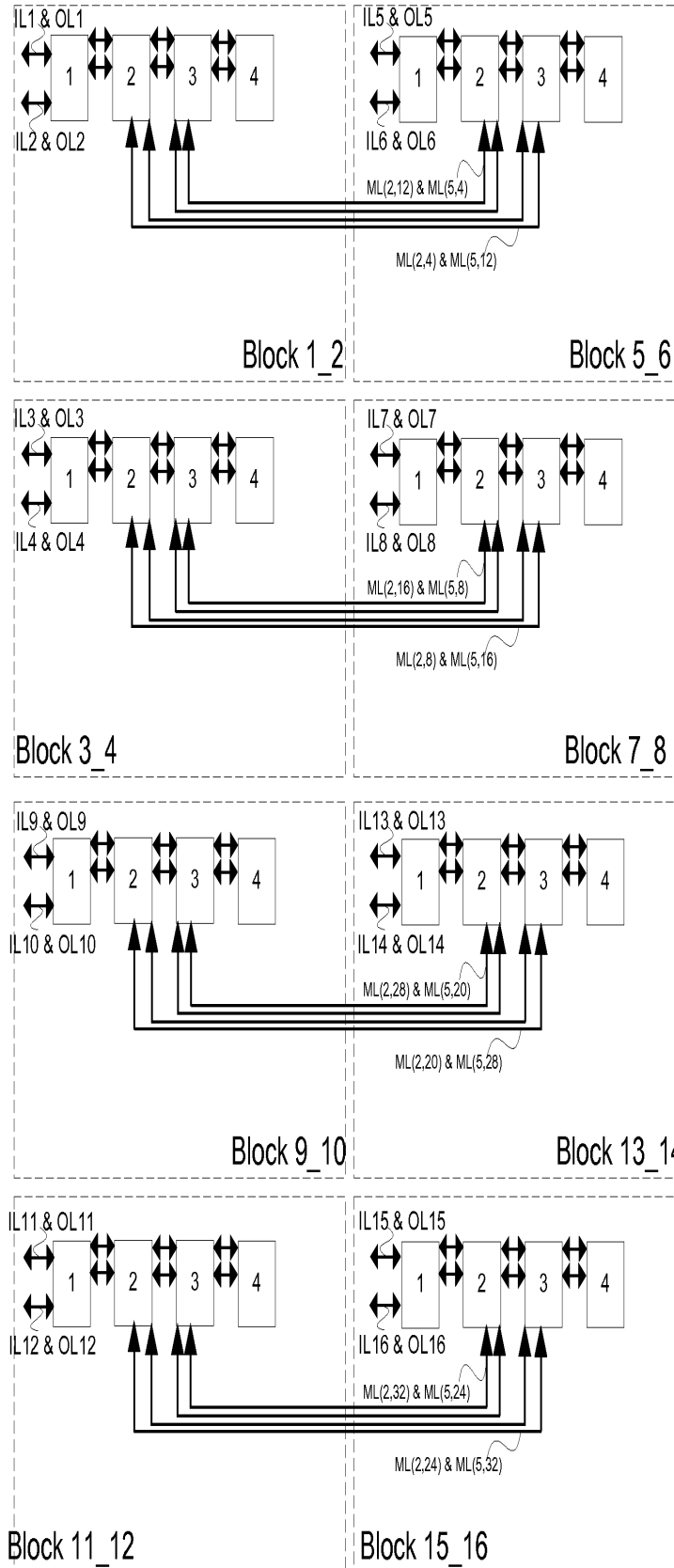


FIG. 2D6

200D6

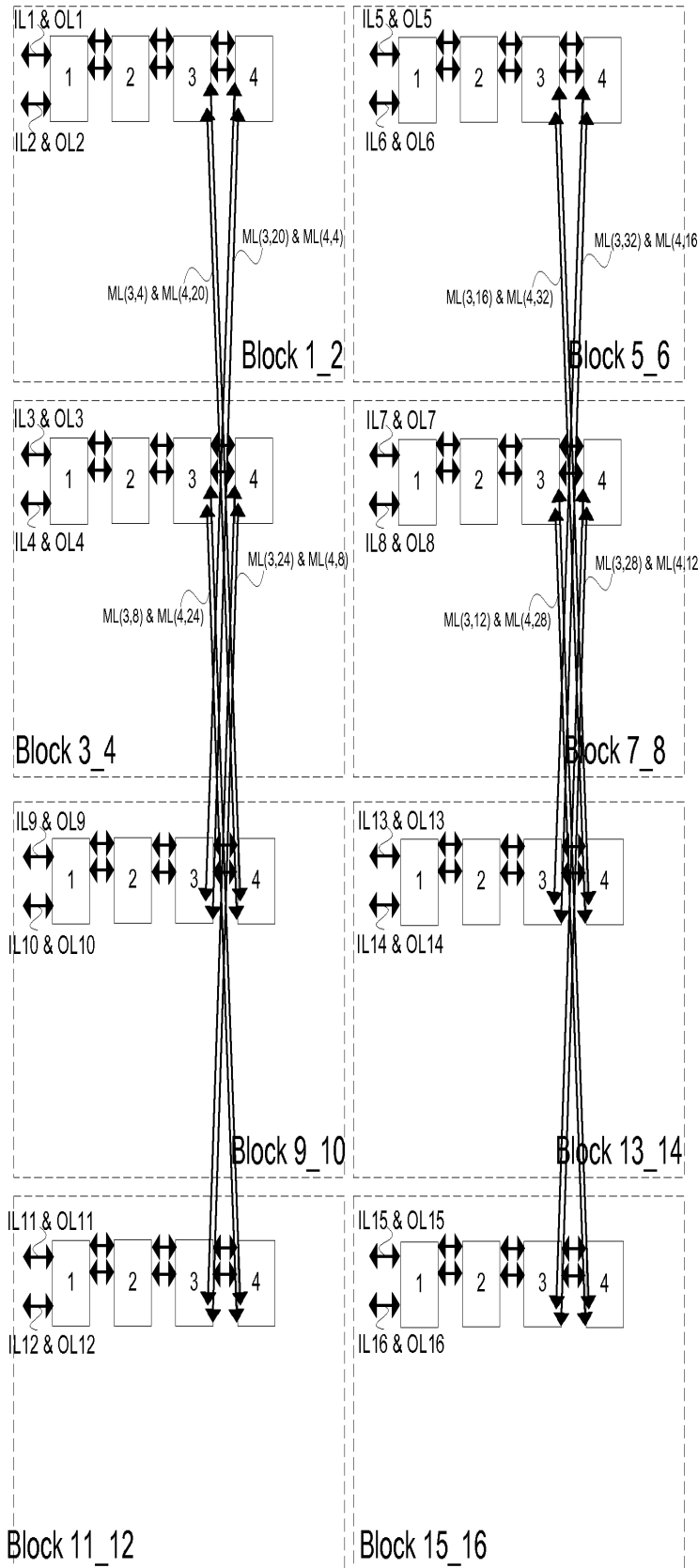


FIG. 3A

300A

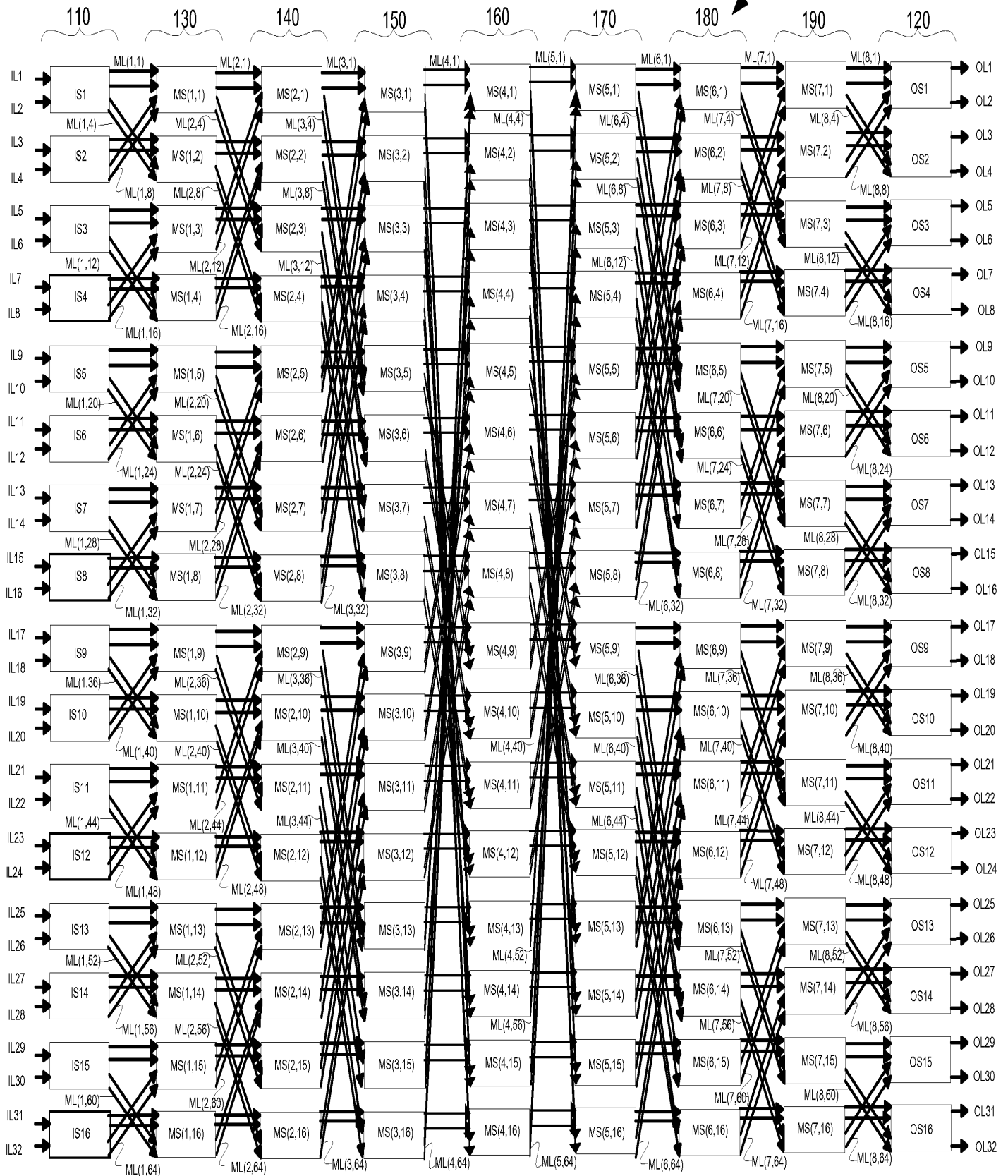
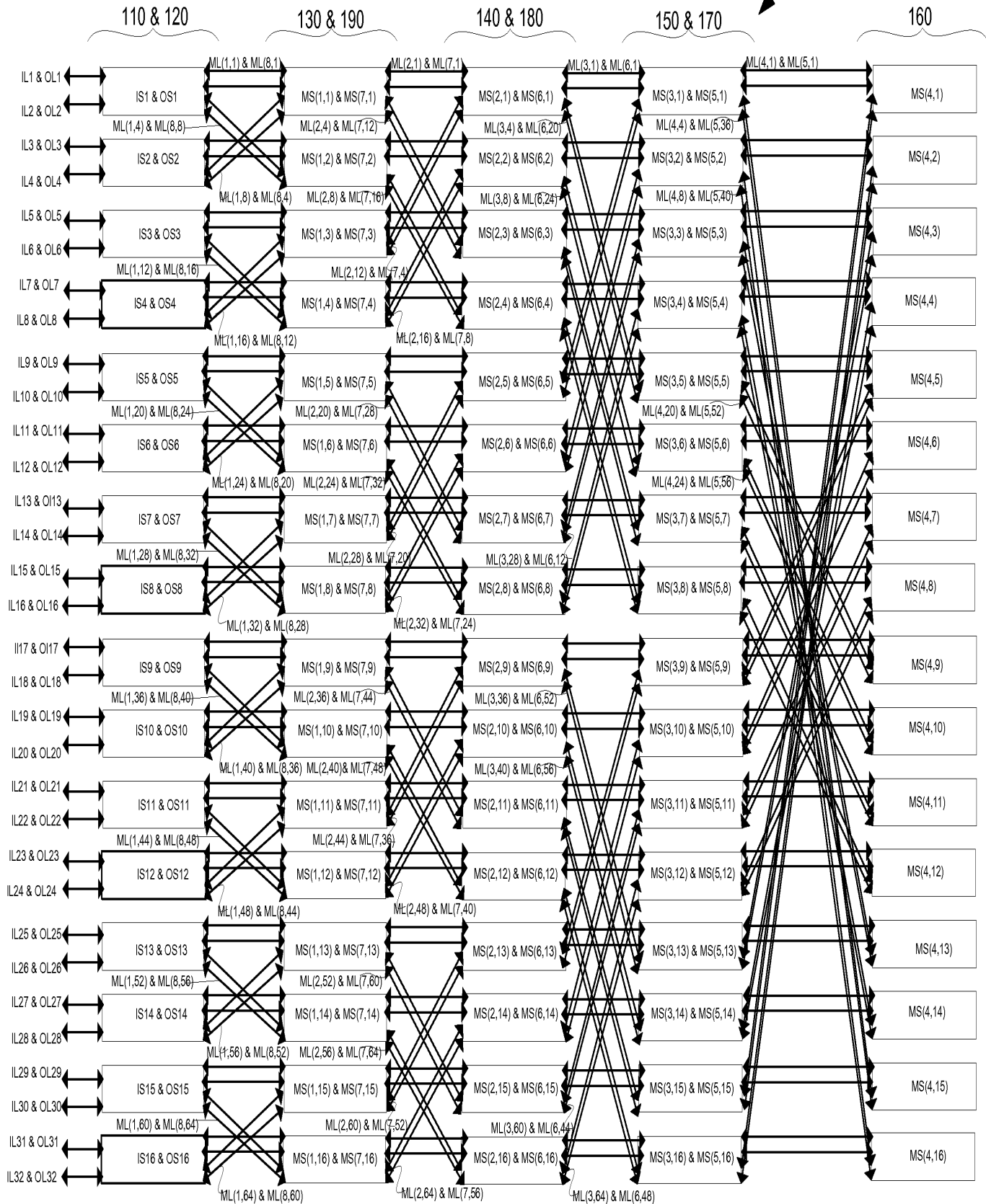


FIG. 3B

300B



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300C

FIG. 3C

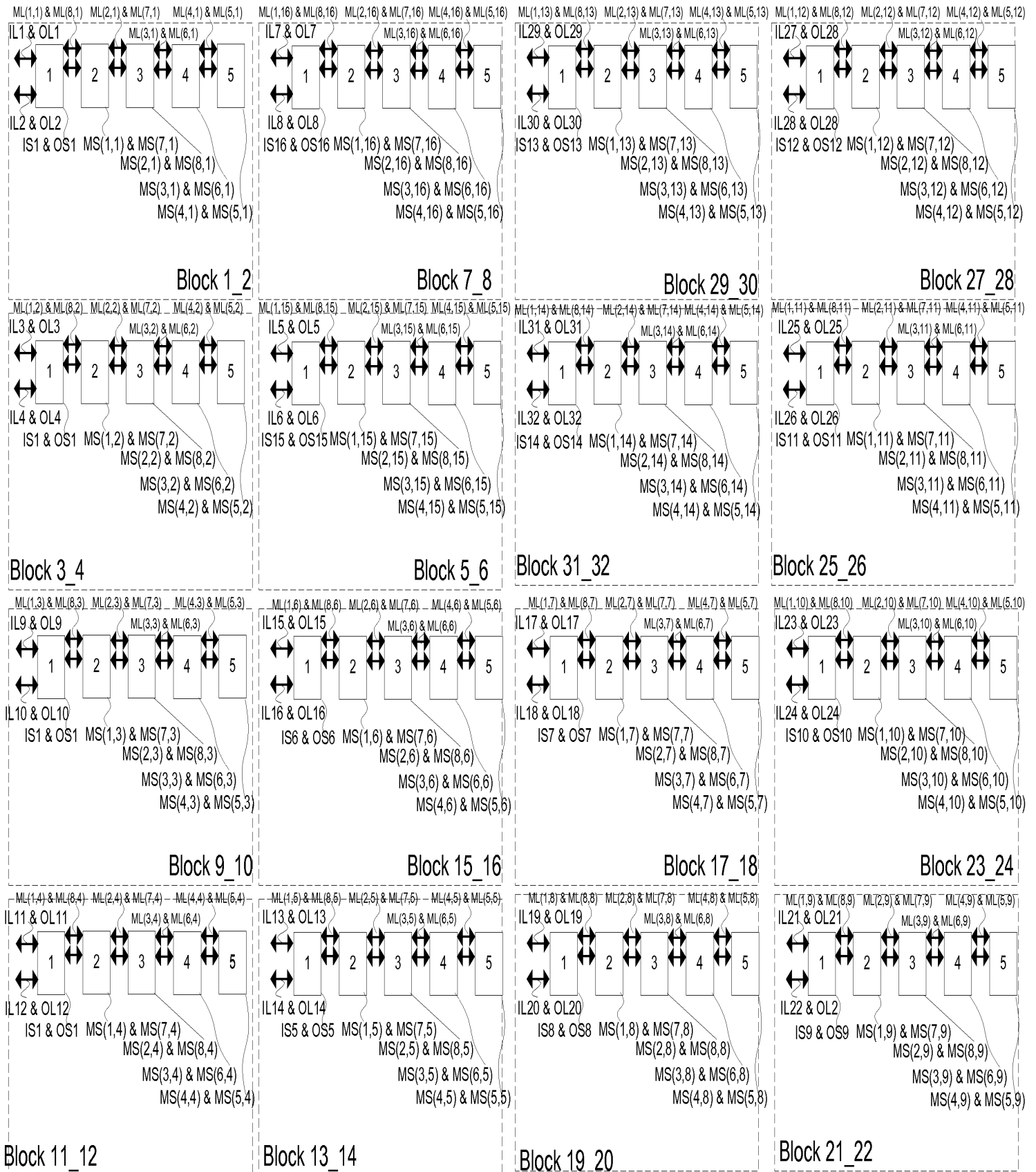


FIG. 3D

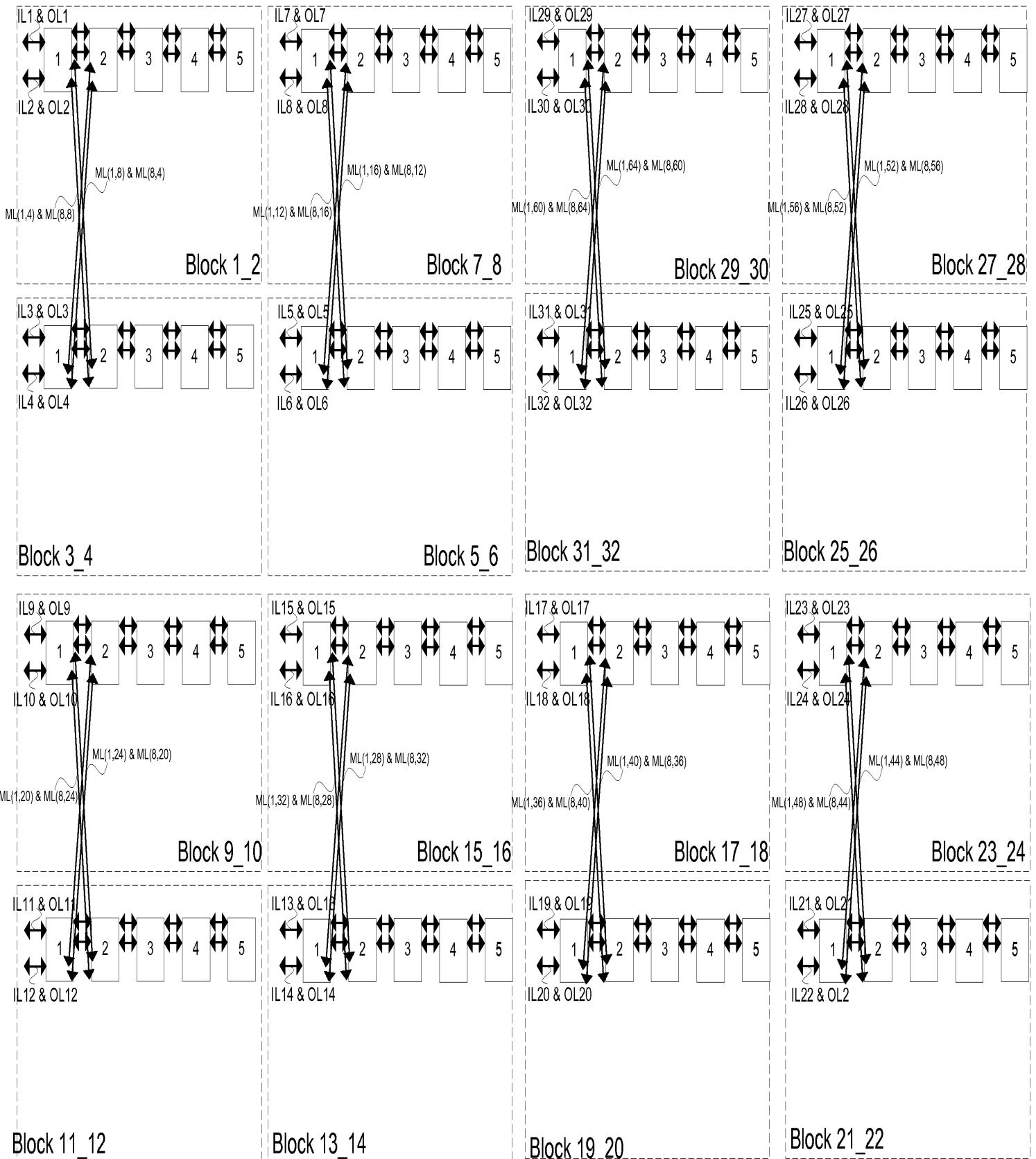




FIG. 3E

300E

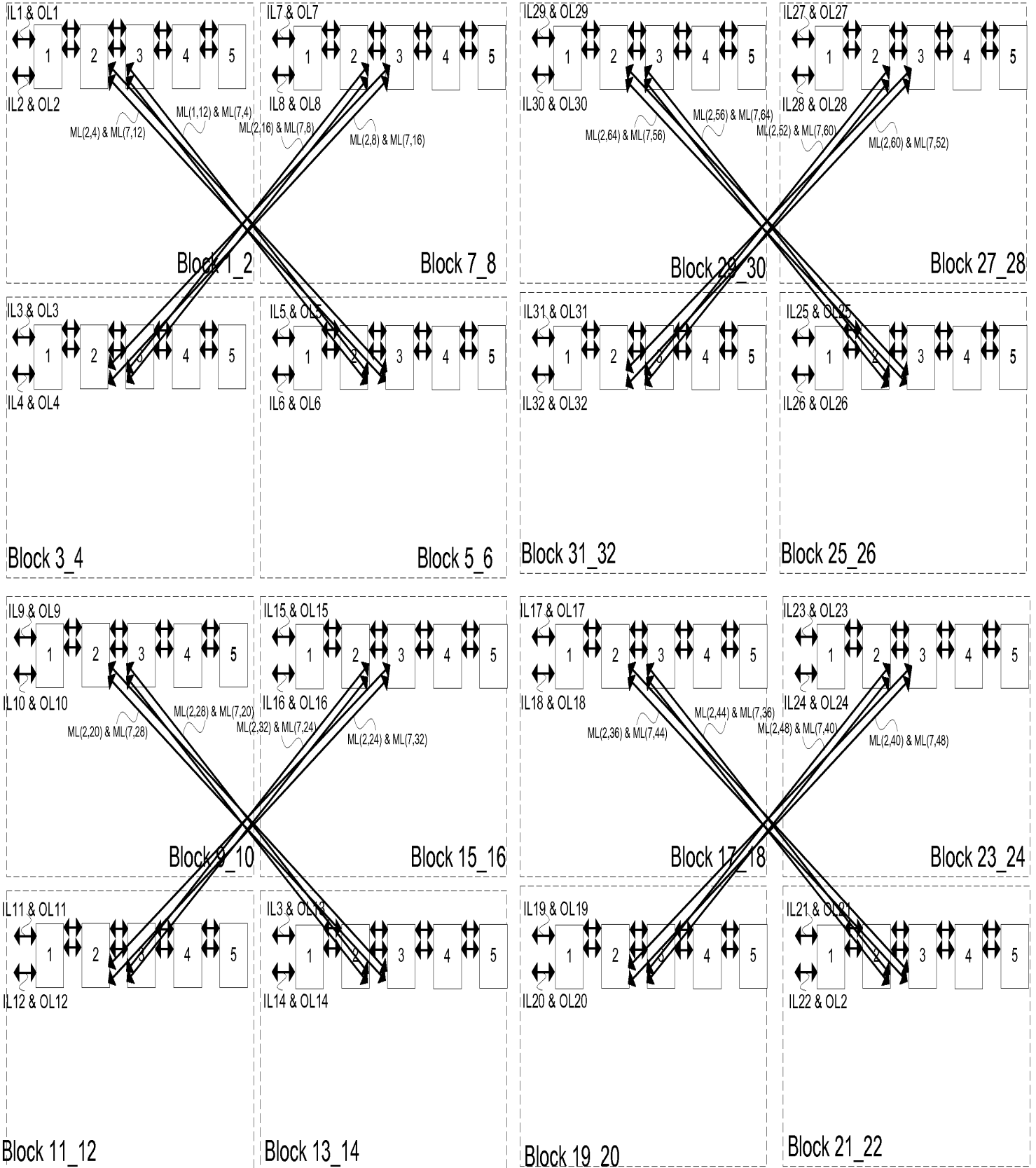


FIG. 3F

300F

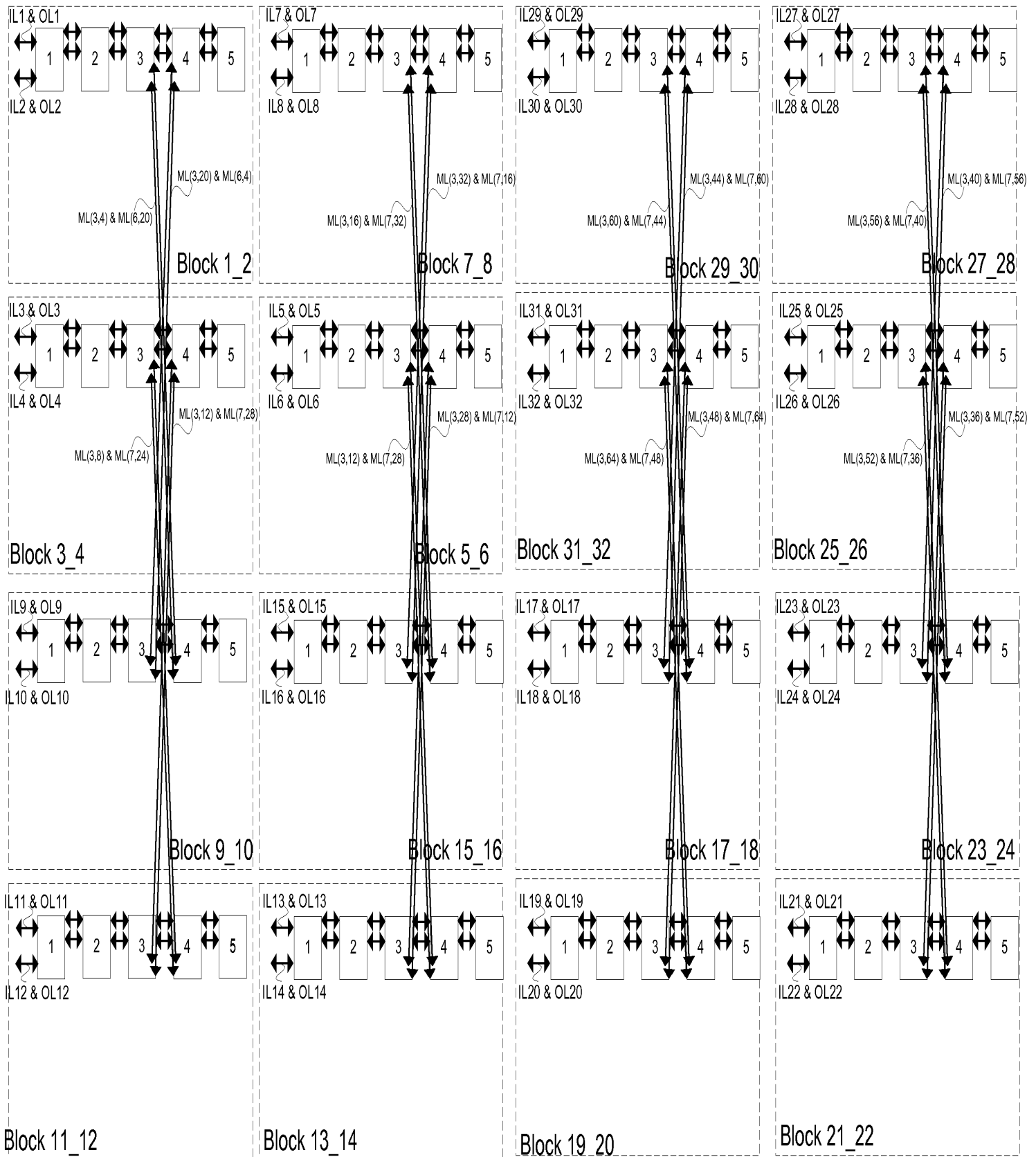
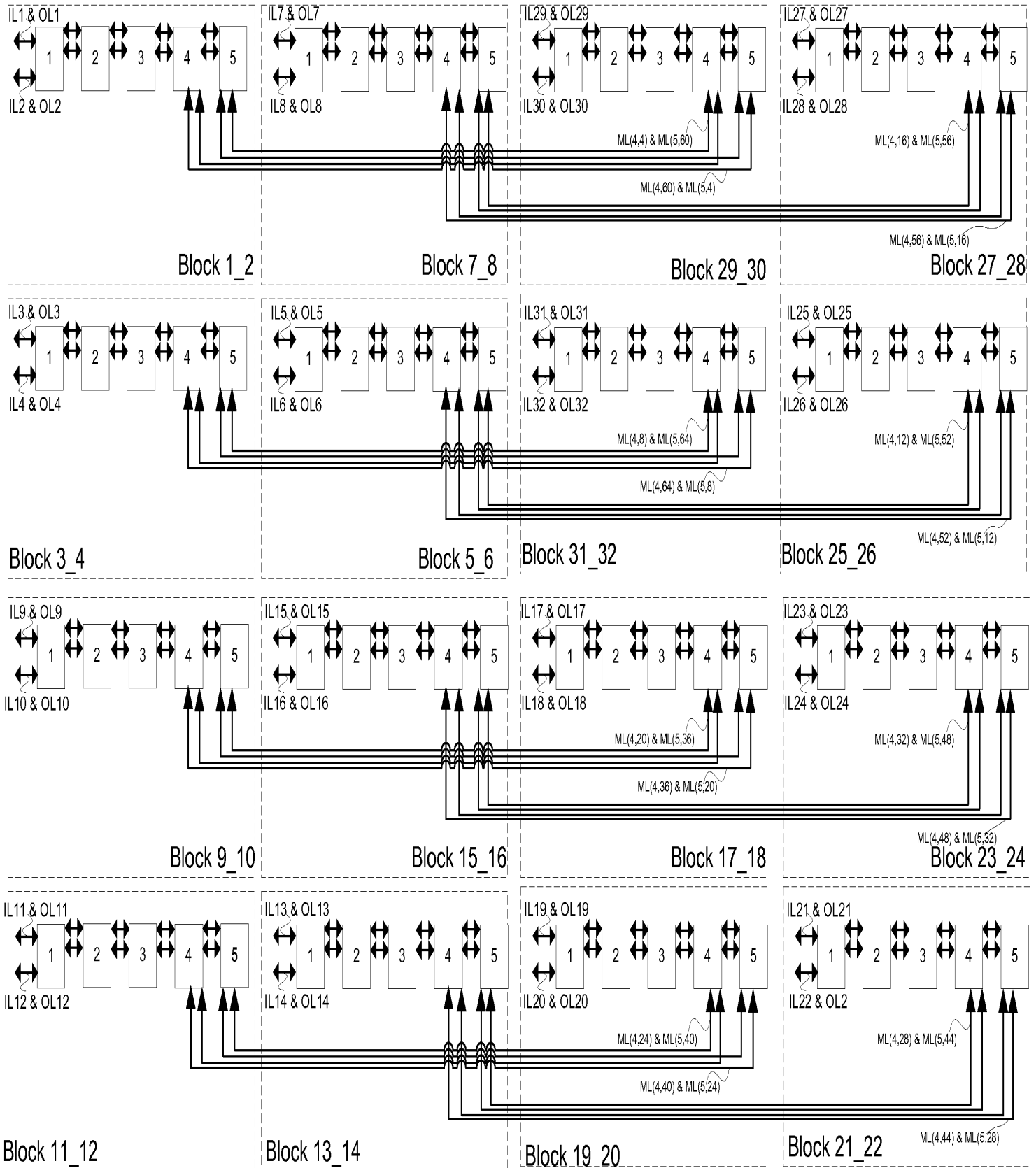


FIG. 3G

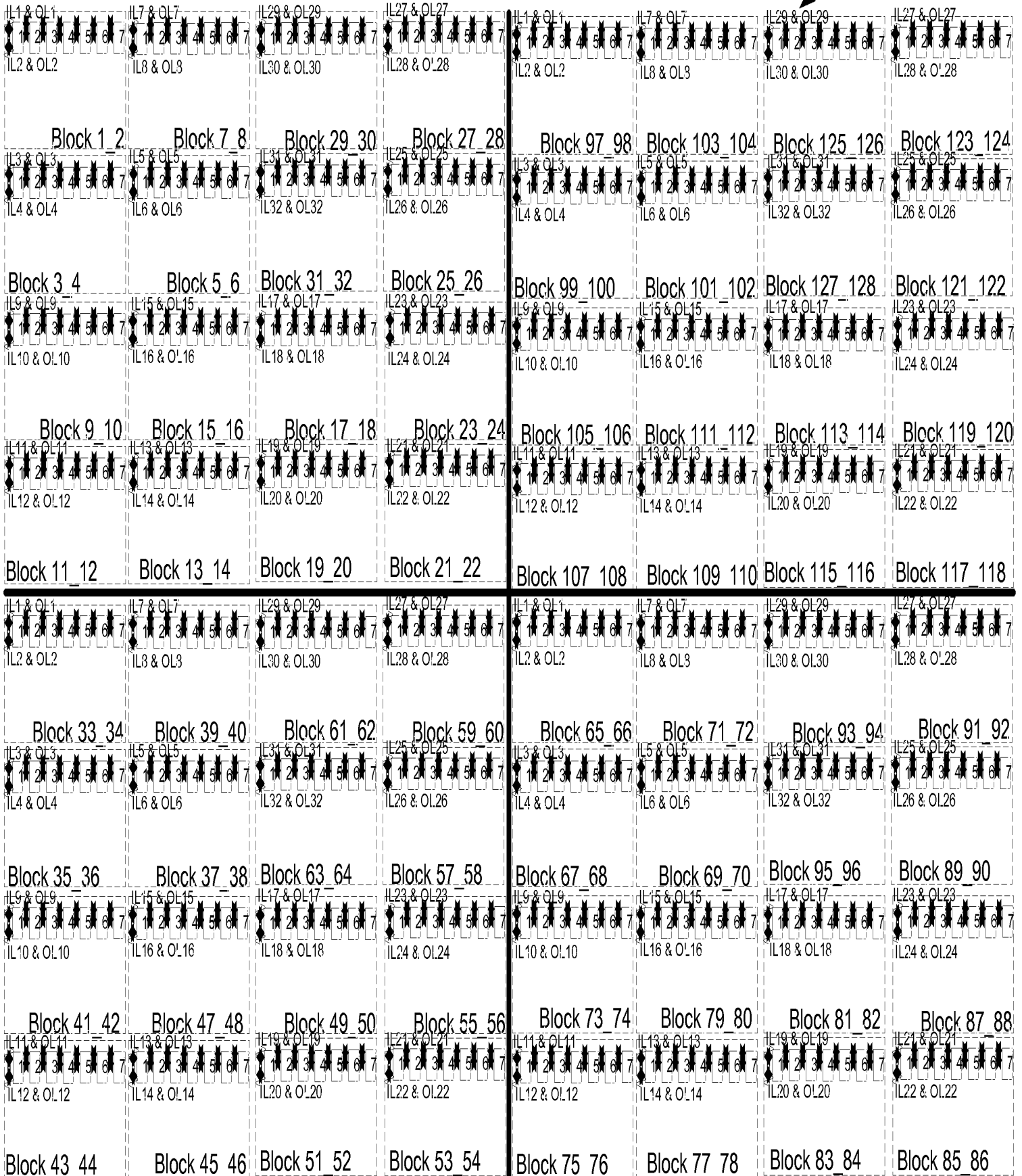
300G



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FIG. 3H

300H



400A

FIG. 4A

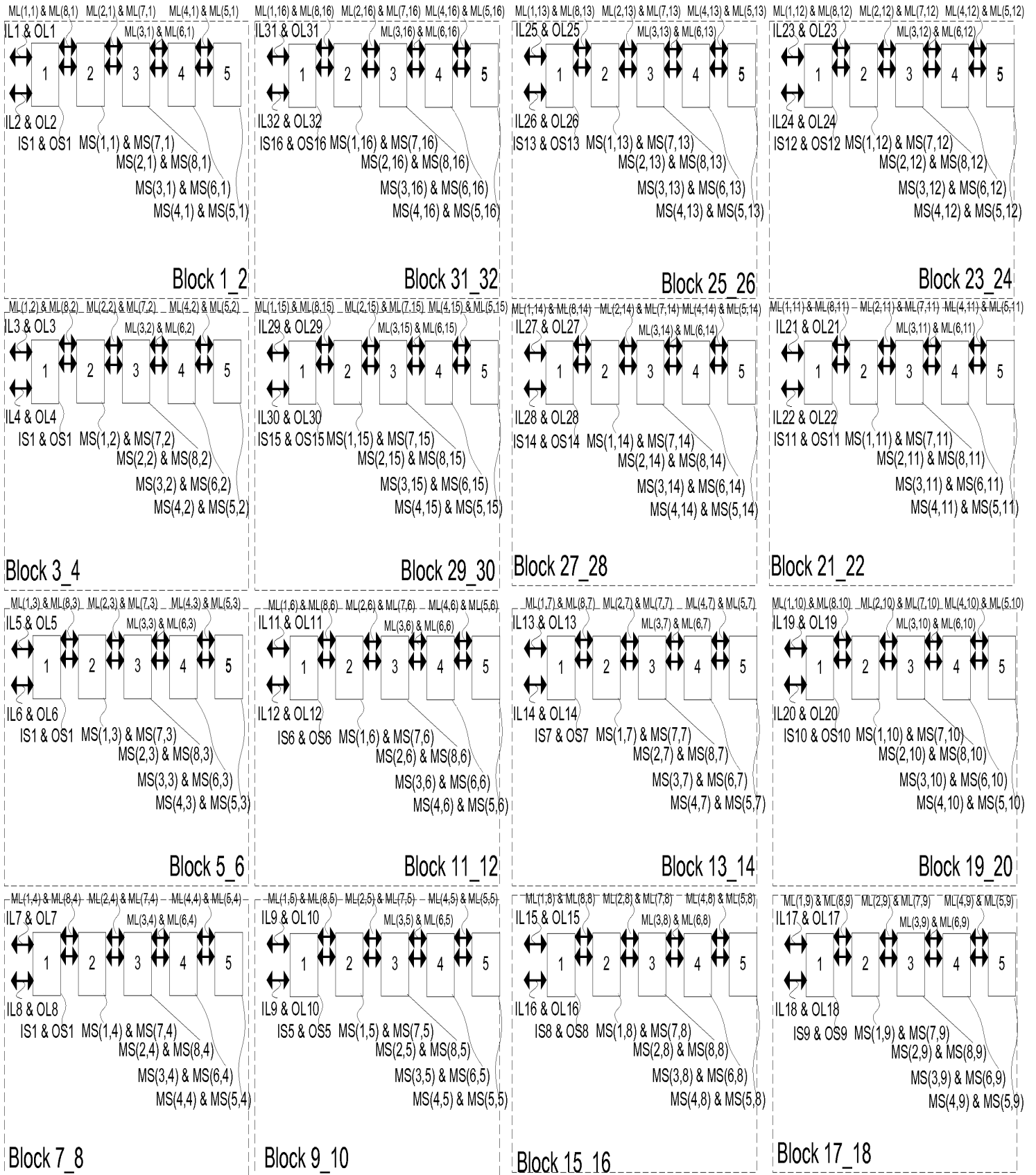


FIG. 4B

400B

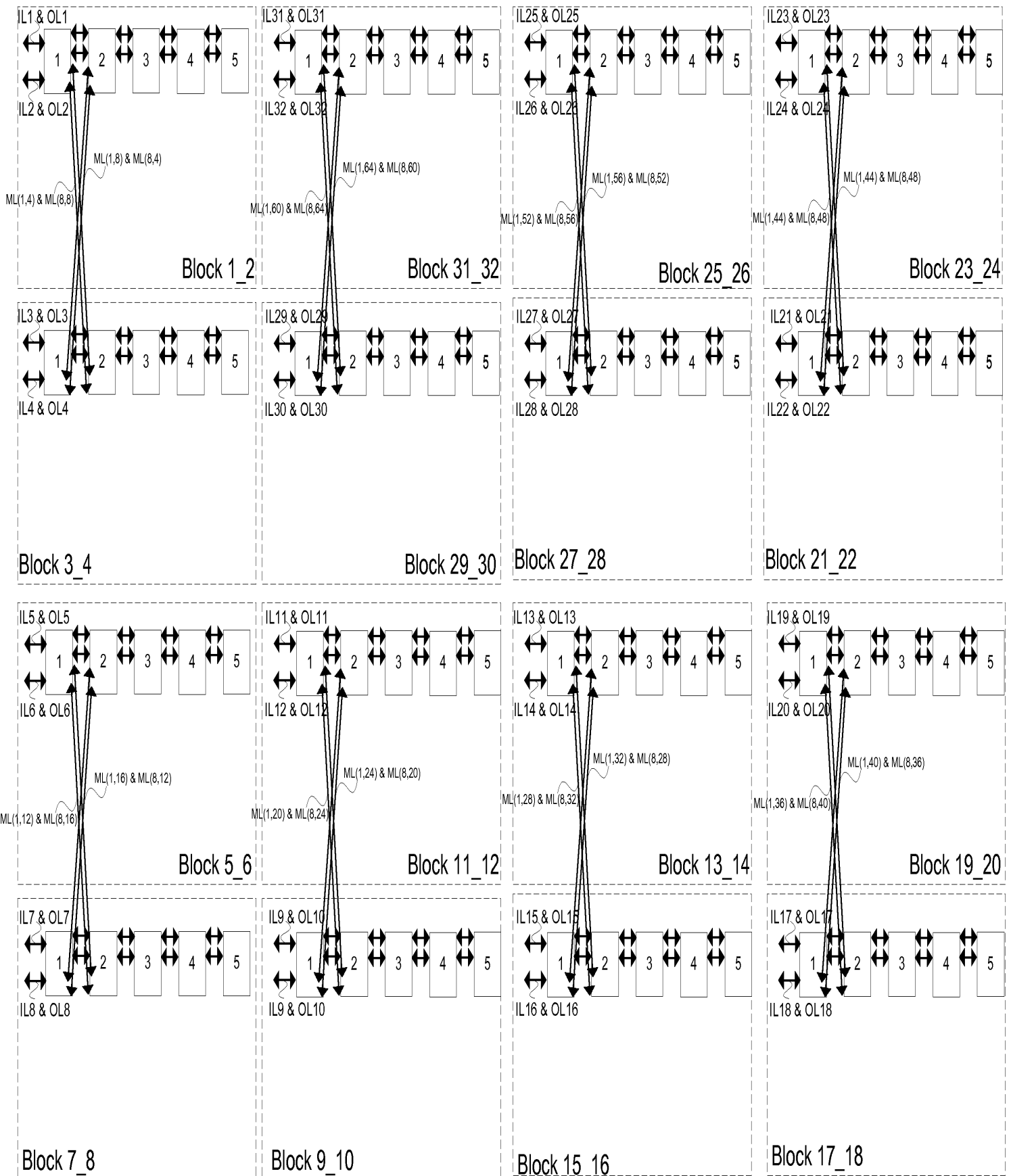


FIG. 4C

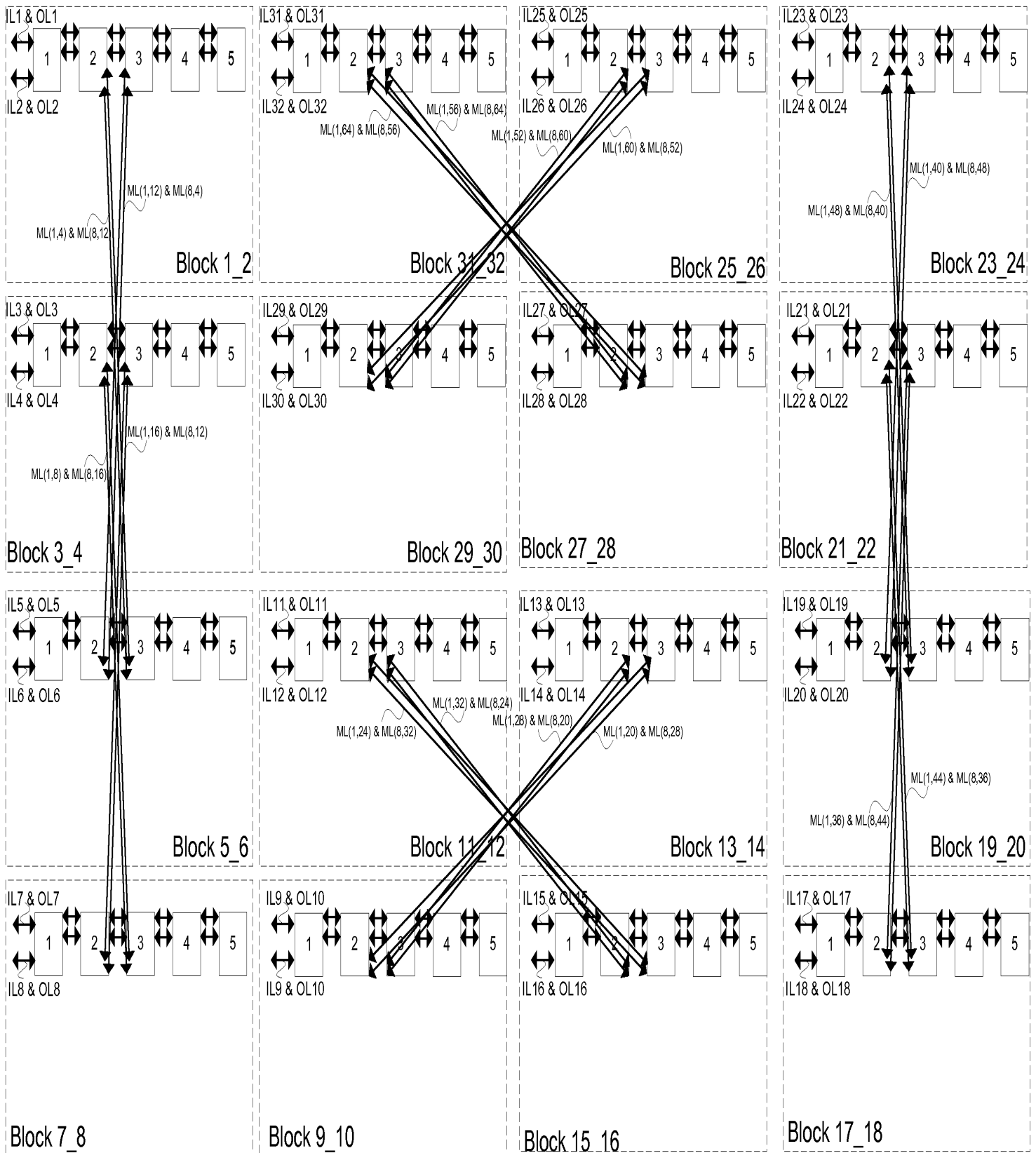


FIG. 4D

400D

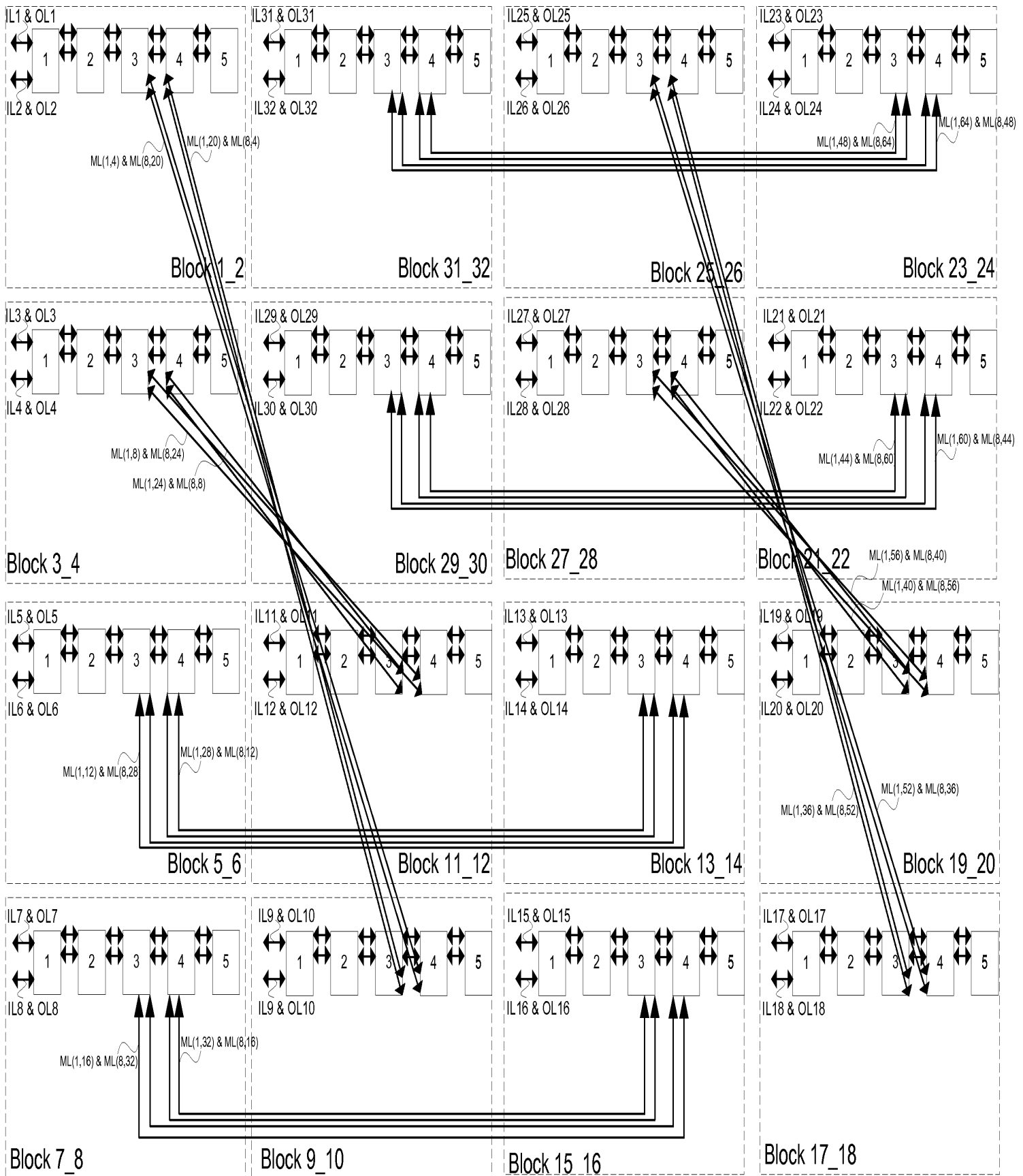




FIG. 4E

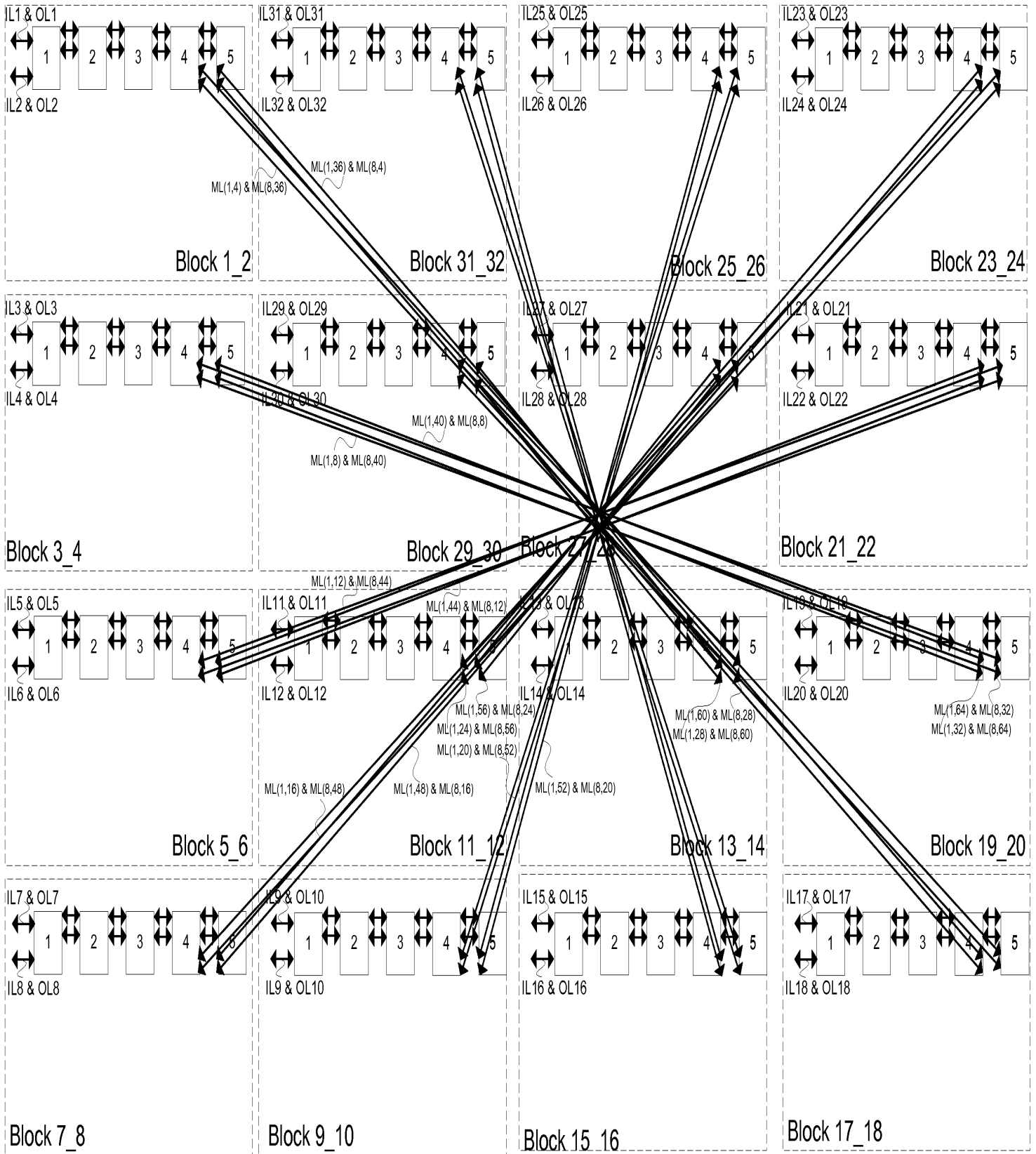
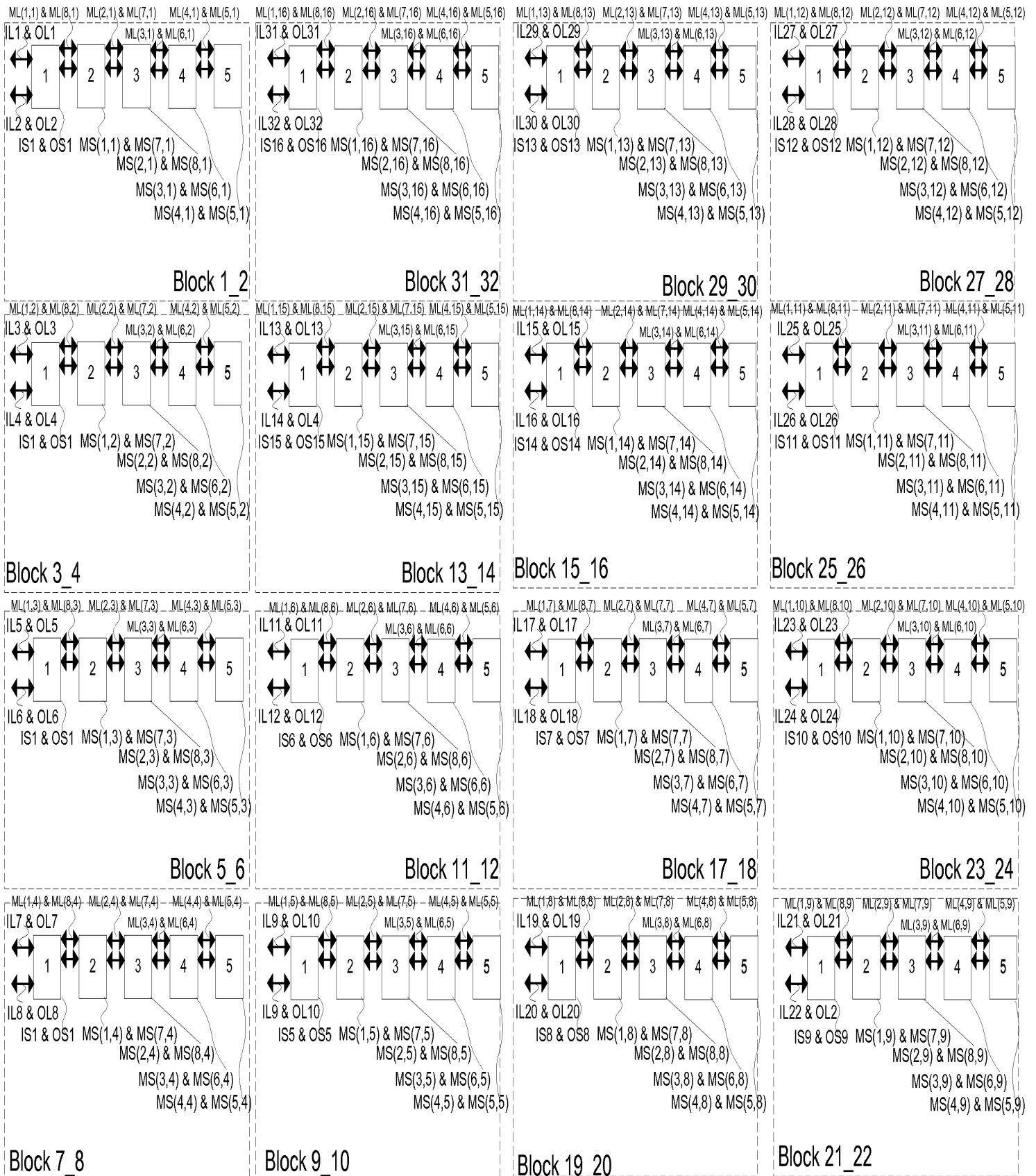
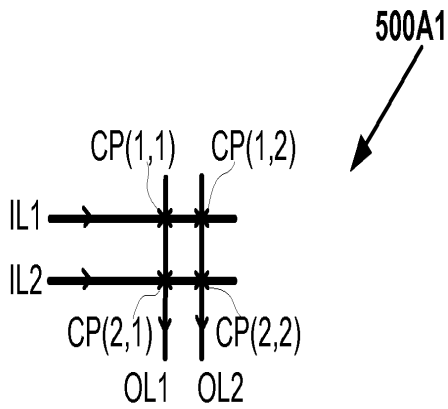


FIG. 4C1

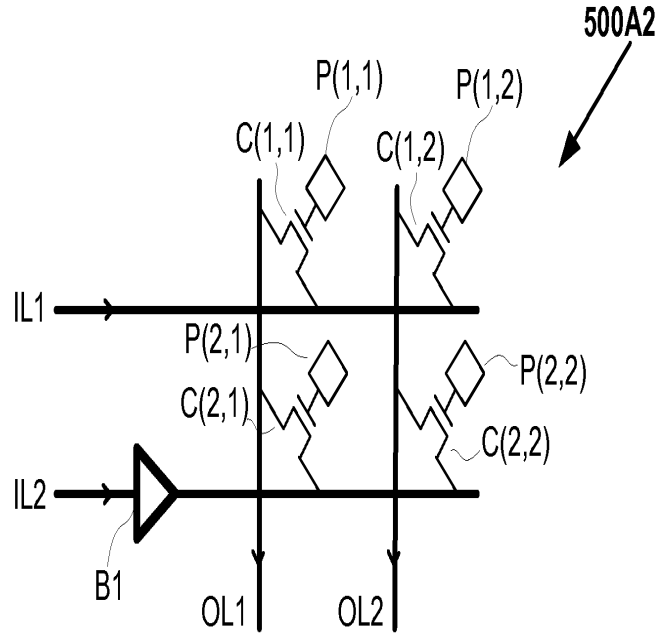
400C1



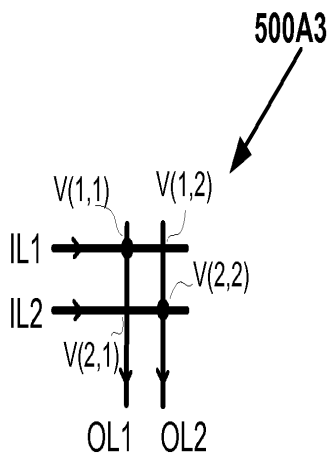
**FIG. 5A**



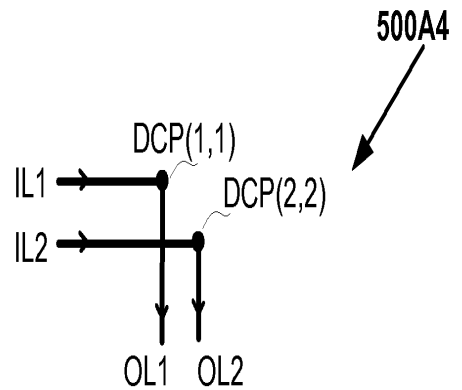
**FIG. 5A1**  
**(Prior Art)**



**FIG. 5A2**  
**(Prior Art)**



**FIG. 5A3**  
**(Prior Art)**



**FIG. 5A4**

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Way, San Jose, CA 95135 (US).

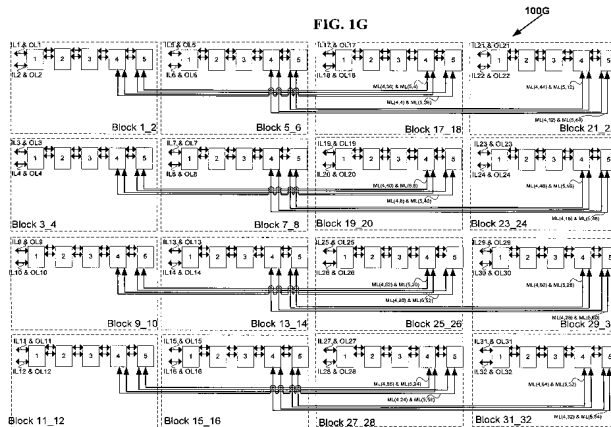
AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

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(54) Title: VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS



(57) Abstract: In accordance with the invention, VLSI layouts of generalized multi-stage networks for broadcast, unicast and multicast connections are presented using only horizontal and vertical links. The VLSI layouts employ shuffle exchange links where outlet links of cross links from switches in a stage in one sub-integrated circuit block are connected to inlet links of switches in the succeeding stage in another sub-integrated circuit block so that said cross links are either vertical links or horizontal and vice versa. In one embodiment the sub-integrated circuit blocks are arranged in a hypercube arrangement in a two-dimensional plane. The VLSI layouts exploit the benefits of significantly lower cross points, lower signal latency, lower power and full connectivity with significantly fast compilation.



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**VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS****Venkat Konda**

## 5 CROSS REFERENCE TO RELATED APPLICATIONS

This application is Continuation In Part PCT Application to and incorporates by reference in its entirety the U.S. Provisional Patent Application Serial No. 60/940, 394 entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25,  
10 2007.

This application is related to and incorporates by reference in its entirety the PCT Application Serial No. PCT/US08/56064 entitled "FULLY CONNECTED GENERALIZED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed March 6, 2008, the U.S. Provisional Patent  
15 Application Serial No. 60/905,526 entitled "LARGE SCALE CROSSPOINT REDUCTION WITH NONBLOCKING UNICAST & MULTICAST IN ARBITRARILY LARGE MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed March 6, 2007, and the U.S. Provisional Patent Application Serial No. 60/940, 383 entitled "FULLY CONNECTED  
20 GENERALIZED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

This application is related to and incorporates by reference in its entirety the PCT Application Docket No. S-0038PCT entitled "FULLY CONNECTED GENERALIZED BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same  
25 assignee as the current application, filed concurrently, the U.S. Provisional Patent Application Serial No. 60/940, 387 entitled "FULLY CONNECTED GENERALIZED BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same

assignee as the current application, filed May 25, 2007, and the U.S. Provisional Patent Application Serial No. 60/940, 390 entitled "FULLY CONNECTED GENERALIZED MULTI-LINK BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007

5           This application is related to and incorporates by reference in its entirety the PCT Application Docket No. S-0039PCT entitled "FULLY CONNECTED GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed concurrently, the U.S. Provisional Patent Application Serial No. 60/940, 389 entitled "FULLY CONNECTED GENERALIZED  
10 REARRANGEABLY NONBLOCKING MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007, the U.S. Provisional Patent Application Serial No. 60/940, 391 entitled "FULLY CONNECTED GENERALIZED FOLDED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007 and  
15 the U.S. Provisional Patent Application Serial No. 60/940, 392 entitled "FULLY CONNECTED GENERALIZED STRICTLY NONBLOCKING MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

          This application is related to and incorporates by reference in its entirety the U.S.  
20 Provisional Patent Application Serial No. 60/984, 724 entitled "VLSI LAYOUTS OF FULLY CONNECTED NETWORKS WITH LOCALITY EXPLOITATION" by Venkat Konda assigned to the same assignee as the current application, filed November 2, 2007.

          This application is related to and incorporates by reference in its entirety the U.S.  
Provisional Patent Application Serial No. 61/018, 494 entitled "VLSI LAYOUTS OF  
25 FULLY CONNECTED GENERALIZED AND PYRAMID NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed January 1, 2008.

## BACKGROUND OF INVENTION

Multi-stage interconnection networks such as Benes networks and butterfly fat tree networks are widely useful in telecommunications, parallel and distributed computing. However VLSI layouts, known in the prior art, of these interconnection  
5 networks in an integrated circuit are inefficient and complicated.

Other multi-stage interconnection networks including butterfly fat tree networks, Banyan networks, Batcher-Banyan networks, Baseline networks, Delta networks, Omega networks and Flip networks have been widely studied particularly for self routing packet switching applications. Also Benes Networks with radix of two have been widely studied  
10 and it is known that Benes Networks of radix two are shown to be built with back to back baseline networks which are rearrangeably nonblocking for unicast connections.

The most commonly used VLSI layout in an integrated circuit is based on a two-dimensional grid model comprising only horizontal and vertical tracks. An intuitive interconnection network that utilizes two-dimensional grid model is 2D Mesh Network  
15 and its variations such as segmented mesh networks. Hence routing networks used in VLSI layouts are typically 2D mesh networks and its variations. However Mesh Networks require large scale cross points typically with a growth rate of  $O(N^2)$  where  $N$  is the number of computing elements, ports, or logic elements depending on the application.

20 Multi-stage interconnection with a growth rate of  $O(N \times \log N)$  requires significantly small number of cross points. U.S. Patent 6,185,220 entitled "Grid Layouts of Switching and Sorting Networks" granted to Muthukrishnan et al. describes a VLSI layout using existing VLSI grid model for Benes and Butterfly networks. U.S. Patent 6,940,308 entitled "Interconnection Network for a Field Programmable Gate Array"  
25 granted to Wong describes a VLSI layout where switches belonging to lower stage of Benes Network are layed out close to the logic cells and switches belonging to higher stages are layed out towards the center of the layout.

Due to the inefficient and in some cases impractical VLSI layout of Benes and butterfly fat tree networks on a semiconductor chip, today mesh networks and segmented mesh networks are widely used in the practical applications such as field programmable gate arrays (FPGAs), programmable logic devices (PLDs), and parallel computing interconnects. The prior art VLSI layouts of Benes and butterfly fat tree networks and VLSI layouts of mesh networks and segmented mesh networks require large area to implement the switches on the chip, large number of wires, longer wires, with increased power consumption, increased latency of the signals which effect the maximum clock speed of operation. Some networks may not even be implemented practically on a chip due to the lack of efficient layouts.

#### SUMMARY OF INVENTION

When large scale sub-integrated circuit blocks with inlet and outlet links are layed out in an integrated circuit device in a two-dimensional grid arrangement, (for example in an FPGA where the sub-integrated circuit blocks are Lookup Tables) the most intuitive routing network is a network that uses horizontal and vertical links only (the most often used such a network is one of the variations of a 2D Mesh network). A direct embedding of a generalized multi-stage network on to a 2D Mesh network is neither simple nor efficient.

In accordance with the invention, VLSI layouts of generalized multi-stage networks for broadcast, unicast and multicast connections are presented using only horizontal and vertical links. The VLSI layouts employ shuffle exchange links where outlet links of cross links from switches in a stage in one sub-integrated circuit block are connected to inlet links of switches in the succeeding stage in another sub-integrated circuit block so that said cross links are either vertical links or horizontal and vice versa. In one embodiment the sub-integrated circuit blocks are arranged in a hypercube arrangement in a two-dimensional plane. The VLSI layouts exploit the benefits of significantly lower cross points, lower signal latency, lower power and full connectivity with significantly fast compilation.



The VLSI layouts presented are applicable to generalized multi-stage networks  $V(N_1, N_2, d, s)$ , generalized folded multi-stage networks  $V_{fold}(N_1, N_2, d, s)$ , generalized butterfly fat tree networks  $V_{bft}(N_1, N_2, d, s)$ , generalized multi-link multi-stage networks  $V_{mlink}(N_1, N_2, d, s)$ , generalized folded multi-link multi-stage networks  $V_{fold-mlink}(N_1, N_2, d, s)$ , generalized multi-link butterfly fat tree networks  $V_{mlink-bft}(N_1, N_2, d, s)$ , and generalized hypercube networks  $V_{cube}(N_1, N_2, d, s)$  for  $s = 1, 2, 3$  or any number in general. The embodiments of VLSI layouts are useful in wide target applications such as FPGAs, CPLDs, pSoCs, ASIC placement and route tools, networking applications, parallel & distributed computing, and reconfigurable computing.

10

#### BRIEF DESCRIPTION OF DRAWINGS

FIG. 1A is a diagram 100A of an exemplary symmetrical multi-link multi-stage network  $V_{fold-mlink}(N, d, s)$  having inverse Benes connection topology of nine stages with  $N = 32$ ,  $d = 2$  and  $s=2$ , strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1B is a diagram 100B of the equivalent symmetrical folded multi-link multi-stage network  $V_{fold-mlink}(N, d, s)$  of the network 100A shown in FIG. 1A, having inverse Benes connection topology of five stages with  $N = 32$ ,  $d = 2$  and  $s=2$ , strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1C is a diagram 100C layout of the network  $V_{fold-mlink}(N, d, s)$  shown in FIG. 1B, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 1D is a diagram 100D layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 1B, in one embodiment, illustrating the connection links ML(1,i) for  $i = [1, 64]$  and ML(8,i) for  $i = [1, 64]$ .

FIG. 1E is a diagram 100E layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 1B, in one embodiment, illustrating the connection links ML(2,i) for  $i = [1, 64]$  and ML(7,i) for  $i = [1, 64]$ .

FIG. 1F is a diagram 100F layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 1B, in one embodiment, illustrating the connection links ML(3,i) for  $i = [1, 64]$  and ML(6,i) for  $i = [1, 64]$ .

FIG. 1G is a diagram 100G layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 1B, in one embodiment, illustrating the connection links ML(4,i) for  $i = [1, 64]$  and ML(5,i) for  $i = [1, 64]$ .

FIG. 1H is a diagram 100H layout of a network  $V_{fold-link}(N, d, s)$  where  $N = 128$ ,  $d = 2$ , and  $s = 2$ , in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 1I is a diagram 100I detailed connections of BLOCK 1\_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing  $V(N, d, s)$  or  $V_{fold}(N, d, s)$ .

FIG. 1J is a diagram 100J detailed connections of BLOCK 1\_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing  $V(N, d, s)$  or  $V_{fold}(N, d, s)$ .

FIG. 1K is a diagram 100K detailed connections of BLOCK 1\_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing  $V(N, d, s)$  or  $V_{fold}(N, d, s)$ .

FIG. 1K1 is a diagram 100M1 detailed connections of BLOCK 1\_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing  $V(N, d, s)$  or  $V_{fold}(N, d, s)$  for  $s = 1$ .

FIG. 1L is a diagram 100L detailed connections of BLOCK 1\_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing  $V(N, d, s)$  or  $V_{fold}(N, d, s)$ .

FIG. 1L1 is a diagram 100L1 detailed connections of BLOCK 1\_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing  $V(N, d, s)$  or  $V_{fold}(N, d, s)$  for  $s = 1$ .

FIG. 2A1 is a diagram 200A1 of an exemplary symmetrical multi-link multi-stage network  $V_{fold-link}(N, d, s)$  having inverse Benes connection topology of one stage with  $N = 2$ ,  $d = 2$  and  $s=2$ , strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention. FIG. 2A2 is a diagram 200A2 of the equivalent symmetrical folded multi-link multi-stage network  $V_{fold-link}(N, d, s)$  of the network 200A1 shown in FIG. 2A1, having inverse Benes connection topology of one stage with  $N = 2$ ,  $d = 2$  and  $s=2$ , strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention. FIG. 2A3 is a diagram 200A3 layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 2A2, in one embodiment, illustrating all the connection links.

FIG. 2B1 is a diagram 200B1 of an exemplary symmetrical multi-link multi-stage network  $V_{fold-link}(N, d, s)$  having inverse Benes connection topology of one stage with  $N = 4$ ,  $d = 2$  and  $s=2$ , strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention. FIG. 2B2 is a diagram 200B2 of the equivalent symmetrical folded multi-link multi-stage network  $V_{fold-link}(N, d, s)$  of the network

200B1 shown in FIG. 2B1, having inverse Benes connection topology of one stage with  $N = 4$ ,  $d = 2$  and  $s=2$ , strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention. FIG. 2B3 is a diagram 200B3 layout of the network

5  $V_{fold-link}(N, d, s)$  shown in FIG. 2B2, in one embodiment, illustrating the connection links belonging with in each block only. FIG. 2B4 is a diagram 200B4 layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 2B2, in one embodiment, illustrating the connection links ML(1,i) for  $i = [1, 8]$  and ML(2,i) for  $i = [1,8]$ .

FIG. 2C11 is a diagram 200C11 of an exemplary symmetrical multi-link multi-

10 stage network  $V_{fold-link}(N, d, s)$  having inverse Benes connection topology of one stage with  $N = 8$ ,  $d = 2$  and  $s=2$ , strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention. FIG. 2C12 is a diagram 200C12 of the equivalent symmetrical folded multi-link multi-stage network  $V_{fold-link}(N, d, s)$  of the network

15 200C11 shown in FIG. 2C11, having inverse Benes connection topology of one stage with  $N = 8$ ,  $d = 2$  and  $s=2$ , strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 2C21 is a diagram 200C21 layout of the network  $V_{fold-link}(N, d, s)$  shown in

20 FIG. 2C12, in one embodiment, illustrating the connection links belonging with in each block only. FIG. 2C22 is a diagram 200C22 layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 2C12, in one embodiment, illustrating the connection links ML(1,i) for  $i = [1, 16]$  and ML(4,i) for  $i = [1,16]$ . FIG. 2C23 is a diagram 200C23 layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 2C12, in one embodiment, illustrating the connection

25 links ML(2,i) for  $i = [1, 16]$  and ML(3,i) for  $i = [1,16]$ .

FIG. 2D1 is a diagram 200D1 of an exemplary symmetrical multi-link multi-stage network  $V_{fold-link}(N, d, s)$  having inverse Benes connection topology of one stage with  $N = 16$ ,  $d = 2$  and  $s=2$ , strictly nonblocking network for unicast connections and

rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 2D2 is a diagram 200D2 of the equivalent symmetrical folded multi-link multi-stage network  $V_{fold-link}(N, d, s)$  of the network 200D1 shown in FIG. 2D1, having  
 5 inverse Benes connection topology of one stage with  $N = 16$ ,  $d = 2$  and  $s=2$ , strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 2D3 is a diagram 200D3 layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 2D2, in one embodiment, illustrating the connection links belonging with in each  
 10 block only.

FIG. 2D4 is a diagram 200D4 layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 2D2, in one embodiment, illustrating the connection links  $ML(1,i)$  for  $i = [1, 32]$  and  $ML(6,i)$  for  $i = [1,32]$ .

FIG. 2D5 is a diagram 200D5 layout of the network  $V_{fold-link}(N, d, s)$  shown in  
 15 FIG. 2D2, in one embodiment, illustrating the connection links  $ML(2,i)$  for  $i = [1, 32]$  and  $ML(5,i)$  for  $i = [1,32]$ .

FIG. 2D6 is a diagram 200D6 layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 2D2, in one embodiment, illustrating the connection links  $ML(3,i)$  for  $i = [1, 32]$  and  $ML(4,i)$  for  $i = [1,32]$ .

20 FIG. 3A is a diagram 300A of an exemplary symmetrical multi-link multi-stage network  $V_{cube}(N, d, s)$  having inverse Benes connection topology of nine stages with  $N = 32$ ,  $d = 2$  and  $s=2$ , strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

25 FIG. 3B is a diagram 300B of the equivalent symmetrical folded multi-link multi-stage network  $V_{cube}(N, d, s)$  of the network 300A shown in FIG. 3A, having inverse

Benes connection topology of five stages with  $N = 32$ ,  $d = 2$  and  $s=2$ , strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 3C is a diagram 300C layout of the network  $V_{hcube}(N, d, s)$  shown in FIG. 3B, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 3D is a diagram 100D layout of the network  $V_{hcube}(N, d, s)$  shown in FIG. 3B, in one embodiment, illustrating the connection links  $ML(1,i)$  for  $i = [1, 64]$  and  $ML(8,i)$  for  $i = [1,64]$ .

FIG. 3E is a diagram 300E layout of the network  $V_{hcube}(N, d, s)$  shown in FIG. 3B, in one embodiment, illustrating the connection links  $ML(2,i)$  for  $i = [1, 64]$  and  $ML(7,i)$  for  $i = [1,64]$ .

FIG. 3F is a diagram 300F layout of the network  $V_{hcube}(N, d, s)$  shown in FIG. 3B, in one embodiment, illustrating the connection links  $ML(3,i)$  for  $i = [1, 64]$  and  $ML(6,i)$  for  $i = [1,64]$ .

FIG. 3G is a diagram 300G layout of the network  $V_{hcube}(N, d, s)$  shown in FIG. 3B, in one embodiment, illustrating the connection links  $ML(4,i)$  for  $i = [1, 64]$  and  $ML(5,i)$  for  $i = [1,64]$ .

FIG. 3H is a diagram 300H layout of a network  $V_{hcube}(N, d, s)$  where  $N = 128$ ,  $d = 2$ , and  $s = 2$ , in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 4A is a diagram 400A layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 1B, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 4B is a diagram 400B layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 1B, in one embodiment, illustrating the connection links ML(1,i) for  $i = [1, 64]$  and ML(8,i) for  $i = [1, 64]$ .

FIG. 4C is a diagram 400C layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 4C, in one embodiment, illustrating the connection links ML(2,i) for  $i = [1, 64]$  and ML(7,i) for  $i = [1, 64]$ .

FIG. 4D is a diagram 400D layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 4D, in one embodiment, illustrating the connection links ML(3,i) for  $i = [1, 64]$  and ML(6,i) for  $i = [1, 64]$ .

FIG. 4E is a diagram 400E layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 4E, in one embodiment, illustrating the connection links ML(4,i) for  $i = [1, 64]$  and ML(5,i) for  $i = [1, 64]$ .

FIG. 4C1 is a diagram 400C1 layout of the network  $V_{fold-link}(N, d, s)$  shown in FIG. 1B, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 5A1 is a diagram 500A1 of an exemplary prior art implementation of a two by two switch; FIG. 5A2 is a diagram 500A2 for programmable integrated circuit prior art implementation of the diagram 500A1 of FIG. 5A1; FIG. 5A3 is a diagram 500A3 for one-time programmable integrated circuit prior art implementation of the diagram 500A1 of FIG. 5A1; FIG. 5A4 is a diagram 500A4 for integrated circuit placement and route implementation of the diagram 500A1 of FIG. 5A1.

#### DETAILED DESCRIPTION OF THE INVENTION

The present invention is concerned with the VLSI layouts of arbitrarily large switching networks for broadcast, unicast and multicast connections. Particularly switching networks considered in the current invention include: generalized multi-stage

networks  $V(N_1, N_2, d, s)$ , generalized folded multi-stage networks  $V_{fold}(N_1, N_2, d, s)$ , generalized butterfly fat tree networks  $V_{bft}(N_1, N_2, d, s)$ , generalized multi-link multi-stage networks  $V_{mlink}(N_1, N_2, d, s)$ , generalized folded multi-link multi-stage networks  $V_{fold-mlink}(N_1, N_2, d, s)$ , generalized multi-link butterfly fat tree networks  $V_{mlink-bft}(N_1, N_2, d, s)$ , and generalized hypercube networks  $V_{hcube}(N_1, N_2, d, s)$  for  $s = 1, 2, 3$  or any number in general.

Efficient VLSI layout of networks on a semiconductor chip are very important and greatly influence many important design parameters such as the area taken up by the network on the chip, total number of wires, length of the wires, latency of the signals, capacitance and hence the maximum clock speed of operation. Some networks may not even be implemented practically on a chip due to the lack of efficient layouts. The different varieties of multi-stage networks described above have not been implemented previously on the semiconductor chips efficiently. For example in Field Programmable Gate Array (FPGA) designs, multi-stage networks described in the current invention have not been successfully implemented primarily due to the lack of efficient VLSI layouts. Current commercial FPGA products such as Xilinx Vertex, Altera's Stratix implement island-style architecture using mesh and segmented mesh routing interconnects using either full crossbars or sparse crossbars. These routing interconnects consume large silicon area for crosspoints, long wires, large signal propagation delay and hence consume lot of power.

The current invention discloses the VLSI layouts of numerous types of multi-stage networks which are very efficient. Moreover they can be embedded on to mesh and segmented mesh routing interconnects of current commercial FPGA products. The VLSI layouts disclosed in the current invention are applicable to including the numerous generalized multi-stage networks disclosed in the following patent applications, filed concurrently:

1) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-stage networks  $V(N_1, N_2, d, s)$  with numerous connection



topologies and the scheduling methods are described in detail in the PCT Application Serial No. PCT/US08/56064 that is incorporated by reference above.

2) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized butterfly fat tree networks  $V_{bft}(N_1, N_2, d, s)$  with numerous  
 5 connection topologies and the scheduling methods are described in detail in U.S. Provisional Patent Application Serial No. 60/940, 387 that is incorporated by reference above.

3) Rearrangeably nonblocking for arbitrary fan-out multicast and unicast, and strictly nonblocking for unicast for generalized multi-link multi-stage networks  
 10  $V_{mlink}(N_1, N_2, d, s)$  and generalized folded multi-link multi-stage networks  $V_{fold-mlink}(N_1, N_2, d, s)$  with numerous connection topologies and the scheduling methods are described in detail in U.S. Provisional Patent Application Serial No. 60/940, 389 that is incorporated by reference above.

4) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-link butterfly fat tree networks  $V_{mlink-bft}(N_1, N_2, d, s)$  with  
 15 numerous connection topologies and the scheduling methods are described in detail in U.S. Provisional Patent Application Serial No. 60/940, 390 that is incorporated by reference above.

5) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized folded multi-stage networks  $V_{fold}(N_1, N_2, d, s)$  with numerous  
 20 connection topologies and the scheduling methods are described in detail in U.S. Provisional Patent Application Serial No. 60/940, 391 that is incorporated by reference above.

6) Strictly nonblocking for arbitrary fan-out multicast for generalized multi-link multi-stage networks  $V_{mlink}(N_1, N_2, d, s)$  and generalized folded multi-link multi-stage  
 25 networks  $V_{fold-mlink}(N_1, N_2, d, s)$  with numerous connection topologies and the scheduling

methods are described in detail in U.S. Provisional Patent Application Serial No. 60/940, 392 that is incorporated by reference above.

7) VLSI layouts of numerous types of multi-stage networks with locality exploitation are described in U.S. Provisional Patent Application Serial No. 60/984, 724  
5 that is incorporated by reference above.

8) VLSI layouts of numerous types of multistage pyramid networks are described in U.S. Provisional Patent Application Serial No. 61/018, 494 that is incorporated by reference above.

In addition the layouts of the current invention are also applicable to generalized  
10 multi-stage pyramid networks  $V_p(N_1, N_2, d, s)$ , generalized folded multi-stage pyramid networks  $V_{fold-p}(N_1, N_2, d, s)$ , generalized butterfly fat pyramid networks  $V_{bfp}(N_1, N_2, d, s)$ , generalized multi-link multi-stage pyramid networks  $V_{mlink-p}(N_1, N_2, d, s)$ , generalized folded multi-link multi-stage pyramid networks  $V_{fold-mlink-p}(N_1, N_2, d, s)$ , generalized multi-link butterfly fat pyramid networks  
15  $V_{mlink-bfp}(N_1, N_2, d, s)$ , and generalized hypercube networks  $V_{hcube}(N_1, N_2, d, s)$  for  $s = 1, 2, 3$  or any number in general.

**Symmetric RNB generalized multi-link multi-stage network  $V_{mlink}(N_1, N_2, d, s)$ :**

Referring to diagram 100A in FIG. 1A, in one embodiment, an exemplary  
20 generalized multi-link multi-stage network  $V_{mlink}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$  with nine stages of one hundred and forty four switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, 150, 160, 170, 180 and 190 is shown where input stage 110  
25 consists of sixteen, two by four switches IS1-IS16 and output stage 120 consists of sixteen, four by two switches OS1-OS16. And all the middle stages namely the middle

stage 130 consists of sixteen, four by four switches MS(1,1) - MS(1,16), middle stage 140 consists of sixteen, four by four switches MS(2,1) - MS(2,16), middle stage 150 consists of sixteen, four by four switches MS(3,1) - MS(3,16), middle stage 160 consists of sixteen, four by four switches MS(4,1) - MS(4,16), middle stage 170 consists of  
 5 sixteen, four by four switches MS(5,1) - MS(5,16), middle stage 180 consists of sixteen, four by four switches MS(6,1) - MS(6,16), and middle stage 190 consists of sixteen, four by four switches MS(7,1) - MS(7,16).

As disclosed in U.S. Provisional Patent Application Serial No. 60/940,389 that is incorporated by reference above, such a network can be operated in rearrangeably non-  
 10 blocking manner for arbitrary fan-out multicast connections and also can be operated in strictly non-blocking manner for unicast connections.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable  $\frac{N}{d}$ , where  $N$  is the total  
 15 number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by  $\frac{N}{d}$ . The size of each input switch IS1-IS4 can be denoted in general with the notation  $d * 2d$  and each output switch OS1-OS4 can be denoted in general with the notation  $2d * d$ . Likewise, the size of each switch in any of the middle stages can be denoted as  $2d * 2d$ . A switch as used herein can be either a crossbar switch, or a  
 20 network of switches each of which in turn may be a crossbar switch or a network of switches. A symmetric multi-stage network can be represented with the notation  $V_{mlink}(N, d, s)$ , where  $N$  represents the total number of inlet links of all input switches (for example the links IL1-IL32),  $d$  represents the inlet links of each input switch or outlet links of each output switch, and  $s$  is the ratio of number of outgoing links from  
 25 each input switch to the inlet links of each input switch.

Each of the  $\frac{N}{d}$  input switches IS1 - IS16 are connected to exactly  $d$  switches in middle stage 130 through two links each for a total of  $2 \times d$  links (for example input

switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2), and also connected to middle switch MS(1,2) through the links ML(1,3) and ML(1,4). The middle links which connect switches in the same row in two successive middle stages are called hereinafter straight middle links; and the middle links which connect  
 5 switches in different rows in two successive middle stages are called hereinafter cross middle links. For example, the middle links ML(1,1) and ML(1,2) connect input switch IS1 and middle switch MS(1,1), so middle links ML(1,1) and ML(1,2) are straight middle links; where as the middle links ML(1,3) and ML(1,4) connect input switch IS1 and middle switch MS(1,2), since input switch IS1 and middle switch MS(1,2) belong to two  
 10 different rows in diagram 100A of FIG. 1A, middle links ML(1,3) and ML(1,4) are cross middle links.

Each of the  $\frac{N}{d}$  middle switches MS(1,1) – MS(1,16) in the middle stage 130 are connected from exactly  $d$  input switches through two links each for a total of  $2 \times d$  links (for example the links ML(1,1) and ML(1,2) are connected to the middle switch MS(1,1)  
 15 from input switch IS1, and the links ML(1,7) and ML(1,8) are connected to the middle switch MS(1,1) from input switch IS2) and also are connected to exactly  $d$  switches in middle stage 140 through two links each for a total of  $2 \times d$  links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1), and the links ML(2,3) and ML(2,4) are connected from middle switch MS(1,1)  
 20 to middle switch MS(2,3)).

Each of the  $\frac{N}{d}$  middle switches MS(2,1) – MS(2,16) in the middle stage 140 are connected from exactly  $d$  input switches through two links each for a total of  $2 \times d$  links (for example the links ML(2,1) and ML(2,2) are connected to the middle switch MS(2,1)  
 from input switch MS(1,1), and the links ML(1,11) and ML(1,12) are connected to the  
 25 middle switch MS(2,1) from input switch MS(1,3)) and also are connected to exactly  $d$  switches in middle stage 150 through two links each for a total of  $2 \times d$  links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1), and the links ML(3,3) and ML(3,4) are connected from middle switch MS(2,1) to middle switch MS(3,5)).

Each of the  $\frac{N}{d}$  middle switches MS(3,1) – MS(3,16) in the middle stage 150 are connected from exactly  $d$  input switches through two links each for a total of  $2 \times d$  links (for example the links ML(3,1) and ML(3,2) are connected to the middle switch MS(3,1) from input switch MS(2,1), and the links ML(2,19) and ML(2,20) are connected to the middle switch MS(3,1) from input switch MS(2,5)) and also are connected to exactly  $d$  switches in middle stage 160 through two links each for a total of  $2 \times d$  links (for example the links ML(4,1) and ML(4,2) are connected from middle switch MS(3,1) to middle switch MS(4,1), and the links ML(4,3) and ML(4,4) are connected from middle switch MS(3,1) to middle switch MS(4,9)).

10 Each of the  $\frac{N}{d}$  middle switches MS(4,1) – MS(4,16) in the middle stage 160 are connected from exactly  $d$  input switches through two links each for a total of  $2 \times d$  links (for example the links ML(4,1) and ML(4,2) are connected to the middle switch MS(4,1) from input switch MS(3,1), and the links ML(4,35) and ML(4,36) are connected to the middle switch MS(4,1) from input switch MS(3,9)) and also are connected to exactly  $d$  switches in middle stage 170 through two links each for a total of  $2 \times d$  links (for example the links ML(5,1) and ML(5,2) are connected from middle switch MS(4,1) to middle switch MS(5,1), and the links ML(5,3) and ML(5,4) are connected from middle switch MS(4,1) to middle switch MS(5,9)).

20 Each of the  $\frac{N}{d}$  middle switches MS(5,1) – MS(5,16) in the middle stage 170 are connected from exactly  $d$  input switches through two links each for a total of  $2 \times d$  links (for example the links ML(5,1) and ML(5,2) are connected to the middle switch MS(5,1) from input switch MS(4,1), and the links ML(5,35) and ML(5,36) are connected to the middle switch MS(5,1) from input switch MS(4,9)) and also are connected to exactly  $d$  switches in middle stage 180 through two links each for a total of  $2 \times d$  links (for example the links ML(6,1) and ML(6,2) are connected from middle switch MS(5,1) to middle switch MS(6,1), and the links ML(6,3) and ML(6,4) are connected from middle switch MS(5,1) to middle switch MS(6,5)).

Each of the  $\frac{N}{d}$  middle switches MS(6,1) – MS(6,16) in the middle stage 180 are connected from exactly  $d$  input switches through two links each for a total of  $2 \times d$  links (for example the links ML(6,1) and ML(6,2) are connected to the middle switch MS(6,1) from input switch MS(5,1), and the links ML(6,19) and ML(6,20) are connected to the middle switch MS(6,1) from input switch MS(5,5)) and also are connected to exactly  $d$  switches in middle stage 190 through two links each for a total of  $2 \times d$  links (for example the links ML(7,1) and ML(7,2) are connected from middle switch MS(6,1) to middle switch MS(7,1), and the links ML(7,3) and ML(7,4) are connected from middle switch MS(6,1) to middle switch MS(7,3)).

10 Each of the  $\frac{N}{d}$  middle switches MS(7,1) – MS(7,16) in the middle stage 190 are connected from exactly  $d$  input switches through two links each for a total of  $2 \times d$  links (for example the links ML(7,1) and ML(7,2) are connected to the middle switch MS(7,1) from input switch MS(6,1), and the links ML(7,11) and ML(7,12) are connected to the middle switch MS(7,1) from input switch MS(6,3)) and also are connected to exactly  $d$  switches in middle stage 120 through two links each for a total of  $2 \times d$  links (for example the links ML(8,1) and ML(8,2) are connected from middle switch MS(7,1) to middle switch MS(8,1), and the links ML(8,3) and ML(8,4) are connected from middle switch MS(7,1) to middle switch OS2).

Each of the  $\frac{N}{d}$  middle switches OS1 – OS16 in the middle stage 120 are connected from exactly  $d$  input switches through two links each for a total of  $2 \times d$  links (for example the links ML(8,1) and ML(8,2) are connected to the output switch OS1 from input switch MS(7,1), and the links ML(8,7) and ML(7,8) are connected to the output switch OS1 from input switch MS(7,2)).

25 Finally the connection topology of the network 100A shown in FIG. 1A is known to be back to back inverse Benes connection topology.

Referring to diagram 100B in FIG. 1B, is a folded version of the multi-link multi-stage network 100A shown in FIG. 1A. The network 100B in FIG. 1B shows input stage

110 and output stage 120 are placed together. That is input switch IS1 and output switch OS1 are placed together, input switch IS2 and output switch OS2 are placed together, and similarly input switch IS16 and output switch OS16 are placed together. All the right going middle links (hereinafter “forward connecting links”) {i.e., inlet links IL1 – IL32 and middle links ML(1,1) - ML(1,64)} correspond to input switches IS1 - IS16, and all the left going middle links (hereinafter “backward connecting links”) {i.e., middle links ML(8,1) - ML(8,64) and outlet links OL1-OL32} correspond to output switches OS1 - OS16.

Middle stage 130 and middle stage 190 are placed together. That is middle switches MS(1,1) and MS(7,1) are placed together, middle switches MS(1,2) and MS(7,2) are placed together, and similarly middle switches MS(1,16) and MS(7,16) are placed together. All the right going middle links {i.e., middle links ML(1,1) - ML(1,64) and middle links ML(2,1) – ML(2,64)} correspond to middle switches MS(1,1) – MS(1,16), and all the left going middle links {i.e., middle links ML(7,1) - ML(7,64) and middle links ML(8,1) and ML(8,64)} correspond to middle switches MS(7,1) – MS(7,16).

Middle stage 140 and middle stage 180 are placed together. That is middle switches MS(2,1) and MS(6,1) are placed together, middle switches MS(2,2) and MS(6,2) are placed together, and similarly middle switches MS(2,16) and MS(6,16) are placed together. All the right going middle links {i.e., middle links ML(2,1) - ML(2,64) and middle links ML(3,1) – ML(3,64)} correspond to middle switches MS(2,1) – MS(2,16), and all the left going middle links {i.e., middle links ML(6,1) - ML(6,64) and middle links ML(7,1) and ML(7,64)} correspond to middle switches MS(6,1) – MS(6,16).

Middle stage 150 and middle stage 170 are placed together. That is middle switches MS(3,1) and MS(5,1) are placed together, middle switches MS(3,2) and MS(5,2) are placed together, and similarly middle switches MS(3,16) and MS(5,16) are placed together. All the right going middle links {i.e., middle links ML(3,1) - ML(3,64) and middle links ML(4,1) – ML(4,64)} correspond to middle switches MS(3,1) – MS(3,16), and all the left going middle links {i.e., middle links ML(5,1) - ML(5,64) and

middle links ML(6,1) and ML(6,64)} correspond to middle switches MS(5,1) – MS(5,16).

Middle stage 160 is placed alone. All the right going middle links are the middle links ML(4,1) - ML(4,64) and all the left going middle links are middle links ML(5,1) -  
5 ML(5,64).

In one embodiment, in the network 100B of FIG. 1B, the switches that are placed together are implemented as separate switches then the network 100B is the generalized folded multi-link multi-stage network  $V_{fold-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$  with nine stages as disclosed in U.S. Provisional Patent Application Serial No.  
10 60/940,389 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a two by four switch and a four by two switch. For example the switch input switch IS1 and output switch OS1 are placed together; so input switch IS1 is implemented as two by four switch with the inlet links IL1 and IL2 being the inputs of the input switch IS1 and middle links ML(1,1) – ML(1,4) being the outputs of the input switch IS1; and output switch OS1 is  
15 implemented as four by two switch with the middle links ML(8,1), ML(8,2), ML(8,7) and ML(8,8) being the inputs of the output switch OS1 and outlet links OL1 – OL2 being the outputs of the output switch OS1. Similarly in this embodiment of network 100B all the switches that are placed together in each middle stage are implemented as separate  
20 switches.

### **Hypercube Topology layout schemes:**

Referring to layout 100C of FIG. 1C, in one embodiment, there are sixteen blocks namely Block 1\_2, Block 3\_4, Block 5\_6, Block 7\_8, Block 9\_10, Block 11\_12, Block  
25 13\_14, Block 15\_16, Block 17\_18, Block 19\_20, Block 21\_22, Block 23\_24, Block 25\_26, Block 27\_28, Block 29\_30, and Block 31\_32. Each block implements all the switches in one row of the network 100B of FIG. 1B, one of the key aspects of the current invention. For example Block 1\_2 implements the input switch IS1, output Switch OS1,



middle switch MS(1,1), middle switch MS(7,1), middle switch MS(2,1), middle switch MS(6,1), middle switch MS(3,1), middle switch MS(5,1), and middle switch MS(4,1). For the simplification of illustration, Input switch IS1 and output switch OS1 together are denoted as switch 1; Middle switch MS(1,1) and middle switch MS(7,1) together are  
5 denoted by switch 2; Middle switch MS(2,1) and middle switch MS(6,1) together are denoted by switch 3; Middle switch MS(3,1) and middle switch MS(5,1) together are denoted by switch 4; Middle switch MS(4,1) is denoted by switch 5.

All the straight middle links are illustrated in layout 100C of FIG. 1C. For example in Block 1\_2, inlet links IL1 – IL2, outlet links OL1 – OL2, middle link  
10 ML(1,1), middle link ML(1,2), middle link ML(8,1), middle link ML(8,2), middle link ML(2,1), middle link ML(2,2), middle link ML(7,1), middle link ML(7,2), middle link ML(3,1), middle link ML(3,2), middle link ML(6,1), middle link ML(6,2), middle link ML(4,1), middle link ML(4,2), middle link ML(5,1) and middle link ML(5,2) are illustrated in layout 100C of FIG. 1C.

15 Even though it is not illustrated in layout 100C of FIG. 1C, in each block, in addition to the switches there may be Configurable Logic Blocks (CLB) or any arbitrary digital circuit (hereinafter “sub-integrated circuit block”) depending on the applications in different embodiments. There are four quadrants in the layout 100C of FIG. 1C namely top-left, bottom-left, top-right and bottom-right quadrants. Top-left quadrant implements  
20 Block 1\_2, Block 3\_4, Block 5\_6, and Block 7\_8. Bottom-left quadrant implements Block 9\_10, Block 11\_12, Block 13\_14, and Block 15\_16. Top-right quadrant implements Block 17\_18, Block 19\_20, Block 21\_22, and Block 23\_24. Bottom-right quadrant implements Block 25\_26, Block 27\_28, Block 29\_30, and Block 31\_32. There are two halves in layout 100C of FIG. 1C namely left-half and right-half. Left-half  
25 consists of top-left and bottom-left quadrants. Right-half consists of top-right and bottom-right quadrants.

Recursively in each quadrant there are four sub-quadrants. For example in top-left quadrant there are four sub-quadrants namely top-left sub-quadrant, bottom-left sub-quadrant, top-right sub-quadrant and bottom-right sub-quadrant. Top-left sub-quadrant of  
30 top-left quadrant implements Block 1\_2. Bottom-left sub-quadrant of top-left quadrant

implements Block 3\_4. Top-right sub-quadrant of top-left quadrant implements Block 5\_6. Finally bottom-right sub-quadrant of top-left quadrant implements Block 7\_8. Similarly there are two sub-halves in each quadrant. For example in top-left quadrant there are two sub-halves namely left-sub-half and right-sub-half. Left-sub-half of top-left quadrant implements Block 1\_2 and Block 3\_4. Right-sub-half of top-left quadrant implements Block 5\_6 and Block 7\_8. Finally applicant notes that in each quadrant or half the blocks are arranged as a general binary hypercube. Recursively in larger multi-stage network  $V_{fold-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 > 32$ , the layout in this embodiment in accordance with the current invention, will be such that the super-quadrants will also be arranged in d-ary hypercube manner. (In the embodiment of the layout 100C of FIG. 1C, it is binary hypercube manner since  $d = 2$ , in the network  $V_{fold-link}(N_1, N_2, d, s)$  100B of FIG. 1B).

Layout 100D of FIG. 1D illustrates the inter-block links between switches 1 and 2 of each block. For example middle links ML(1,3), ML(1,4), ML(8,7), and ML(8,8) are connected between switch 1 of Block 1\_2 and switch 2 of Block 3\_4. Similarly middle links ML(1,7), ML(1,8), ML(8,3), and ML(8,4) are connected between switch 2 of Block 1\_2 and switch 1 of Block 3\_4. Applicant notes that the inter-block links illustrated in layout 100D of FIG. 1D can be implemented as vertical tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(1,4) and ML(8,8) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(1,4) and ML(8,8) are implemented as a time division multiplexed single track).

Layout 100E of FIG. 1E illustrates the inter-block links between switches 2 and 3 of each block. For example middle links ML(2,3), ML(2,4), ML(7,11), and ML(7,12) are connected between switch 2 of Block 1\_2 and switch 3 of Block 3\_4. Similarly middle links ML(2,11), ML(2,12), ML(7,3), and ML(7,4) are connected between switch 3 of Block 1\_2 and switch 2 of Block 3\_4. Applicant notes that the inter-block links illustrated in layout 100E of FIG. 1E can be implemented as horizontal tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for

example middle links ML(2,12) and ML(7,4) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(2,12) and ML(7,4) are implemented as a time division multiplexed single track).

5           Layout 100F of FIG. 1F illustrates the inter-block links between switches 3 and 4 of each block. For example middle links ML(3,3), ML(3,4), ML(6,19), and ML(6,20) are connected between switch 3 of Block 1\_2 and switch 4 of Block 3\_4. Similarly middle links ML(3,19), ML(3,20), ML(6,3), and ML(6,4) are connected between switch 4 of Block 1\_2 and switch 3 of Block 3\_4. Applicant notes that the inter-block links illustrated in layout 100F of FIG. 1F can be implemented as vertical tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(3,4) and ML(6,20) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(3,4) and ML(6,20) are implemented as a time division multiplexed single track).

          Layout 100G of FIG. 1G illustrates the inter-block links between switches 4 and 5 of each block. For example middle links ML(4,3), ML(4,4), ML(5,35), and ML(5,36) are connected between switch 4 of Block 1\_2 and switch 5 of Block 3\_4. Similarly middle links ML(4,35), ML(4,36), ML(5,3), and ML(5,4) are connected between switch 5 of Block 1\_2 and switch 4 of Block 3\_4. Applicant notes that the inter-block links illustrated in layout 100G of FIG. 1G can be implemented as horizontal tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(4,4) and ML(5,36) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(4,4) and ML(5,36) are implemented as a time division multiplexed single track).

          The complete layout for the network 100B of FIG. 1B is given by combining the links in layout diagrams of 100C, 100D, 100E, 100F, and 100G. Applicant notes that in the layout 100C of FIG. 1C, the inter-block links between switch 1 and switch 2 of corresponding blocks are vertical tracks as shown in layout 100D of FIG. 1D; the inter-

block links between switch 2 and switch 3 of corresponding blocks are horizontal tracks as shown in layout 100E of FIG. 1E; the inter-block links between switch 3 and switch 4 of corresponding blocks are vertical tracks as shown in layout 100F of FIG. 1F; and finally the inter-block links between switch 4 and switch 5 of corresponding blocks are horizontal tracks as shown in layout 100G of FIG. 1G. The pattern is alternate vertical tracks and horizontal tracks. It continues recursively for larger networks of  $N > 32$  as will be illustrated later.

Some of the key aspects of the current invention are discussed. 1) All the switches in one row of the multi-stage network 100B are implemented in a single block. 2) The blocks are placed in such a way that all the inter-block links are either horizontal tracks or vertical tracks; 3) Since all the inter-block links are either horizontal or vertical tracks, all the inter-block links can be mapped on to island-style architectures in current commercial FPGA's; 4) The length of the longest wire is about half of the width (or length) of the complete layout (For example middle link ML(4,4) is about half the width of the complete layout).

In accordance with the current invention, the layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized folded multi-link multi-stage network  $V_{fold-link}(N_1, N_2, d, s)$  the sub-quadrants, quadrants, and super-quadrants are arranged in d-ary hypercube manner and also the inter-blocks are accordingly connected in d-ary hypercube topology. Even though all the embodiments in the current invention are illustrated for  $N_1 = N_2$ , the embodiments can be extended for  $N_1 \neq N_2$ .

Referring to layout 100H of FIG. 1H, illustrates the extension of layout 100C for the network  $V_{fold-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 128$ ;  $d = 2$ ; and  $s = 2$ . There are four super-quadrants in layout 100H namely top-left super-quadrant, bottom-left super-quadrant, top-right super-quadrant, bottom-right super-quadrant. Total number of blocks in the layout 100H is sixty four. Top-left super-quadrant implements the blocks from block 1\_2 to block 31\_32. Each block in all the super-quadrants has two more switches namely switch 6 and switch 7 in addition to the switches [1-5] illustrated in layout 100C of FIG. 1C. The inter-block link connection topology is the exactly the same between the

switches 1 and 2; switches 2 and 3; switches 3 and 4; switches 4 and 5 as it is shown in the layouts of FIG. 1D, FIG. 1E, FIG. 1F, and FIG. 1G respectively.

Bottom-left super-quadrant implements the blocks from block 33\_34 to block 63\_64. Top-right super-quadrant implements the blocks from block 65\_66 to block 95\_96. And bottom-right super-quadrant implements the blocks from block 97\_98 to block 127\_128. In all these three super-quadrants also, the inter-block link connection topology is the exactly the same between the switches 1 and 2; switches 2 and 3; switches 3 and 4; switches 4 and 5 as that of the top-left super-quadrant.

Recursively in accordance with the current invention, the inter-block links connecting the switch 5 and switch 6 will be vertical tracks between the corresponding switches of top-left super-quadrant and bottom-left super-quadrant. And similarly the inter-block links connecting the switch 5 and switch 6 will be vertical tracks between the corresponding switches of top-right super-quadrant and bottom-right super-quadrant. The inter-block links connecting the switch 6 and switch 7 will be horizontal tracks between the corresponding switches of top-left super-quadrant and top-right super-quadrant. And similarly the inter-block links connecting the switch 6 and switch 7 will be horizontal tracks between the corresponding switches of bottom-left super-quadrant and bottom-right super-quadrant.

Referring to diagram 100I of FIG. 1I illustrates a high-level implementation of Block 1\_2 (Each of the other blocks have similar implementation) of the layout 100C of FIG. 1C which represents a generalized folded multi-link multi-stage network  $V_{fold-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$ . Block 1\_2 in 100I illustrates both the intra-block and inter-block links connected to Block 1\_2. The layout diagram 100I corresponds to the embodiment where the switches that are placed together are implemented as separate switches in the network 100B of FIG. 1B. As noted before then the network 100B is the generalized folded multi-link multi-stage network  $V_{fold-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$  with nine stages as disclosed in U.S. Provisional Patent Application Serial No. 60/940,389 that is incorporated by reference above.

That is the switches that are placed together in Block 1\_2 as shown in FIG. 1I are namely input switch IS1 and output switch OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the switches implemented are input switch IS1 and output switch OS1); middle switch  
 5 MS(1,1) and middle switch MS(7,1) belonging to switch 2; middle switch MS(2,1) and middle switch MS(6,1) belonging to switch 3; middle switch MS(3,1) and middle switch MS(5,1) belonging to switch 4; And middle switch MS(4,1) belonging to switch 5.

Input switch IS1 is implemented as two by four switch with the inlet links IL1 and IL2 being the inputs of the input switch IS1 and middle links ML(1,1) – ML(1,4) being  
 10 the outputs of the input switch IS1; and output switch OS1 is implemented as four by two switch with the middle links ML(8,1) – ML(8,4) being the inputs of the output switch OS1 and outlet links OL1 – OL2 being the outputs of the output switch OS1.

Middle switch MS(1,1) is implemented as four by four switch with the middle links ML(1,1), ML(1,2), ML(1,7) and ML(1,8) being the inputs and middle links ML(2,1)  
 15 – ML(2,4) being the outputs; and middle switch MS(7,1) is implemented as four by four switch with the middle links ML(7,1), ML(7,2), ML(7,11) and ML(7,12) being the inputs and middle links ML(8,1) – ML(8,4) being the outputs. Similarly all the other middle switches are also implemented as four by four switches as illustrated in 100I of FIG. 1I.

Now the VLSI layouts of generalized multi-link multi-stage network  
 20  $V_{mlink}(N_1, N_2, d, s)$  where  $N_1 = N_2 < 32$ ;  $d = 2$ ;  $s = 2$  and its corresponding version of folded generalized multi-link multi-stage network  $V_{fold-mlink}(N_1, N_2, d, s)$  where  $N_1 = N_2 < 32$ ;  $d = 2$ ;  $s = 2$  are discussed. Referring to diagram 200A1 of FIG. 2A1 is generalized multi-link multi-stage network  $V_{mlink}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 2$ ;  $d = 2$ . Diagram 200A2 of FIG. 2A2 illustrates the corresponding folded generalized multi-link multi-  
 25 stage network  $V_{fold-mlink}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 2$ ;  $d = 2$ , version of the diagram 200A1 of FIG. 2A1. Layout 200A3 of FIG. 2A3 illustrates the VLSI layout of the network 200A2 of FIG. 2A2. There is only one block i.e., Block 1\_2 comprising switch 1. Just like in the layout 100C of FIG. 1C, switch 1 consists of input switch IS1 and output switch OS1.

Referring to diagram 200B1 of FIG. 2B1 is generalized multi-link multi-stage network  $V_{mlink}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 4$ ;  $d = 2$ ;  $s = 2$ . Diagram 200B2 of FIG. 2B2 illustrates the corresponding folded generalized multi-link multi-stage network  $V_{fold-mlink}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 4$ ;  $d = 2$ ;  $s = 2$ , version of the diagram 200B1 of

5 FIG. 2B1. Layout 200B3 of FIG. 2B3 illustrates the VLSI layout of the network 200B2 of FIG. 2B2. There are two blocks i.e., Block 1\_2 and Block 3\_4 each comprising switch 1 and switch 2. Switch 1 in each block consists of the corresponding input switch and output switch. For example switch 1 in Block 1\_2 consists of input switch IS1 and output switch OS1. Similarly switch 2 in Block 1\_2 consists of middle switch (1,1). Layout

10 200B4 of FIG. 2B4 illustrates the inter-block links of the VLSI layout diagram 200B3 of FIG. 2B3. For example middle links ML(1,4) and ML(2,8). It must be noted that all the inter-block links are vertical tracks in this layout. (Alternatively all the inter-blocks can also be implemented as horizontal tracks).

Referring to diagram 200C11 of FIG. 2C11 is generalized multi-link multi-stage

15 network  $V_{mlink}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 8$ ;  $d = 2$ ;  $s = 2$ . Diagram 200C12 of FIG. 2C12 illustrates the corresponding folded generalized multi-link multi-stage network  $V_{fold-mlink}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 8$ ;  $d = 2$ ;  $s = 2$ , version of the diagram 200C11 of FIG. 2C11. Layout 200C21 of FIG. 2C21 illustrates the VLSI layout of the network 200C12 of FIG. 2C12. There are four blocks i.e., Block 1\_2, Block 3\_4, Block 5\_6, and

20 Block 7\_8 each comprising switch 1, switch 2 and switch 3. For example switch 1 in Block 1\_2 consists of input switch IS1 and output switch OS1; Switch 2 in Block 1\_2 consists of MS(1,1) and MS(3,1). Switch 3 in Block 1\_2 consists of MS(2,1).

Layout 200C22 of FIG. 2C22 illustrates the inter-block links between the switch 1 and switch 2 of the VLSI layout diagram 200C21 of FIG. 2C21. For example middle

25 links ML(1,4) and ML(4,8) are connected between Block 1\_2 and Block 3\_4. It must be noted that all the inter-block links between switch 1 and switch 2 of all blocks are vertical tracks in this layout. Layout 200C23 of FIG. 2C23 illustrates the inter-block links between the switch 2 and switch 3 of the VLSI layout diagram 200C21 of FIG. 2C21. For example middle links ML(2,12) and ML(3,4) are connected between Block 1\_2 and

Block 5\_6. It must be noted that all the inter-block links between switch 2 and switch 3 of all blocks are horizontal tracks in this layout

Referring to diagram 200D1 of FIG. 2D1 is generalized multi-link multi-stage network  $V_{m-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 16$ ;  $d = 2$ ;  $s = 2$ . Diagram 200D2 of FIG. 2D2 illustrates the corresponding folded generalized multi-link multi-stage network  $V_{fold-m-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 16$ ;  $d = 2$ ;  $s = 2$ , version of the diagram 200D1 of FIG. 2D1. Layout 200D3 of FIG. 2D3 illustrates the VLSI layout of the network 200D2 of FIG. 2D2. There are eight blocks i.e., Block 1\_2, Block 3\_4, Block 5\_6, Block 7\_8, Block 9\_10, Block 11\_12, Block 13\_14 and Block 15\_16 each comprising switch 1, switch 2, switch 3 and switch 4. For example switch 1 in Block 1\_2 consists of input switch IS1 and output switch OS1; Switch 2 in Block 1\_2 consists of MS(1,1) and MS(5,1). Switch 3 in Block 1\_2 consists of MS(2,1) and MS(4,1), and switch 4 in Block 1\_2 consists of MS(3,1).

Layout 200D4 of FIG. 2D4 illustrates the inter-block links between the switch 1 and switch 2 of the VLSI layout diagram 200D3 of FIG. 2D3. For example middle links ML(1,4) and ML(6,8) are connected between Block 1\_2 and Block 3\_4. It must be noted that all the inter-block links between switch 1 and switch 2 of all blocks are vertical tracks in this layout. Layout 200D5 of FIG. 2D5 illustrates the inter-block links between the switch 2 and switch 3 of the VLSI layout diagram 200D3 of FIG. 2D3. For example middle links ML(2,12) and ML(5,4) are connected between Block 1\_2 and Block 5\_6. It must be noted that all the inter-block links between switch 2 and switch 3 of all blocks are horizontal tracks in this layout. Layout 200D6 of FIG. 2D6 illustrates the inter-block links between the switch 3 and switch 4 of the VLSI layout diagram 200D3 of FIG. 2D3. For example middle links ML(3,4) and ML(4,20) are connected between Block 1\_2 and Block 9\_10. It must be noted that all the inter-block links between switch 3 and switch 4 of all blocks are vertical tracks in this layout.

#### **Generalized Multi-link Butterfly Fat Tree Network Embodiment:**

In another embodiment in the network 100B of FIG. 1B, the switches that are placed together are implemented as combined switch then the network 100B is the



generalized multi-link butterfly fat tree network  $V_{mlink-bft}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$  with five stages as disclosed in U.S. Provisional Patent Application Serial No. 60/940,390 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a six by six switch. For example the input switch IS1 and output switch OS1 are placed together; so input switch IS1 and output OS1 are implemented as a six by six switch with the inlet links IL1, IL2, ML(8,1), ML(8,2), ML(8,7) and ML(8,8) being the inputs of the combined switch (denoted as IS1&OS1) and middle links ML(1,1), ML(1,2), ML(1,3), ML(1,4), OL1 and OL2 being the outputs of the combined switch IS1&OS1. Similarly in this embodiment of network 100B all the switches that are placed together are implemented as a combined switch.

Layout diagrams 100C in FIG. 1C, 100D in FIG. 1D, 100E in FIG. 1E, 100F in FIG. 1G are also applicable to generalized multi-link butterfly fat tree network  $V_{mlink-bft}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$  with five stages. The layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized multi-link butterfly fat tree network  $V_{mlink-bft}(N_1, N_2, d, s)$ . Accordingly layout 100H of FIG. 1H is also applicable to generalized multi-link butterfly fat tree network  $V_{mlink-bft}(N_1, N_2, d, s)$ .

Referring to diagram 100J of FIG. 1J illustrates a high-level implementation of Block 1\_2 (Each of the other blocks have similar implementation) of the layout 100C of FIG. 1C which represents a generalized multi-link butterfly fat tree network  $V_{mlink-bft}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$ . Block 1\_2 in 100J illustrates both the intra-block and inter-block links. The layout diagram 100J corresponds to the embodiment where the switches that are placed together are implemented as combined switch in the network 100B of FIG. 1B. As noted before then the network 100B is the generalized multi-link butterfly fat tree network  $V_{mlink-bft}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$  with five stages as disclosed in U.S. Provisional Patent Application Serial No. 60/940,390 that is incorporated by reference above.

That is the switches that are placed together in Block 1\_2 as shown in FIG. 1J are namely the combined input and output switch IS1&OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the switch implemented is combined input and output switch IS1&OS1); middle switch  
 5 MS(1,1) belonging to switch 2; middle switch MS(2,1) belonging to switch 3; middle switch MS(3,1) belonging to switch 4; And middle switch MS(4,1) belonging to switch 5.

Combined input and output switch IS1&OS1 is implemented as six by six switch with the inlet links IL1, IL2 and ML(8,1) – ML(8,4) being the inputs and middle links ML(1,1) – ML(1,4), and outlet links OL1 – OL2 being the outputs.

10 Middle switch MS(1,1) is implemented as eight by eight switch with the middle links ML(1,1), ML(1,2), ML(1,7), ML(1,8), ML(7,1), ML(7,2), ML(7,11) and ML(7,12) being the inputs and middle links ML(2,1) – ML(2,4) and middle links ML(8,1) – ML(8,4) being the outputs. Similarly all the other middle switches are also implemented as eight by eight switches as illustrated in 100J of FIG. 1J. Applicant observes that in  
 15 middle switch MS(1,1) any one of the right going middle links can be switched to any one of the left going middle links and hereinafter middle switch MS(1,1) provides U-turn links. In general, in the network  $V_{mlink-bft}(N_1, N_2, d, s)$  each input switch, each output switch and each middle switch provides U-turn links.

In another embodiment, middle switch MS(1,1) (or the middle switches in any of  
 20 the middle stage excepting the root middle stage) of Block 1\_2 of  $V_{mlink-bft}(N_1, N_2, d, s)$  can be implemented as a four by eight switch and a four by four switch to save cross points. This is because the left going middle links of these middle switches are never setup to the right going middle links. For example, in middle switch MS(1,1) of Block 1\_2 as shown FIG. 1J, the left going middle links namely ML(7,1),  
 25 ML(7,2), ML(7,11), and ML(7,12) are never switched to the right going middle links ML(2,1), ML(2,2), ML(2,3), and ML(2,4). And hence to implement MS(1,1) two switches namely: 1) a four by eight switch with the middle links ML(1,1), ML(1,2), ML(1,7), and ML(1,8) as inputs and the middle links ML(2,1), ML(2,2), ML(2,3), ML(2,4), ML(8,1), ML(8,2), ML(8,3), and ML(8,4) as outputs and 2) a four by four

switch with the middle links ML(7,1), ML(7,2), ML(7,11), and ML(7,12) as inputs and the middle links ML(8,1), ML(8,2), ML(8,3), and ML(8,4) as outputs are sufficient without losing any connectivity of the embodiment of MS(1,1) being implemented as an eight by eight switch as described before.)

## 5 Generalized multi-stage network Embodiment:

In one embodiment, in the network 100B of FIG. 1B, the switches that are placed together are implemented as two separate switches in input stage 110 and output stage 120; and as four separate switches in all the middle stages, then the network 100B is the generalized folded multi-stage network  $V_{fold}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; 10 and  $s = 2$  with nine stages as disclosed in U.S. Provisional Patent Application Serial No. 60/940,391 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a two by four switch and a four by two switch respectively. For example the switch input switch IS1 and output switch OS1 are placed together; so input switch IS1 is implemented as two by four 15 switch with the inlet links IL1 and IL2 being the inputs and middle links ML(1,1) – ML(1,4) being the outputs; and output switch OS1 is implemented as four by two switch with the middle links ML(8,1), ML(8,4), ML(8,7) and ML(8,8) being the inputs and outlet links OL1 – OL2 being the outputs.

The switches, corresponding to the middle stages that are placed together are 20 implemented as four two by two switches. For example middle switches MS(1,1), MS(1,17), MS(7,1), and MS(7,17) are placed together; so middle switch MS(1,1) is implemented as two by two switch with middle links ML(1,1) and ML(1,7) being the inputs and middle links ML(2,1) and ML(2,3) being the outputs; middle switch MS(1,17) is implemented as two by two switch with the middle links ML(1,2) and ML(1,8) being 25 the inputs and middle links ML(2,2) and ML(2,4) being the outputs; middle switch MS(7,1) is implemented as two by two switch with middle links ML(7,1) and ML(7,11) being the inputs and middle links ML(8,1) and ML(8,3) being the outputs; And middle switch MS(7,17) is implemented as two by two switch with the middle links ML(7,2) and ML(7,12) being the inputs and middle links ML(8,2) and ML(8,4) being the outputs;

Similarly in this embodiment of network 100B all the switches that are placed together are implemented as separate switches.

Layout diagrams 100C in FIG. 1C, 100D in FIG. 1D, 100E in FIG. 1E, 100F in FIG. 1G are also applicable to generalized folded multi-stage network

- 5  $V_{fold}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$  with nine stages. The layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized folded multi-stage network  $V_{fold}(N_1, N_2, d, s)$ . Accordingly layout 100H of FIG. 1H is also applicable to generalized folded multi-stage network  $V_{fold}(N_1, N_2, d, s)$ .

- Referring to diagram 100K of FIG. 1K illustrates a high-level implementation of Block 1\_2 (Each of the other blocks have similar implementation) of the layout 100C of FIG. 1C which represents a generalized folded multi-stage network

- 10  $V_{fold}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$ . Block 1\_2 in 100K illustrates both the intra-block and inter-block links. The layout diagram 100K corresponds to the embodiment where the switches that are placed together are implemented as separate switches in the network 100B of FIG. 1B. As noted before then the network 100B is the
- 15 generalized folded multi-stage network  $V_{fold}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$  with nine stages as disclosed in U.S. Provisional Patent Application Serial No. 60/940,391 that is incorporated by reference above.

- That is the switches that are placed together in Block 1\_2 as shown in FIG. 1K are
- 20 namely the input switch IS1 and output switch OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the switches implemented are input switch IS1 and output switch OS1); middle switches MS(1,1), MS(1,17), MS(7,1) and MS(7,17) belonging to switch 2; middle switches MS(2,1), MS(2,17), MS(6,1) and MS(6,17) belonging to switch 3; middle switches
- 25 MS(3,1), MS(3,17), MS(5,1) and MS(5,17) belonging to switch 4; And middle switches MS(4,1), and MS(4,17) belonging to switch 5.

Input switch IS1 and output switch OS1 are placed together; so input switch IS1 is implemented as two by four switch with the inlet links IL1 and IL2 being the inputs and

middle links ML(1,1) – ML(1,4) being the outputs; and output switch OS1 is implemented as four by two switch with the middle links ML(8,1), ML(8,4), ML(8,7) and ML(8,8) being the inputs and outlet links OL1 – OL2 being the outputs.

Middle switches MS(1,1), MS(1,17), MS(7,1), and MS(7,17) are placed together;  
 5 so middle switch MS(1,1) is implemented as two by two switch with middle links ML(1,1) and ML(1,7) being the inputs and middle links ML(2,1) and ML(2,3) being the outputs; middle switch MS(1,17) is implemented as two by two switch with the middle links ML(1,2) and ML(1,8) being the inputs and middle links ML(2,2) and ML(2,4) being the outputs; middle switch MS(7,1) is implemented as two by two switch with middle  
 10 links ML(7,1) and ML(7,11) being the inputs and middle links ML(8,1) and ML(8,3) being the outputs; And middle switch MS(7,17) is implemented as two by two switch with the middle links ML(7,2) and ML(7,12) being the inputs and middle links ML(8,2) and ML(8,4) being the outputs. Similarly all the other middle switches are also implemented as two by two switches as illustrated in 100K of FIG. 1K.

#### 15 **Generalized multi-stage network Embodiment with S = 1:**

In one embodiment, in the network 100B of FIG. 1B (where it is implemented with  $s = 1$ ), the switches that are placed together are implemented as two separate switches in input stage 110 and output stage 120; and as two separate switches in all the middle stages, then the network 100B is the generalized folded multi-stage network  
 20  $V_{fold}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 1$  with nine stages as disclosed in U.S. Provisional Patent Application Serial No. 60/940,391 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a two by two switch and a two by two switch. For  
 25 example the switch input switch IS1 and output switch OS1 are placed together; so input switch IS1 is implemented as two by two switch with the inlet links IL1 and IL2 being the inputs and middle links ML(1,1) – ML(1,2) being the outputs; and output switch OS1 is implemented as two by two switch with the middle links ML(8,1) and ML(8,3) being the inputs and outlet links OL1 – OL2 being the outputs.

The switches, corresponding to the middle stages that are placed together are implemented as two, two by two switches. For example middle switches MS(1,1) and MS(7,1) are placed together; so middle switch MS(1,1) is implemented as two by two switch with middle links ML(1,1) and ML(1,3) being the inputs and middle links ML(2,1) and ML(2,2) being the outputs; middle switch MS(7,1) is implemented as two by two switch with middle links ML(7,1) and ML(7,5) being the inputs and middle links ML(8,1) and ML(8,2) being the outputs; Similarly in this embodiment of network 100B all the switches that are placed together are implemented as two separate switches.

Layout diagrams 100C in FIG. 1C, 100D in FIG. 1D, 100E in FIG. 1E, 100F in FIG. 1G are also applicable to generalized folded multi-stage network  $V_{fold}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 1$  with nine stages. The layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized folded multi-stage network  $V_{fold}(N_1, N_2, d, s)$ . Accordingly layout 100H of FIG. 1H is also applicable to generalized folded multi-stage network  $V_{fold}(N_1, N_2, d, s)$ .

Referring to diagram 100K1 of FIG. 1K1 illustrates a high-level implementation of Block 1\_2 (Each of the other blocks have similar implementation) for the layout 100C of FIG. 1C when  $s = 1$  which represents a generalized folded multi-stage network  $V_{fold}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 1$  (All the double links are replaced by single links when  $s = 1$ ). Block 1\_2 in 100K1 illustrates both the intra-block and inter-block links. The layout diagram 100K1 corresponds to the embodiment where the switches that are placed together are implemented as separate switches in the network 100B of FIG. 1B when  $s = 1$ . As noted before then the network 100B is the generalized folded multi-stage network  $V_{fold}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 1$  with nine stages as disclosed in U.S. Provisional Patent Application Serial No. 60/940,391 that is incorporated by reference above.

That is the switches that are placed together in Block 1\_2 as shown in FIG. 1K1 are namely the input switch IS1 and output switch OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the switches implemented are input switch IS1 and output switch OS1); middle switches

MS(1,1) and MS(7,1) belonging to switch 2; middle switches MS(2,1) and MS(6,1) belonging to switch 3; middle switches MS(3,1) and MS(5,1) belonging to switch 4; And middle switch MS(4,1) belonging to switch 5.

Input switch IS1 and output switch OS1 are placed together; so input switch IS1 is  
 5 implemented as two by two switch with the inlet links IL1 and IL2 being the inputs and middle links ML(1,1) – ML(1,2) being the outputs; and output switch OS1 is implemented as two by two switch with the middle links ML(8,1) and ML(8,3) being the inputs and outlet links OL1 – OL2 being the outputs.

Middle switches MS(1,1) and MS(7,1) are placed together; so middle switch  
 10 MS(1,1) is implemented as two by two switch with middle links ML(1,1) and ML(1,3) being the inputs and middle links ML(2,1) and ML(2,2) being the outputs; And middle switch MS(7,1) is implemented as two by two switch with middle links ML(7,1) and ML(7,5) being the inputs and middle links ML(8,1) and ML(8,2) being the outputs. Similarly all the other middle switches are also implemented as two by two switches as  
 15 illustrated in 100K1 of FIG. 1K1.

#### **Generalized Butterfly Fat Tree Network Embodiment:**

In another embodiment in the network 100B of FIG. 1B, the switches that are placed together are implemented as two combined switches then the network 100B is the generalized butterfly fat tree network  $V_{bf}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$  with five stages as disclosed in U.S. Provisional Patent Application Serial No. 60/940,387 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a six by six switch. For example the input switch IS1 and output switch OS1 are placed together; so input  
 20 output switch IS1&OS1 are implemented as a six by six switch with the inlet links IL1, IL2, ML(8,1), ML(8,2), ML(8,7) and ML(8,8) being the inputs of the combined switch (denoted as IS1&OS1) and middle links ML(1,1), ML(1,2), ML(1,3), ML(1,4), OL1 and OL2 being the outputs of the combined switch IS1&OS1.

The switches, corresponding to the middle stages that are placed together are implemented as two four by four switches. For example middle switches MS(1,1) and MS(1,17) are placed together; so middle switch MS(1,1) is implemented as four by four switch with middle links ML(1,1), ML(1,7), ML(7,1) and ML(7,11) being the inputs and middle links ML(2,1), ML(2,3), ML(8,1) and ML(8,3) being the outputs; middle switch MS(1,17) is implemented as four by four switch with the middle links ML(1,2), ML(1,8), ML(7,2) and ML(7,12) being the inputs and middle links ML(2,2), ML(2,4), ML(8,2) and ML(8,4) being the outputs. Similarly in this embodiment of network 100B all the switches that are placed together are implemented as a two combined switches.

Layout diagrams 100C in FIG. 1C, 100D in FIG. 1D, 100E in FIG. 1E, 100F in FIG. 1G are also applicable to generalized butterfly fat tree network  $V_{bft}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$  with five stages. The layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized butterfly fat tree network  $V_{bft}(N_1, N_2, d, s)$ . Accordingly layout 100H of FIG. 1H is also applicable to generalized butterfly fat tree network  $V_{bft}(N_1, N_2, d, s)$ .

Referring to diagram 100L of FIG. 1L illustrates a high-level implementation of Block 1\_2 (Each of the other blocks have similar implementation) of the layout 100C of FIG. 1C which represents a generalized butterfly fat tree network  $V_{bft}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$ . Block 1\_2 in 100L illustrates both the intra-block and inter-block links. The layout diagram 100L corresponds to the embodiment where the switches that are placed together are implemented as two combined switches in the network 100B of FIG. 1B. As noted before then the network 100B is the generalized butterfly fat tree network  $V_{bft}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$  with five stages as disclosed in U.S. Provisional Patent Application Serial No. 60/940,387 that is incorporated by reference above.

That is the switches that are placed together in Block 1\_2 as shown in FIG. 1L are namely the combined input and output switch IS1&OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the switch implemented is combined input and output switch IS1&OS1); middle switch



MS(1,1) and MS(1,17) belonging to switch 2; middle switch MS(2,1) and MS(2,17) belonging to switch 3; middle switch MS(3,1) and MS(3,17) belonging to switch 4; And middle switch MS(4,1) belonging to switch 5.

5 Combined input and output switch IS1&OS1 is implemented as six by six switch with the inlet links IL1, IL2, ML(8,1), ML(8,2), ML(8,7) and ML(8,8) being the inputs and middle links ML(1,1) – ML(1,4) and outlet links OL1 – OL2 being the outputs.

Middle switch MS(1,1) is implemented as four by four switch with middle links ML(1,1), ML(1,7), ML(7,1) and ML(7,11) being the inputs and middle links ML(2,1), ML(2,3), ML(8,1) and ML(8,3) being the outputs; And middle switch MS(1,17) is  
 10 implemented as four by four switch with the middle links ML(1,2), ML(1,8), ML(7,2) and ML(7,12) being the inputs and middle links ML(2,2), ML(2,4), ML(8,2) and ML(8,4) being the outputs. Similarly all the other middle switches are also implemented as two four by four switches as illustrated in 100L of FIG. 1L. Applicant observes that in middle switch MS(1,1) any one of the right going middle links can be switched to any one of the  
 15 left going middle links and hereinafter middle switch MS(1,1) provides U-turn links. In general, in the network  $V_{bfi}(N_1, N_2, d, s)$  each input switch, each output switch and each middle switch provides U-turn links.

In another embodiment, middle switch MS(1,1) (or the middle switches in any of the middle stage excepting the root middle stage) of Block 1\_2 of  $V_{bfi}(N_1, N_2, d, s)$  can  
 20 be implemented as a two by four switch and a two by two switch to save cross points. This is because the left going middle links of these middle switches are never setup to the right going middle links. For example, in middle switch MS(1,1) of Block 1\_2 as shown FIG. 1L, the left going middle links namely ML(7,1) and ML(7,11) are never switched to the right going middle links ML(2,1) and ML(2,3). And hence to implement MS(1,1)  
 25 two switches namely: 1) a two by four switch with the middle links ML(1,1) and ML(1,7) as inputs and the middle links ML(2,1), ML(2,3), ML(8,1), and ML(8,3) as outputs and 2) a two by two switch with the middle links ML(7,1) and ML(7,11) as inputs and the middle links ML(8,1) and ML(8,3) as outputs are sufficient without losing any

connectivity of the embodiment of MS(1,1) being implemented as an eight by eight switch as described before.)

### Generalized Butterfly Fat Tree Network Embodiment with S = 1:

5            In one embodiment, in the network 100B of FIG. 1B (where it is implemented with  $s = 1$ ), the switches that are placed together are implemented as a combined switch in input stage 110 and output stage 120; and as a combined switch in all the middle stages, then the network 100B is the generalized butterfly fat tree network  $V_{bft}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 1$  with five stages as disclosed in

10 U.S. Provisional Patent Application Serial No. 60/940,387 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a four by four switch. For example the switch input switch IS1 and output switch OS1 are placed together; so input and output switch IS1&OS1 is implemented as four by four switch with the inlet links IL1, IL2, ML(8,1)

15 and ML(8,3) being the inputs and middle links ML(1,1) – ML(1,2) and outlet links OL1 – OL2 being the outputs

The switches, corresponding to the middle stages that are placed together are implemented as a four by four switch. For example middle switches MS(1,1) is implemented as four by four switch with middle links ML(1,1), ML(1,3), ML(7,1) and

20 ML(7,5) being the inputs and middle links ML(2,1), ML(2,2), ML(8,1) and ML(8,2) being the outputs..

Layout diagrams 100C in FIG. 1C, 100D in FIG. 1D, 100E in FIG. 1E, 100F in FIG. 1G are also applicable to generalized butterfly fat tree network  $V_{bft}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 1$  with five stages. The layout 100C

25 in FIG. 1C can be recursively extended for any arbitrarily large generalized butterfly fat tree network  $V_{bft}(N_1, N_2, d, s)$ . Accordingly layout 100H of FIG. 1H is also applicable to generalized butterfly fat tree network  $V_{bft}(N_1, N_2, d, s)$ .

Referring to diagram 100L1 of FIG. 1L1 illustrates a high-level implementation of Block 1\_2 (Each of the other blocks have similar implementation) for the layout 100C of FIG. 1C when  $s = 1$  which represents a generalized butterfly fat tree network  $V_{bft}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 1$  (All the double links are replaced by single links when  $s = 1$ ). Block 1\_2 in 100K1 illustrates both the intra-block and inter-block links. The layout diagram 100L1 corresponds to the embodiment where the switches that are placed together are implemented as a combined switch in the network 100B of FIG. 1B when  $s = 1$ . As noted before then the network 100B is the generalized butterfly fat tree network  $V_{bft}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 1$  with nine stages as disclosed in U.S. Provisional Patent Application Serial No. 60/940,387 that is incorporated by reference above.

That is the switches that are placed together in Block 1\_2 as shown in FIG. 1L1 are namely the input and output switch IS1&OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the switches implemented are input switch IS1 and output switch OS1); middle switch MS(1,1) belonging to switch 2; middle switch MS(2,1) belonging to switch 3; middle switch MS(3,1) belonging to switch 4; And middle switch MS(4,1) belonging to switch 5.

Input and output switch IS1&OS1 are placed together; so input and output switch IS1&OS1 is implemented as four by four switch with the inlet links IL1, IL2, ML(8,1) and ML(8,3) being the inputs and middle links ML(1,1) – ML(1,2) and outlet links OL1 – OL2 being the outputs.

Middle switch MS(1,1) is implemented as four by four switch with middle links ML(1,1), ML(1,3), ML(7,1) and ML(7,5) being the inputs and middle links ML(2,1), ML(2,2), ML(8,1) and ML(8,2) being the outputs. Similarly all the other middle switches are also implemented as four by four switches as illustrated in 100L1 of FIG. 1L1.

In another embodiment, middle switch MS(1,1) (or the middle switches in any of the middle stage excepting the root middle stage) of Block 1\_2 of

$V_{mlink-bft}(N_1, N_2, d, s)$  can be implemented as a two by four switch and a two by two

switch to save cross points. This is because the left going middle links of these middle switches are never setup to the right going middle links. For example, in middle switch MS(1,1) of Block 1\_2 as shown FIG. 1L1, the left going middle links namely ML(7,1) and ML(7,5) are never switched to the right going middle links ML(2,1) and ML(2,2).

5 And hence to implement MS(1,1) two switches namely: 1) a two by four switch with the middle links ML(1,1) and ML(1,3) as inputs and the middle links ML(2,1), ML(2,2), ML(8,1), and ML(8,2) as outputs and 2) a two by two switch with the middle links ML(7,1) and ML(7,5) as inputs and the middle links ML(8,1) and ML(8,2) as outputs are sufficient without losing any connectivity of the embodiment of MS(1,1) being

10 implemented as an eight by eight switch as described before.)

### Hypercube-like Topology layout schemes:

Referring to diagram 300A in FIG. 3A, in one embodiment, an exemplary generalized multi-link multi-stage network  $V_{m\text{link}}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d =$

15 2; and  $s = 2$  with nine stages of one hundred and forty four switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, 150, 170, 170, 180 and 190 is shown where input stage 110 consists of sixteen, two by four switches IS1-IS16 and output stage 120 consists of

20 sixteen, four by two switches OS1-OS16.

As disclosed in U.S. Provisional Patent Application Serial No. 60/940,389 that is incorporated by reference above, such a network can be operated in rearrangeably non-blocking manner for arbitrary fan-out multicast connections and also can be operated in strictly non-blocking manner for unicast connections.

25 The diagram 300A in FIG. 3A is exactly the same as the diagram 100A in FIG. 1A excepting the connection links between middle stage 150 and middle stage 160 as well as between middle stage 160 and middle stage 170.

Each of the  $\frac{N}{d}$  middle switches are connected to exactly  $d$  switches in middle stage 160 through two links each for a total of  $2 \times d$  links (for example the links ML(4,1) and ML(4,2) are connected from middle switch MS(3,1) to middle switch MS(4,1), and the links ML(4,3) and ML(4,4) are connected from middle switch MS(3,1) to middle switch MS(4,15)).

Each of the  $\frac{N}{d}$  middle switches MS(4,1) – MS(4,16) in the middle stage 160 are connected from exactly  $d$  input switches through two links each for a total of  $2 \times d$  links (for example the links ML(4,1) and ML(4,2) are connected to the middle switch MS(4,1) from input switch MS(3,1), and the links ML(4,59) and ML(4,60) are connected to the middle switch MS(4,1) from input switch MS(3,15)) and also are connected to exactly  $d$  switches in middle stage 170 through two links each for a total of  $2 \times d$  links (for example the links ML(5,1) and ML(5,2) are connected from middle switch MS(4,1) to middle switch MS(5,1), and the links ML(5,3) and ML(5,4) are connected from middle switch MS(4,1) to middle switch MS(5,15)).

Each of the  $\frac{N}{d}$  middle switches MS(5,1) – MS(5,16) in the middle stage 170 are connected from exactly  $d$  input switches through two links each for a total of  $2 \times d$  links (for example the links ML(5,1) and ML(5,2) are connected to the middle switch MS(5,1) from input switch MS(4,1), and the links ML(5,59) and ML(5,60) are connected to the middle switch MS(5,1) from input switch MS(4,15)).

Finally the connection topology of the network 100A shown in FIG. 1A is also basically back to back inverse Benes connection topology but with a slight variation. All the cross middle links from middle switches MS(3,1) - MS(3,8) connect to middle switches MS(4,9) – MS(4,16) and all the cross middle links from middle switches MS(3,9) - MS(3,16) connect to middle switches MS(4,1) – MS(4,8). Applicant makes a key observation that there are many combinations of connections possible using this property. The difference in the connection topology between diagram 100A of FIG. 1A and diagram 300A of FIG. 3A is that the connections formed by cross middle links

between middle stage 150 and middle stage 160 are made of two different combinations otherwise both the diagrams 100A and 300A implement back to back inverse Benes connection topology. Since these networks implement back to back inverse Benes topologies since there is difference in the connections of cross middle links between  
 5 middle stage 150 and middle stage 160, the same difference in the connections of cross middle links between 160 and middle stage 170 occurs.

Referring to diagram 300B in FIG. 3B, is a folded version of the multi-link multi-stage network 300A shown in FIG. 3A. The network 300B in FIG. 3B shows input stage 110 and output stage 120 are placed together. That is input switch IS1 and output switch  
 10 OS1 are placed together, input switch IS2 and output switch OS2 are placed together, and similarly input switch IS16 and output switch OS16 are placed together. All the right going middle links {i.e., inlet links IL1 – IL32 and middle links ML(1,1) - ML(1,64)} correspond to input switches IS1 - IS16, and all the left going middle links {i.e., middle links ML(7,1) - ML(7,64) and outlet links OL1-OL32} correspond to output switches  
 15 OS1 - OS16.

Just the same way there is difference in the connection topology between diagram 100A of FIG. 1A and diagram 300A of FIG. 3A in the way the connections are formed by cross middle links between middle stage 150 and middle stage 160 and also between middle stage 160 and middle stage 170, the exact similar difference is there between the  
 20 diagram 100B of FIG. 1B and the diagram 300B of FIG. 3B, i.e., in the way the connections are formed by cross middle links between middle stage 150 and middle stage 160 and also between middle stage 160 and middle stage 170.

In one embodiment, in the network 300B of FIG. 3B, the switches that are placed together are implemented as separate switches then the network 300B is the generalized  
 25 folded multi-link multi-stage network  $V_{fold-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 32$ ;  $d = 2$ ; and  $s = 2$  with nine stages as disclosed in U.S. Provisional Patent Application Serial No. 60/940,389 that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a two by four switch and a four by two switch. For example the switch input switch IS1 and output switch OS1  
 30 are placed together; so input switch IS1 is implemented as two by four switch with the

inlet links IL1 and IL2 being the inputs of the input switch IS1 and middle links ML(1,1) – ML(1,4) being the outputs of the input switch IS1; and output switch OS1 is implemented as four by two switch with the middle links ML(8,1), ML(8,2), ML(8,7) and ML(8,8) being the inputs of the output switch OS1 and outlet links OL1 – OL2 being the  
5 outputs of the output switch OS1. Similarly in this embodiment of network 300B all the switches that are placed together are implemented as separate switches.

Referring to layout 300C of FIG. 3C, in one embodiment, there are sixteen blocks namely Block 1\_2, Block 3\_4, Block 5\_6, Block 7\_8, Block 9\_10, Block 11\_12, Block 13\_14, Block 15\_16, Block 17\_18, Block 19\_20, Block 21\_22, Block 23\_24, Block  
10 25\_26, Block 27\_28, Block 29\_30, and Block 31\_32. Each block implements all the switches in one row of the network 300B of FIG. 3B, one of the key aspects of the current invention. For example Block 1\_2 implements the input switch IS1, output Switch OS1, middle switch MS(1,1), middle switch MS(7,1), middle switch MS(2,1), middle switch MS(6,1), middle switch MS(3,1), middle switch MS(5,1), and middle switch MS(4,1).  
15 For the simplification of illustration, Input switch IS1 and output switch OS1 together are denoted as switch 1; Middle switch MS(1,1) and middle switch MS(7,1) together are denoted by switch 2; Middle switch MS(2,1) and middle switch MS(6,1) together are denoted by switch 3; Middle switch MS(3,1) and middle switch MS(5,1) together are denoted by switch 4; And middle switch MS(4,1) is denoted by switch 5.

All the straight middle links are illustrated in layout 300C of FIG. 3C. For  
20 example in Block 1\_2, inlet links IL1 – IL2, outlet links OL1 – OL2, middle link ML(1,1), middle link ML(1,2), middle link ML(8,1), middle link ML(8,2), middle link ML(2,1), middle link ML(2,2), middle link ML(7,1), middle link ML(7,2), middle link ML(3,1), middle link ML(3,2), middle link ML(6,1), middle link ML(6,2), middle link  
25 ML(4,1), middle link ML(4,2), middle link ML(5,1) and middle link ML(5,2) are illustrated in layout 300C of FIG. 3C.

Even though it is not illustrated in layout 300C of FIG. 3C, in each block, in addition to the switches there may be Configurable Logic Blocks (CLB) or any arbitrary digital circuit or sub-integrated circuit block depending on the applications in different  
30 embodiments. There are four quadrants in the layout 300C of FIG. 3C namely top-left,

bottom-left, top-right and bottom-right quadrants. Top-left quadrant implements Block 1\_2, Block 3\_4, Block 5\_6, and Block 7\_8. Bottom-left quadrant implements Block 9\_10, Block 11\_12, Block 13\_14, and Block 15\_16. Top-right quadrant implements Block 25\_26, Block 27\_28, Block 29\_30, and Block 31\_32. Bottom-right quadrant implements Block 17\_18, Block 19\_20, Block 21\_22, and Block 23\_24. There are two halves in layout 300C of FIG. 3C namely left-half and right-half. Left-half consists of top-left and bottom-left quadrants. Right-half consists of top-right and bottom-right quadrants.

10 Recursively in each quadrant there are four sub-quadrants. For example in top-left quadrant there are four sub-quadrants namely top-left sub-quadrant, bottom-left sub-quadrant, top-right sub-quadrant and bottom-right sub-quadrant. Top-left sub-quadrant of top-left quadrant implements Block 1\_2. Bottom-left sub-quadrant of top-left quadrant implements Block 3\_4. Top-right sub-quadrant of top-left quadrant implements Block 7\_8. Finally bottom-right sub-quadrant of top-left quadrant implements Block 5\_6.

15 Similarly there are two sub-halves in each quadrant. For example in top-left quadrant there are two sub-halves namely left-sub-half and right-sub-half. Left-sub-half of top-left quadrant implements Block 1\_2 and Block 3\_4. Right-sub-half of top-left quadrant implements Block 7\_8 and Block 5\_6. Recursively in larger multi-stage network  $V_{fold-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 > 32$ , the layout in this embodiment in accordance

20 with the current invention, will be such that the super-quadrants will also be arranged in a similar manner.

Layout 300D of FIG. 3D illustrates the inter-block links (in the layout 300C of FIG. 3C all the cross middle links are inter-block links) between switches 1 and 2 of each block. For example middle links ML(1,3), ML(1,4), ML(8,7), and ML(8,8) are connected

25 between switch 1 of Block 1\_2 and switch 2 of Block 3\_4. Similarly middle links ML(1,7), ML(1,8), ML(8,3), and ML(8,4) are connected between switch 2 of Block 1\_2 and switch 1 of Block 3\_4. Applicant notes that the inter-block links illustrated in layout 100D of FIG. 1D can be implemented as vertical tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example

30 middle links ML(1,4) and ML(8,8) are implemented as two different tracks); or in an



alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(1,4) and ML(8,8) are implemented as a time division multiplexed single track).

5           Layout 300E of FIG. 3E illustrates the inter-block links between switches 2 and 3 of each block. For example middle links ML(2,3), ML(2,4), ML(7,11), and ML(7,12) are connected between switch 2 of Block 1\_2 and switch 3 of Block 3\_4. Similarly middle links ML(2,11), ML(2,12), ML(7,3), and ML(7,4) are connected between switch 3 of Block 1\_2 and switch 2 of Block 3\_4. Applicant notes that the inter-block links illustrated in layout 300E of FIG. 3E can be implemented as diagonal tracks in one embodiment.

10          Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(2,12) and ML(7,4) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(2,12) and ML(7,4) are implemented as a time division multiplexed single track).

15           Layout 300F of FIG. 3F illustrates the inter-block links between switches 3 and 4 of each block. For example middle links ML(3,3), ML(3,4), ML(6,19), and ML(6,20) are connected between switch 3 of Block 1\_2 and switch 4 of Block 3\_4. Similarly middle links ML(3,19), ML(3,20), ML(6,3), and ML(6,4) are connected between switch 4 of Block 1\_2 and switch 3 of Block 3\_4. Applicant notes that the inter-block links illustrated

20          in layout 300F of FIG. 3F can be implemented as vertical tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(3,4) and ML(6,20) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(3,4) and ML(6,20) are implemented as a time

25          division multiplexed single track).

          Layout 300G of FIG. 3G illustrates the inter-block links between switches 4 and 5 of each block. For example middle links ML(4,3), ML(4,4), ML(5,35), and ML(5,36) are connected between switch 4 of Block 1\_2 and switch 5 of Block 3\_4. Similarly middle links ML(4,35), ML(4,36), ML(5,3), and ML(5,4) are connected between switch 5 of

30          Block 1\_2 and switch 4 of Block 3\_4. Applicant notes that the inter-block links illustrated

in layout 300G of FIG. 3G can be implemented as horizontal tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(4,4) and ML(5,36) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division  
 5 multiplexed single track (for example middle links ML(4,4) and ML(5,36) are implemented as a time division multiplexed single track).

The complete layout for the network 300B of FIG. 3B is given by combining the links in layout diagrams of 300C, 300D, 300E, 300F, and 300G. Applicant notes that in the layout 300C of FIG. 3C, the inter-block links between switch 1 and switch 2 are  
 10 vertical tracks as shown in layout 300D of FIG. 3D; the inter-block links between switch 2 and switch 3 are horizontal tracks as shown in layout 300E of FIG. 3E; the inter-block links between switch 3 and switch 4 are vertical tracks as shown in layout 300F of FIG. 3F; and finally the inter-block links between switch 4 and switch 5 are horizontal tracks as shown in layout 300G of FIG. 3G. The pattern is either vertical tracks, horizontal  
 15 tracks or diagonal tracks. It continues recursively for larger networks of  $N > 32$  as will be illustrated later.

Some of the key aspects of the current invention related to layout diagram 300C of IFG. 3C are noted. 1) All the switches in one row of the multi-stage network 300B are implemented in a single block. 2) The blocks are placed in such a way that all the inter-  
 20 block links are either horizontal tracks, vertical tracks or diagonal tracks; 3) The length of the longest wire is about half of the width (or length) of the complete layout (For example middle link ML(4,4) is about half the width of the complete layout.);

The layout 300C in FIG. 3C can be recursively extended for any arbitrarily large generalized folded multi-link multi-stage network  $V_{fold-link}(N_1, N_2, d, s)$ . Referring to  
 25 layout 300H of FIG. 3H, illustrates the extension of layout 300C for the network  $V_{fold-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 = 128$ ;  $d = 2$ ; and  $s = 2$ . There are four super-quadrants in layout 300H namely top-left super-quadrant, bottom-left super-quadrant, top-right super-quadrant, bottom-right super-quadrant. Total number of blocks in the layout 300H is sixty four. Top-left super-quadrant implements the blocks from block 1\_2

to block 31\_32. Each block in all the super-quadrants has two more switches namely switch 6 and switch 7 in addition to the switches [1-5] illustrated in layout 300C of FIG. 3C. The inter-block link connection topology is the exactly the same between the switches 1 and 2; switches 2 and 3; switches 3 and 4; switches 4 and 5 as it is shown in the layouts of FIG. 3D, FIG. 3E, FIG. 3F, and FIG. 3G respectively.

Bottom-left super-quadrant implements the blocks from block 33\_34 to block 63\_64. Top-right super-quadrant implements the blocks from block 65\_66 to block 95\_96. And bottom-right super-quadrant implements the blocks from block 97\_98 to block 127\_128. In all these three super-quadrants also, the inter-block link connection topology is the exactly the same between the switches 1 and 2; switches 2 and 3; switches 3 and 4; switches 4 and 5 as that of the top-left super-quadrant.

Recursively in accordance with the current invention, the inter-block links connecting the switch 5 and switch 6 will be vertical tracks between the corresponding switches of top-left super-quadrant and bottom-left super-quadrant. And similarly the inter-block links connecting the switch 5 and switch 6 will be vertical tracks between the corresponding switches of top-right super-quadrant and bottom-right super-quadrant. The inter-block links connecting the switch 6 and switch 7 will be horizontal tracks between the corresponding switches of top-left super-quadrant and top-right super-quadrant. And similarly the inter-block links connecting the switch 6 and switch 7 will be horizontal tracks between the corresponding switches of bottom-left super-quadrant and bottom-right super-quadrant.

### **Ring Topology layout schemes:**

Layout diagram 400C of FIG. 4C is another embodiment for the generalized folded multi-link multi-stage network  $V_{fold-mlink}(N_1, N_2, d, s)$  diagram 100B in FIG. 1B.

Referring to layout 400C of FIG. 4C, there are sixteen blocks namely Block 1\_2, Block 3\_4, Block 5\_6, Block 7\_8, Block 9\_10, Block 11\_12, Block 13\_14, Block 15\_16, Block 17\_18, Block 19\_20, Block 21\_22, Block 23\_24, Block 25\_26, Block 27\_28,

Block 29\_30, and Block 31\_32. Each block implements all the switches in one row of the network 100B of FIG. 1B, one of the key aspects of the current invention. For example Block 1\_2 implements the input switch IS1, output Switch OS1, middle switch MS(1,1), middle switch MS(7,1), middle switch MS(2,1), middle switch MS(6,1), middle switch MS(3,1), middle switch MS(5,1), and middle switch MS(4,1). For the simplification of illustration, Input switch IS1 and output switch OS1 together are denoted as switch 1; Middle switch MS(1,1) and middle switch MS(7,1) together are denoted by switch 2; Middle switch MS(2,1) and middle switch MS(6,1) together are denoted by switch 3; Middle switch MS(3,1) and middle switch MS(5,1) together are denoted by switch 4; And middle switch MS(4,1) is denoted by switch 5.

All the straight middle links are illustrated in layout 400C of FIG. 4C. For example in Block 1\_2, inlet links IL1 – IL2, outlet links OL1 – OL2, middle link ML(1,1), middle link ML(1,2), middle link ML(8,1), middle link ML(8,2), middle link ML(2,1), middle link ML(2,2), middle link ML(7,1), middle link ML(7,2), middle link ML(3,1), middle link ML(3,2), middle link ML(6,1), middle link ML(6,2), middle link ML(4,1), middle link ML(4,2), middle link ML(5,1) and middle link ML(5,2) are illustrated in layout 400C of FIG. 4C.

Even though it is not illustrated in layout 400C of FIG. 4C, in each block, in addition to the switches there may be Configurable Logic Blocks (CLB) or any arbitrary digital circuit or sub-integrated circuit block depending on the applications in different embodiments. The topology of the layout 400C in FIG. 4C is a ring. For each of the neighboring rows in diagram 100B of FIG. 1B the corresponding blocks are also physically neighbors in layout diagram 400C of FIG. 4C. In addition the topmost row is also logically considered as neighbor to the bottommost row. For example Block 1\_2 (implementing the switches belonging to a row in diagram 100B of FIG. 1B) has Block 3\_4 as neighbor since Block 3\_4 implements the switches in its neighboring row. Similarly Block 1\_2 also has Block 31\_32 as neighbor since Block 1\_2 implements topmost row of switches and Block 31\_32 implements bottommost row of switches in diagram 100B of FIG. 1B. The ring layout scheme illustrated in 400C of FIG. 4C can be

generalized for a large multi-stage network  $V_{fold-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 > 32$ , in accordance with the current invention.

Layout 400B of FIG. 4B illustrates the inter-block links (in the layout 400A of FIG. 4A all the cross middle links are inter-block links) between switches 1 and 2 of each block. For example middle links ML(1,3), ML(1,4), ML(8,7), and ML(8,8) are connected between switch 1 of Block 1\_2 and switch 2 of Block 3\_4. Similarly middle links ML(1,7), ML(1,8), ML(8,3), and ML(8,4) are connected between switch 2 of Block 1\_2 and switch 1 of Block 3\_4. Applicant notes that the inter-block links illustrated in layout 400B of FIG. 4B are implemented as vertical tracks or horizontal tracks or diagonal tracks. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(1,4) and ML(8,8) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(1,4) and ML(8,8) are implemented as a time division multiplexed single track).

Layout 400C of FIG. 4C illustrates the inter-block links between switches 2 and 3 of each block. For example middle links ML(2,3), ML(2,4), ML(7,11), and ML(7,12) are connected between switch 2 of Block 1\_2 and switch 3 of Block 3\_4. Similarly middle links ML(2,11), ML(2,12), ML(7,3), and ML(7,4) are connected between switch 3 of Block 1\_2 and switch 2 of Block 3\_4. Applicant notes that the inter-block links illustrated in layout 400C of FIG. 4C are implemented as vertical tracks or horizontal tracks or diagonal tracks. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(2,12) and ML(7,4) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(2,12) and ML(7,4) are implemented as a time division multiplexed single track).

Layout 400D of FIG. 4D illustrates the inter-block links between switches 3 and 4 of each block. For example middle links ML(3,3), ML(3,4), ML(6,19), and ML(6,20) are connected between switch 3 of Block 1\_2 and switch 4 of Block 3\_4. Similarly middle links ML(3,19), ML(3,20), ML(6,3), and ML(6,4) are connected between switch 4 of Block 1\_2 and switch 3 of Block 3\_4. Applicant notes that the inter-block links illustrated

in layout 400D of FIG. 4D are implemented as vertical tracks or horizontal tracks or diagonal tracks. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(3,4) and ML(6,20) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(3,4) and ML(6,20) are implemented as a time division multiplexed single track).

Layout 400E of FIG. 4E illustrates the inter-block links between switches 4 and 5 of each block. For example middle links ML(4,3), ML(4,4), ML(5,35), and ML(5,36) are connected between switch 4 of Block 1\_2 and switch 5 of Block 3\_4. Similarly middle links ML(4,35), ML(4,36), ML(5,3), and ML(5,4) are connected between switch 5 of Block 1\_2 and switch 4 of Block 3\_4. Applicant notes that the inter-block links illustrated in layout 400E of FIG. 4E are implemented as vertical tracks or horizontal tracks or diagonal tracks. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(4,4) and ML(5,36) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(4,4) and ML(5,36) are implemented as a time division multiplexed single track).

The complete layout for the network 100B of FIG. 1B is given by combining the links in layout diagrams of 400A, 400B, 400C, 400D, and 400E.

Some of the key aspects of the current invention related to layout diagram 400A of FIG. 4A are noted. 1) All the switches in one row of the multi-stage network 100B are implemented in a single block. 2) The blocks are placed in such a way that all the inter-block links are either horizontal tracks, vertical tracks or diagonal tracks; 3) Length of the different wires between the same two middle stages is not the same. However it gives an opportunity to implement the most connected circuits to place and route through the blocks which have shorter wires.

Layout diagram 400C1 of FIG. 4C1 is another embodiment for the generalized folded multi-link multi-stage network  $V_{fold-link}(N_1, N_2, d, s)$  diagram 100B in FIG. 1B. Referring to layout 400C1 of FIG. 4C1, there are sixteen blocks namely Block 1\_2, Block

3\_4, Block 5\_6, Block 7\_8, Block 9\_10, Block 11\_12, Block 13\_14, Block 15\_16, Block 17\_18, Block 19\_20, Block 21\_22, Block 23\_24, Block 25\_26, Block 27\_28, Block 29\_30, and Block 31\_32. Each block implements all the switches in one row of the network 100B of FIG. 1B, one of the key aspects of the current invention. For example

5 Block 1\_2 implements the input switch IS1, output Switch OS1, middle switch MS(1,1), middle switch MS(7,1), middle switch MS(2,1), middle switch MS(6,1), middle switch MS(3,1), middle switch MS(5,1), and middle switch MS(4,1). For the simplification of illustration, Input switch IS1 and output switch OS1 together are denoted as switch 1; Middle switch MS(1,1) and middle switch MS(7,1) together are denoted by switch 2;

10 Middle switch MS(2,1) and middle switch MS(6,1) together are denoted by switch 3; Middle switch MS(3,1) and middle switch MS(5,1) together are denoted by switch 4; And middle switch MS(4,1) is denoted by switch 5.

All the straight middle links are illustrated in layout 400C1 of FIG. 4C1. For example in Block 1\_2, inlet links IL1 – IL2, outlet links OL1 – OL2, middle link

15 ML(1,1), middle link ML(1,2), middle link ML(8,1), middle link ML(8,2), middle link ML(2,1), middle link ML(2,2), middle link ML(7,1), middle link ML(7,2), middle link ML(3,1), middle link ML(3,2), middle link ML(6,1), middle link ML(6,2), middle link ML(4,1), middle link ML(4,2), middle link ML(5,1) and middle link ML(5,2) are illustrated in layout 400C1 of FIG. 4C1.

20 Even though it is not illustrated in layout 400C1 of FIG. 4C1, in each block, in addition to the switches there may be Configurable Logic Blocks (CLB) or any arbitrary digital circuit or sub-integrated circuit block depending on the applications in different embodiments. The topology of the layout 400C1 in FIG. 4C1 is another embodiment of ring layout topology. For each of the neighboring rows in diagram 100B of FIG. 1B the

25 corresponding blocks are also physically neighbors in layout diagram 400C of FIG. 4C. In addition the topmost row is also logically considered as neighbor to the bottommost row. For example Block 1\_2 (implementing the switches belonging to a row in diagram 100B of FIG. 1B) has Block 3\_4 as neighbor since Block 3\_4 implements the switches in its neighboring row. Similarly Block 1\_2 also has Block 31\_32 as neighbor since Block

30 1\_2 implements topmost row of switches and Block 31\_32 implements bottommost row

of switches in diagram 100B of FIG. 1B. The ring layout scheme illustrated in 400C of FIG. 4C can be generalized for a large multi-stage network  $V_{fold-link}(N_1, N_2, d, s)$  where  $N_1 = N_2 > 32$ , in accordance with the current invention.

All the layout embodiments disclosed in the current invention are applicable to  
 5 generalized multi-stage networks  $V(N_1, N_2, d, s)$ , generalized folded multi-stage  
 networks  $V_{fold}(N_1, N_2, d, s)$ , generalized butterfly fat tree networks  $V_{bft}(N_1, N_2, d, s)$ ,  
 generalized multi-link multi-stage networks  $V_{mlink}(N_1, N_2, d, s)$ , generalized folded multi-  
 link multi-stage networks  $V_{fold-link}(N_1, N_2, d, s)$ , generalized multi-link butterfly fat tree  
 networks  $V_{mlink-bft}(N_1, N_2, d, s)$ , and generalized hypercube networks  $V_{hcube}(N_1, N_2, d, s)$   
 10 for  $s = 1, 2, 3$  or any number in general, and for both  $N_1 = N_2 = N$  and  $N_1 \neq N_2$ , and  $d$  is  
 any integer.

Conversely applicant makes another important observation that generalized  
 hypercube networks  $V_{hcube}(N_1, N_2, d, s)$  are implemented with the layout topology being  
 the hypercube topology shown in layout 100C of FIG. 1C with large scale cross point  
 15 reduction as any one of the networks described in the current invention namely:  
 generalized multi-stage networks  $V(N_1, N_2, d, s)$ , generalized folded multi-stage  
 networks  $V_{fold}(N_1, N_2, d, s)$ , generalized butterfly fat tree networks  $V_{bft}(N_1, N_2, d, s)$ ,  
 generalized multi-link multi-stage networks  $V_{mlink}(N_1, N_2, d, s)$ , generalized folded multi-  
 link multi-stage networks  $V_{fold-link}(N_1, N_2, d, s)$ , generalized multi-link butterfly fat tree  
 20 networks  $V_{mlink-bft}(N_1, N_2, d, s)$  for  $s = 1, 2, 3$  or any number in general, and for both  
 $N_1 = N_2 = N$  and  $N_1 \neq N_2$ , and  $d$  is any integer.

### **Applications Embodiments:**

All the embodiments disclosed in the current invention are useful in many  
 25 varieties of applications. FIG. 5A1 illustrates the diagram of 500A1 which is a typical  
 two by two switch with two inlet links namely IL1 and IL2, and two outlet links namely



OL1 and OL2. The two by two switch also implements four crosspoints namely CP(1,1), CP(1,2), CP(2,1) and CP(2,2) as illustrated in FIG. 5A1. For example the diagram of 500A1 may be the implementation of middle switch MS(1,1) of the diagram 100K of FIG. 1K where inlet link IL1 of diagram 500A1 corresponds to middle link ML(1,1) of diagram 100K, inlet link IL2 of diagram 500A1 corresponds to middle link ML(1,7) of diagram 100K, outlet link OL1 of diagram 500A1 corresponds to middle link ML(2,1) of diagram 100K, outlet link OL2 of diagram 500A1 corresponds to middle link ML(2,3) of diagram 100K.

#### 10 **1) Programmable Integrated Circuit Embodiments:**

All the embodiments disclosed in the current invention are useful in programmable integrated circuit applications. FIG. 5A2 illustrates the detailed diagram 500A2 for the implementation of the diagram 500A1 in programmable integrated circuit embodiments. Each crosspoint is implemented by a transistor coupled between the corresponding inlet link and outlet link, and a programmable cell in programmable integrated circuit embodiments. Specifically crosspoint CP(1,1) is implemented by transistor C(1,1) coupled between inlet link IL1 and outlet link OL1, and programmable cell P(1,1); crosspoint CP(1,2) is implemented by transistor C(1,2) coupled between inlet link IL1 and outlet link OL2, and programmable cell P(1,2); crosspoint CP(2,1) is implemented by transistor C(2,1) coupled between inlet link IL2 and outlet link OL1, and programmable cell P(2,1); and crosspoint CP(2,2) is implemented by transistor C(2,2) coupled between inlet link IL2 and outlet link OL2, and programmable cell P(2,2).

If the programmable cell is programmed ON, the corresponding transistor couples the corresponding inlet link and outlet link. If the programmable cell is programmed OFF, the corresponding inlet link and outlet link are not connected. For example if the programmable cell P(1,1) is programmed ON, the corresponding transistor C(1,1) couples the corresponding inlet link IL1 and outlet link OL1. If the programmable cell P(1,1) is programmed OFF, the corresponding inlet link IL1 and outlet link OL1 are not connected. In volatile programmable integrated circuit embodiments the programmable

cell may be an SRAM (Static Random Address Memory) cell. In non-volatile programmable integrated circuit embodiments the programmable cell may be a Flash memory cell. Also the programmable integrated circuit embodiments may implement field programmable logic arrays (FPGA) devices, or programmable Logic devices (PLD),  
5 or Application Specific Integrated Circuits (ASIC) embedded with programmable logic circuits or 3D-FPGAs.

FIG. 5A2 also illustrates a buffer B1 on inlet link IL2. The signals driven along inlet link IL2 are amplified by buffer B1. Buffer B1 can be inverting or non-inverting buffer. Buffers such as B1 are used to amplify the signal in links which are usually long.

## 10 2) One-time Programmable Integrated Circuit Embodiments:

All the embodiments disclosed in the current invention are useful in one-time programmable integrated circuit applications. FIG. 5A3 illustrates the detailed diagram 500A3 for the implementation of the diagram 500A1 in one-time programmable integrated circuit embodiments. Each crosspoint is implemented by a via coupled  
15 between the corresponding inlet link and outlet link in one-time programmable integrated circuit embodiments. Specifically crosspoint CP(1,1) is implemented by via V(1,1) coupled between inlet link IL1 and outlet link OL1; crosspoint CP(1,2) is implemented by via V(1,2) coupled between inlet link IL1 and outlet link OL2; crosspoint CP(2,1) is implemented by via V(2,1) coupled between inlet link IL2 and outlet link OL1; and  
20 crosspoint CP(2,2) is implemented by via V(2,2) coupled between inlet link IL2 and outlet link OL2.

If the via is programmed ON, the corresponding inlet link and outlet link are permanently connected which is denoted by thick circle at the intersection of inlet link and outlet link. If the via is programmed OFF, the corresponding inlet link and outlet link  
25 are not connected which is denoted by the absence of thick circle at the intersection of inlet link and outlet link. For example in the diagram 500A3 the via V(1,1) is programmed ON, and the corresponding inlet link IL1 and outlet link OL1 are connected as denoted by thick circle at the intersection of inlet link IL1 and outlet link OL1; the via V(2,2) is programmed ON, and the corresponding inlet link IL2 and outlet link OL2 are

connected as denoted by thick circle at the intersection of inlet link IL2 and outlet link OL2; the via V(1,2) is programmed OFF, and the corresponding inlet link IL1 and outlet link OL2 are not connected as denoted by the absence of thick circle at the intersection of inlet link IL1 and outlet link OL2; the via V(2,1) is programmed OFF, and the  
5 corresponding inlet link IL2 and outlet link OL1 are not connected as denoted by the absence of thick circle at the intersection of inlet link IL2 and outlet link OL1. One-time programmable integrated circuit embodiments may be anti-fuse based programmable integrated circuit devices or mask programmable structured ASIC devices.

### 3) Integrated Circuit Placement and Route Embodiments:

10 All the embodiments disclosed in the current invention are useful in Integrated Circuit Placement and Route applications, for example in ASIC backend Placement and Route tools. FIG. 5A4 illustrates the detailed diagram 500A4 for the implementation of the diagram 500A1 in Integrated Circuit Placement and Route embodiments. In an integrated circuit since the connections are known a-priori, the switch and crosspoints are  
15 actually virtual. However the concept of virtual switch and virtual crosspoint using the embodiments disclosed in the current invention reduces the number of required wires, wire length needed to connect the inputs and outputs of different netlists and the time required by the tool for placement and route of netlists in the integrated circuit.

Each virtual crosspoint is used to either to hardwire or provide no connectivity  
20 between the corresponding inlet link and outlet link. Specifically crosspoint CP(1,1) is implemented by direct connect point DCP(1,1) to hardwire (i.e., to permanently connect) inlet link IL1 and outlet link OL1 which is denoted by the thick circle at the intersection of inlet link IL1 and outlet link OL1; crosspoint CP(2,2) is implemented by direct connect point DCP(2,2) to hardwire inlet link IL2 and outlet link OL2 which is denoted  
25 by the thick circle at the intersection of inlet link IL2 and outlet link OL2. The diagram 500A4 does not show direct connect point DCP(1,2) and direct connect point DCP(1,3) since they are not needed and in the hardware implementation they are eliminated. Alternatively inlet link IL1 needs to be connected to outlet link OL1 and inlet link IL1 does not need to be connected to outlet link OL2. Also inlet link IL2 needs to be  
30 connected to outlet link OL2 and inlet link IL2 does not need to be connected to outlet

link OL1. Furthermore in the example of the diagram 500A4, there is no need to drive the signal of inlet link IL1 horizontally beyond outlet link OL1 and hence the inlet link IL1 is not even extended horizontally until the outlet link OL2. Also the absence of direct connect point DCP(2,1) illustrates there is no need to connect inlet link IL2 and outlet  
5 link OL1.

In summary in integrated circuit placement and route tools, the concept of virtual switches and virtual cross points is used during the implementation of the placement & routing algorithmically in software, however during the hardware implementation cross points in the cross state are implemented as hardwired connections between the  
10 corresponding inlet link and outlet link, and in the bar state are implemented as no connection between inlet link and outlet link.

### **3) More Application Embodiments:**

All the embodiments disclosed in the current invention are also useful in the  
15 design of SoC interconnects, Field programmable interconnect chips, parallel computer systems and in time-space-time switches.

Numerous modifications and adaptations of the embodiments, implementations, and examples described herein will be apparent to the skilled artisan in view of the disclosure.

CLAIMS

What is claimed is:

1. An integrated circuit device comprising a plurality of sub-integrated circuit blocks and a routing network, and
- 5 Said each plurality of sub-integrated circuit blocks comprising a plurality of inlet links and a plurality of outlet links; and  
Said routing network interconnects any one of said outlet link of one of said sub-integrated circuit block to one or more said inlet links of one or more of said sub-integrated circuit blocks; and
- 10 Said routing network comprising of a plurality of stages  $y$ , starting from the lowest stage to the highest stage; and  
Said routing network comprising a plurality of switches of size  $d \times d$ , where  $d \geq 2$ , in each said stage and each said switch of size  $d \times d$  having  $d$  inlet links and  $d$  outlet links; and
- 15 Said each sub-integrated circuit block comprising a plurality of said switches corresponding to each said stage; and  
Said each sub-integrated circuit block comprising a plurality of forward connecting links connecting from switches in lower stage to switches in the immediate succeeding higher stage, and also comprising a plurality of backward connecting links
- 20 connecting from switches in higher stage to switches in the immediate preceding lower stage; and  
Said each sub-integrated circuit block comprising a plurality straight links in said forward connecting links from switches in lower stage to switches in the immediate succeeding higher stage and a plurality cross links in said forward connecting links from
- 25 switches in lower stage to switches in the immediate succeeding higher stage, and further comprising a plurality of straight links in said backward connecting links from switches

in higher stage to switches in the immediate preceding lower stage and a plurality of cross links in said backward connecting links from switches in higher stage to switches in the immediate preceding lower stage.

2. The integrated circuit device of claim 1, wherein said all straight links are  
5 connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and

said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks.

3. The integrated circuit device of claim 2, wherein said plurality of sub-  
10 integrated circuit blocks arranged in a two-dimensional grid.

4. The integrated circuit device of claim 3, wherein said cross links in succeeding stages are connecting as alternative vertical and horizontal links between switches in said sub-integrated circuit blocks.

5. The integrated circuit device of claim 4, wherein said cross links from  
15 switches in a stage in one of said sub-integrated circuit blocks are connecting to switches in the succeeding stage in another of said sub-integrated circuit blocks so that said cross links are either vertical links or horizontal and vice versa, and hereinafter such cross links are “shuffle exchange links”).

6. The integrated circuit device of claim 5, wherein said all horizontal shuffle  
20 exchange links between switches in any two corresponding said succeeding stages are substantially of equal length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are substantially of equal length in the entire said integrated circuit device.

7. The integrated circuit device of claim 6, wherein the shortest horizontal  
25 shuffle exchange links are connecting at the lowest stage and between switches in two

nearest neighboring said sub-integrated circuit blocks, and length of the horizontal shuffle exchange links is doubled in each succeeding stage; and the shortest vertical shuffle exchange links are connecting at the lowest stage and between switches in two nearest neighboring said sub-integrated circuit blocks, and length of the vertical shuffle exchange links is doubled in each succeeding stage.

8. The integrated circuit device of claim 7, wherein  $y \geq (\log_2 N)$  so that the length of the horizontal shuffle exchange links in the highest stage is equal to half the size of the horizontal size of said two dimensional grid of sub-integrated circuit blocks and the length of the vertical shuffle exchange links in the highest stage is equal to half the size of the vertical size of said two dimensional grid of sub-integrated circuit blocks.

9. The integrated circuit device of claim 8, wherein  $d = 2$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast Benes network with full bandwidth.

10. The integrated circuit device of claim 8, wherein  $d = 2$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast Benes network and rearrangeably nonblocking for arbitrary fan-out multicast Benes network with full bandwidth.

11. The integrated circuit device of claim 8, wherein  $d = 2$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast Benes network with full bandwidth.

12. The integrated circuit device of claim 7, wherein  $y \geq (\log_2 N)$  so that the length of the horizontal shuffle exchange links in the highest stage is equal to half the size of the horizontal size of said two dimensional grid of sub-integrated circuit blocks and the length of the vertical shuffle exchange links in the highest stage is equal to half the size of the vertical size of said two dimensional grid of sub-integrated circuit blocks, and  
5 said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks.

13. The integrated circuit device of claim 12, wherein  $d = 2$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said  
10 forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast butterfly fat tree network with full bandwidth.

14. The integrated circuit device of claim 12, wherein  $d = 2$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting  
15 said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast butterfly fat tree network and rearrangeably nonblocking for arbitrary fan-out multicast butterfly fat tree network with  
20 full bandwidth.

15. The integrated circuit device of claim 12, wherein  $d = 2$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting  
said forward connecting links and there are at least three switches in each said stage in  
each said sub-integrated circuit block connecting said backward connecting links and said  
25 routing network is strictly nonblocking for arbitrary fan-out multicast butterfly fat tree network with full bandwidth.



16. The integrated circuit device of claim 1, wherein said horizontal and vertical links are implemented on two or more metal layers.
17. The integrated circuit device of claim 1, wherein said switches comprising active and reprogrammable cross points and said each cross point is programmable by an SRAM cell or a Flash Cell.
18. The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks are of equal die size.
19. The integrated circuit device of claim 16, wherein said sub-integrated circuit blocks are Lookup Tables (hereinafter "LUTs") and said integrated circuit device is a field programmable gate array (FPGA) device or field programmable gate array (FPGA) block embedded in another integrated circuit device.
20. The integrated circuit device of claim 16, wherein said sub-integrated circuit blocks are AND or OR gates and said integrated circuit device is a programmable logic device (PLD).
21. The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks comprising any arbitrary hardware logic or memory circuits.
22. The integrated circuit device of claim 1, wherein said switches comprising active one-time programmable cross points and said integrated circuit device is a mask programmable gate array (MPGA) device or a structured ASIC device.
23. The integrated circuit device of claim 1, wherein said switches comprising passive cross points or just connection of two links or not and said integrated circuit device is a Application Specific Integrated Circuit (ASIC) device.
24. The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks further recursively comprise one or more super-sub-integrated circuit blocks and a sub-routing network.

25. The integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and  $y \geq (\log_2 N)$ .

5 26. The integrated circuit device of claim 25, wherein  $d = 2$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized multi-stage network with  
10 full bandwidth.

27. The integrated circuit device of claim 25, wherein  $d = 2$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said  
15 routing network is strictly nonblocking for unicast generalized multi-stage network and rearrangeably nonblocking for arbitrary fan-out multicast generalized multi-stage network with full bandwidth.

28. The integrated circuit device of claim 25, wherein  $d = 2$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting  
20 said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized multi-stage network with full bandwidth.

29. The integrated circuit device of claim 5, wherein said all horizontal shuffle  
25 exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and  $y \geq (\log_2 N)$ , and

said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks.

30. The integrated circuit device of claim 29, wherein  $d = 2$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized butterfly fat tree network with full bandwidth.

31. The integrated circuit device of claim 29, wherein  $d = 2$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized butterfly fat tree Network and rearrangeably nonblocking for arbitrary fan-out multicast generalized butterfly fat tree network with full bandwidth.

32. The integrated circuit device of claim 29, wherein  $d = 2$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized butterfly fat tree network with full bandwidth.

33. The integrated circuit device of claim 1, wherein said straight links connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and said cross links are connecting as vertical or horizontal or diagonal links between two different said sub-integrated circuit blocks.

34. The integrated circuit device of claim 8, wherein  $d = 4$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing  
5 network is rearrangeably nonblocking for unicast multi-link Benes network with full bandwidth.

35. The integrated circuit device of claim 8, wherein  $d = 4$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in  
10 each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast multi-link Benes network and rearrangeably nonblocking for arbitrary fan-out multicast multi-link Benes network with full bandwidth.

36. The integrated circuit device of claim 8, wherein  $d = 4$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting  
15 said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast multi-link Benes network with full bandwidth.

20 37. The integrated circuit device of claim 12, wherein  $d = 4$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing  
25 network is rearrangeably nonblocking for unicast multi-link butterfly fat tree network with full bandwidth.

38. The integrated circuit device of claim 12, wherein  $d = 4$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in

each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast multi-link butterfly fat tree network and rearrangeably nonblocking for arbitrary fan-out multicast multi-link butterfly fat tree network with full bandwidth.

5           39.     The integrated circuit device of claim 12, wherein  $d = 4$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast multi-link butterfly  
10 fat tree network with full bandwidth.

40.     The integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and  $y \geq (\log_2 N)$ .

15           41.     The integrated circuit device of claim 40, wherein  $d = 4$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized multi-link multi-stage  
20 network with full bandwidth.

42.     The integrated circuit device of claim 40, wherein  $d = 4$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said  
25 routing network is strictly nonblocking for unicast generalized multi-link multi-stage network and rearrangeably nonblocking for arbitrary fan-out multicast generalized multi-link multi-stage network with full bandwidth.

43. The integrated circuit device of claim 40, wherein  $d = 4$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized multi-link multi-stage network with full bandwidth.

44. The integrated circuit device of claim 5, wherein said all horizontal shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and said vertical shuffle exchange links between switches in any two corresponding said succeeding stages are of different length and  $y \geq (\log_2 N)$ , and said each sub-integrated circuit block further comprising a plurality of U-turn links within switches in each of said stages in each of said sub-integrated circuit blocks.

45. The integrated circuit device of claim 44, wherein  $d = 4$  and there is only one switch in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there is only one switch in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is rearrangeably nonblocking for unicast generalized multi-link butterfly fat tree network with full bandwidth.

46. The integrated circuit device of claim 44, wherein  $d = 4$  and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said forward connecting links and there are at least two switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for unicast generalized multi-link butterfly fat tree Network and rearrangeably nonblocking for arbitrary fan-out multicast generalized multi-link butterfly fat tree network with full bandwidth.

47. The integrated circuit device of claim 44, wherein  $d = 4$  and there are at least three switches in each said stage in each said sub-integrated circuit block connecting

said forward connecting links and there are at least three switches in each said stage in each said sub-integrated circuit block connecting said backward connecting links and said routing network is strictly nonblocking for arbitrary fan-out multicast generalized multi-link butterfly fat tree network with full bandwidth.

5           48.     The integrated circuit device of claim 1, wherein said plurality of forward connecting links use a plurality of buffers to amplify signals driven through them and said plurality of backward connecting links use a plurality of buffers to amplify signals driven through them; and said buffers can be inverting or non-inverting buffers.

10           49.     The integrated circuit device of claim 1, wherein said wherein said all switches of size  $d \times d$  are either fully populated or partially populated.





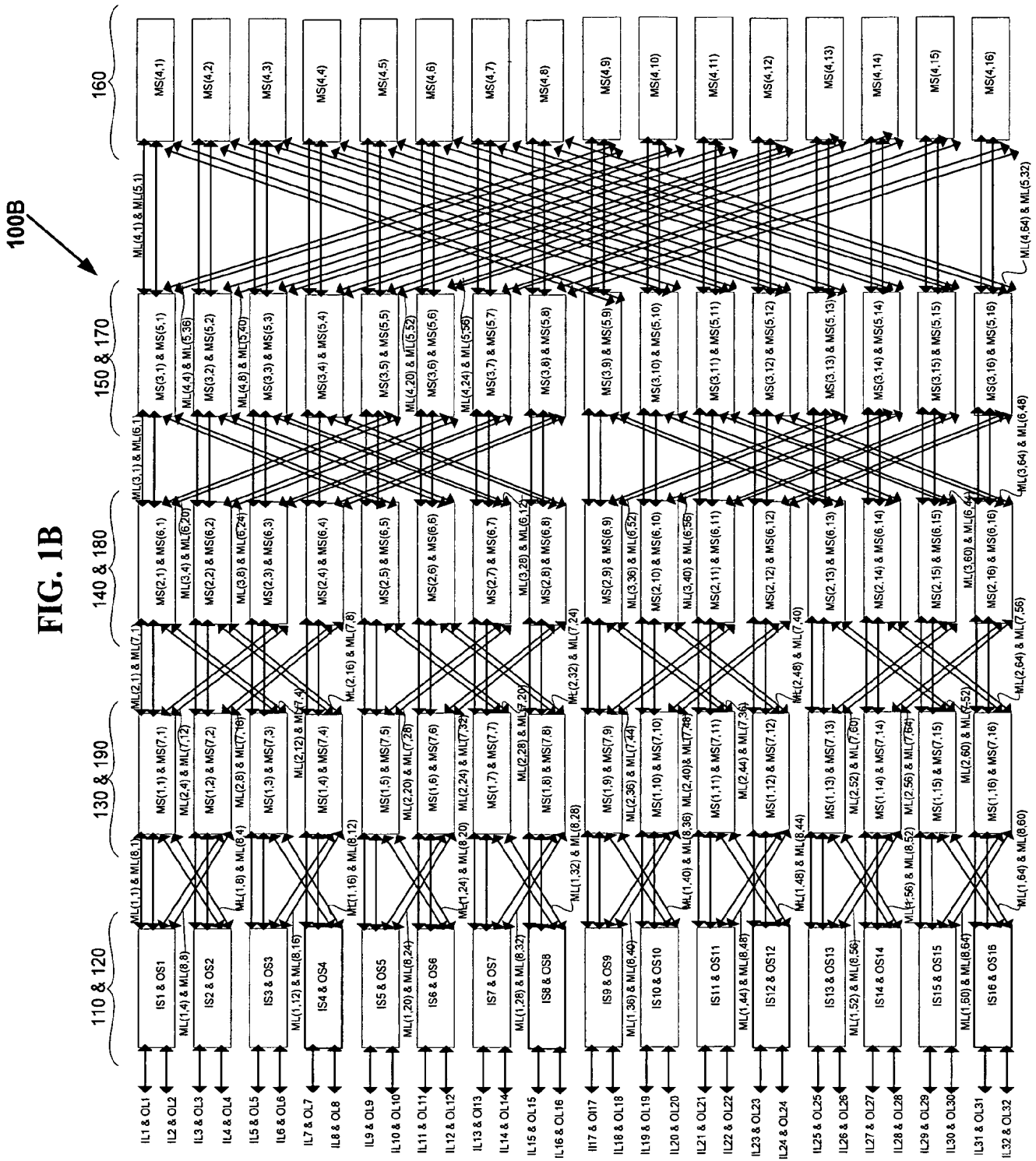
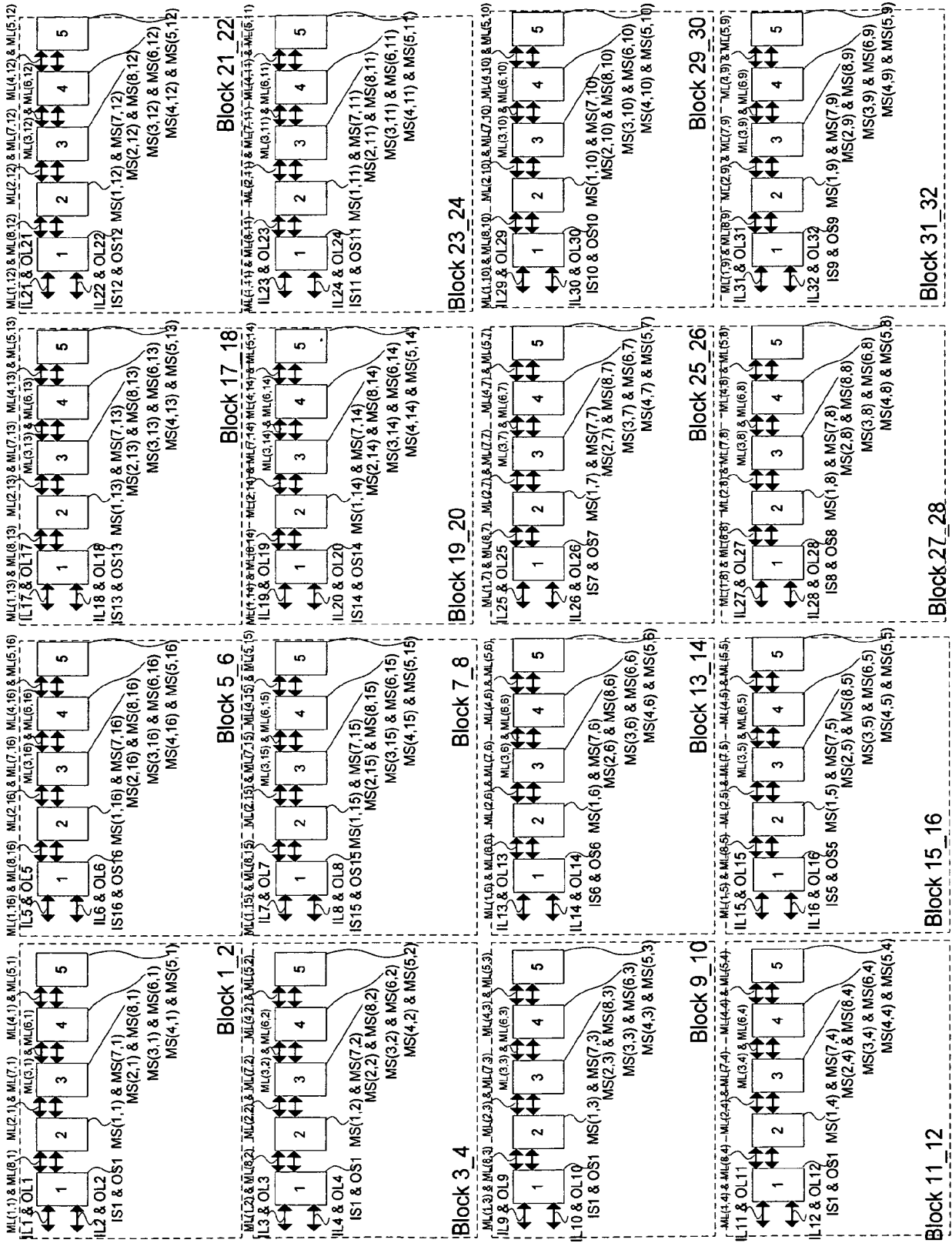


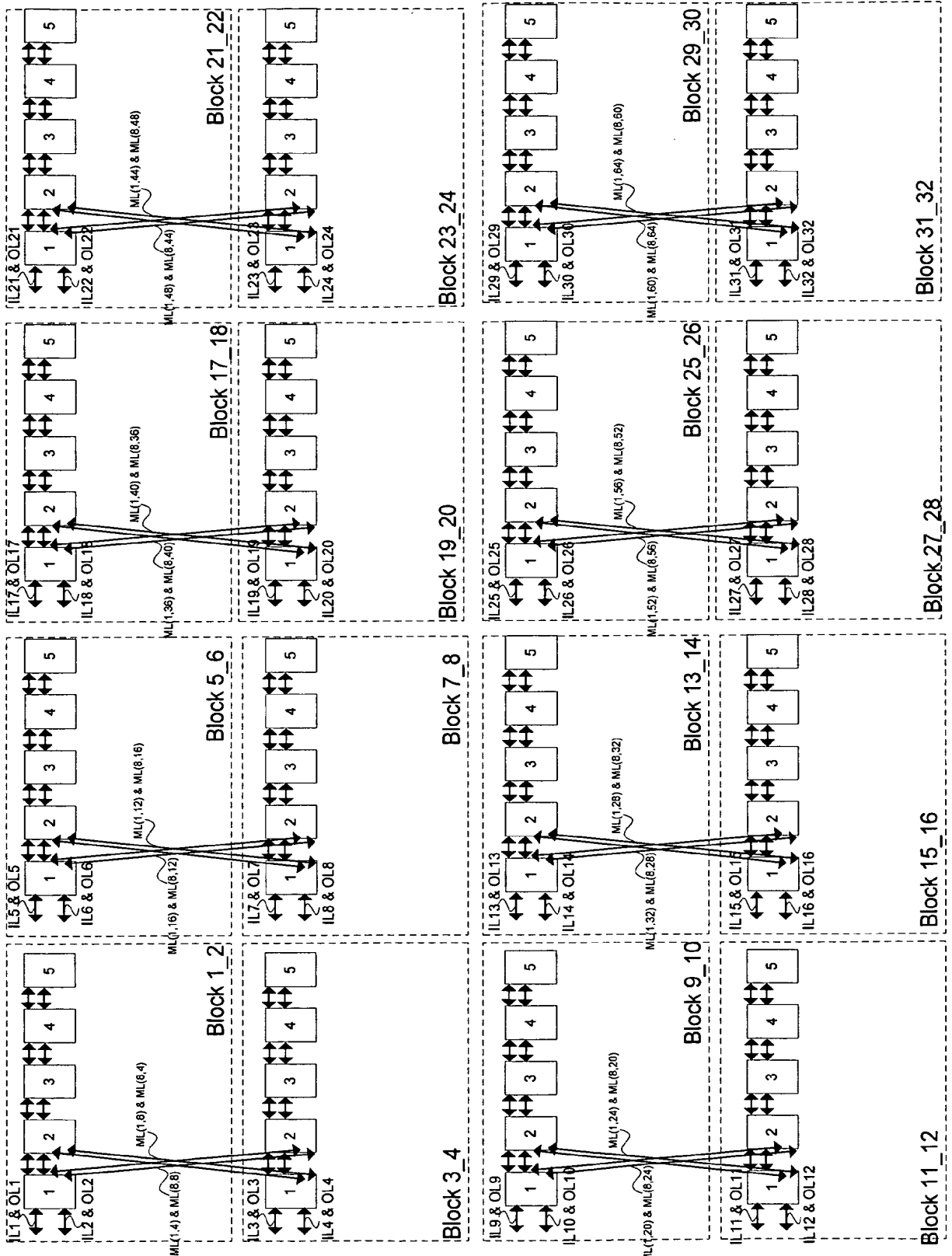
FIG. 1C

100C



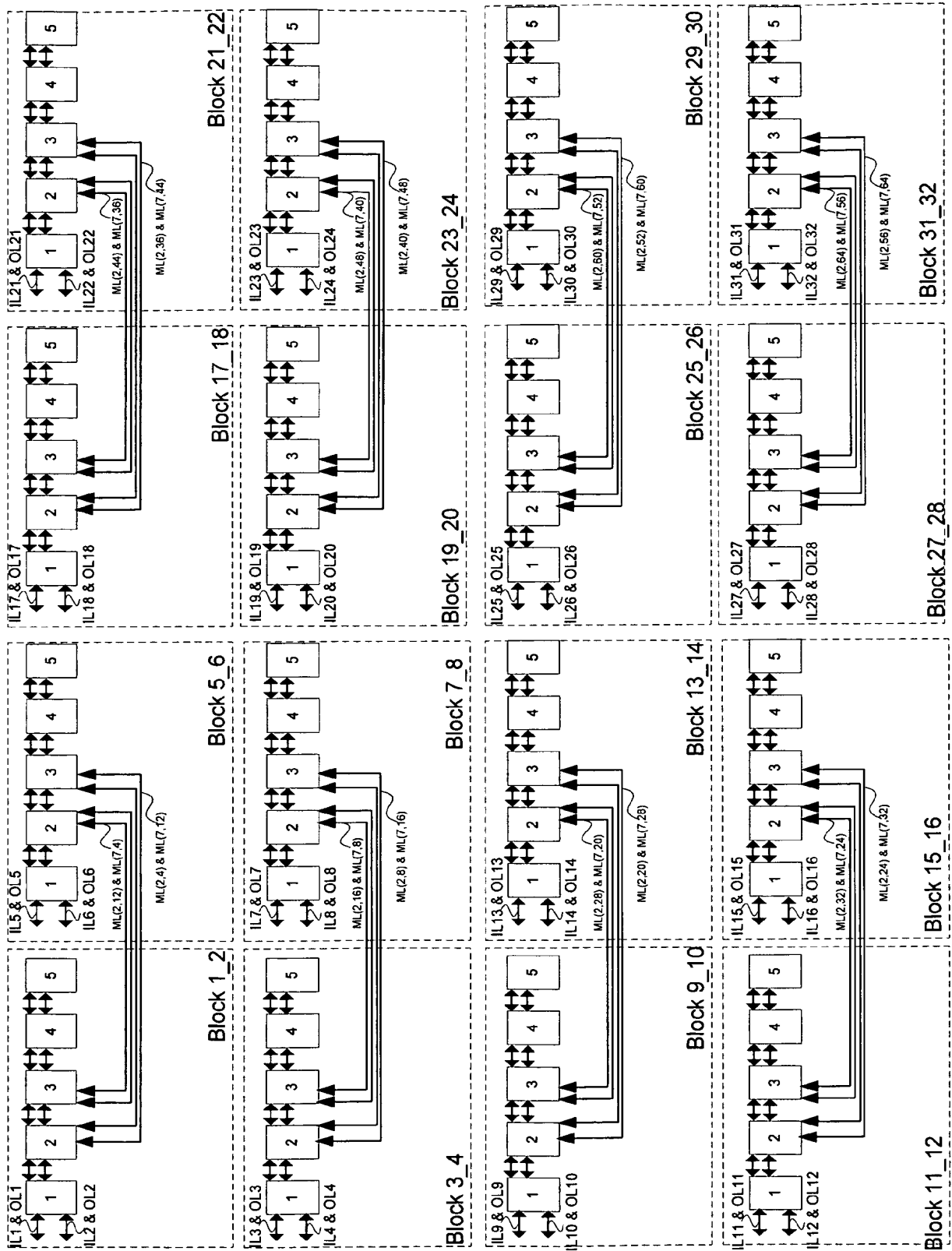
100D

FIG. 1D



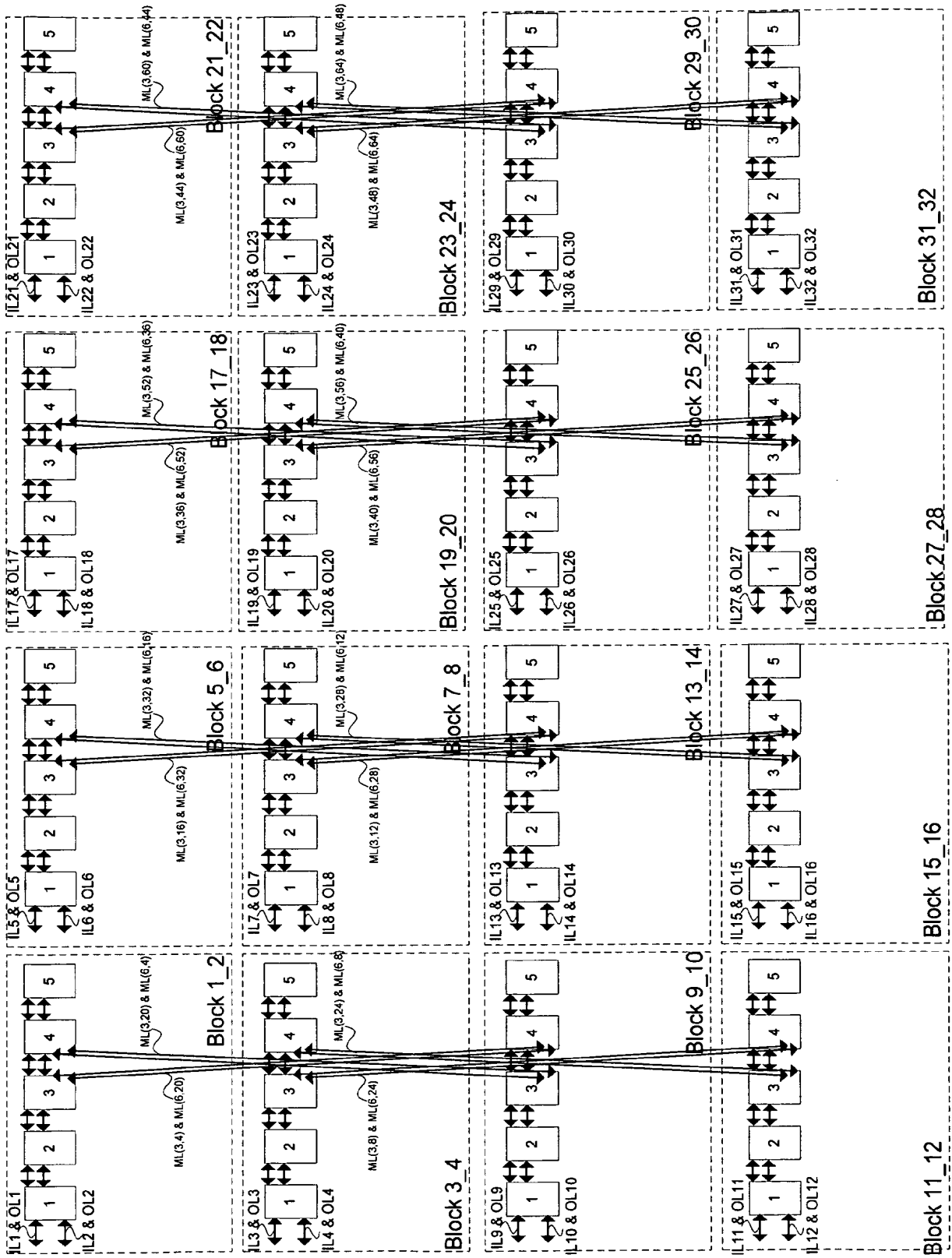
100E

FIG. 1E



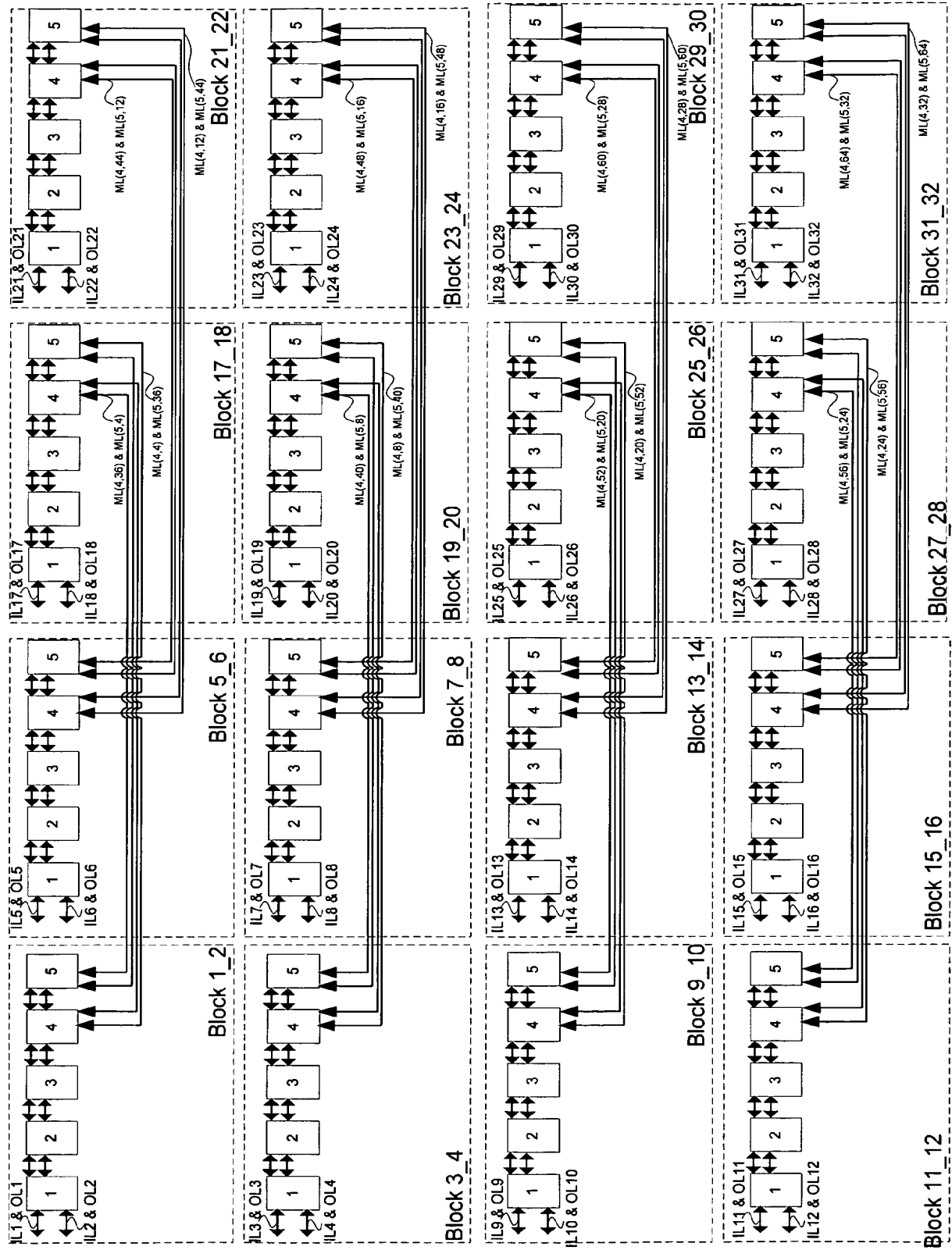
100F

FIG. 1F



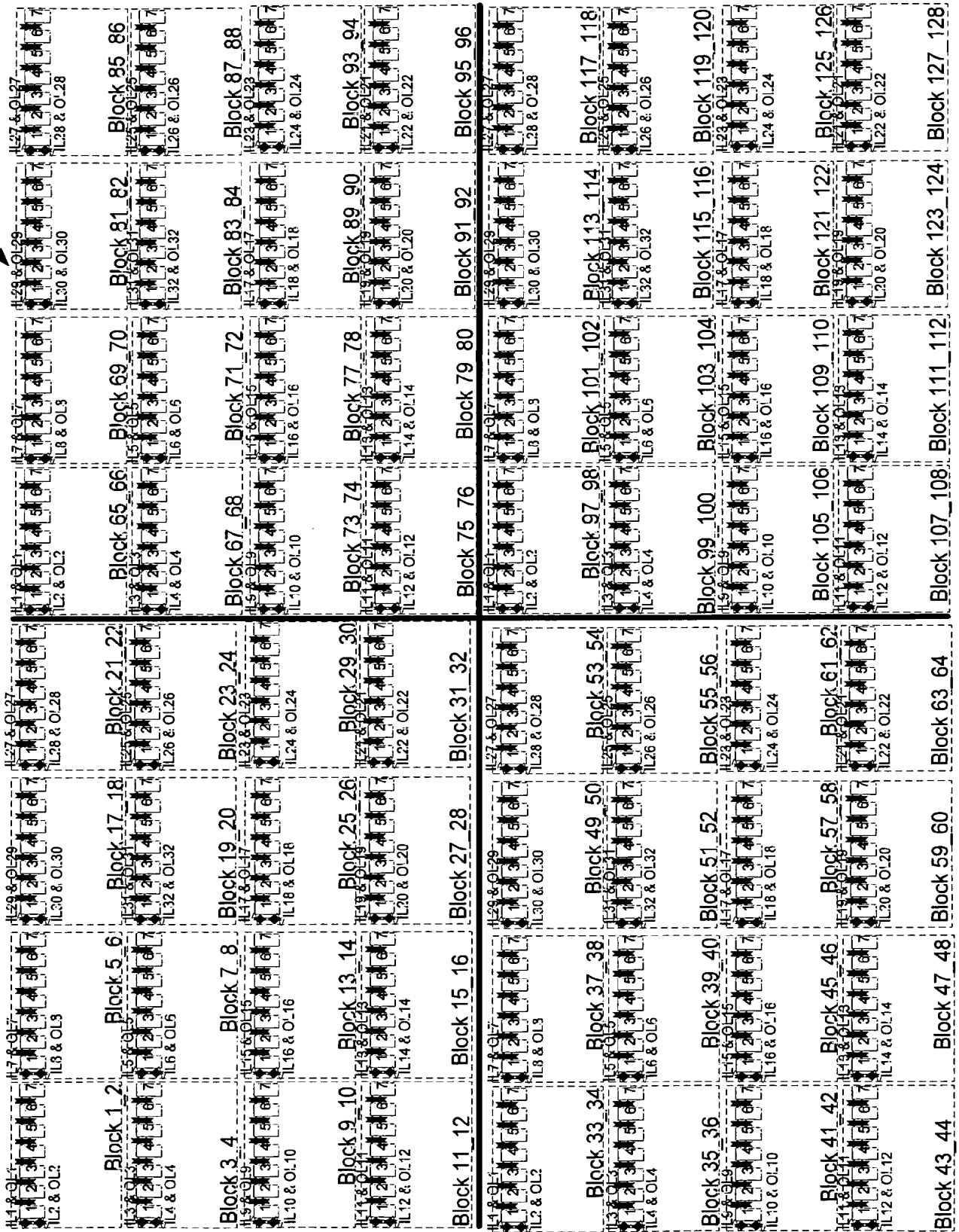
100G

FIG. 1G



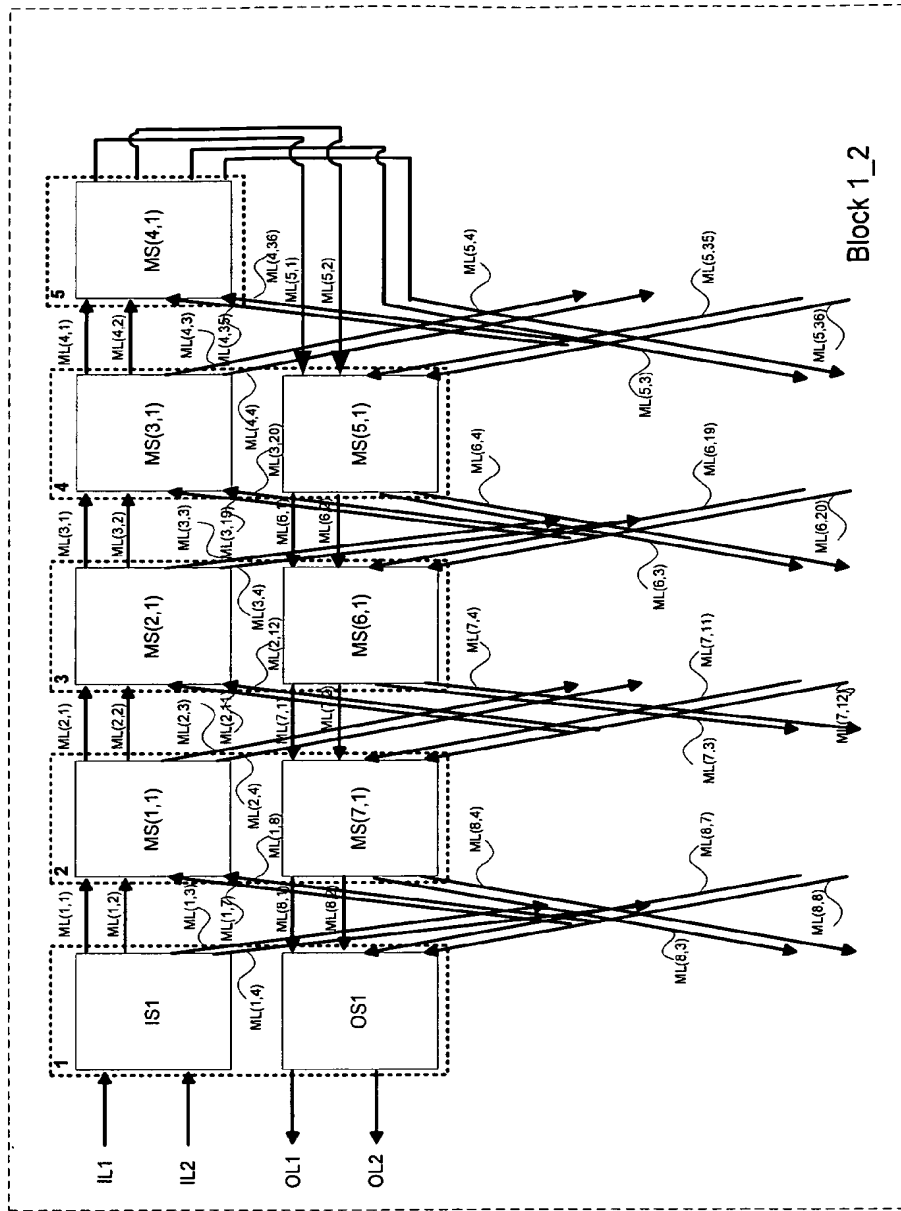
100H

FIG. 1H



1001

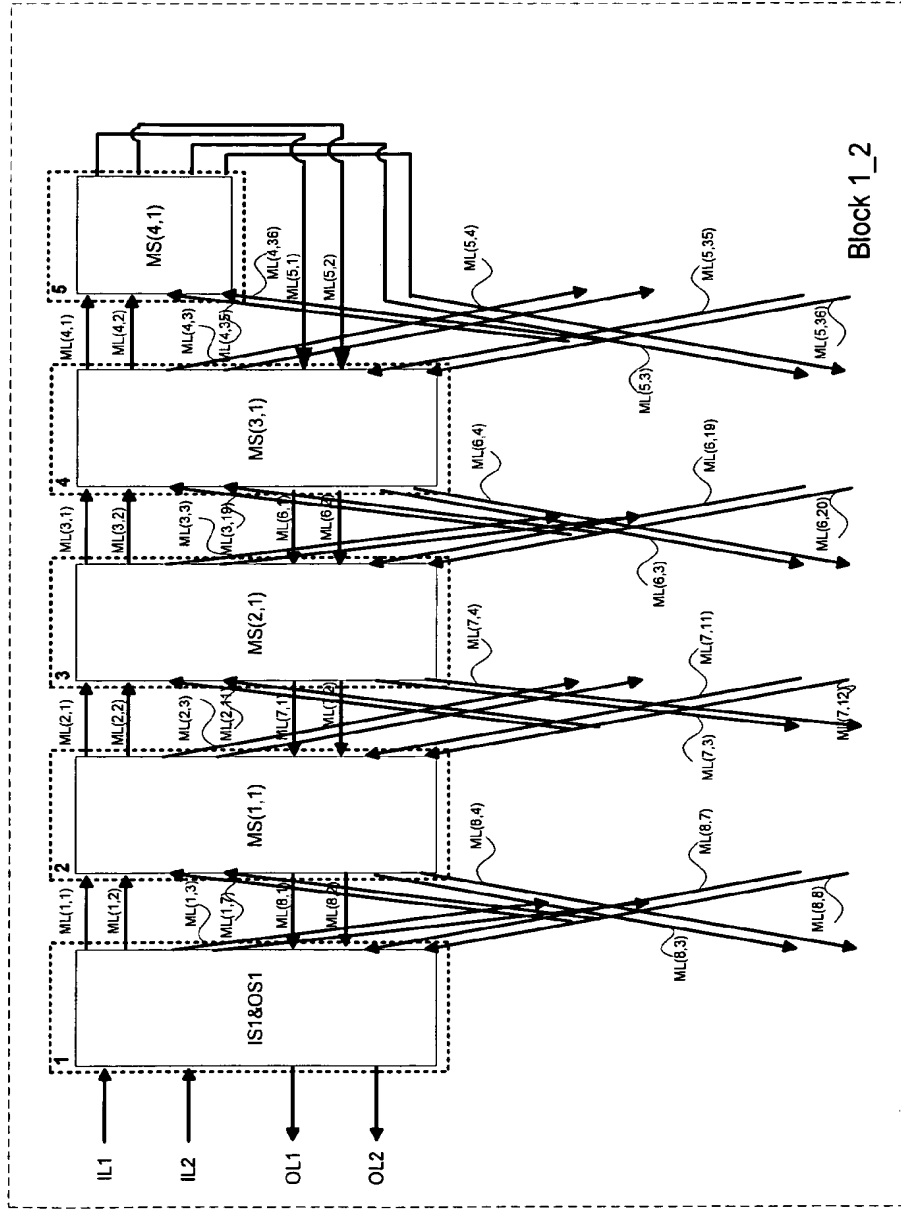
FIG. 11





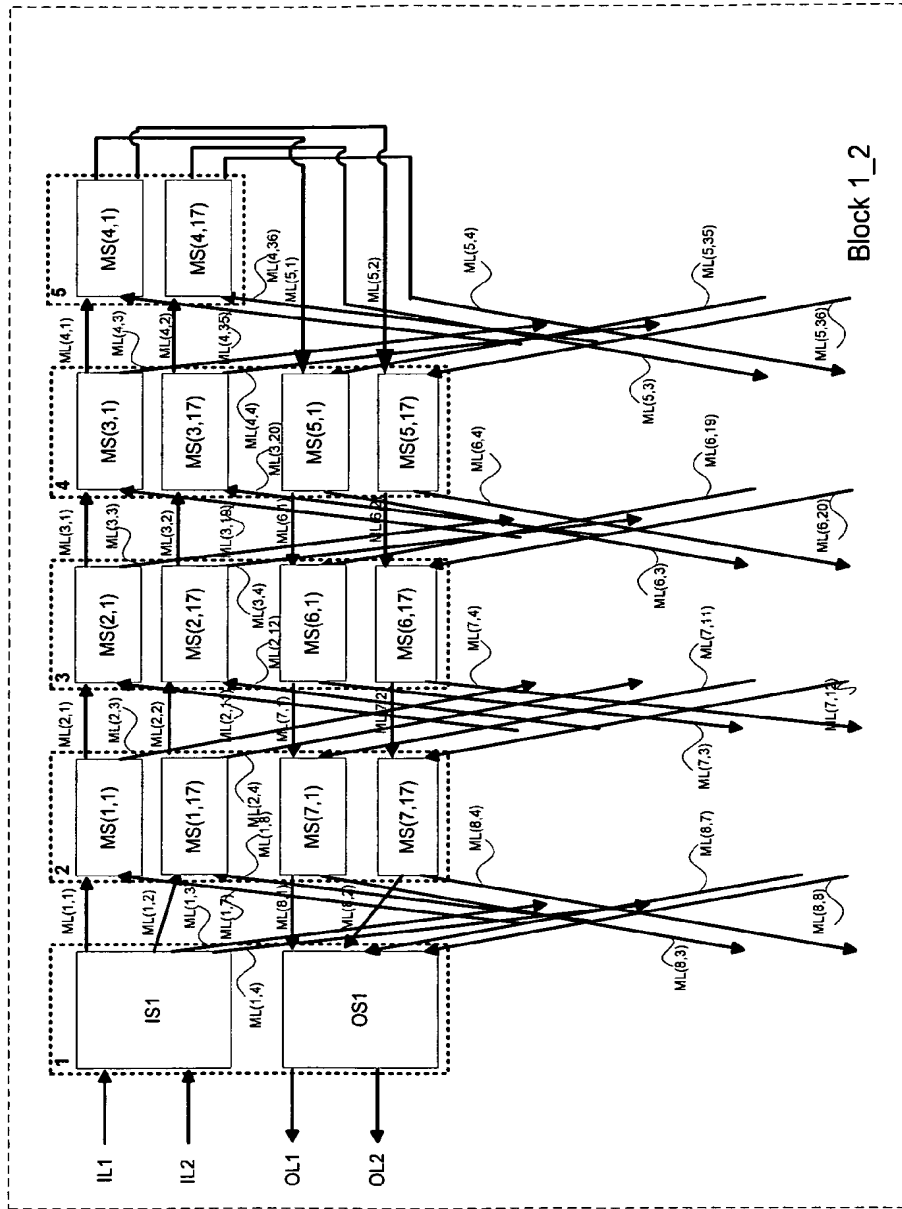
100J

FIG. 1J



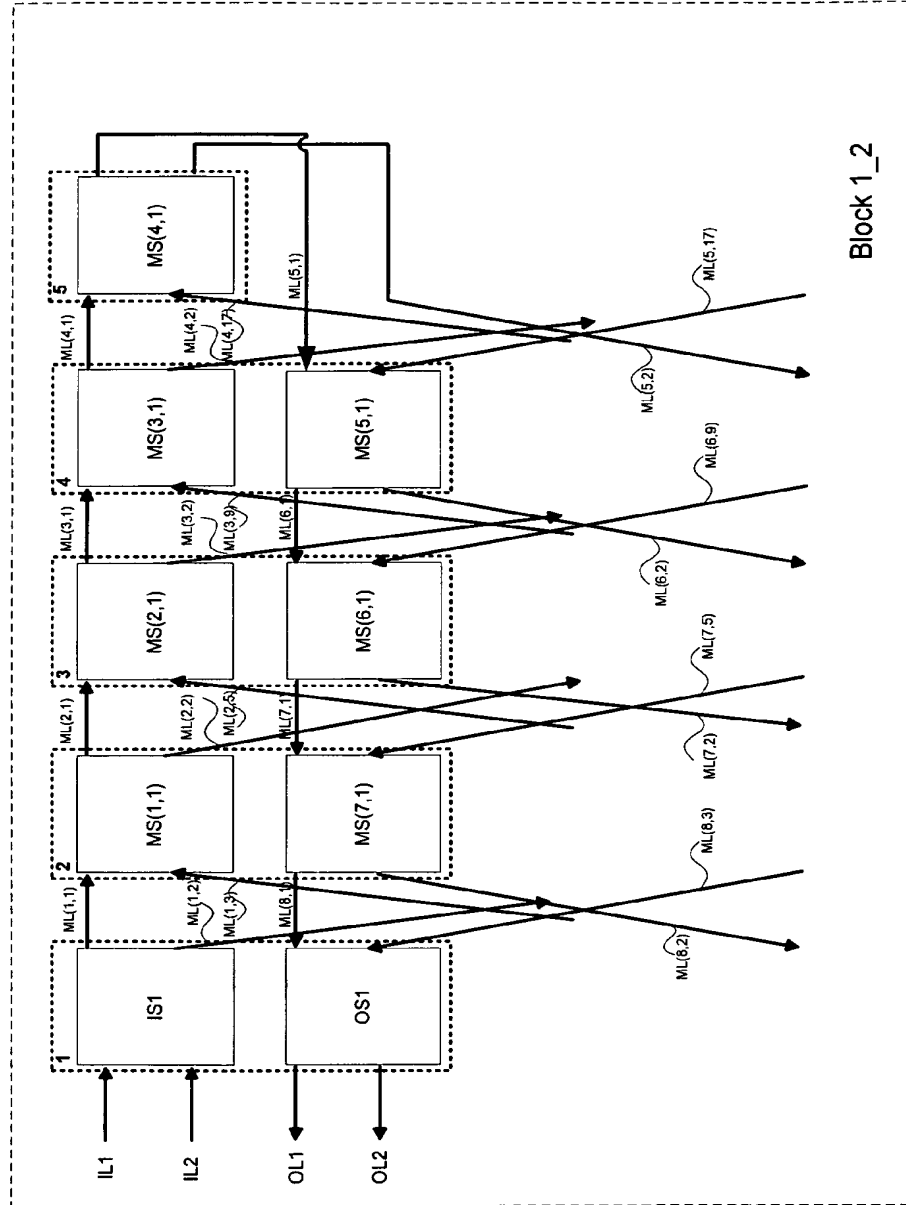
100K

FIG. 1K



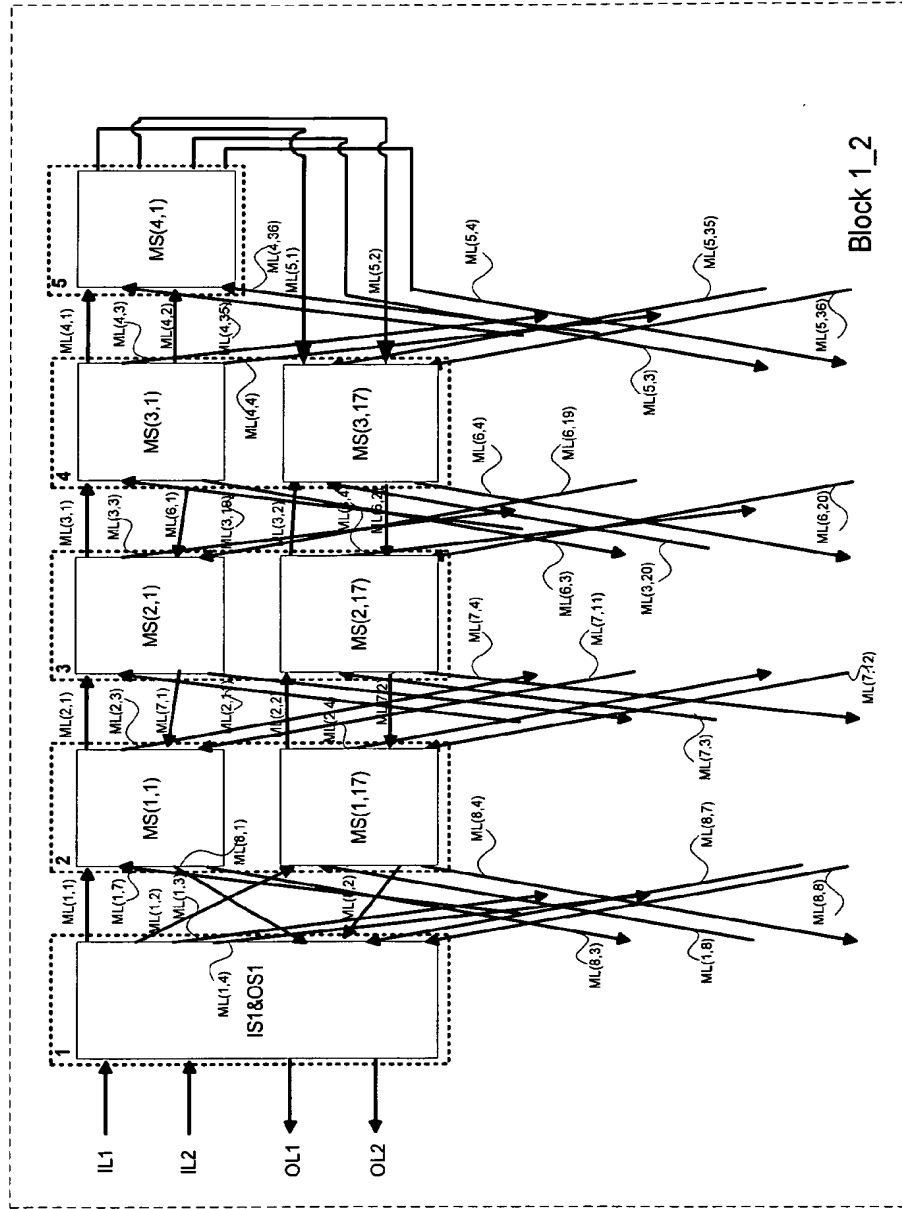
100K1

FIG. 1K1



100L

FIG. 1L



100L1

FIG. 1L1

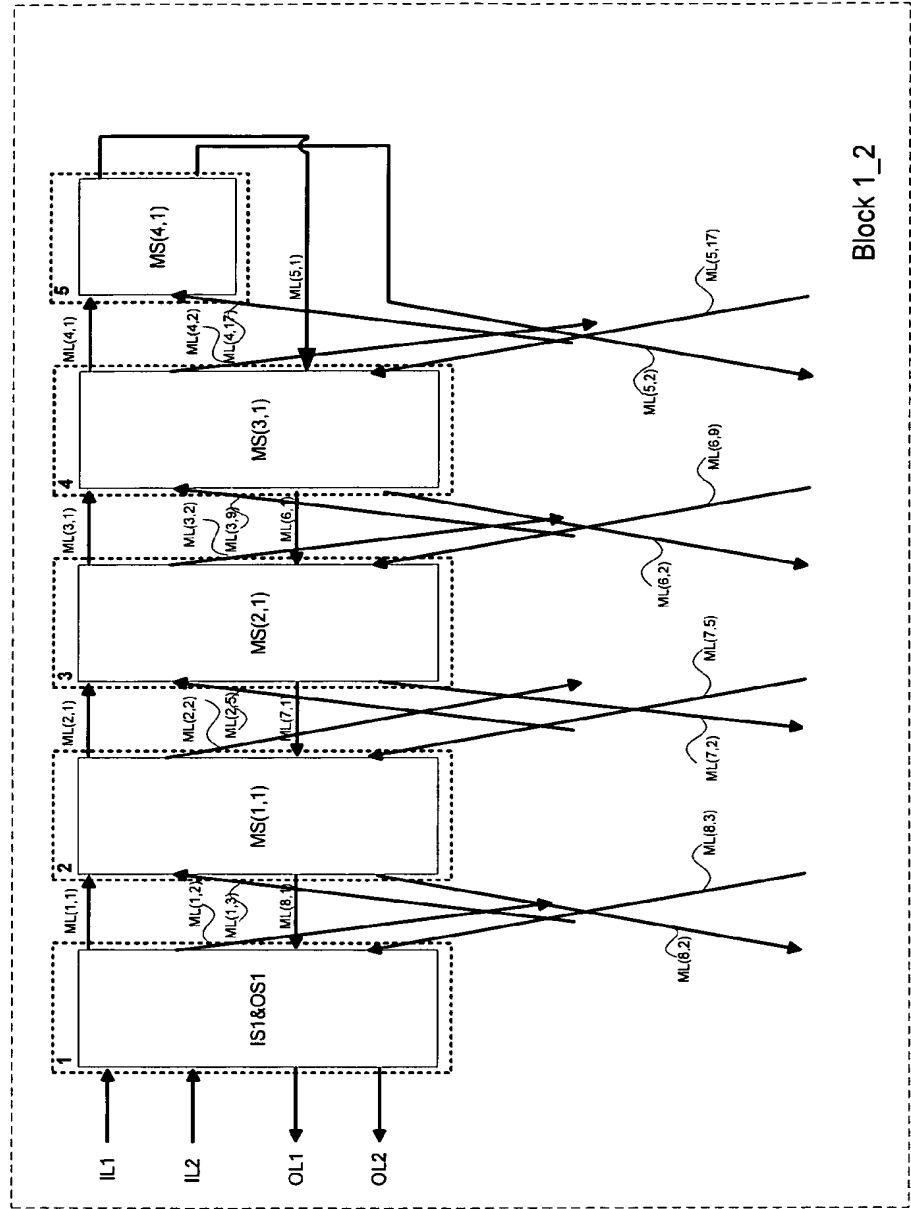


FIG. 2A1

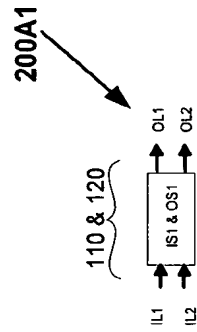


FIG. 2A2

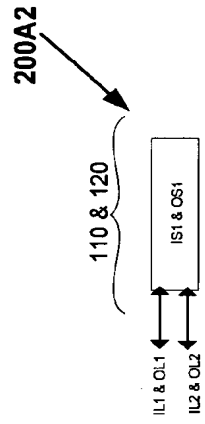
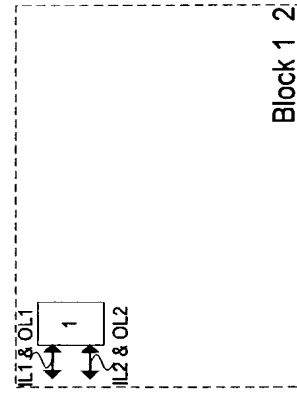


FIG. 2A3

200A3



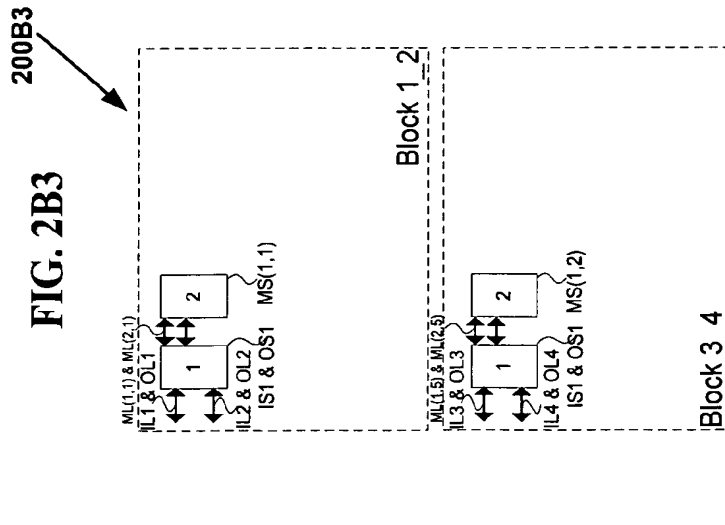
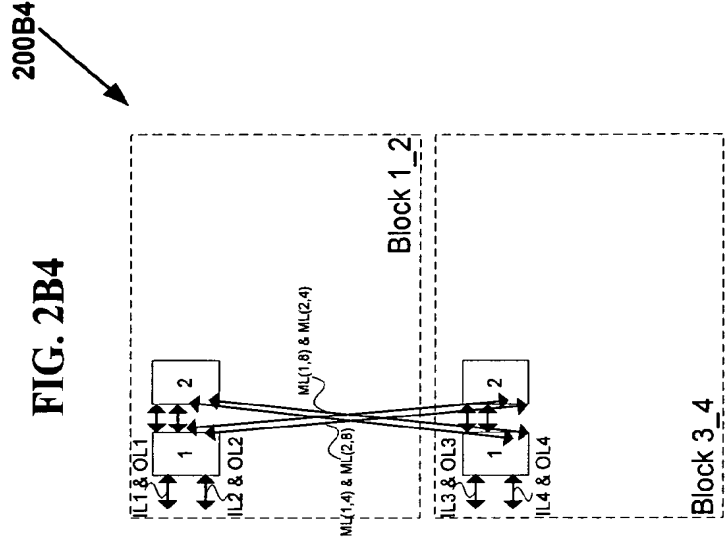
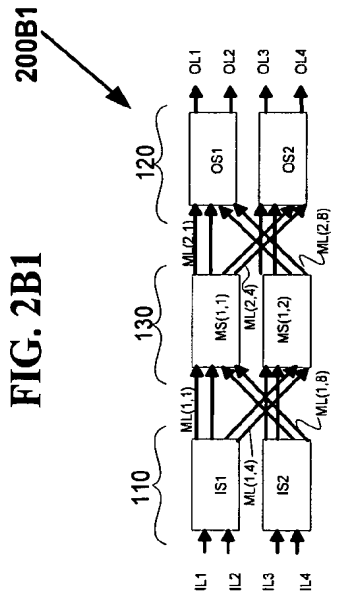
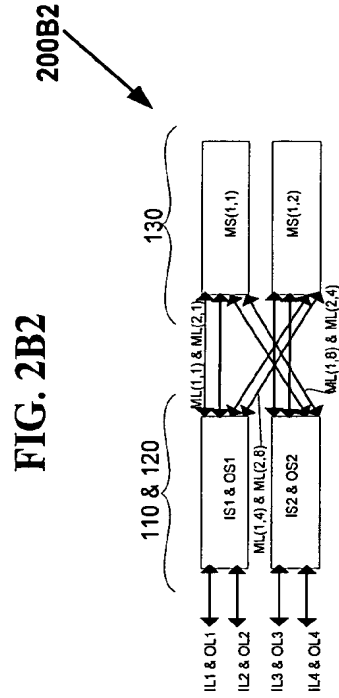


FIG. 2C11

200C11

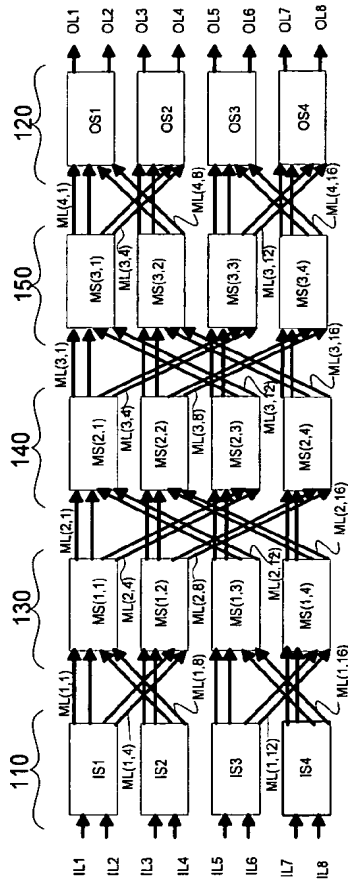


FIG. 2C12

200C12

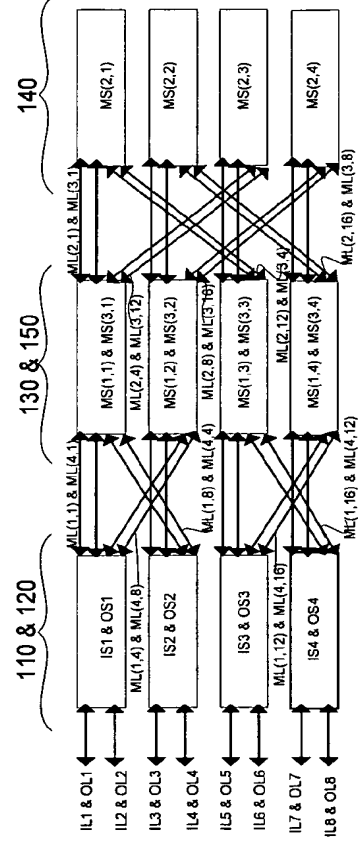
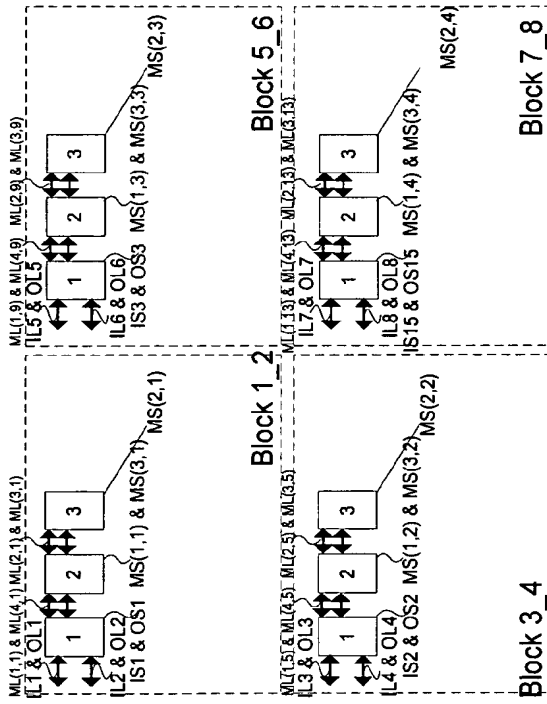


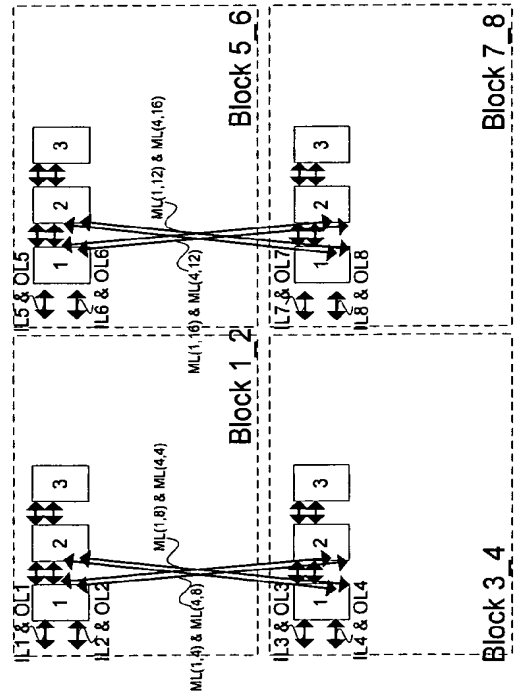


FIG. 2C21



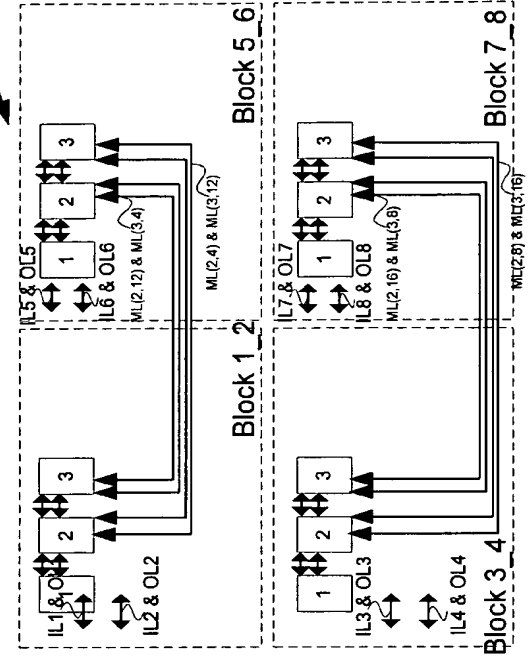
200C21

FIG. 2C22



200C22

FIG. 2C23



200C23

FIG. 2D1

200D1

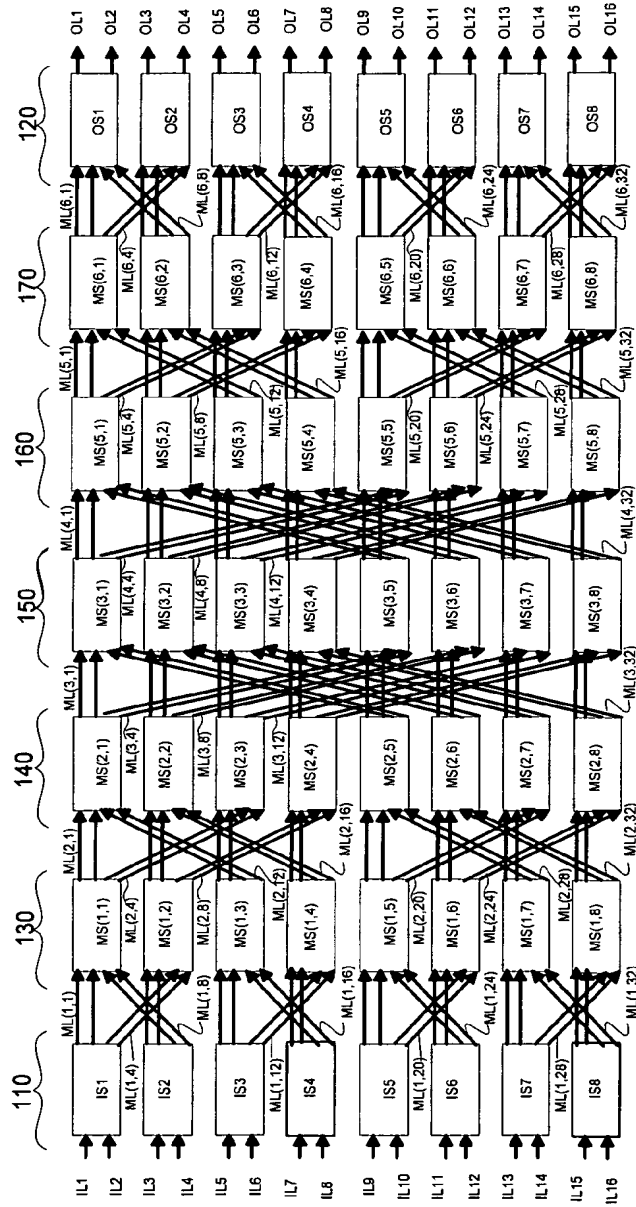
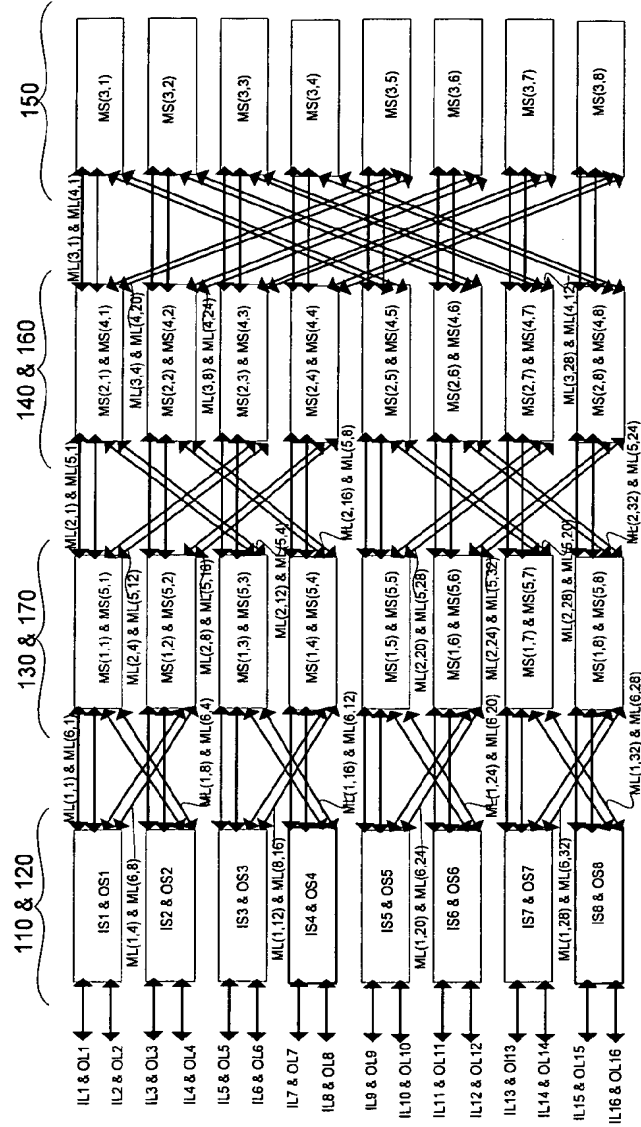


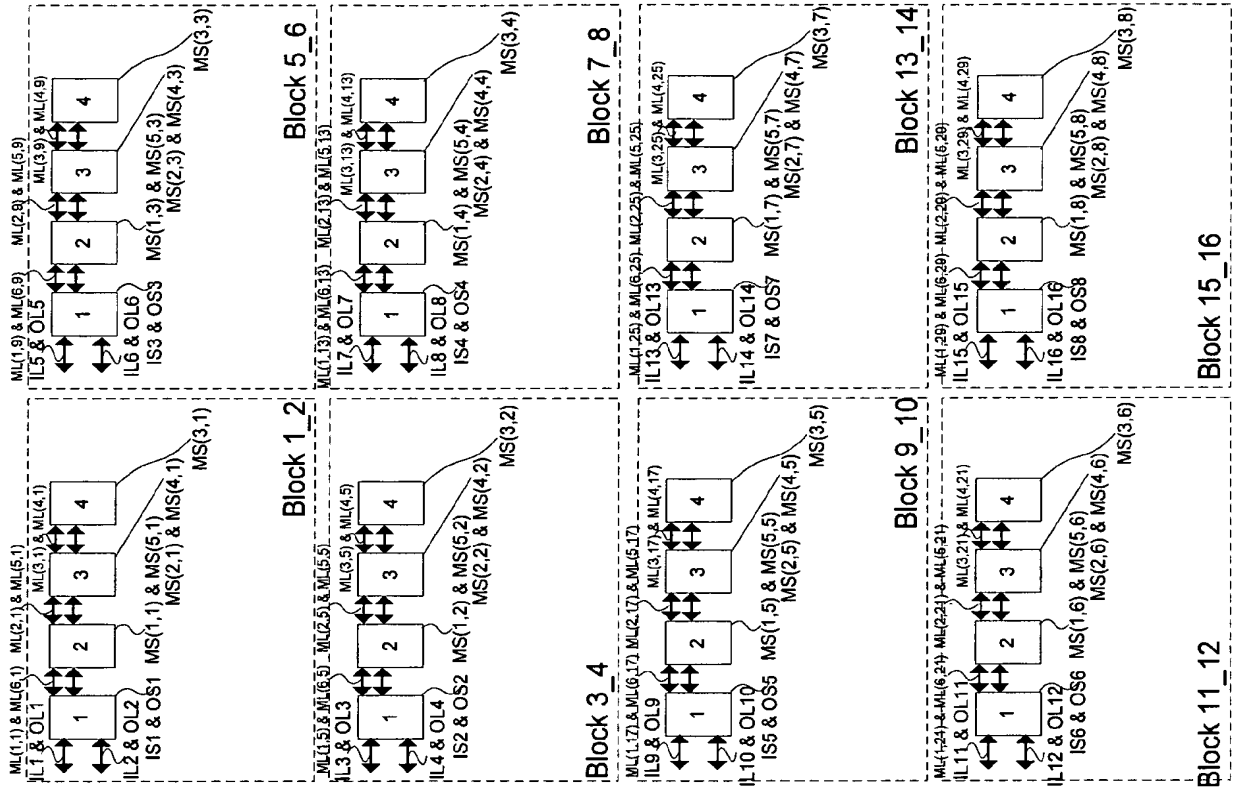
FIG. 2D2

200D2



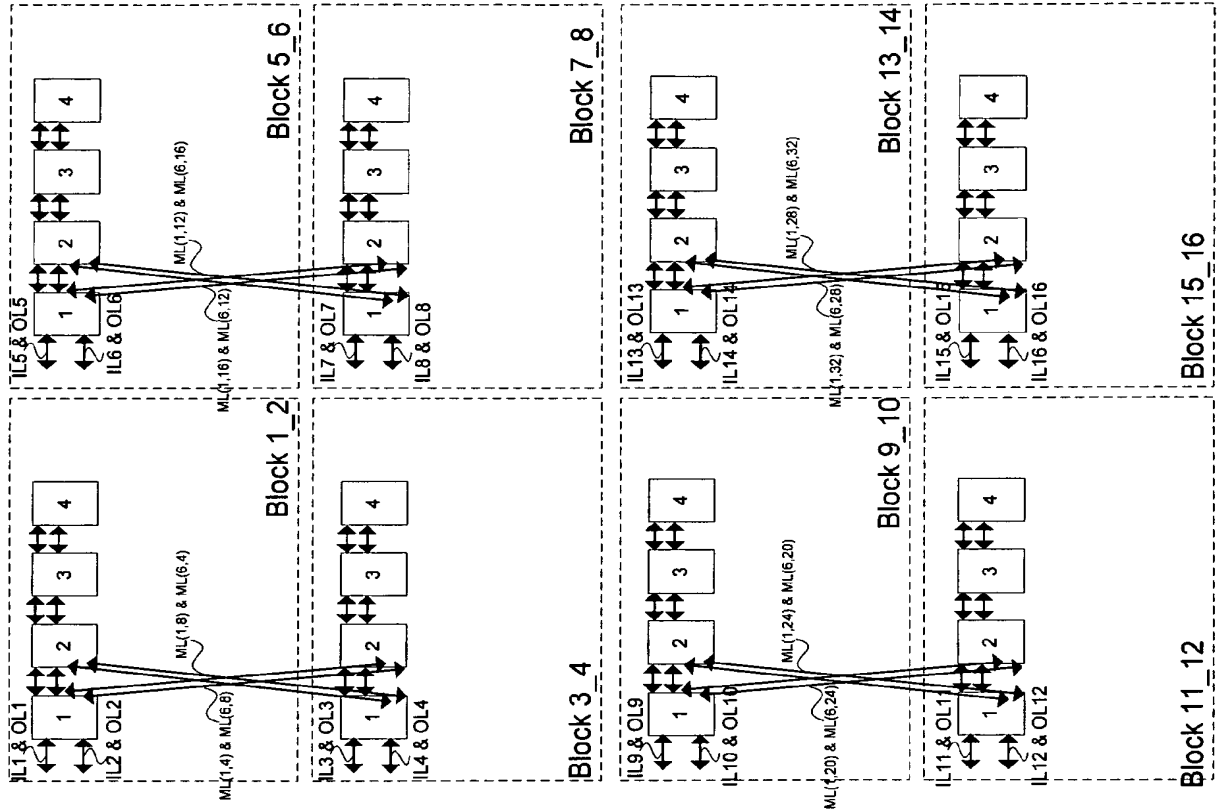
200D3

FIG. 2D3



200D4

FIG. 2D4



200D5

FIG. 2D5

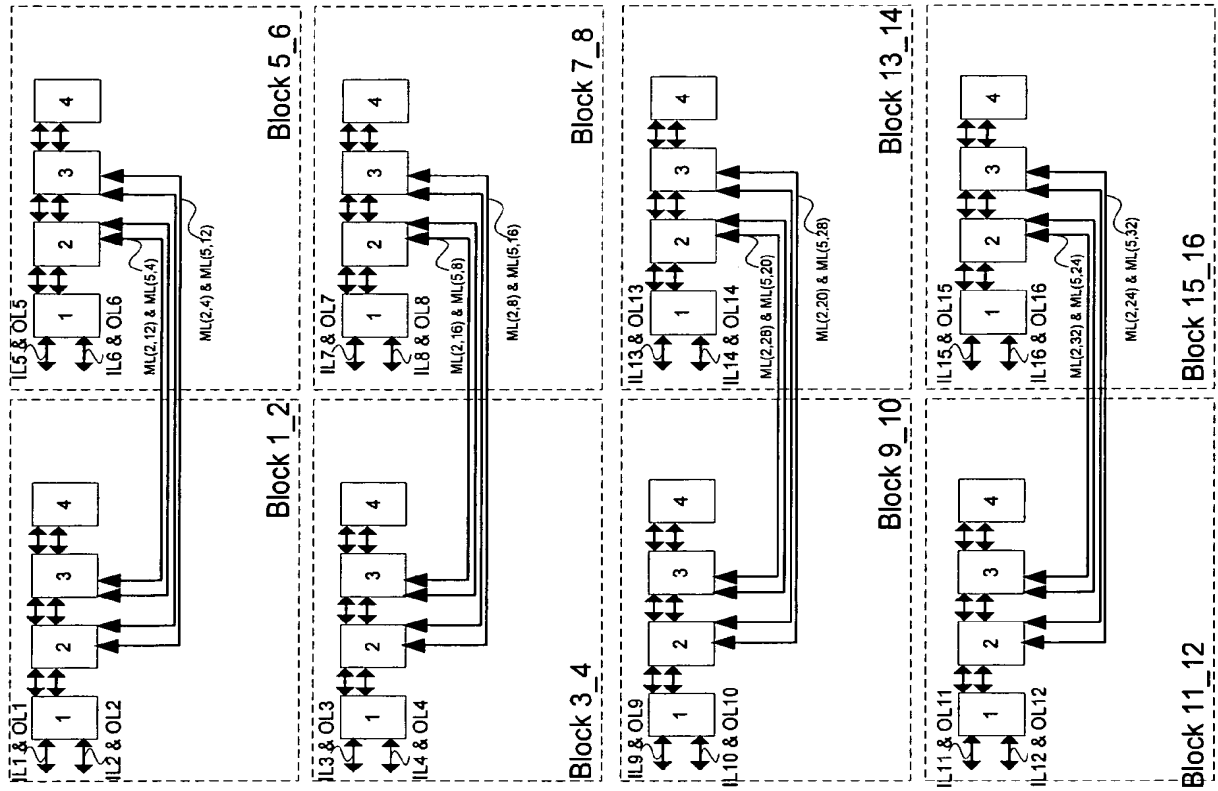
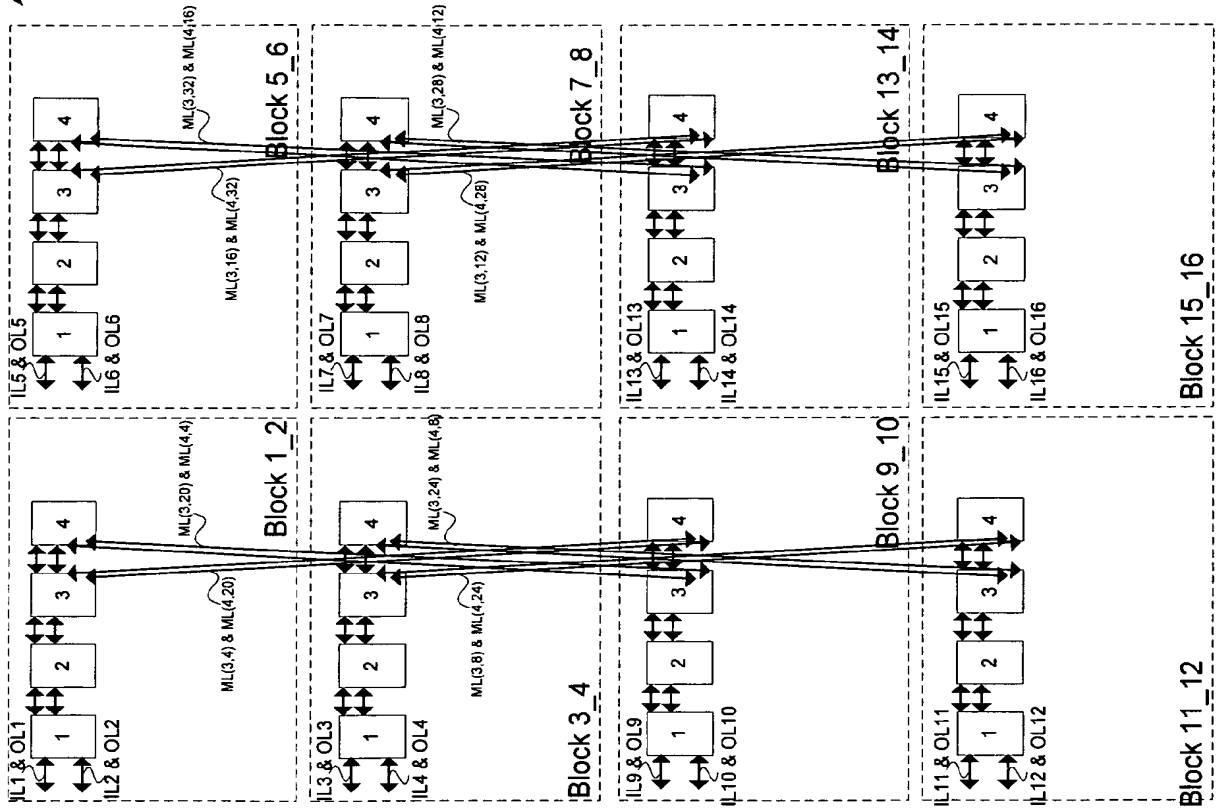
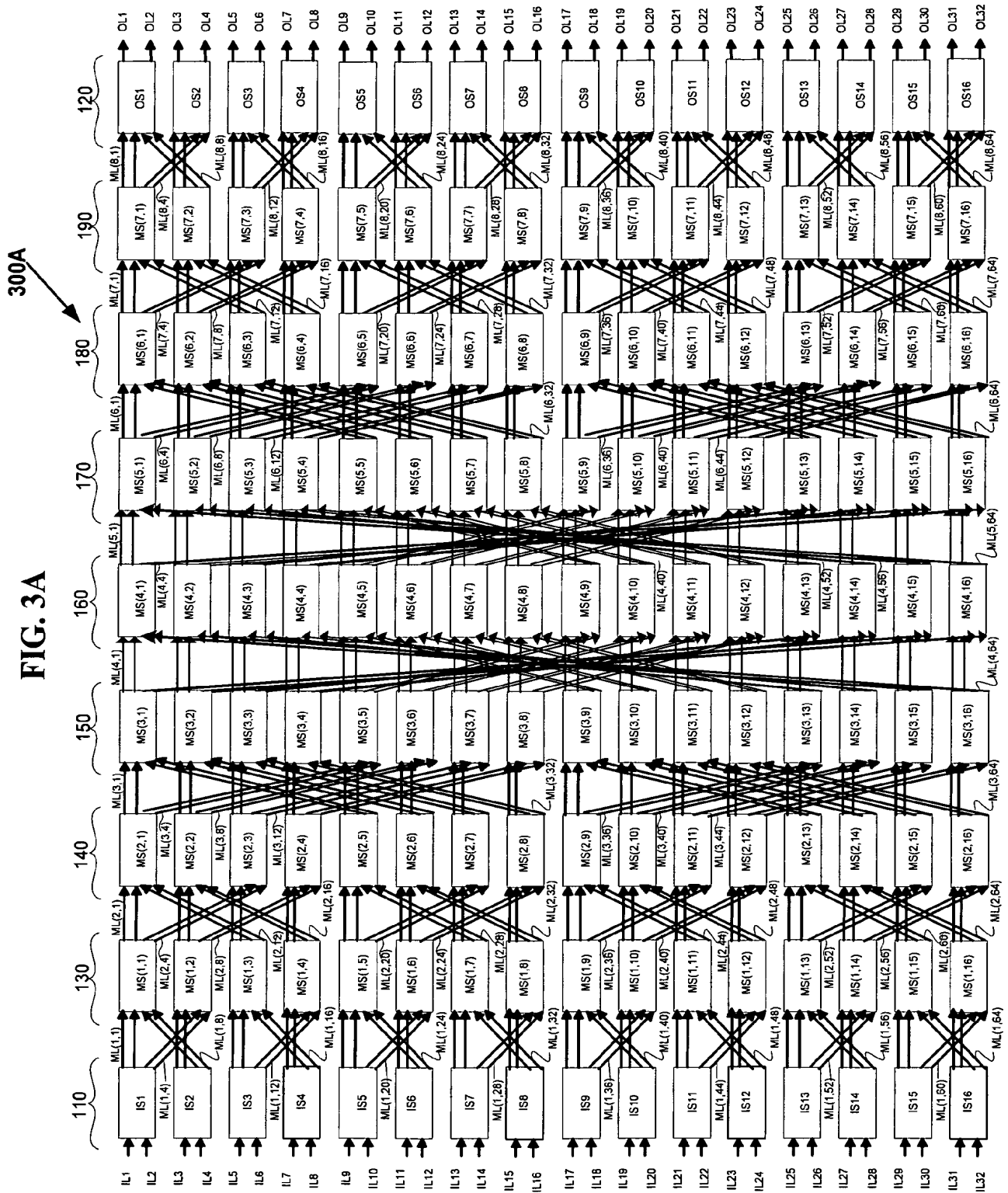


FIG. 2D6

200D6







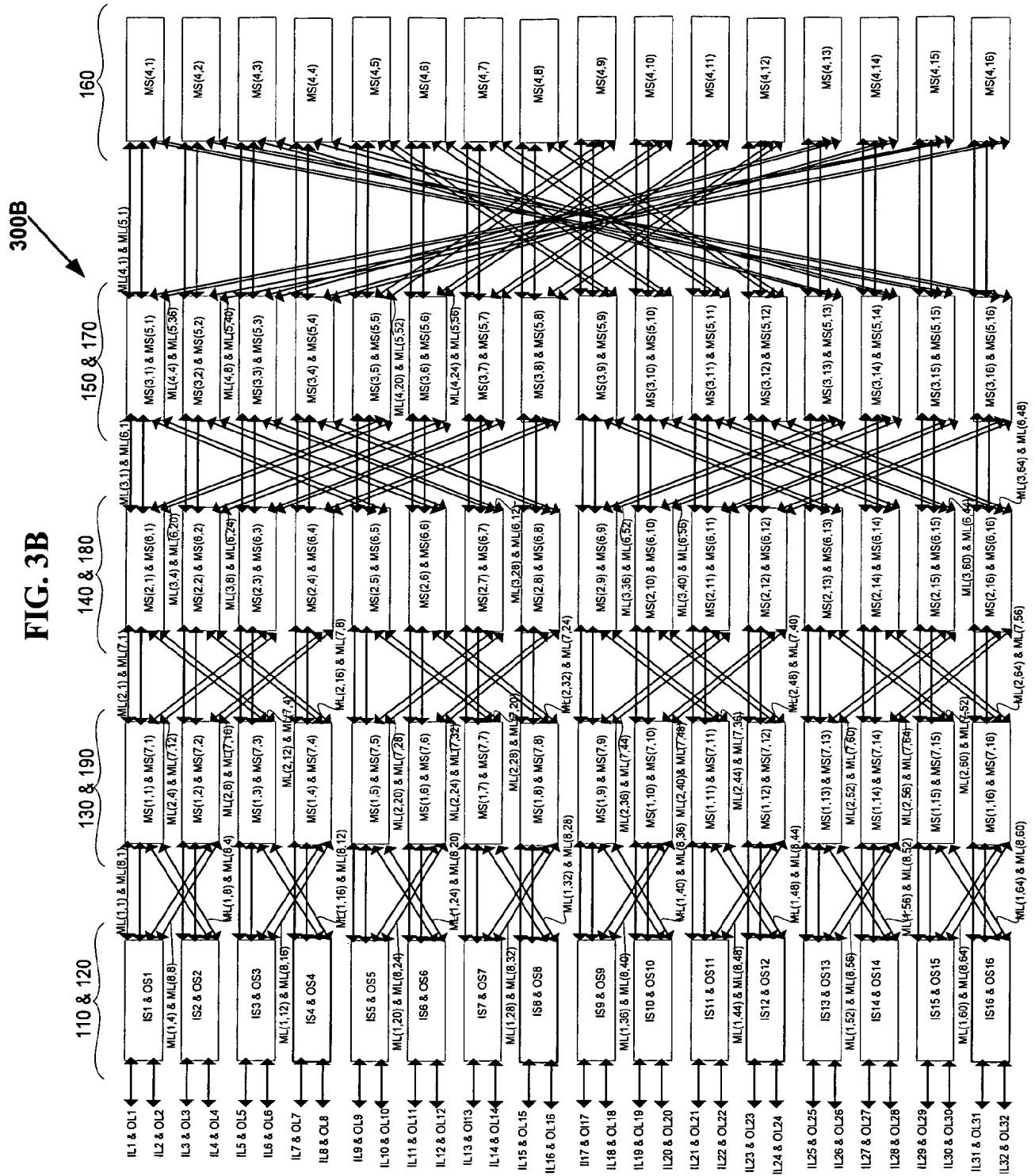
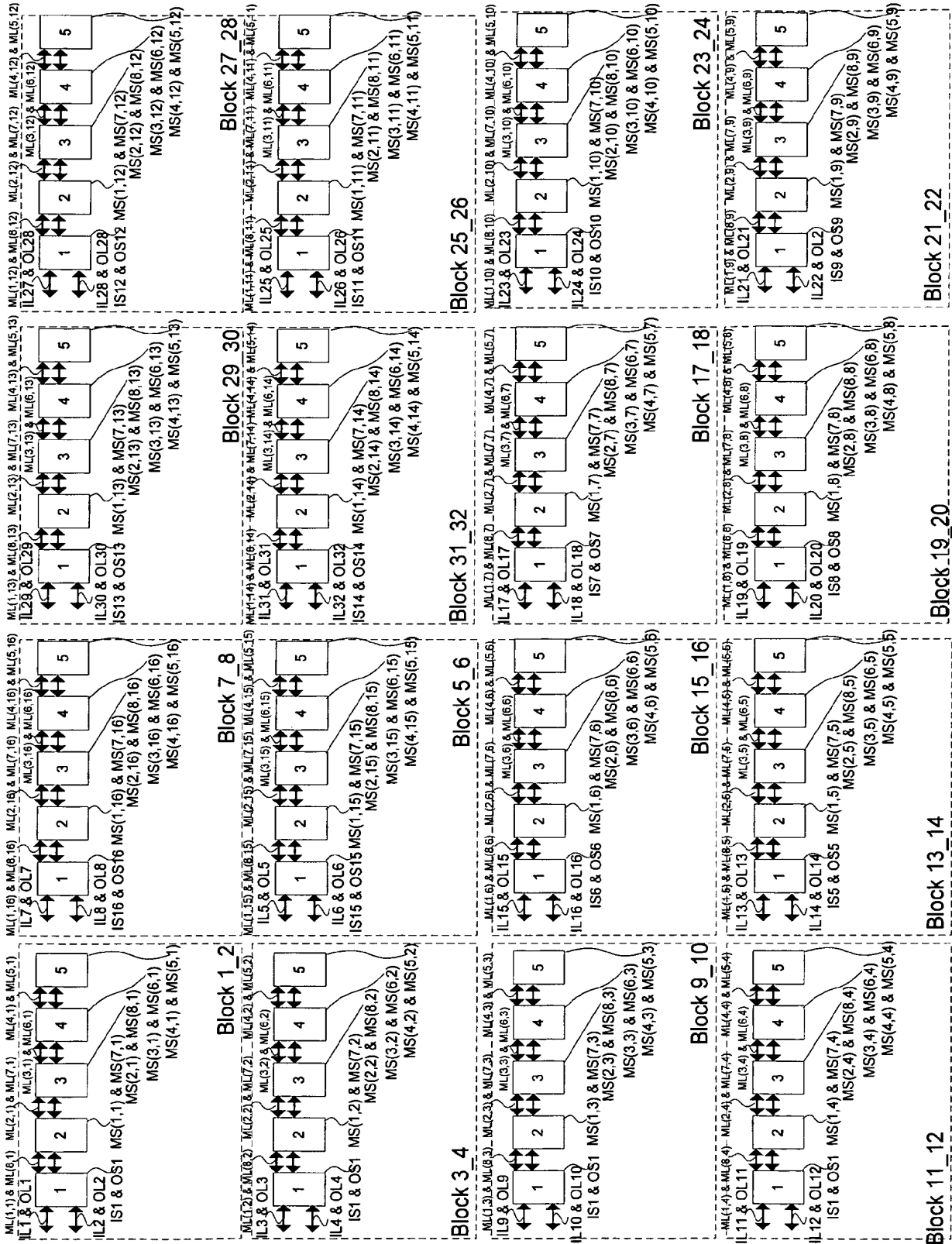


FIG. 3B

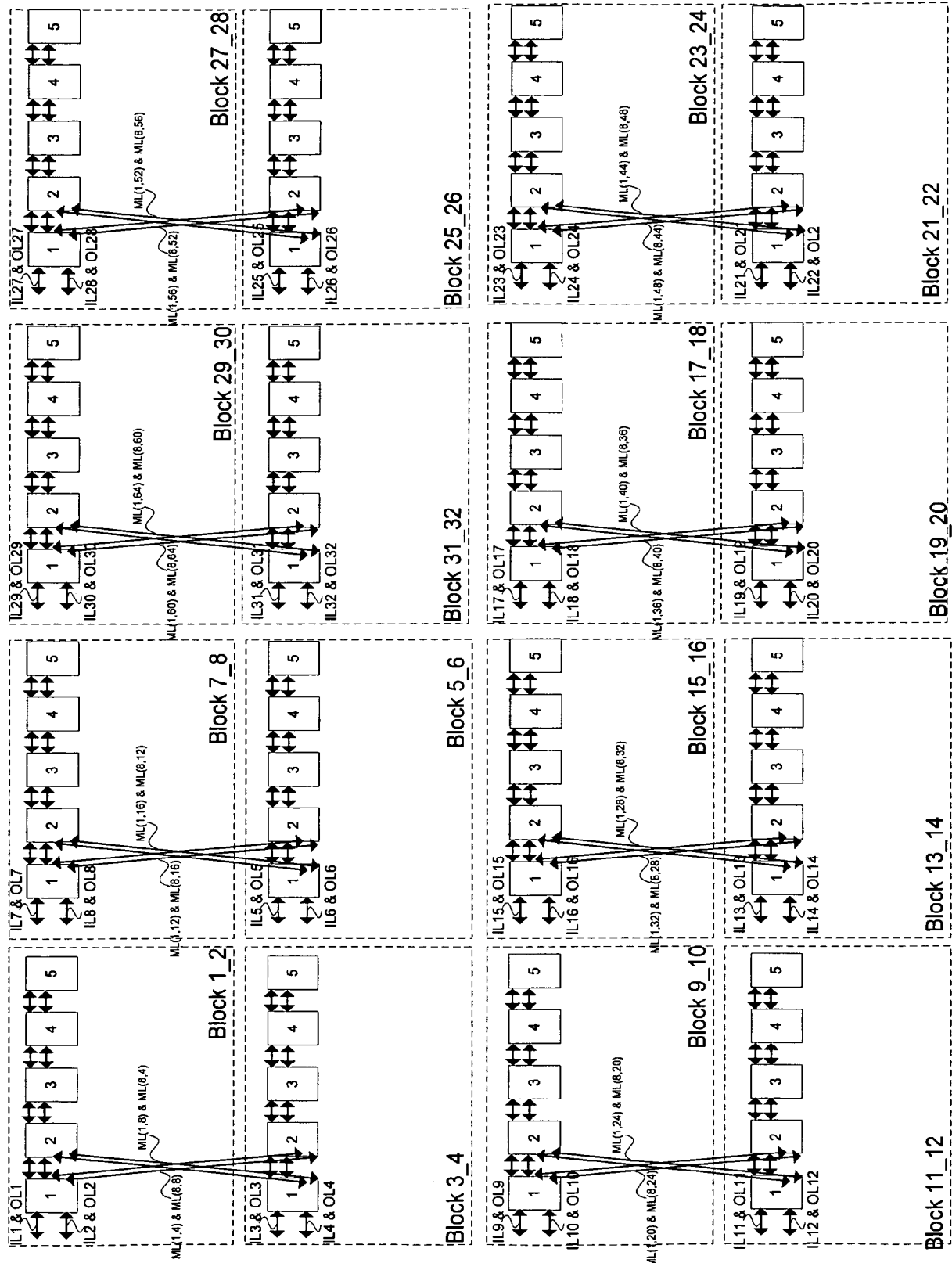
300C

FIG. 3C



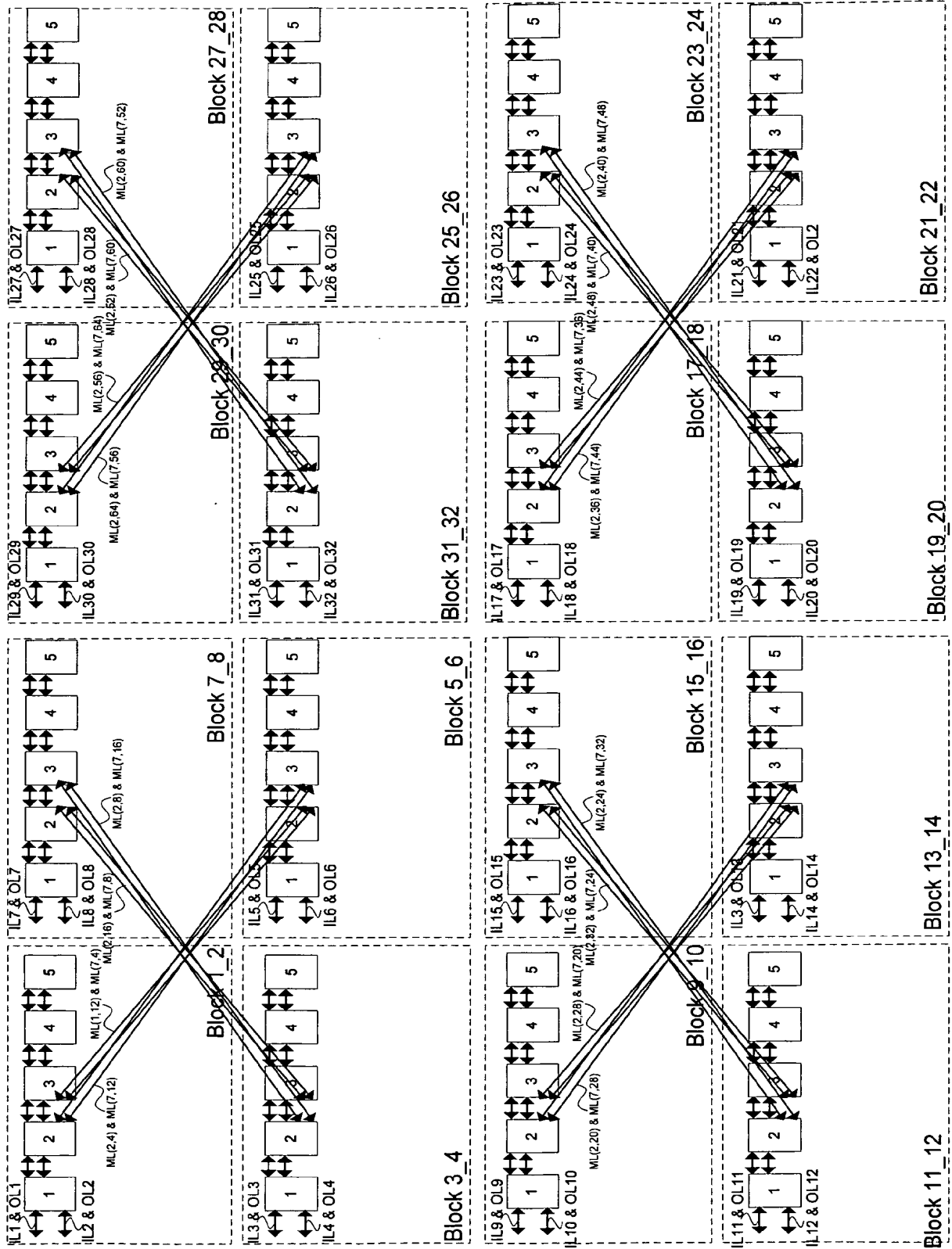
300D

FIG. 3D



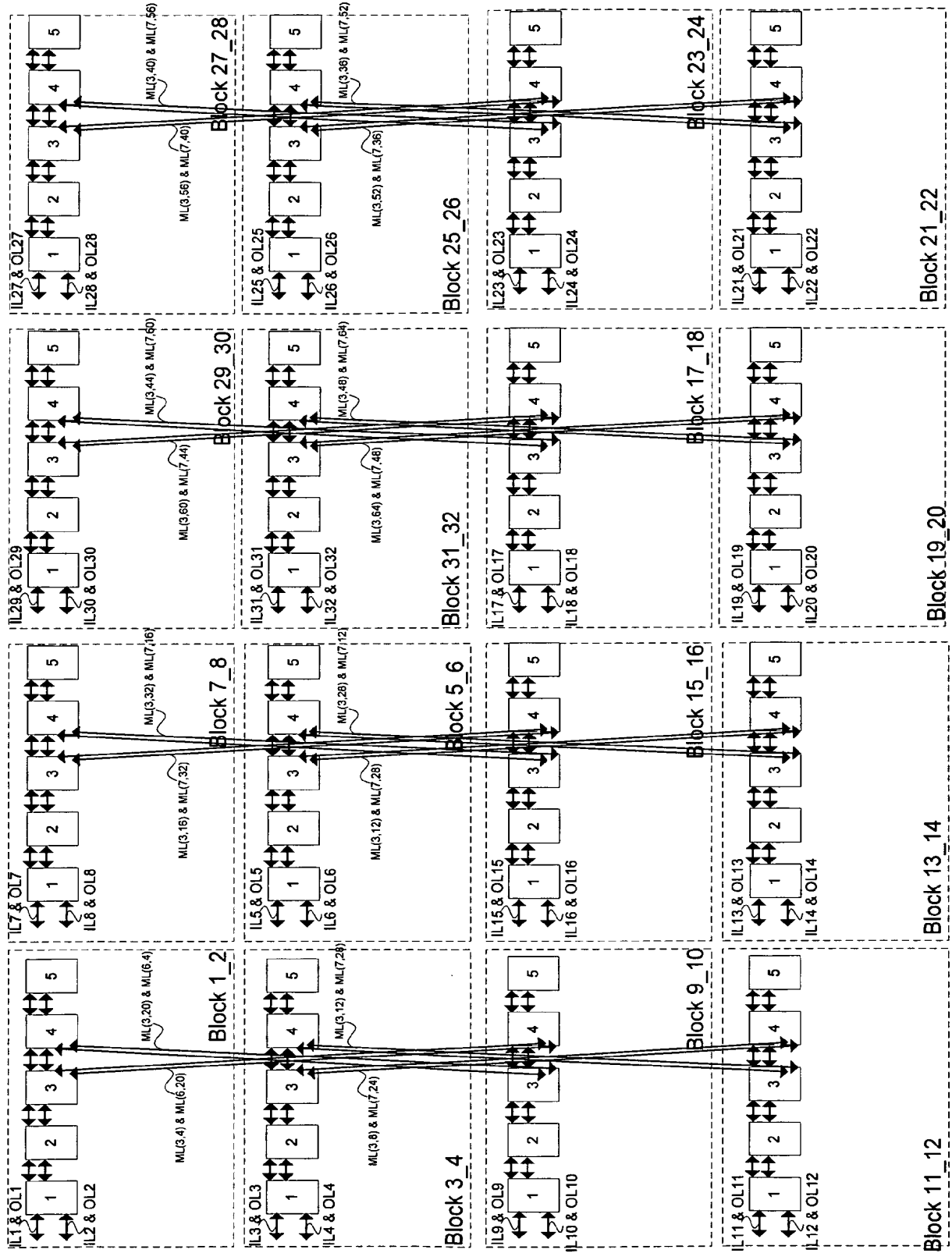
300E

FIG. 3E



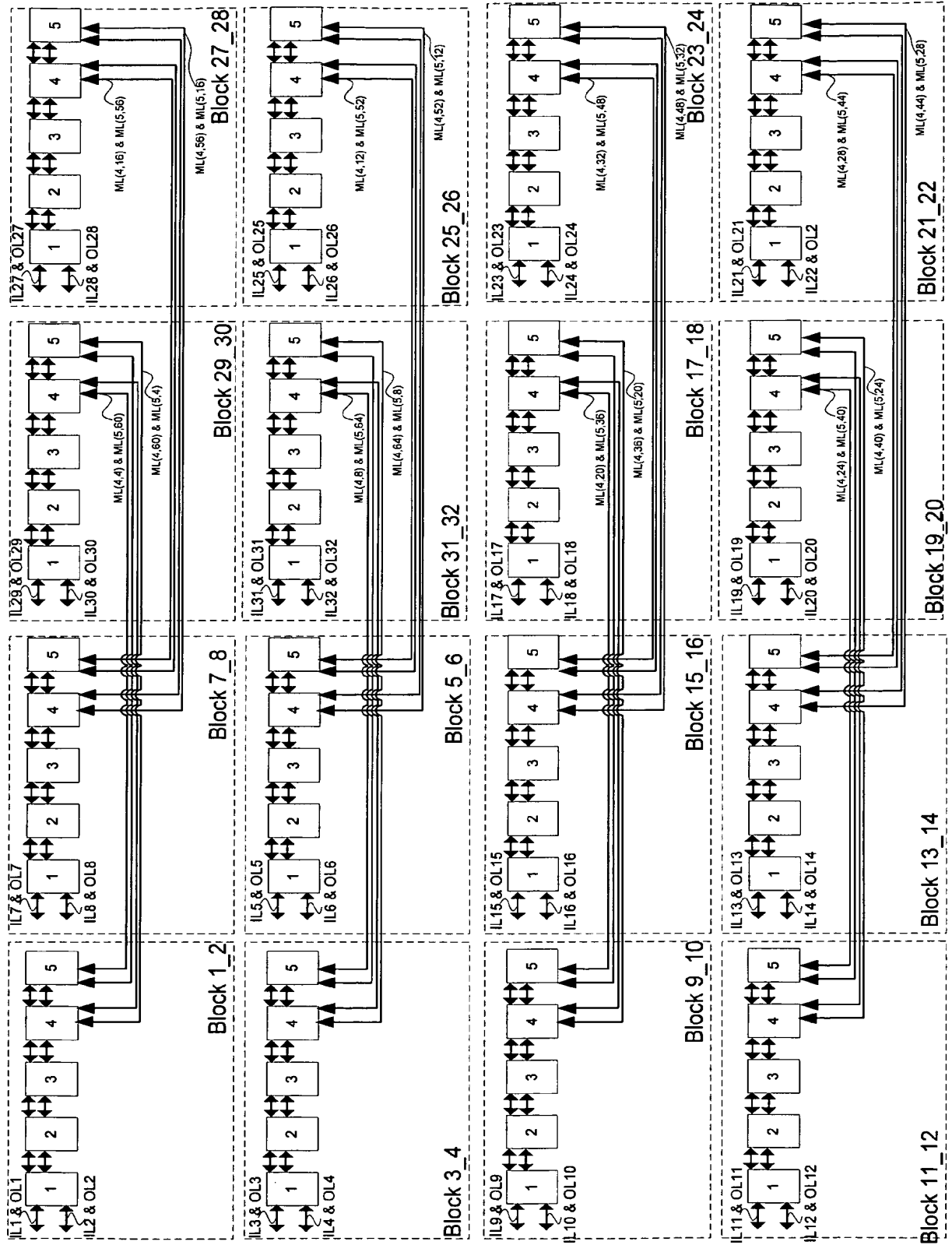
300F

FIG. 3F



300G

FIG. 3G



300H

FIG. 3H

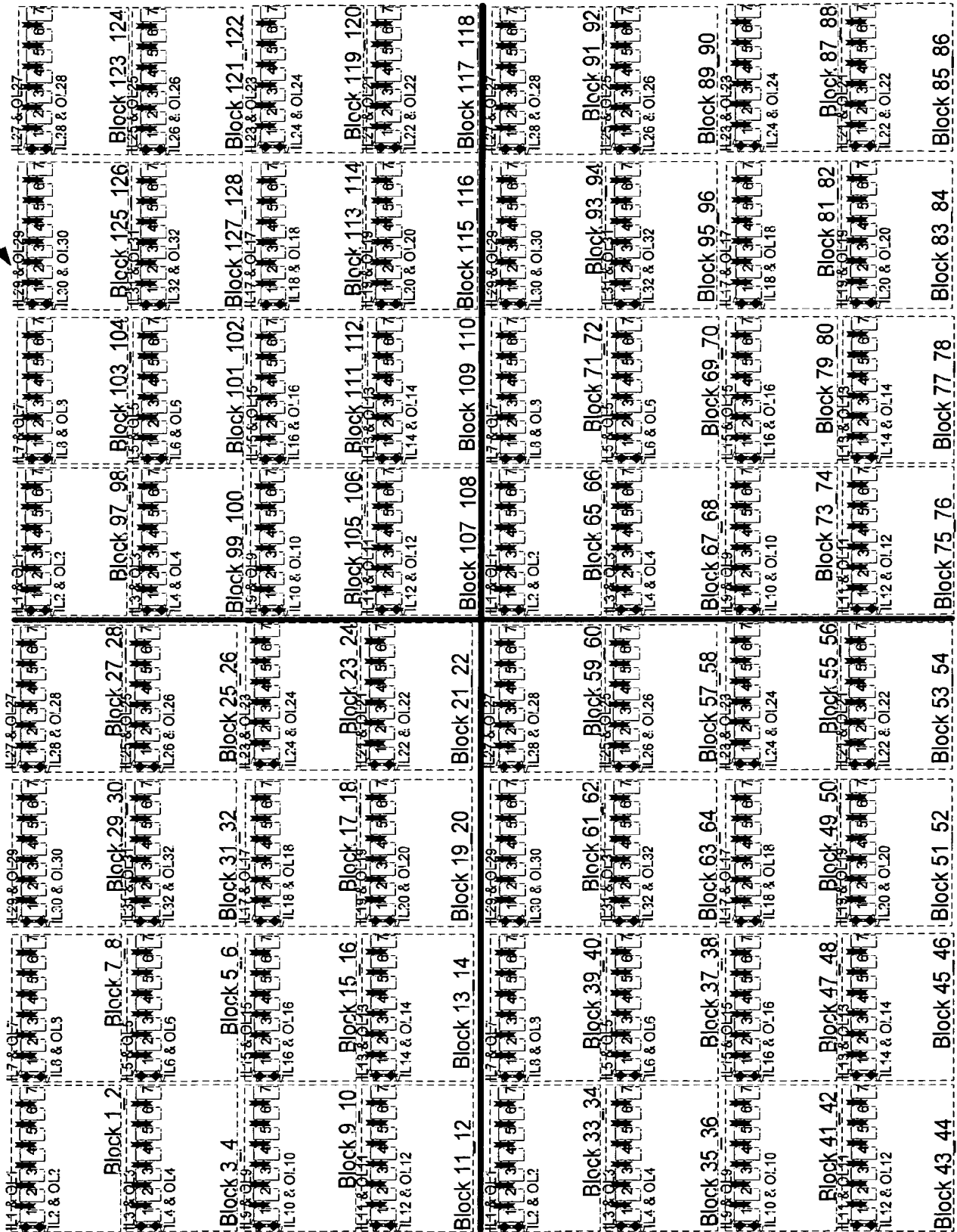
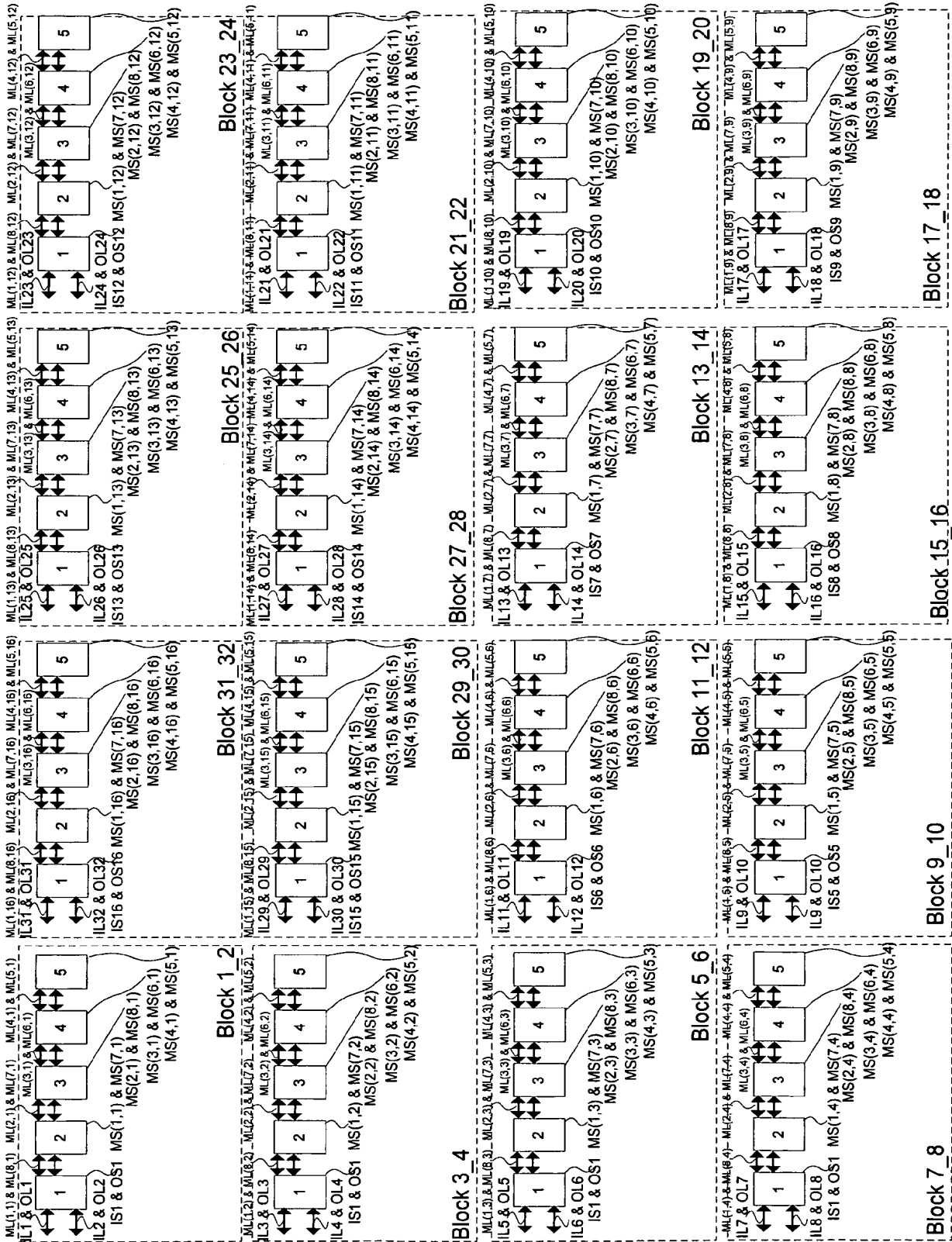




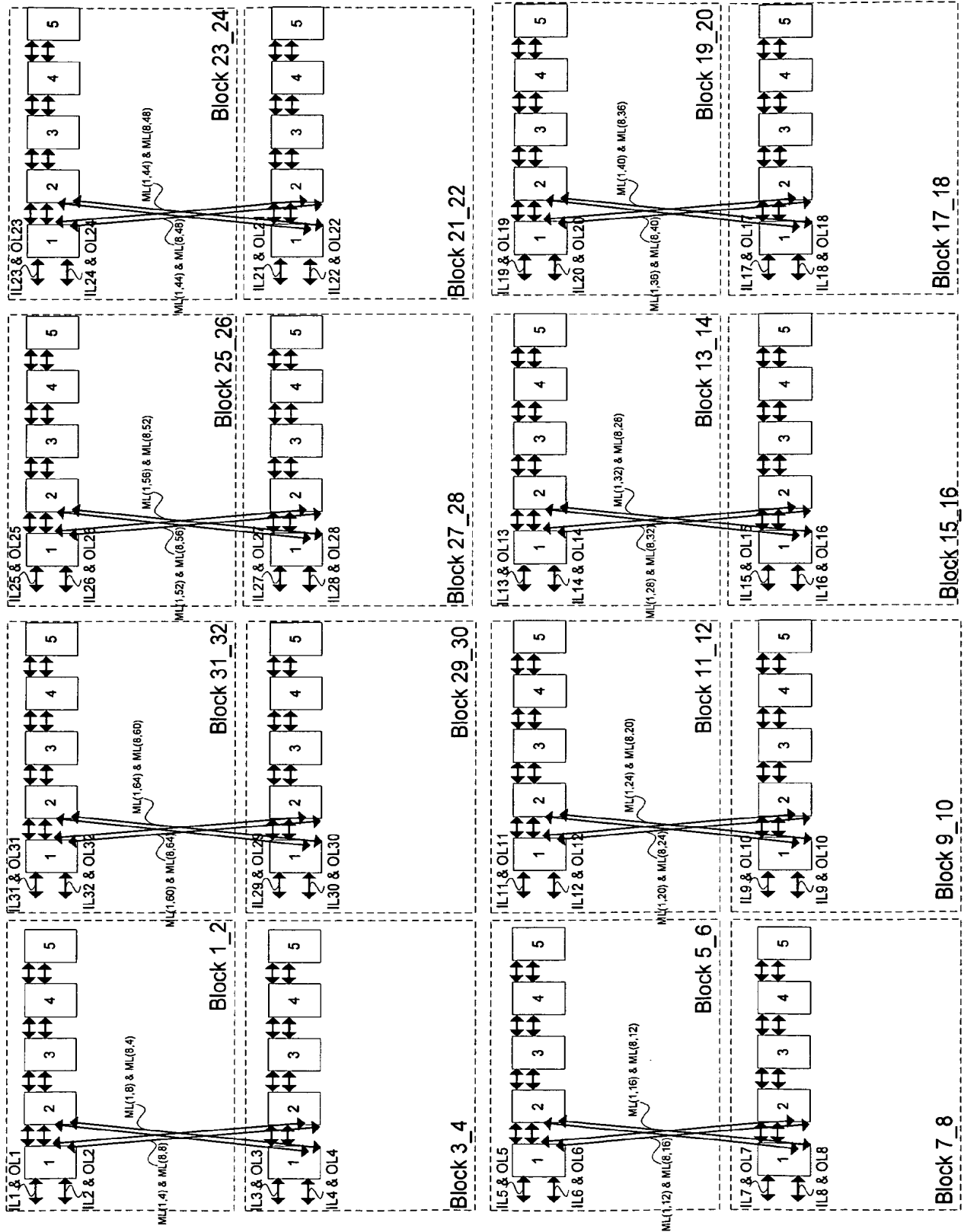
FIG. 4A





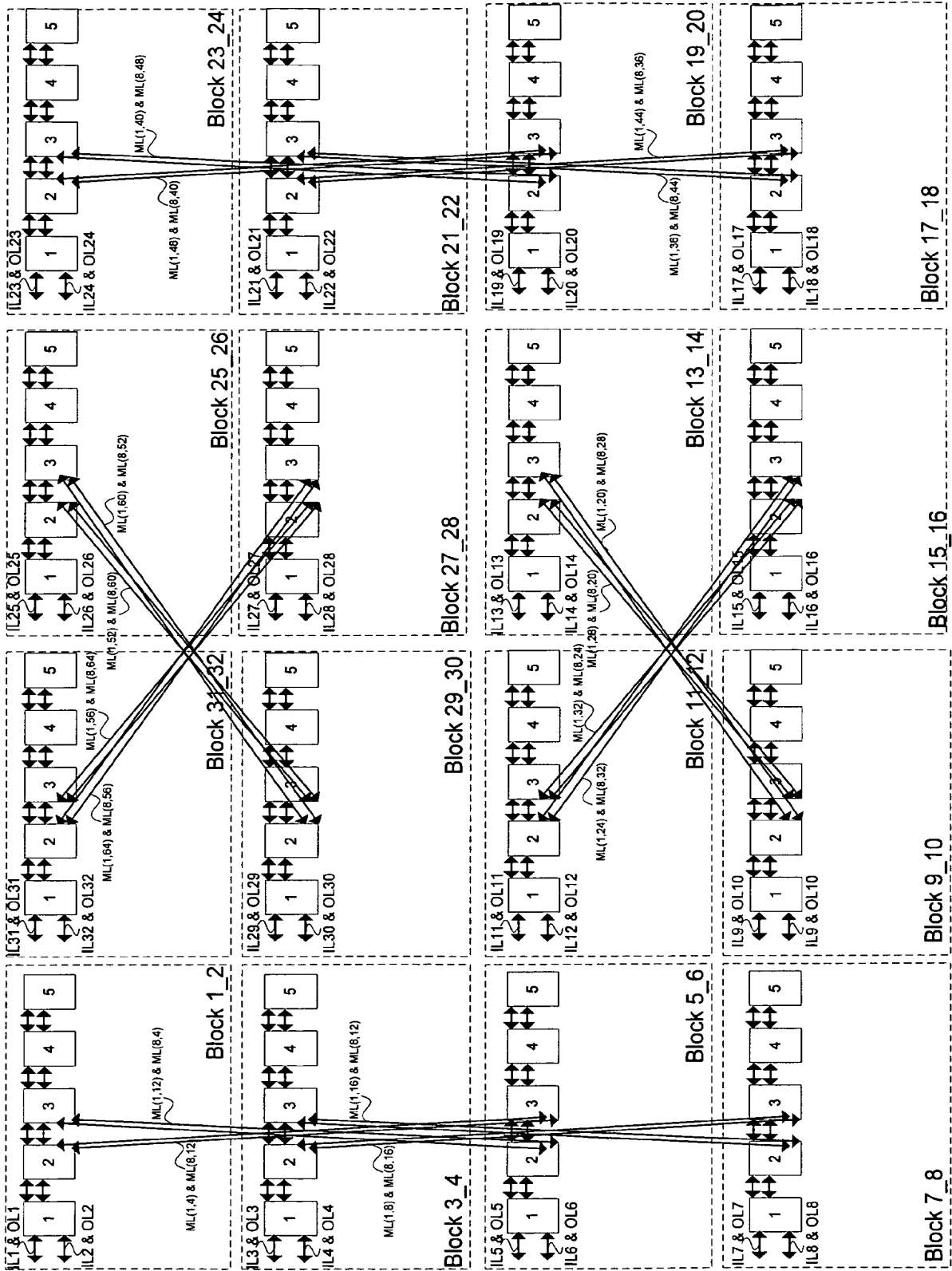
400B

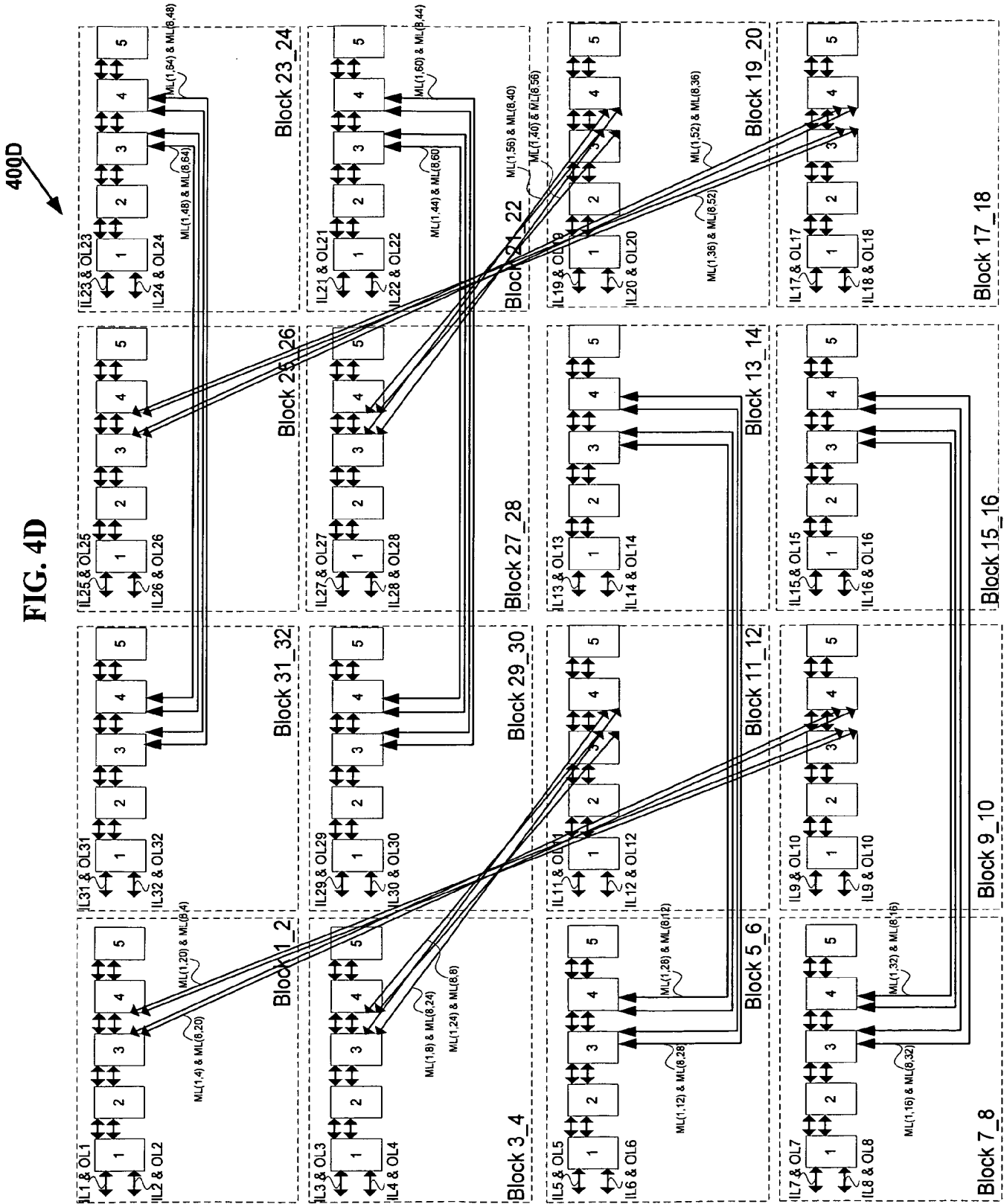
FIG. 4B



400C

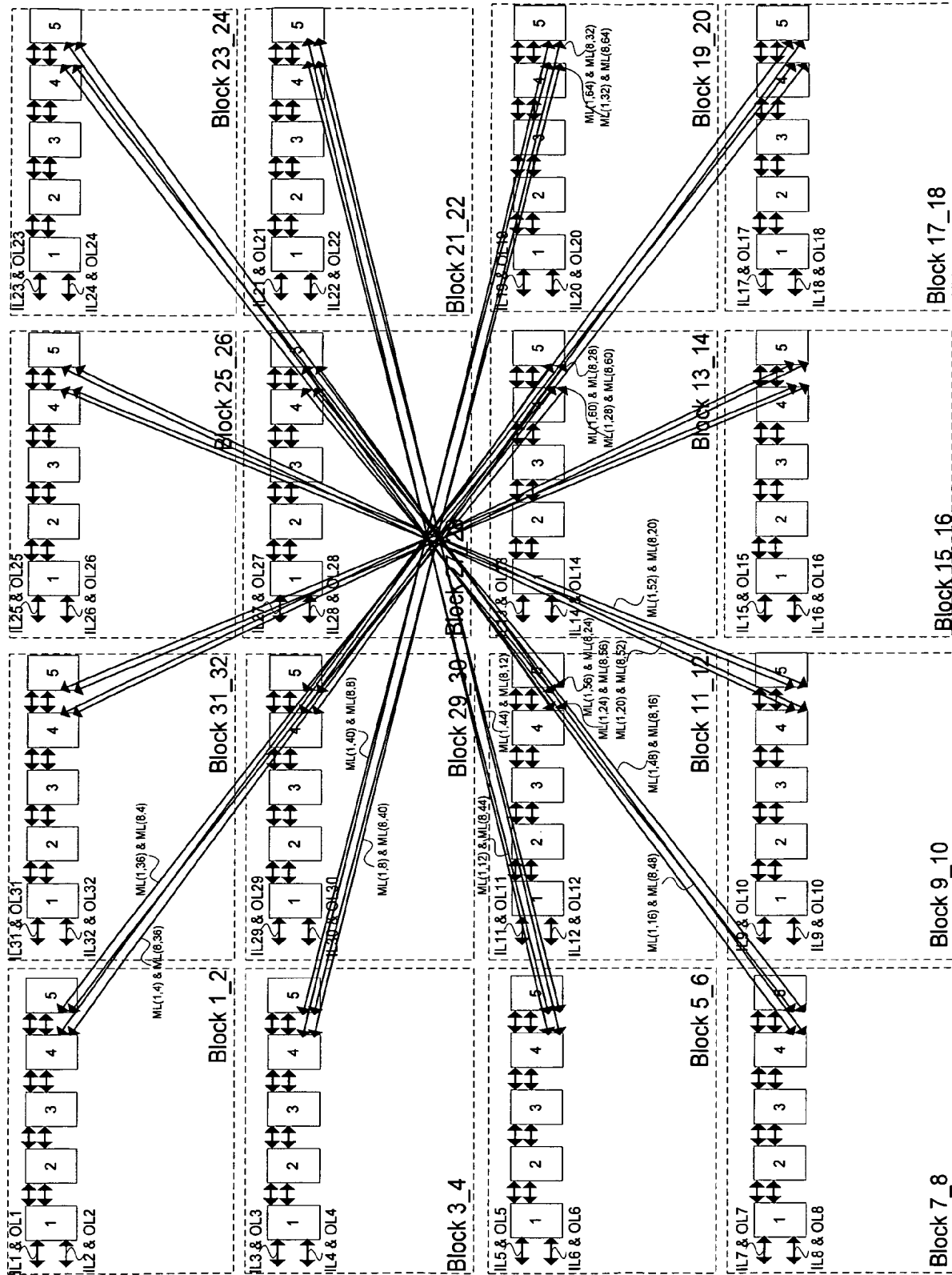
FIG. 4C





400E

FIG. 4E



400C1

FIG. 4C1

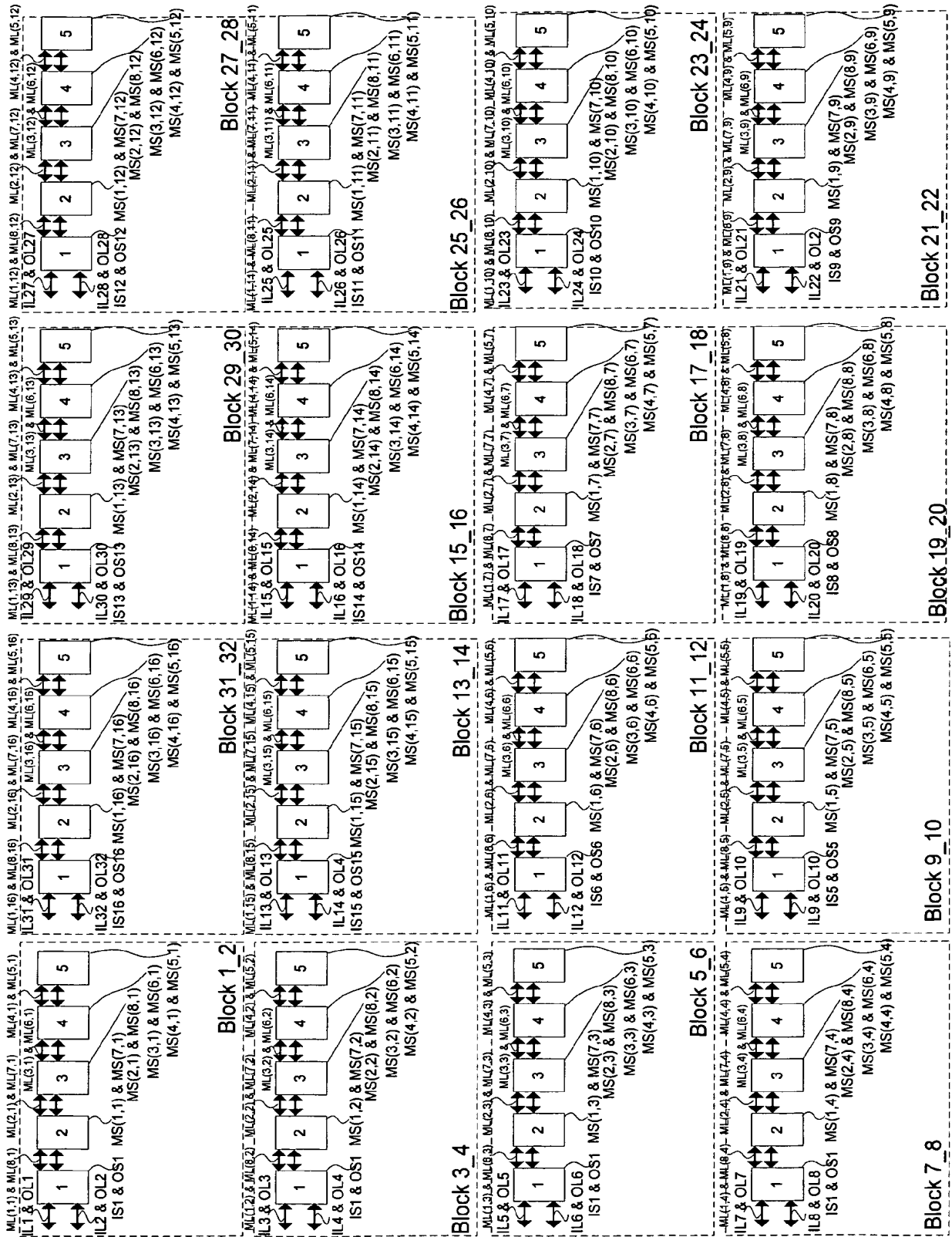


FIG. 5A

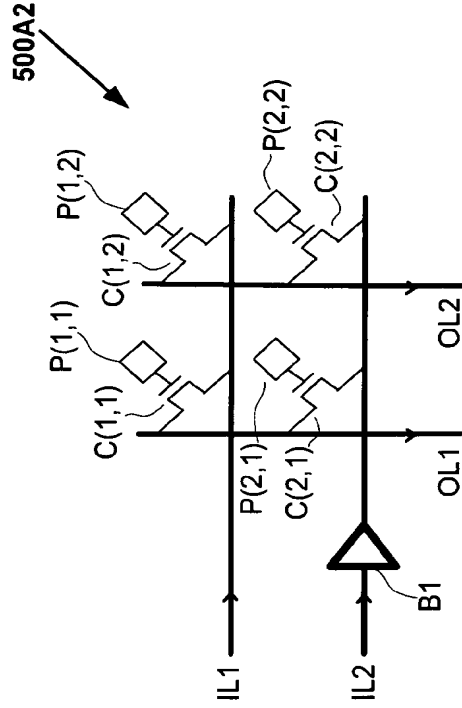


FIG. 5A2  
(Prior Art)

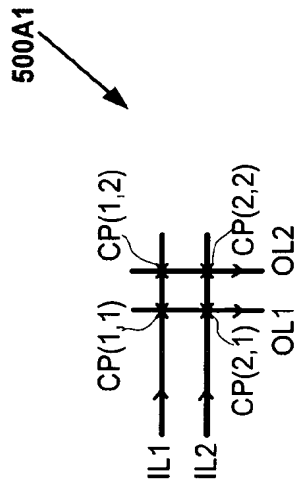


FIG. 5A1  
(Prior Art)

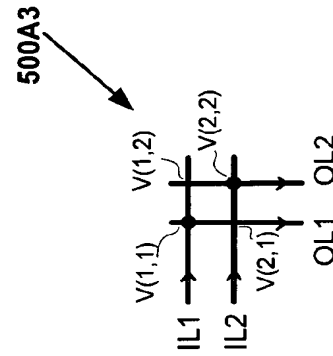


FIG. 5A3  
(Prior Art)

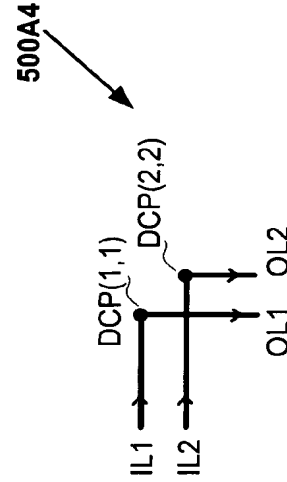


FIG. 5A4