



- [54] **DRAM MEMORY CELL FOR PROGRAMMABLE LOGIC DEVICES**
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- [73] Assignee: **Xilinx, Inc.**, San Jose, Calif.
- [*] Notice: The term of this patent shall not extend beyond the expiration date of Pat. No. 5,581,198.
- [21] Appl. No.: **758,286**
- [22] Filed: **Nov. 1, 1996**

Related U.S. Application Data

- [63] Continuation-in-part of Ser. No. 394,092, Feb. 24, 1995, Pat. No. 5,581,198.
- [51] Int. Cl.⁶ **H03K 19/177; G11C 7/00**
- [52] U.S. Cl. **326/38; 326/41; 365/228; 711/106**
- [58] Field of Search 326/38-40; 365/222, 365/228, 230.03, 230.05, 149; 711/100, 106, 161-162

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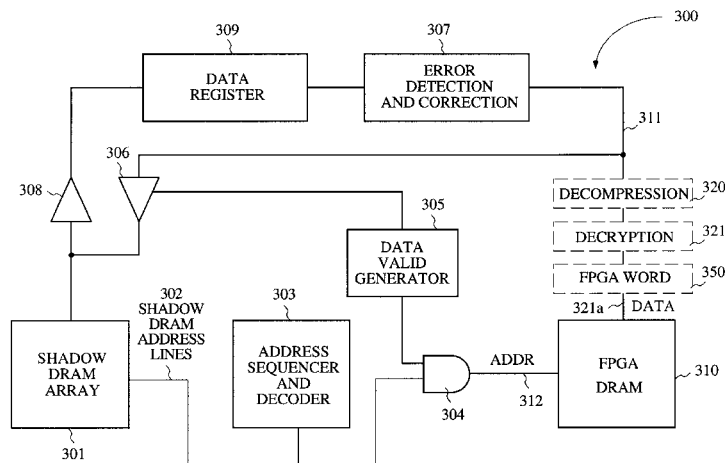
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[57] **ABSTRACT**

A plurality of DRAM cells are used to store the state of the programmable points in a programmable logical device (e.g., a field programmable gate array or FPGA). An individual DRAM cell is used in conjunction with each programmable interconnect point (PIP) within the FPGA to hold a logical state indicating the connectivity state of the PIP. During a refresh cycle, each DRAM memory cell is loaded with its current logical state in order to maintain this state within the PIP. An information store contains duplicate data for each DRAM cell and this duplicate data is supplied and read during the refresh cycle in order to provide each DRAM cell with its proper logical state. In this manner, the refresh cycle does not alter the logic configuration of its associated FPGA DRAM cell. The information store can be a plurality of DRAM cells or the information store can be of non-volatile memory, for instance, read only memory (ROM), programmable ROM (PROM), erasable PROM (EPROM), electrically erasable PROM (EEPROM), or of non-volatile magnetic storage.

23 Claims, 5 Drawing Sheets



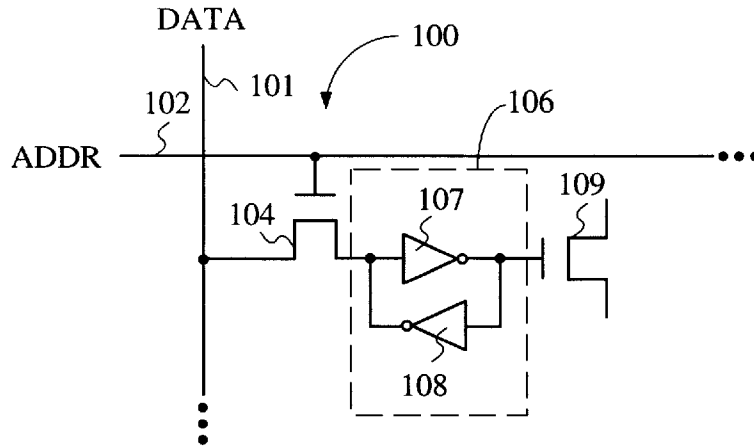


FIG. 1
PRIOR ART

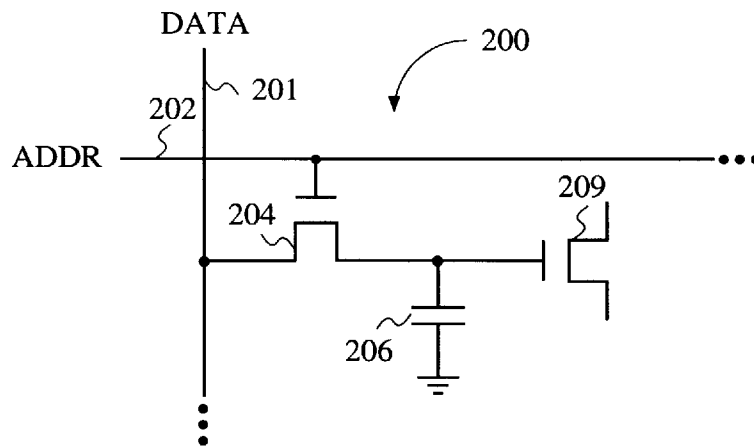


FIG. 2

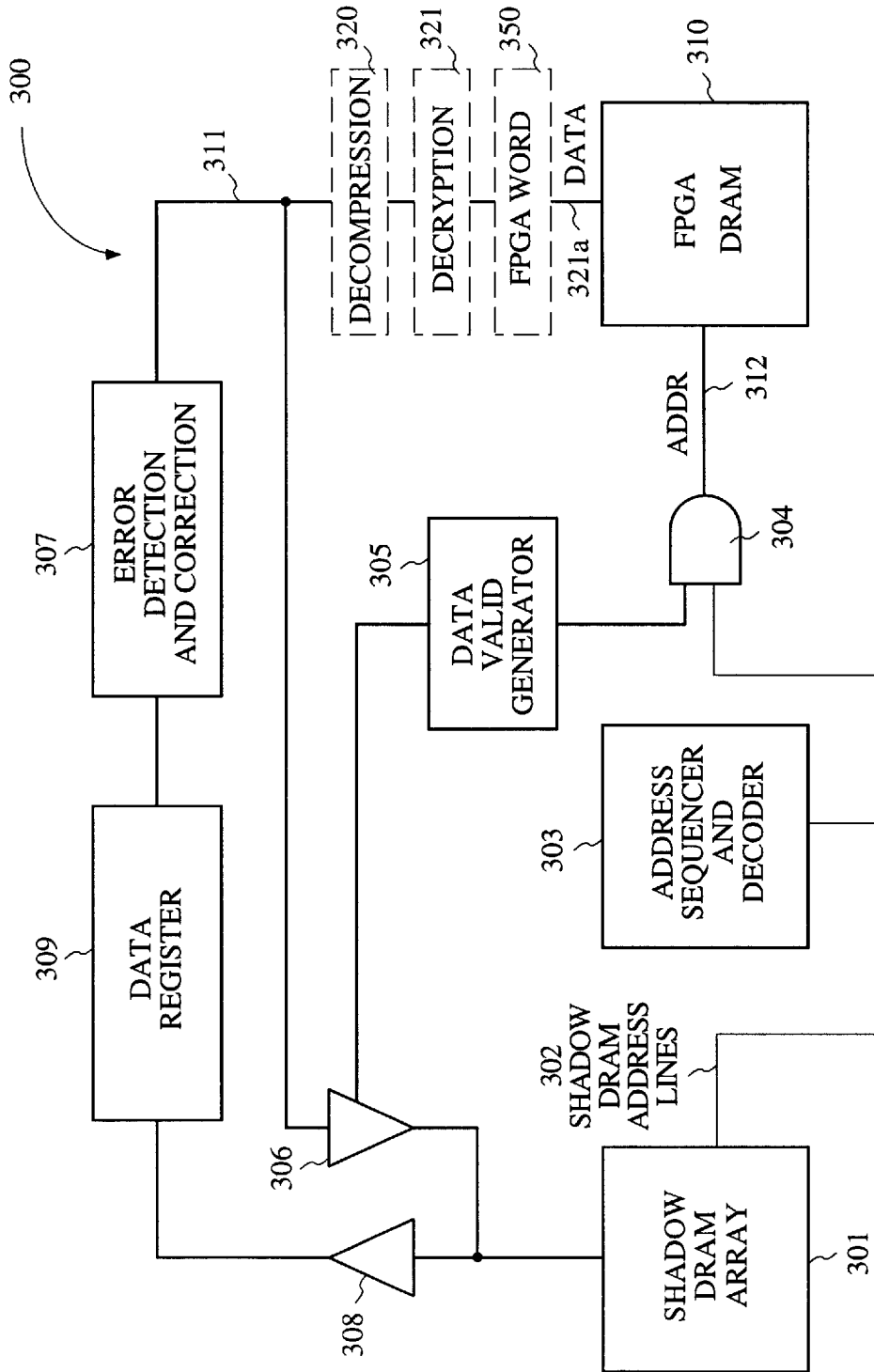


FIG. 3

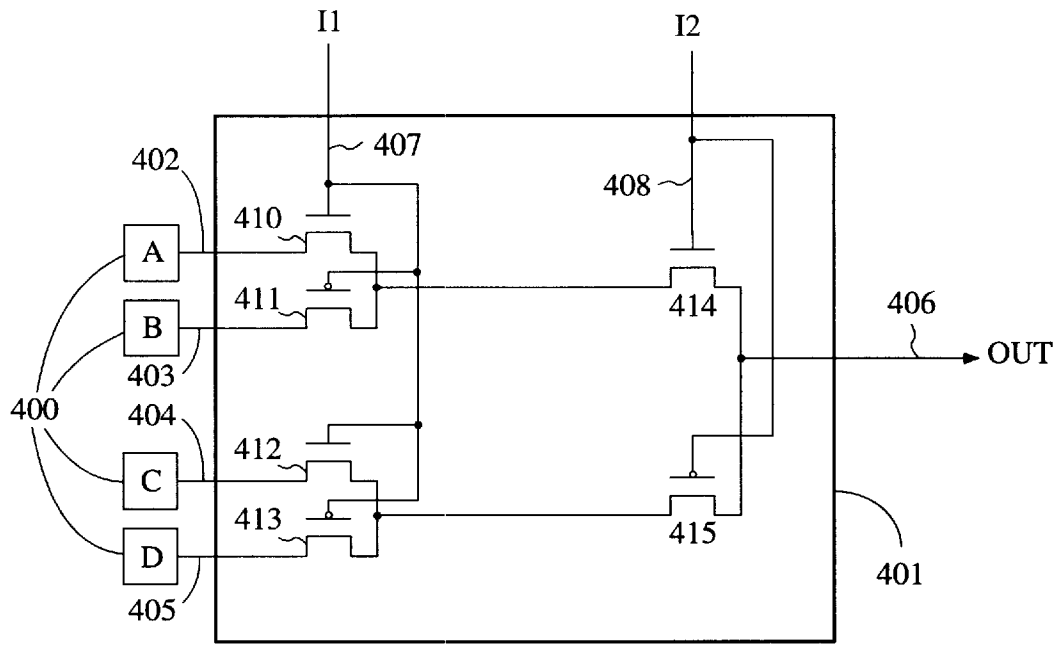


FIG. 4

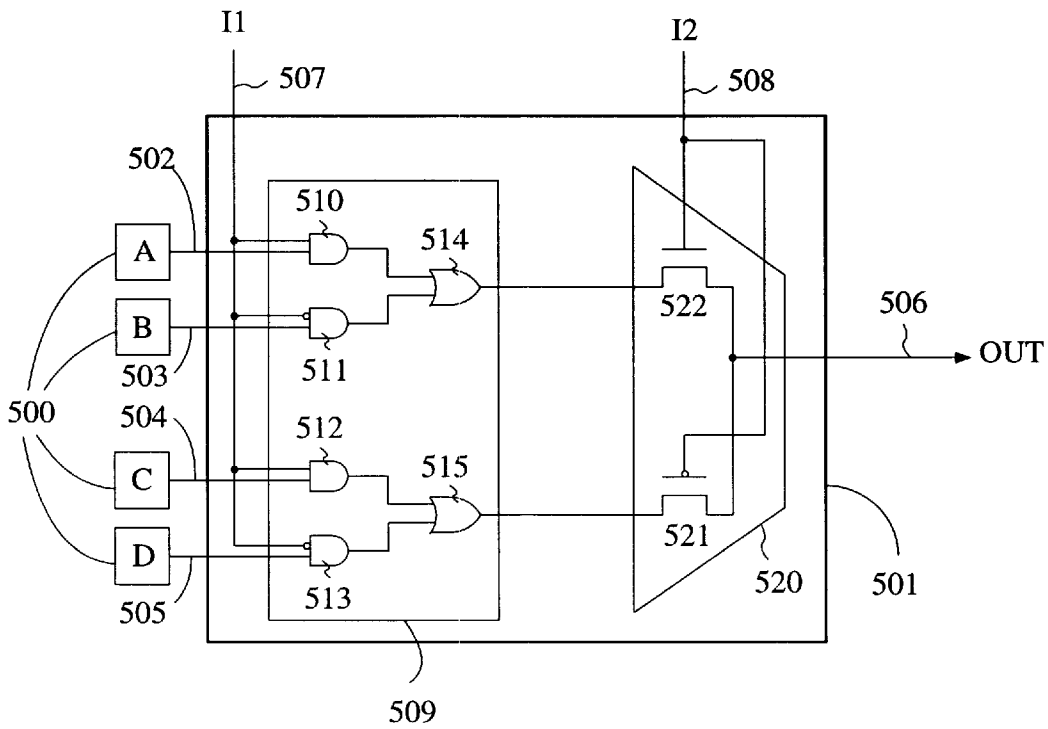


FIG. 5

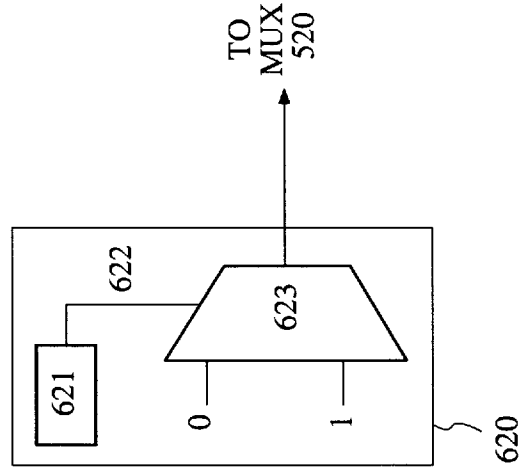


FIG. 6b

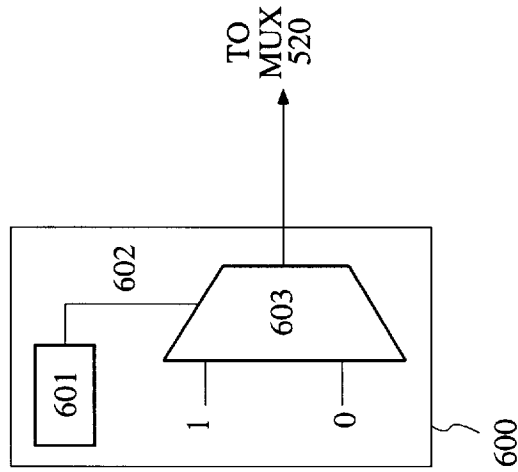


FIG. 6a

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