VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS WITH LOCALITY EXPLOITATION

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CROSS REFERENCE TO RELATED APPLICATIONS

This application is related to and incorporates by reference in its entirety the PCT Application Serial No. PCT/US08/56064 entitled "FULLY CONNECTED GENERALIZED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed March 6, 2008, the U.S. Provisional Patent Application Serial No. 60/905,526 entitled "LARGE SCALE CROSSPOINT REDUCTION WITH NONBLOCKING UNICAST & MULTICAST IN ARBITRARILY LARGE MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed March 6, 2007, and the U.S. Provisional Patent Application Serial No. 60/940, 383 entitled "FULLY CONNECTED GENERALIZED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

This application is related to and incorporates by reference in its entirety the PCT Application Serial No. PCT/US08/64603 entitled "FULLY CONNECTED GENERALIZED BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 22, 2008, the U.S. Provisional Patent Application Serial No. 60/940, 387 entitled "FULLY CONNECTED GENERALIZED BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007, and the U.S. Provisional Patent Application Serial No. 60/940, 390 entitled "FULLY CONNECTED GENERALIZED MULTI-LINK BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007

This application is related to and incorporates by reference in its entirety the PCT Application Serial No. PCT/US08/64604 entitled "FULLY CONNECTED

GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 22, 2008, the U.S. Provisional Patent Application Serial No. 60/940, 389 entitled "FULLY CONNECTED GENERALIZED REARRANGEABLY NONBLOCKING MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007, the U.S. Provisional Patent Application Serial No. 60/940, 391 entitled "FULLY CONNECTED GENERALIZED FOLDED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007 and the U.S. Provisional Patent Application Serial No. 60/940, 392 entitled "FULLY CONNECTED GENERALIZED STRICTLY NONBLOCKING MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

This application is related to and incorporates by reference in its entirety the PCT Application Serial No. PCT/US08/64605 entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 22, 2008, and the U.S. Provisional Patent Application Serial No. 60/940, 394 entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

This application is related to and incorporates by reference in its entirety the U.S. Provisional Patent Application, Attorney Docket No. M-0049 US entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED AND PYRAMID NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed concurrently.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1A is a diagram 100A of an exemplary symmetrical multi-link multi-stage network $V_{fold-mlink}(N,d,s)$ having a variation of inverse Benes connection topology of nine stages with N = 32, d = 2 and s=2, strictly nonblocking network for unicast

connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1B is a diagram 100B of the equivalent symmetrical folded multi-link multi-stage network $V_{fold-mlink}(N,d,s)$ of the network 100A shown in FIG. 1A, having a variation of inverse Benes connection topology of five stages with N = 32, d = 2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1C is a diagram 100C layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 1D is a diagram 100D layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links ML(1,i) for i = [1, 64] and ML(8,i) for i = [1,64].

FIG. 1E is a diagram 100E layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links ML(2,i) for i = [1, 64] and ML(7,i) for i = [1,64].

FIG. 1F is a diagram 100F layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links ML(3,i) for i = [1, 64] and ML(6,i) for i = [1,64].

FIG. 1G is a diagram 100G layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links ML(4,i) for i = [1, 64] and ML(5,i) for i = [1,64].

FIG. 1H is a diagram 100H layout of a network $V_{fold-mlink}(N,d,s)$ where N = 128, d = 2, and s = 2, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 1I is a diagram 100I detailed connections of BLOCK 1_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing $V_{mlink}(N,d,s)$ or $V_{fold-mlink}(N,d,s)$.

FIG. 1J is a diagram 100J detailed connections of BLOCK 1_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing $V_{mlink-bft}(N,d,s)$.

FIG. 1K is a diagram 100K detailed connections of BLOCK 1_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing $V(N,d,s)$ or $V_{fold}(N,d,s)$.

FIG. 1K1 is a diagram 100M1 detailed connections of BLOCK 1_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing $V(N,d,s)$ or $V_{fold}(N,d,s)$ for s = 1.

FIG. 1L is a diagram 100L detailed connections of BLOCK 1_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing $V_{bft}(N,d,s)$.

FIG. 1L1 is a diagram 100L1 detailed connections of BLOCK 1_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing $V_{bft}(N,d,s)$ for s = 1.

FIG. 2A is a diagram 200A of an exemplary symmetrical multi-link multi-stage network $V_{fold-mlink}(N,d,s)$ having inverse Benes connection topology of nine stages with N = 24, d = 2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 2B is a diagram 200B of the equivalent symmetrical folded multi-link multi-stage network $V_{fold-mlink}(N,d,s)$ of the network 200A shown in FIG. 2A, having inverse Benes connection topology of five stages with N = 24, d = 2 and s=2, strictly nonblocking

network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 2C is a diagram 200C layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 2B, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 2D is a diagram 200D layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 2B, in one embodiment, illustrating the connection links ML(1,i) for i = [1, 48] and ML(8,i) for i = [1,48].

FIG. 2E is a diagram 200E layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 2B, in one embodiment, illustrating the connection links ML(2,i) for i = [1, 32] and ML(7,i) for i = [1,32].

FIG. 2F is a diagram 200F layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 2B, in one embodiment, illustrating the connection links ML(3,i) for i = [1, 64] and ML(6,i) for i = [1,64].

FIG. 2G is a diagram 200G layout of the network $V_{fold-mlink}(N,d,s)$ shown in FIG. 2B, in one embodiment, illustrating the connection links ML(4,i) for i = [1, 64] and ML(5,i) for i = [1,64].

FIG. 3A is a diagram 300A layout of the topmost row of the network $V_{fold-mlink}(N,d,s)$ with N = 512, d = 2 and s=2, in one embodiment, illustrating the provisioning of 2's BW.

FIG. 3B is a diagram 300B layout of the topmost row of the network $V_{fold-mlink}(N,d,s)$ with N = 512, d = 2 and s=2, in one embodiment, illustrating the provisioning of 4's BW.

FIG. 3C is a diagram 300C layout of the topmost row of the network $V_{fold-mlink}(N,d,s)$ with N = 512, d = 2 and s=2, in one embodiment, illustrating the provisioning of 8's BW with nearest neighbor connectivity first.

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